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Lab Report 4

ECE 2031 L09

17 February 2022

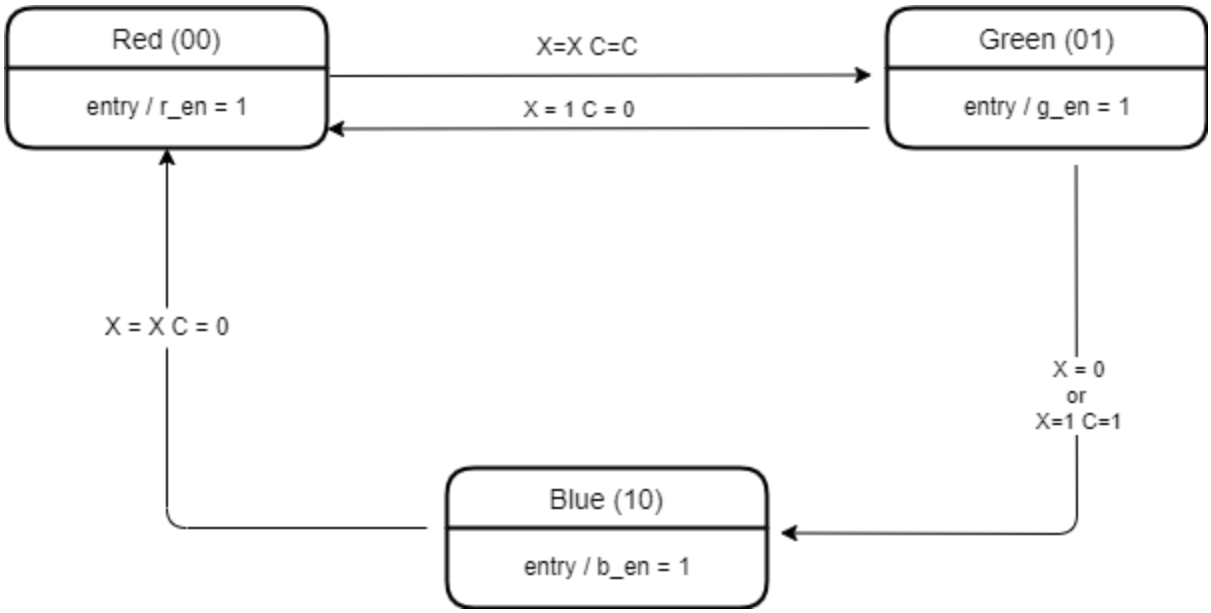


**Figure 1.** The state diagram of a finite state machine that rotates between Red, Green and Blue states. Each state shows what occurs on entry and the requirements to move to the succeeding state.

| Current State | Q1 | Q0 | xmas | cool | Next State | Q1+ | Q0+ | r_en | g_en | b_en |
|---|---|---|---|---|---|---|---|---|---|---|
| Red | 0 | 0 | 0 | 0 | Green | 0 | 1 | 1 | 0 | 0 |
| Red | 0 | 0 | 0 | 1 | Green | 0 | 1 | 1 | 0 | 0 |
| Red | 0 | 0 | 1 | 0 | Green | 0 | 1 | 1 | 0 | 0 |
| Red | 0 | 0 | 1 | 1 | Green | 0 | 1 | 1 | 0 | 0 |
| Green | 0 | 1 | 0 | 0 | Blue | 0 | 1 | 0 | 1 | 0 |
| Green | 0 | 1 | 0 | 1 | Blue | 0 | 1 | 0 | 1 | 0 |
| Green | 0 | 1 | 1 | 0 | Red | 0 | 0 | 0 | 1 | 0 |
| Green | 0 | 1 | 1 | 1 | Blue | 0 | 1 | 0 | 1 | 0 |
| Blue | 1 | 0 | 0 | 0 | Red | 0 | 0 | 0 | 0 | 1 |
| Blue | 1 | 0 | 0 | 1 | Blue | 0 | 1 | 0 | 0 | 1 |
| Blue | 1 | 0 | 1 | 0 | Red | 0 | 0 | 0 | 1 | 1 |
| Blue | 1 | 0 | 1 | 1 | Blue | 0 | 1 | 0 | 1 | 1 |

**Figure 2.** The transition table of a finite state machine that rotates through states Red, Green, and Blue. The table shows all possible combinations of current state and inputs excluding the unused state (11)

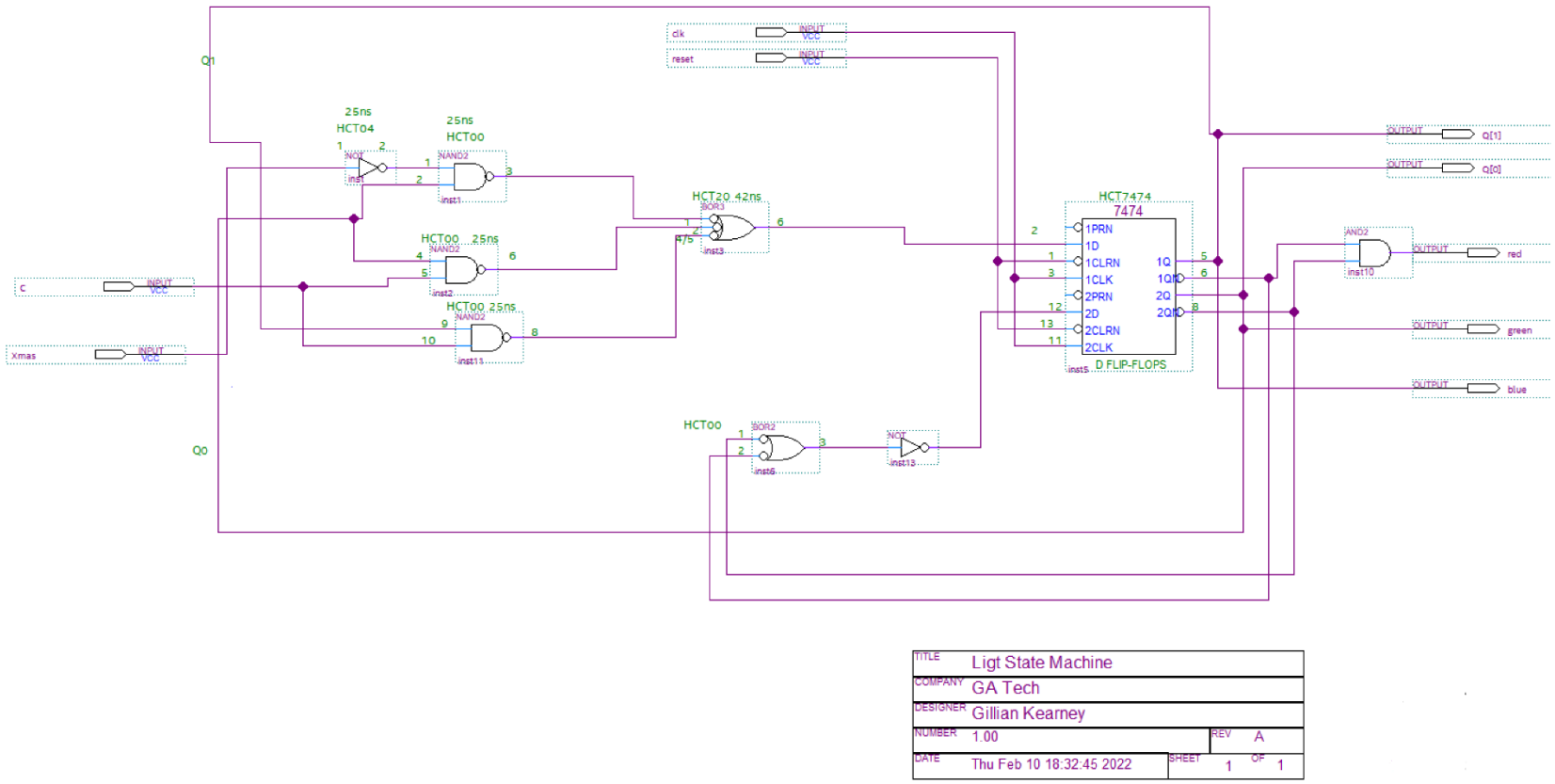


**Figure 3.** Circuit Schematic implementing a finite state machine. Outputs red, green, and blue activate in a cycle continuously unless interrupted by an input of c or xmas in which blue stays active or red and green cycle respectively.

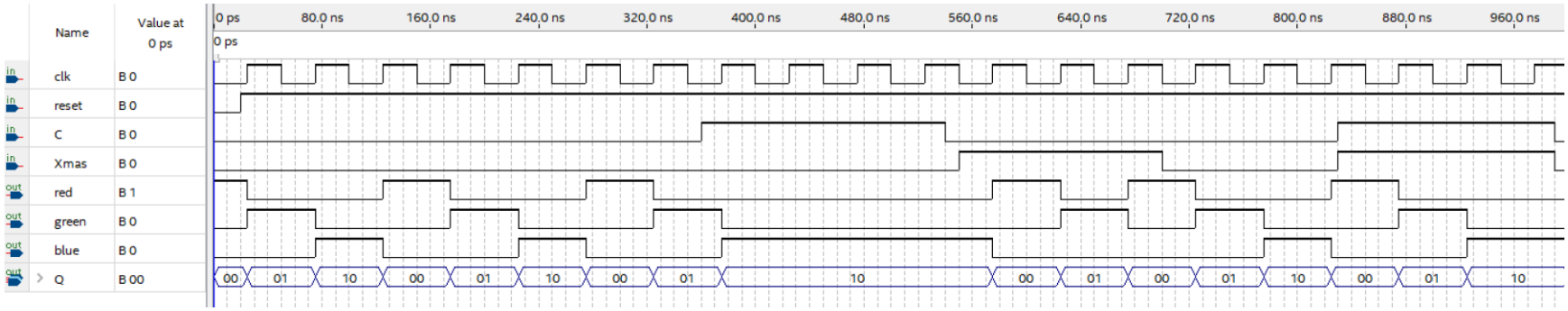


**Figure 4.** Functional simulation waveform of Red, Green, Blue finite state machine with 4 inputs and 4 outputs. The input vector covers all possible input states to prove the correctness of the circuit.

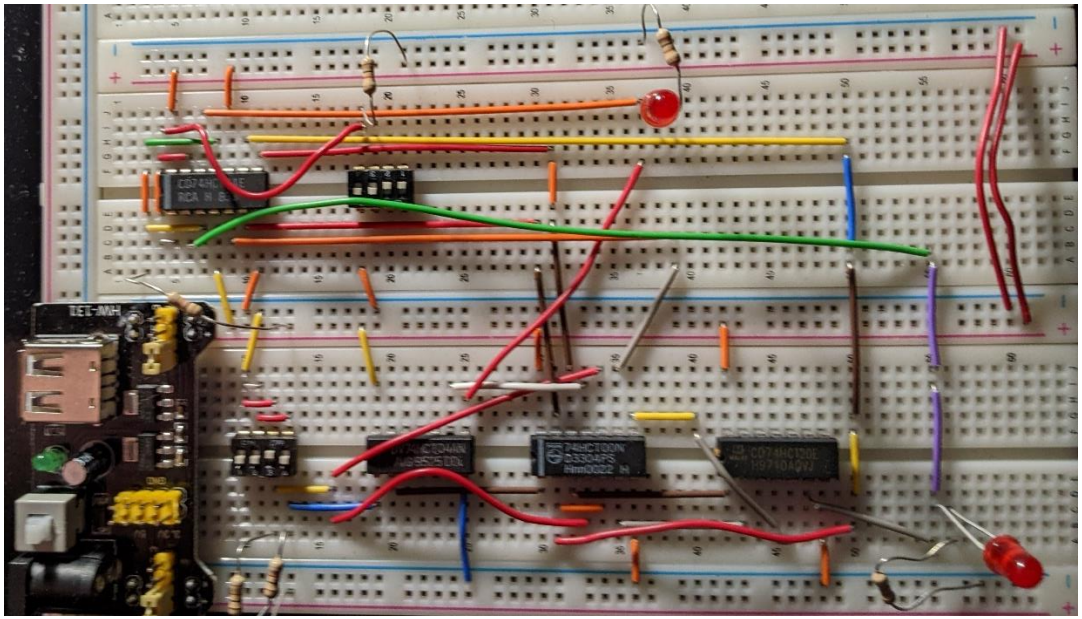

**Figure 5.** The circuit implementation of a finite state machine where the next state is monitored by led lights found on the bottom right and top middle of the circuit.

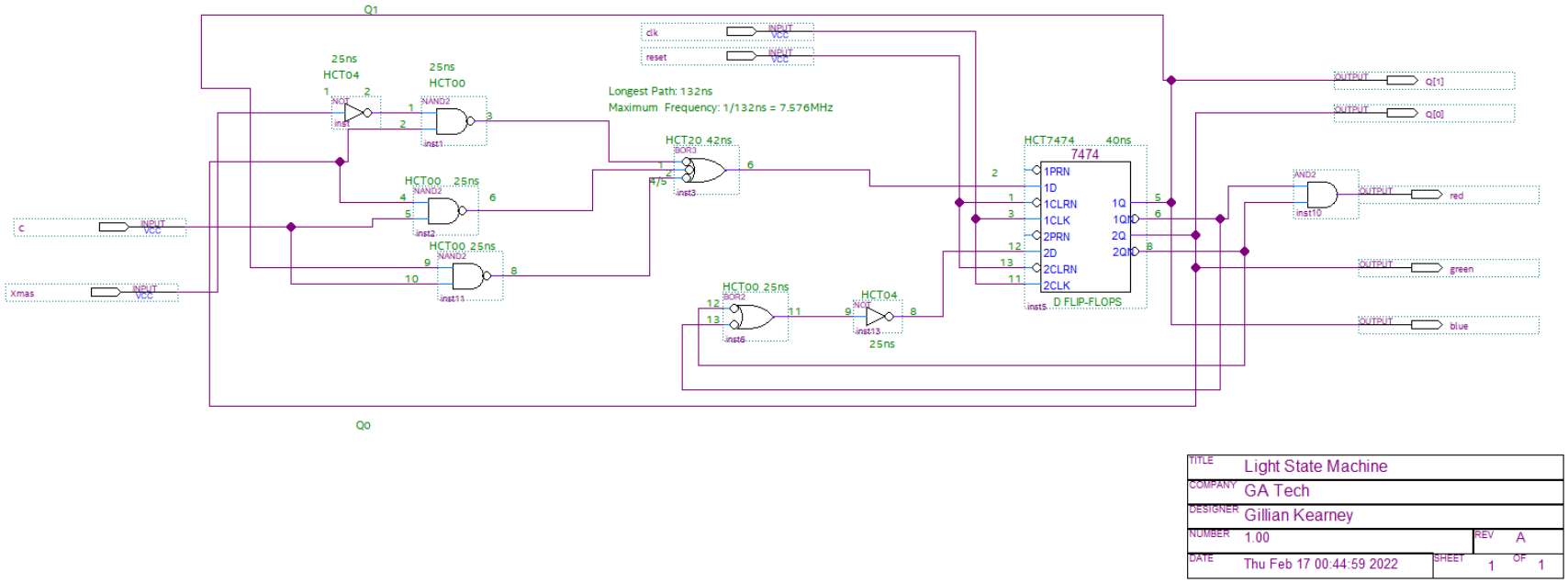


**Figure 6.** Circuit Schematic implementing a finite state machine. It shows each gate's worst case propagation delay and the circuit's worst possible delay of 132ns which runs through the upper path, through an inverter, 2 nand gates and a D flip-flop. The calculated maximum frequency was found to be 7.576MHz.