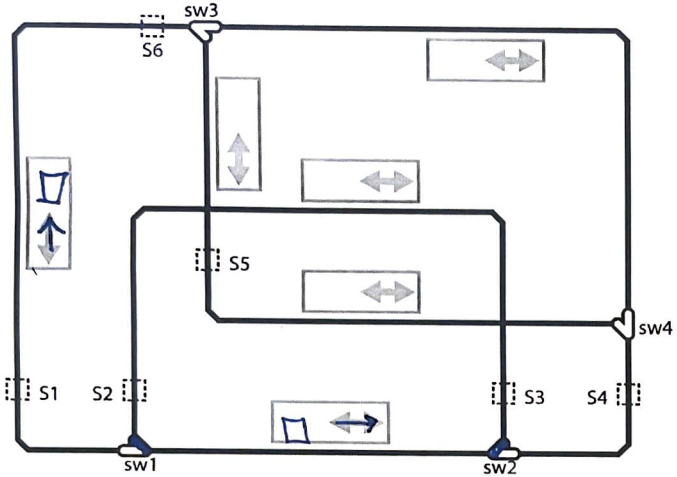
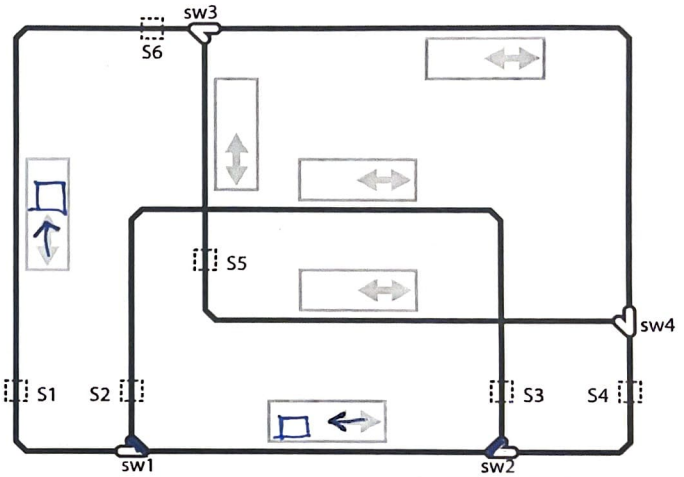
A forward B rev



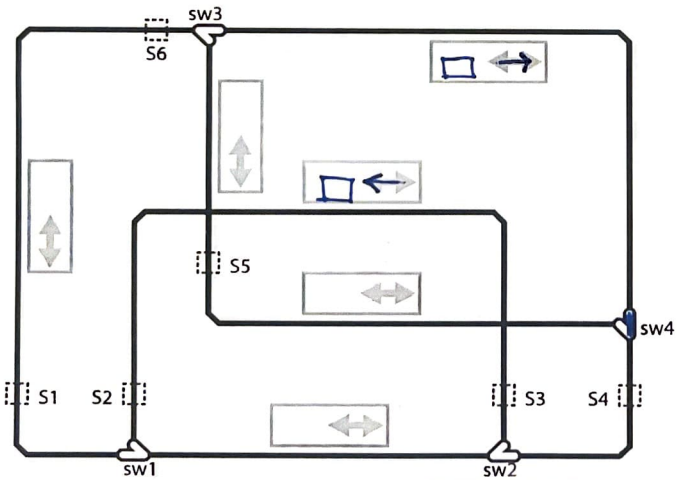
State: Arev Bin

Input	Next State
S3	Start Arev
S4	Bin
S3 S4	Ain Rev



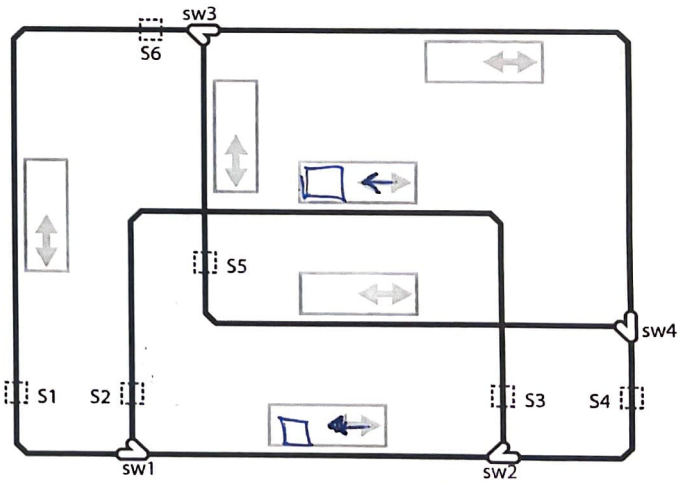
State: ARevBin Rev

Input	Next State
S2	Start Arev Brev
S4	Bin Rev
S2S4	Ain Rev Brev



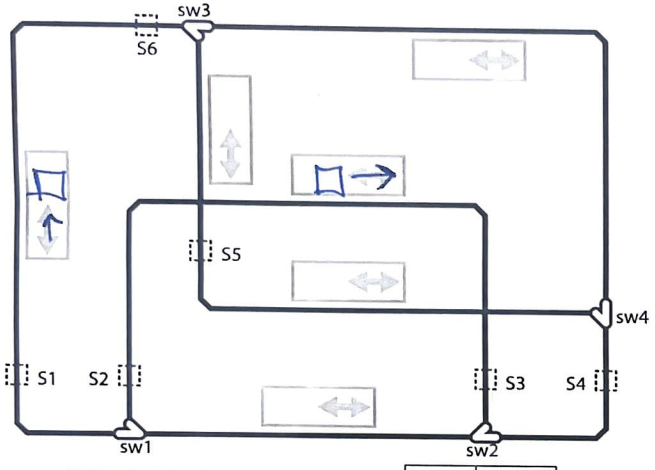
State: Start Arev

Input	Next State
S4	Ain Rev
S2	ARevBin
S4S2	Bin



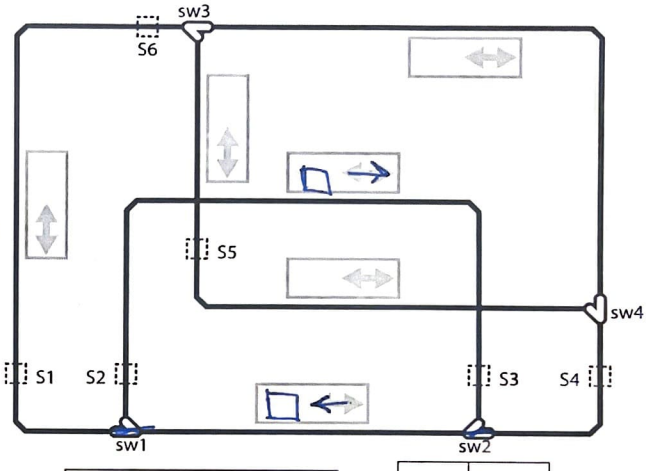
State: Ain Rev

Input	Next State
S1	Start Arev
S2	Ain Brev
S1S2	Arev Bin



State: Start ArevBrev

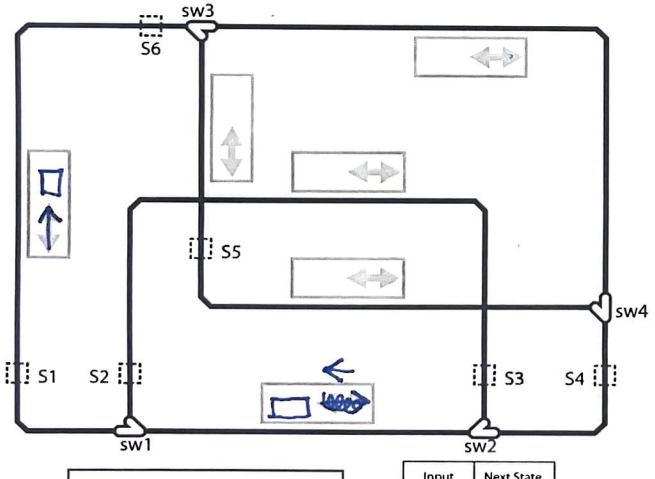
Input	Next State
S4	AinRev Brev
S3	Arev Binrev
S4S3	BinRev



State: AinRev Brev

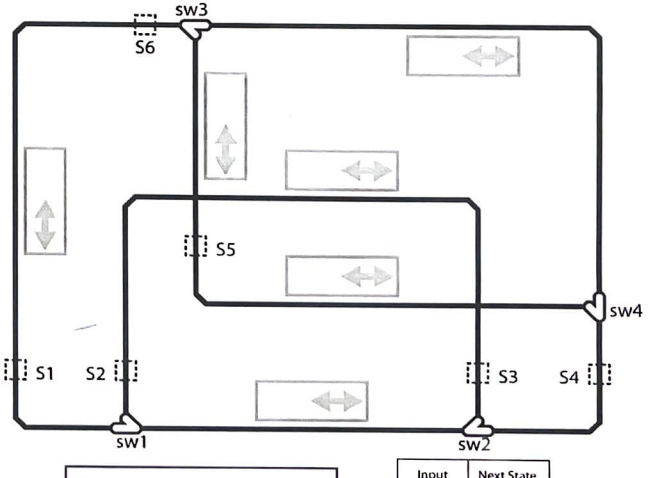
Input	Next State
S1	Start
S3	AinRev
S1S3	ArevBinRev

ArevBrev



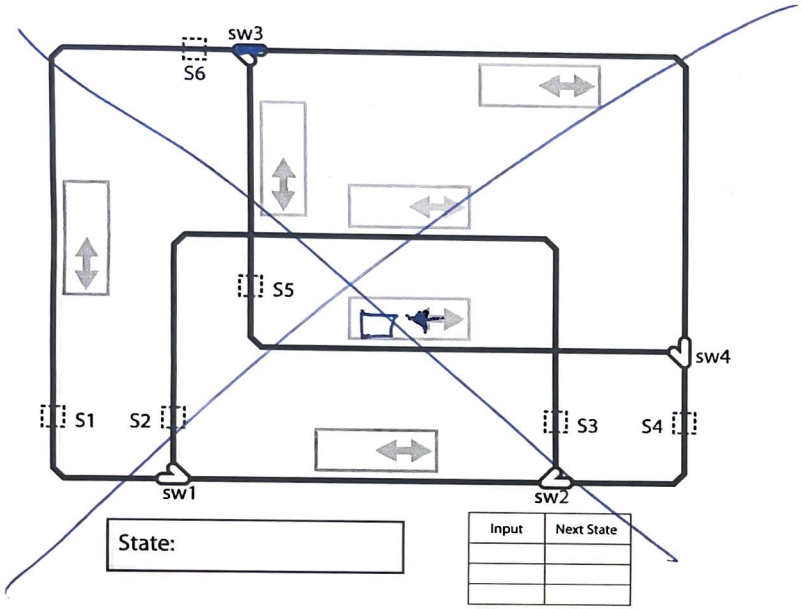
State: Arev Binrev

Input	Next State
S2	Start ArevBrev
S4	BinRev
S2S4	AinRevBrev



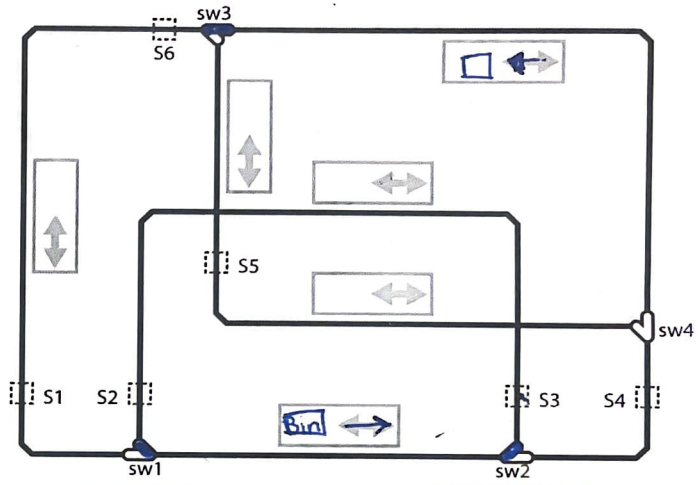
State:

Input	Next State



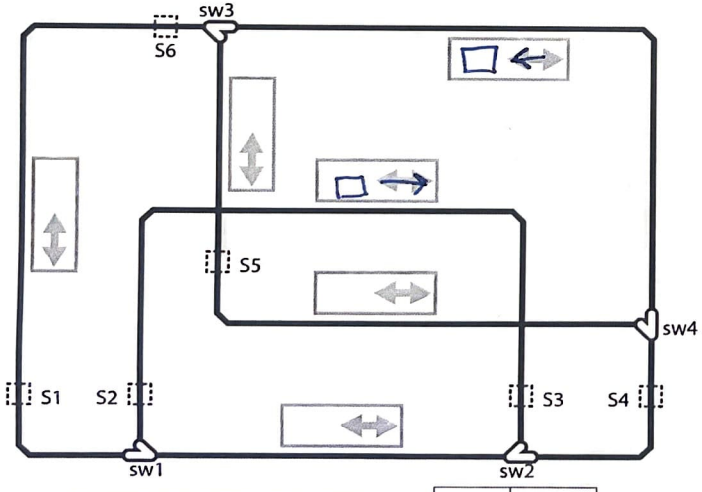
State:

Input	Next State



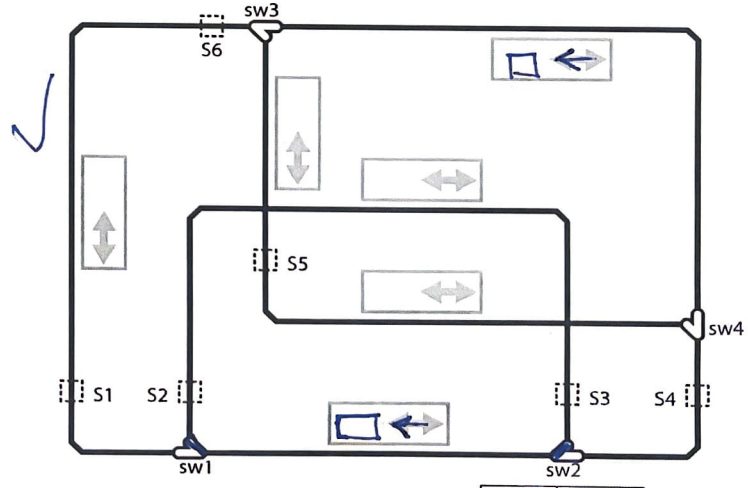
State: Bin

Input	Next State
S3	Start
S1	ARev Bin
S3S1	Ain



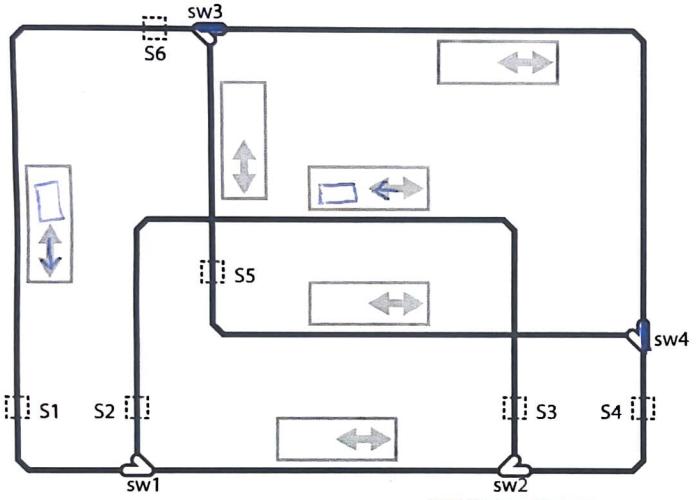
State: Start Brev

Input	Next State
S1	BACK BAin
S3	~~Bin~~ Bin ARev
S1S3	Ain



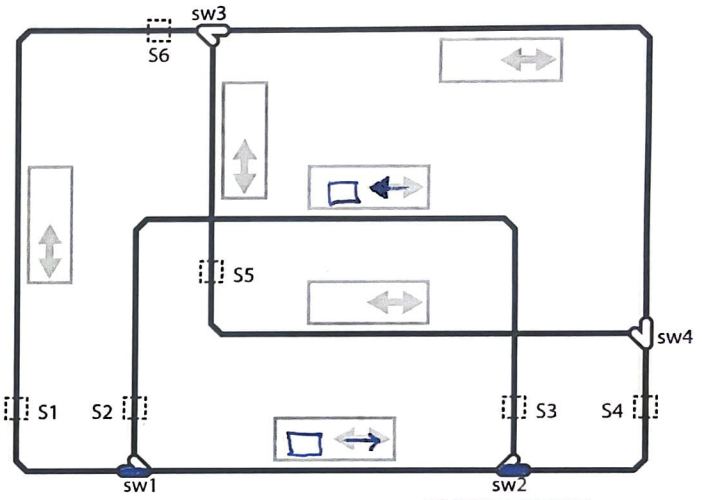
State: Bin Rev

Input	Next State
S3	Start BRev
S1	ARev BinRev
S3S1	Ain Brev



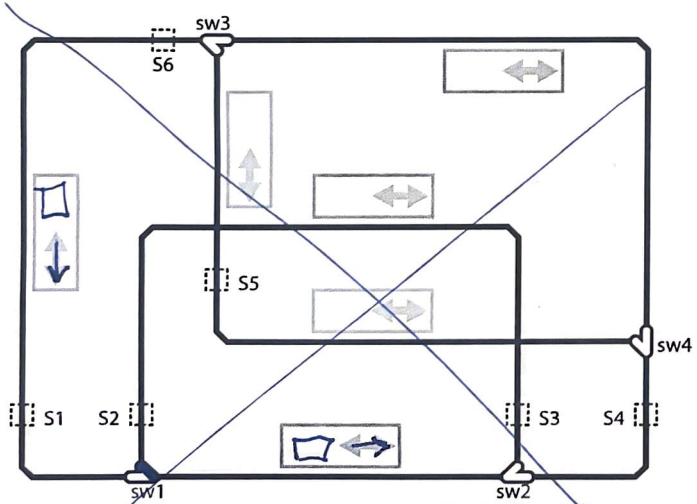
State: Start

Input	Next State
S1	Ain
S2	Bin
SW1	Back BAin
SW2	



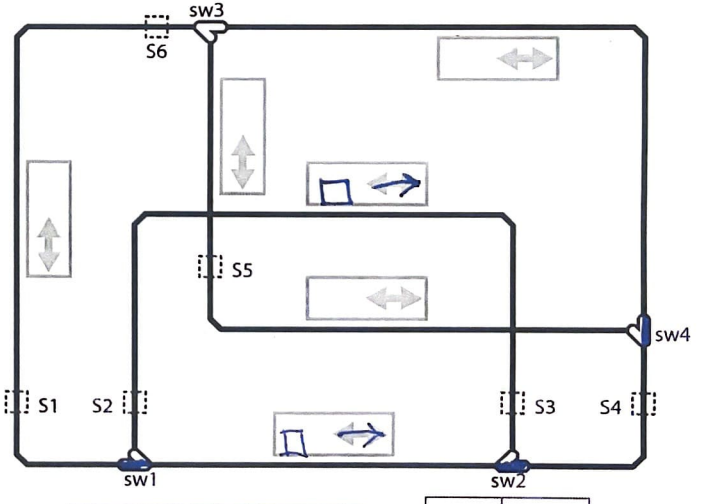
State: Ain

Input	Next State
S2	Back B Ain (Ain Brev)
S4	Start
S3S4	Bin



State: Enter

Input	Next State



State: Back B Ain

AinBrev

Input	Next State
S3	Ain
S4	Start Brev
S3S4	BinRev

1 straigt 1 angled 01 forward 10 back ward

Outputs	States							
	Start	Ain	Ain Brev	Bin	Start Brev	Bin Rev	Start Arev Brev	Ain Arev Brev
Sw1	0	0	0	1	0	1	0	0
Sw2	0	0	0	1	0	1	0	0
Sw3	0 →							→
Sw4	↓							
DA[1..0]	01	01	01	01	01	01	10	10
DB[1..0]	01	01	10	01	10	10	10	10

Outputs	States							
	Arev Bin Rev	Arev Bin	Start Arev	Ain Rev				
Sw1	1	1	0	0				
Sw2	1	1	0	0				
Sw3	0 →							→
Sw4	↓							→
DA[1..0]	10	10	10	10				
DB[1..0]	10	01	01	01				

Outputs	States							
Sw1								
Sw2								
Sw3								
Sw4								
DA[1..0]								
DB[1..0]								