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Lab Report 3

ECE 2031 L09

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-- RPS_VHDL.vhd (VHDL)
-- This code produces the the results of LED rock paper scissors
simulation
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-- ECE 2031 L09
-- 2/10/22

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity RPS_VHDL is
-- Describes the device from the outside
    port(      -- Defines the signals coming into and out of the device
        R1, P1, S1  : in  std_logic;
        R2, P2, S2  : in  std_logic;
        W1, W2      : out std_logic;
        E1, E2      : out std_logic
    );
end RPS_VHDL;

architecture Internals of RPS_VHDL is
    -- Define the internal architecture of the device

    -- Create a 6-bit vector that will give us easy access to all
    -- inputs
    signal all_inputs : std_logic_vector(5 downto 0);

begin
    -- "&" is CONCATENATION, not logical AND.
    all_inputs <= R1 & P1 & S1 & R2 & P2 & S2;

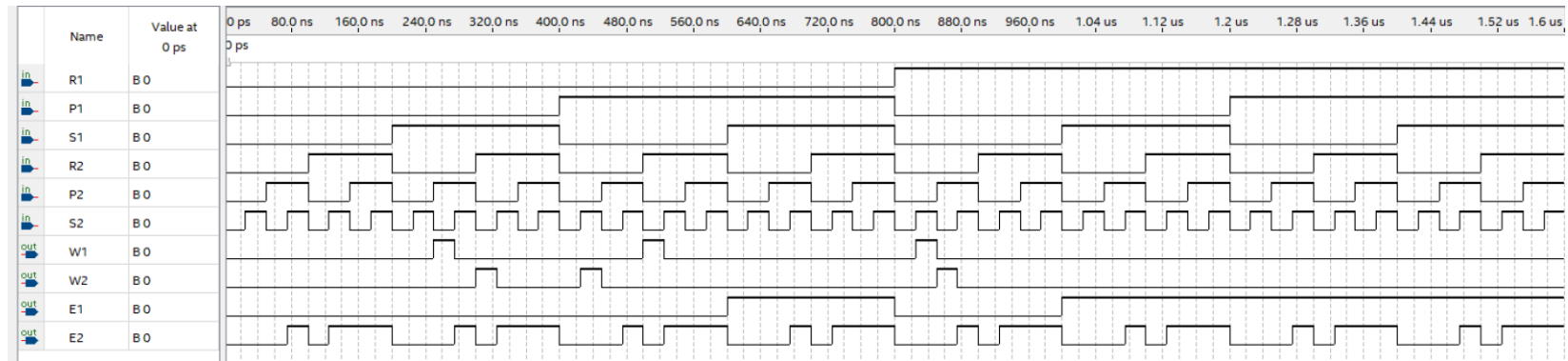
    -- Using a "selected signal assignment", aka "with/select"
    with all_inputs select
    W1 <=
        '1' when "100001",
        '1' when "010100",
        '1' when "001010",
        '0' when others;

    -- Using a "conditional signal assignment", aka "when/else"
    W2 <=
        '1' when (all_inputs = "100010") or (all_inputs = "001100")
        or (all_inputs = "010001") else
        '0';

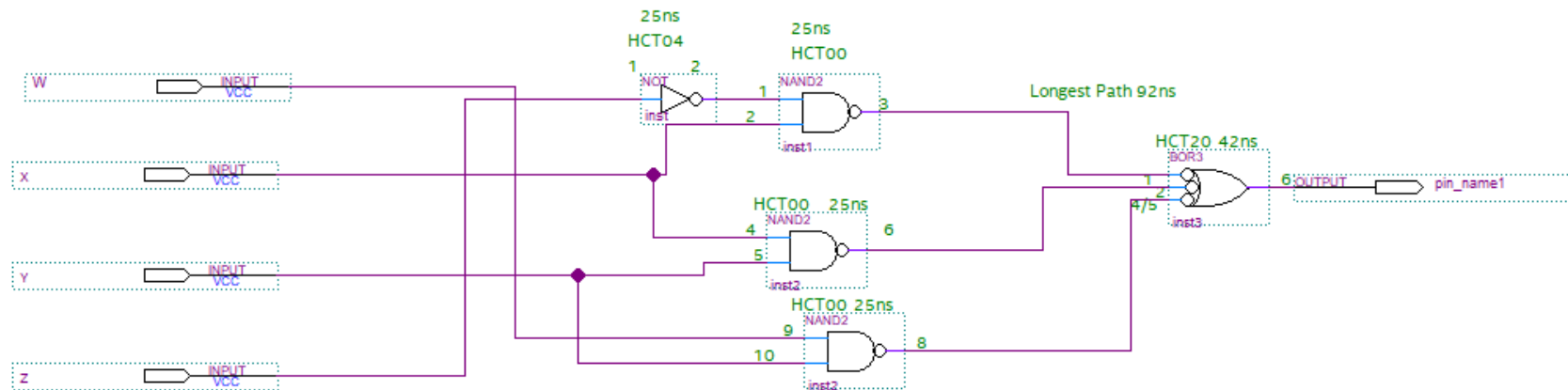
    -- Using when/else in a different way
    E1 <=
        '1' when ((R1 = '1') and (S1 = '1')) or ((R1 = '1') and (P1
        = '1')) or ((S1 = '1') and (P1 = '1')) else
        '0';
    -- Using Boolean expression
    E2 <= (R2 and S2) or (R2 and P2) or (S2 and P2);
end Internals;

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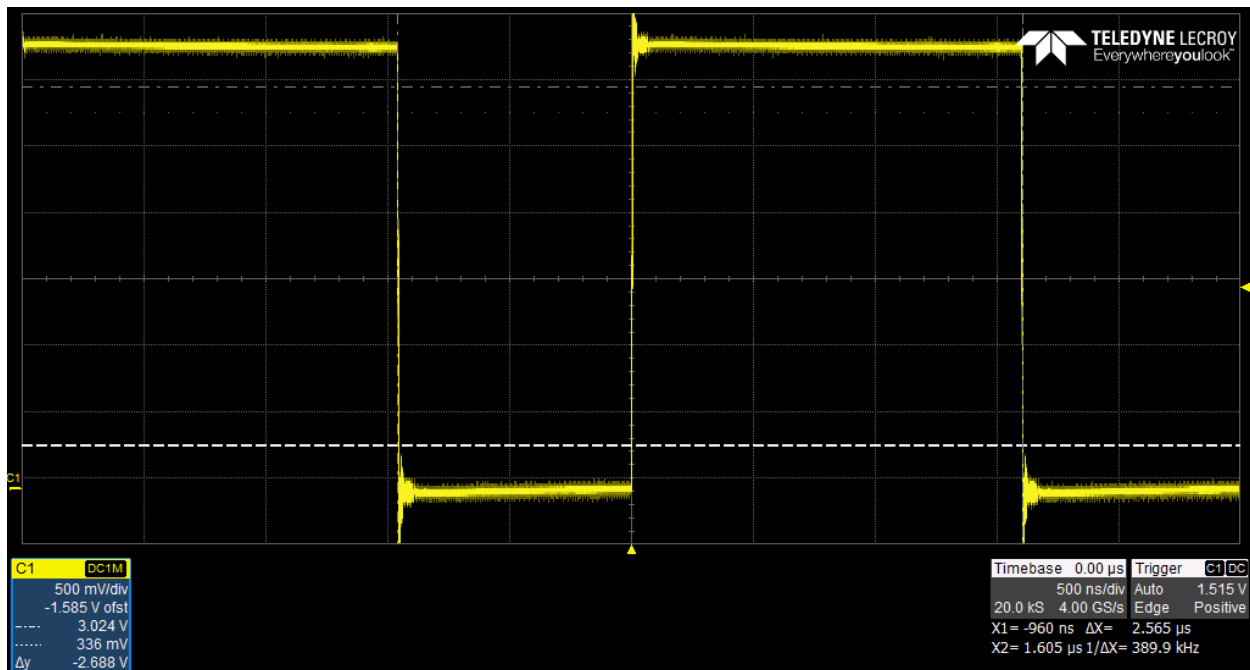
**Figure 1.** VHDL Code used to emulate the results of a rock, paper, scissors game.



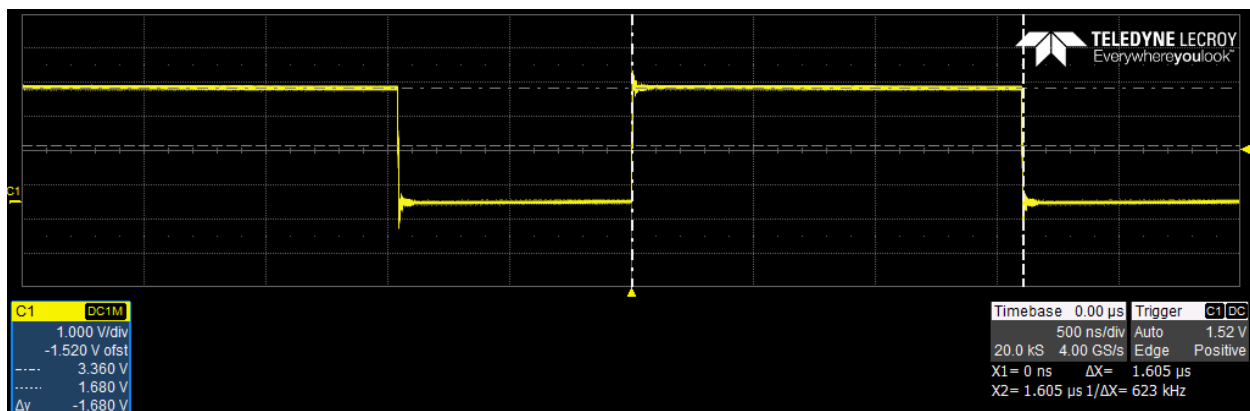
**Figure 2.** Functional simulation waveform of rock, paper, scissors emulator with 6 inputs and 4 outputs. The input vector covers all possible input states to prove the correctness of the circuit.



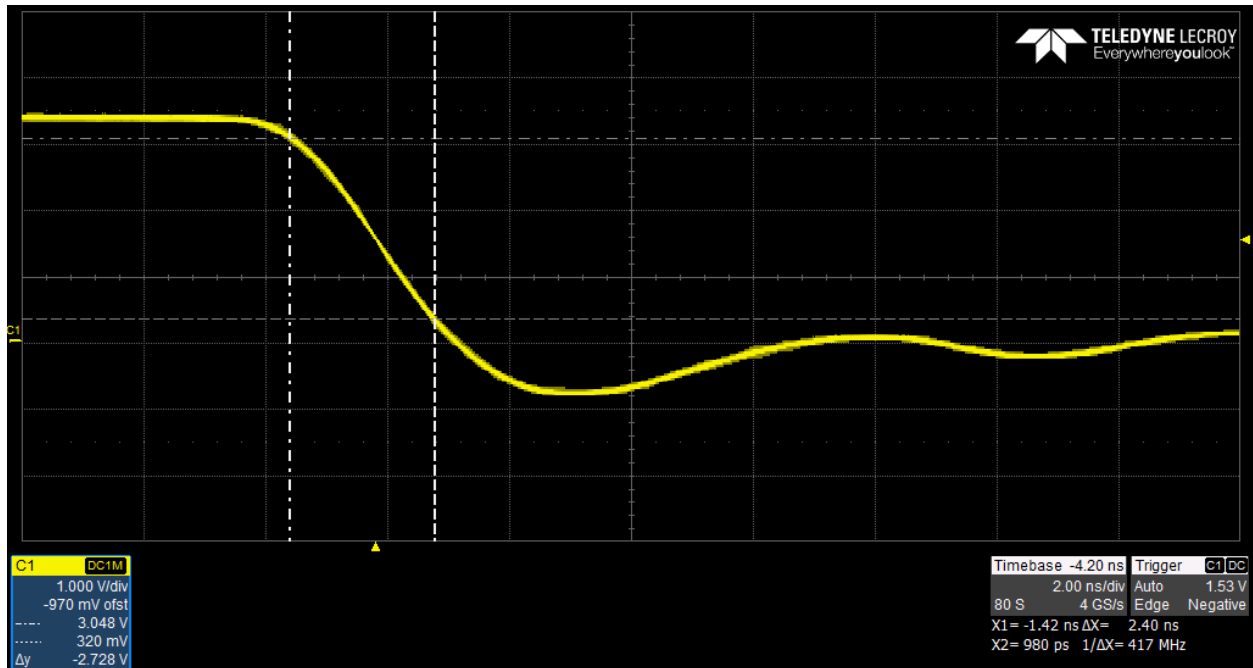
**Figure 3.** Circuit Schematic implanting the logic function  $\text{Output} = X/Z + X \cdot Y + Y \cdot W$ . It shows each gate's worst case propagation delay and the circuit's worst possible delay of 92ns which runs through the upper path, through an inverter, and 2 nand gates.



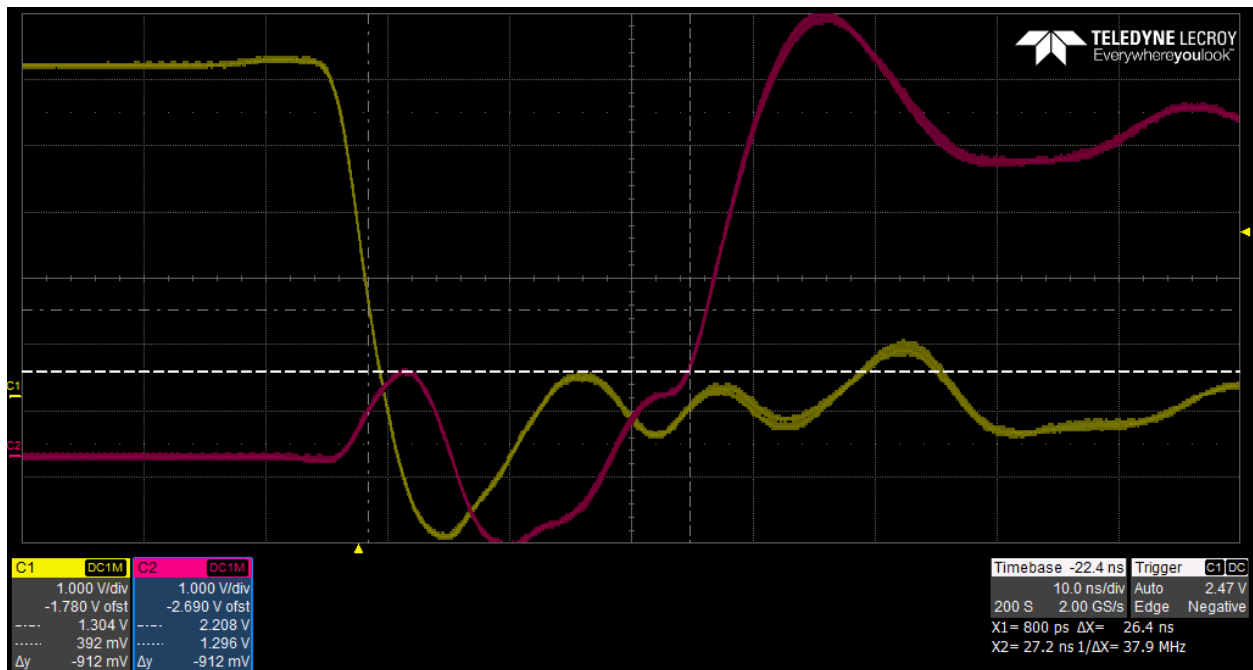
**Figure 4.** The unknown circuit in Lab3SignalGen.sof running on a DE10-Lite board. The period of the unknown square wave was calculated ( $\Delta X$  in the corner) to be 2.565  $\mu\text{s}$ .



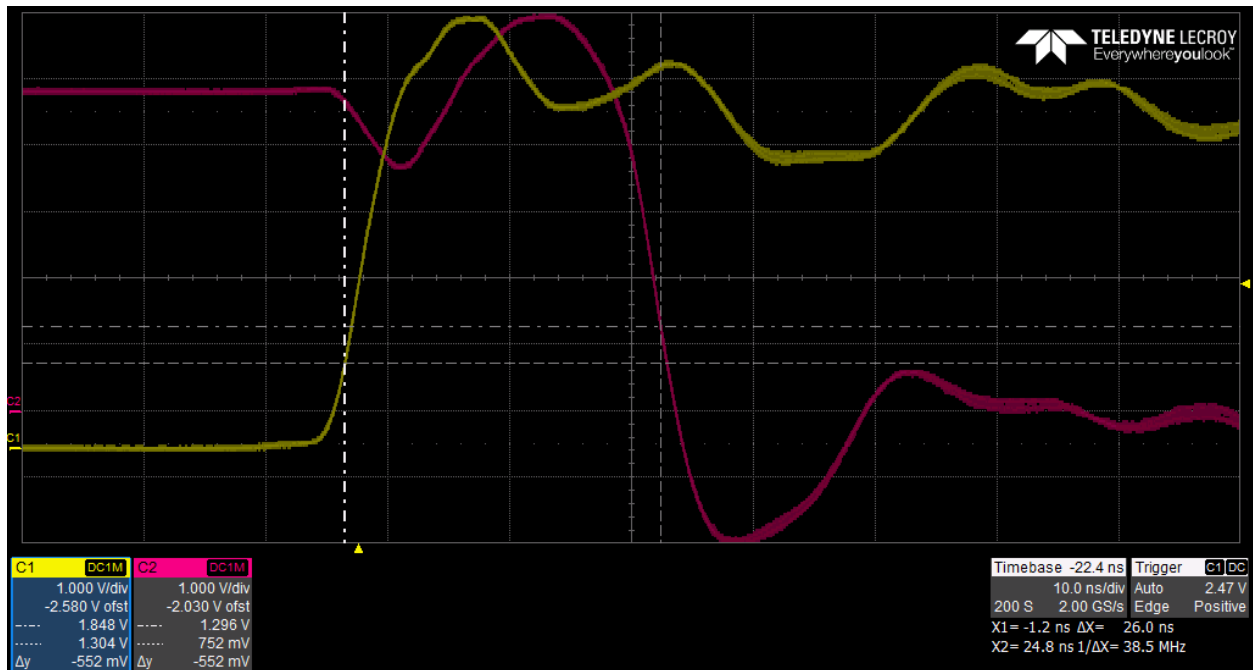
**Figure 5.** The unknown circuit in Lab3SignalGen.sof running on a DE10-Lite board. The duty cycle of the unknown square wave was calculated ( $\Delta X$  in the corner over the period) to be 65.497%.



**Figure 6.** The unknown circuit in Lab3SignalGen.sof running on a DE10-Lite board. The fall time of the unknown square wave was calculated ( $\Delta X$  in the corner) to be 2.40  $\mu\text{s}$ .



**Figure 7.** A measure of the propagation delay of a breadboard circuit. The input is the yellow waveform and the output is the magenta waveform. The high to low propagation delay was found to be 26.4  $\mu\text{s}$ .



**Figure 8.** A measure of the propagation delay of a breadboard circuit. The input is in yellow and the output is in magenta. The high to low propagation delay was found to be 26.0  $\mu$ s.