Integrated Smart Sensor Concept

2

2.1 Introduction

In this chapter we will present a concept for implementing smart sensor interfaces [1]. Within the scope of this work we cannot discuss many types of sensors or sensor interfaces, hence we limit ourselves to two common sensor types, for measuring temperature, and for measuring pressure. This limitation does not mean that the presented matter cannot be extended to other types of sensors.

We will explain the basic principle of operation of a monolithic temperature sensor, and a pressure sensor based on piezoresistors. We will then show the circuitry which is necessary to read out the sensors and derive signals suitable for AD-conversion. The preferred type of AD-converter, a sigma-delta converter, will also be explained, as well as a possible serial bus interface.

G. van der Horn et al., *Integrated Smart Sensors*

2.2 Silicon sensors

The temperature sensor and the pressure sensor are both IC-compatible and thus very suitable examples in the context of smart sensors.

2.2.1 Temperature sensor

The difference in base-emitter voltage of two transistors with different current densities exhibits a linear relation with respect to the absolute temperature [2,3]. We take two equal transistors and bias them with currents that are scaled by a factor of four, as illustrated in Fig.2-1.

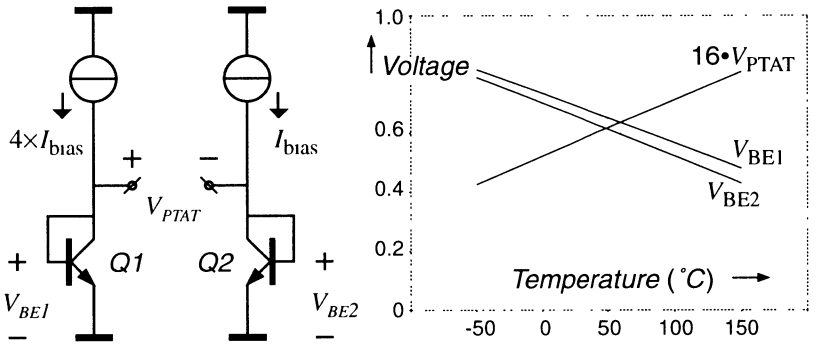

Fig. 2-1 *Temperature sensor principle based on PTAT voltage.*

We can easily derive from the formulas for the collector currents,

$$I_{C_{Q1}} = I_{S_{Q1}} \cdot e^{\left(\frac{q}{kT} V_{BE_{Q1}}\right)} = 4 \times I_{BIAS}$$
$$I_{C_{Q2}} = I_{S_{Q2}} \cdot e^{\left(\frac{q}{kT} V_{BE_{Q2}}\right)} = I_{BIAS} \qquad (2\text{-}1)$$

that a (PTAT) voltage proportional to the absolute temperature T results:

$$\Delta V_{BE} = V_{BE_{Q1}} - V_{BE_{Q2}} = \frac{kT}{q} \cdot \ln\left(4 \cdot \frac{I_{S_{Q2}}}{I_{S_{Q1}}}\right) \qquad (2\text{-}2)$$

In which k represents Boltzmann's constant, q the electron charge and I_S the transistor saturation current. The case of equation (2-2), using a current density ratio of four, and $I_{SQ1} \approx I_{SQ2}$, results in a small positive temperature coefficient of approximately 0.12 mV per Kelvin. The base-emitter voltage itself demonstrates a much larger but slightly less linear temperature dependency which can be expressed in the form of a Taylor expansion of the V_{BE} curve at a reference temperature T_R:

$$V_{BE} = V_{BG_{T=0}} + (\eta - m) \cdot \frac{kT_R}{q} + \lambda_{T=T_R} \cdot T - \frac{1}{2}(\eta - m) \cdot \frac{kT_R}{q} \cdot \left(\frac{T - T_R}{T_R}\right)^2 \quad (2\text{-}3)$$

In this equation V_{BG} represents the silicon bandgap voltage, λ the linear temperature coefficient which measures approximately -1.9 mV/K at T_R=300K, and (η-m) a physical parameter of about 3.5 which is somewhat process dependent. The voltage signals V_{BE} and V_{PTAT} are displayed in Fig.2-1, where the PTAT voltage had to be magnified by a factor of 16 to obtain a comparable temperature coefficient. Both effects can be used for measuring temperature. In section 2.3.1 will be shown how to combine both signals in a fully integrated circuit and to circumvent the need for an external reference voltage.

2.2.2 Pressure sensor

A well-known principle for measuring pressure is by the use of a thin membrane or diaphragm, because a diaphragm tends to deflect under pressure. Micromachining techniques make it possible to fabricate thin mechanical structures on a silicon wafer, even without harming the integrated circuits processed on the same wafer [4,5,6,7,8,9]. A common technique, known as bulk-micromachining and also accomplished at DIMES, is to (KOH) etch the masked backside of the wafer (p-substrate) and obtain an electrochemical etch stop by applying a voltage to the n-epi or buried-n layer at the frontside. In that way the wafer thickness (~500μm) can be locally reduced, under an angle of approximately 55°, to epi-thickness (~3-7μm), whereas the horizontal dimensions can be controlled by the backside mask [10,11]. In this way, a structure as illustrated in the pictures of Fig.2-2 can easily be fabricated.

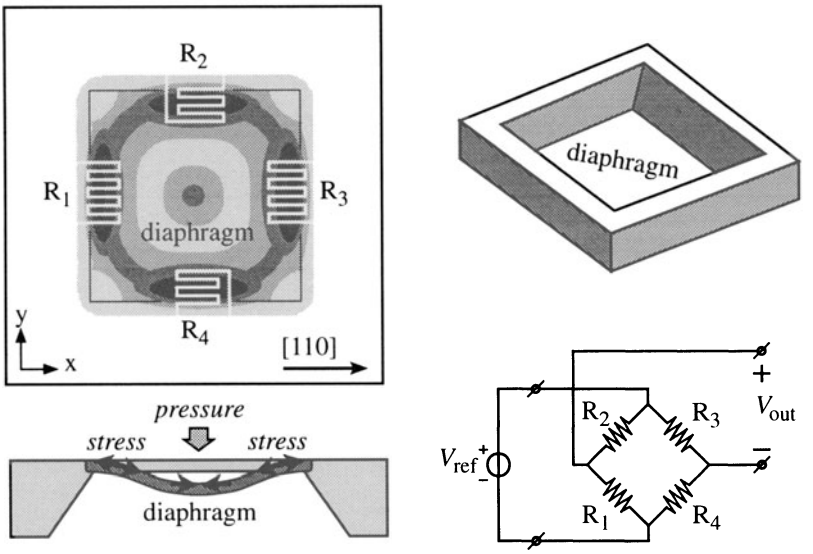

Fig. 2-2 *Pressure sensor principle with Wheatstone bridge.*

Now the art is in electrically sensing the pressure induced deflection of the micromachined diaphragm. A capacitive technique seems attractive but has the disadvantage that another capacitor plate is required, which has to be fabricated/mounted as close as possible to the diaphragm for maximum capacitance signal [12,13,14]. This is problematic considering the packaging and the electrical connections, as well as incompatible with some of the pressure sensor types indicated in Fig.2-3 because of the required backside opening [7]. Solutions making use of wafer-to-wafer or wafer-to-glass bonding are still under development [5,11,15,15].

An already well-developed method makes use of silicon piezo-resistors [7,16,17]. As indicated in the cross-section and top view of the sensor in Fig.2-2, the deflection of the diaphragm results in a shear stress at the surface of the diaphragm. Provided that the silicon lattice is correctly oriented, the piezoresistance effect of silicon can be used to sense the change in stress [4,17,18]. The topview also gives an impression of the (absolute) stress profile when under pressure; the darker areas have larger stress, and the stress-sensitive piezoresistors are thus placed in those areas. The orientation of the resistors is such that the stress results in an increase of resistance for R_1 and R_3 and a decrease for R_2 and R_4. The silicon resistors (shallow-*p* diffusion) can be fabricated using standard IC

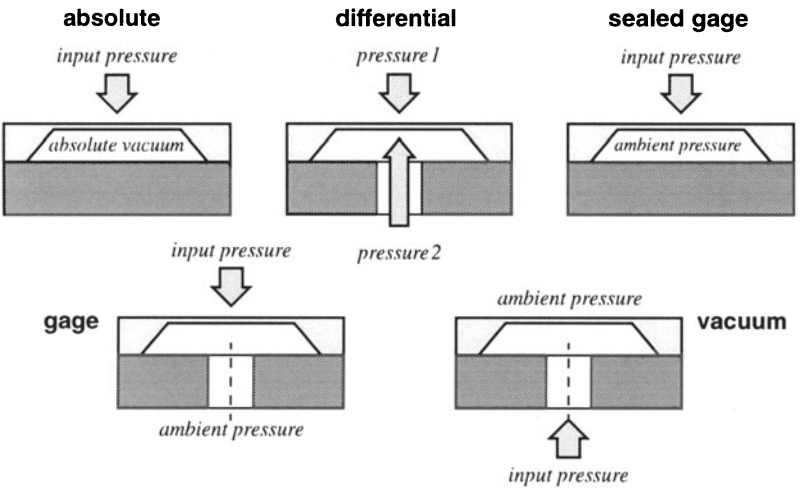

Fig. 2-3 *Different types of pressure sensors.*

processing (on the same wafer), and are connected in a Wheatstone bridge configuration, as shown in Fig.2-2. A pressure-related output voltage signal, V_{out}, proportional to the bridge supply voltage, V_{ref}, is thus generated [7].

2.2.3 Measurement errors

In the fabrication of sensors certain changes in process parameters and also in material (wafer) properties will have to be tolerated, and, ergo, a variation in the properties of the sensors, even when produced in the same process, must be expected. This usually results in a statistical (Gaussian) distribution of the errors in the transfer of the sensors with respect to the average sensor transfer. The manufacturer tries to get the average sensor transfer as close as possible to the desired sensor function, and to minimize the deviation of the transfer errors. Generally the spread in the error is much larger than the desired accuracy, and selection or calibration is required in order to obtain accurate sensors.

In case of the PTAT sensor the variations in the transfer are determined by the matching properties of standard electronic components. This will be examined in section 2.3.1.

In the framework of a master thesis' project on pressure sensor self-test some bulk-micromachined pressure sensors have been developed and realized in the DIMES-01 process. We will use those sensors as an example. Several of these devices have been measured using DRUCK test equipment. Fig.2-4 shows the transfer, relative bridge output voltage versus pressure, of two sensors (Sensor1 & Sensor2) with a diaphragm of $400 \times 400\ \mu m^2$, and two sensors (Sensor3 & Sensor4) with a larger diaphragm of $800 \times 800\ \mu m^2$. Naturally, the dimensions of the diaphragm (size and thickness) determine the pressure sensitivity and the pressure range in which the sensors can be used.

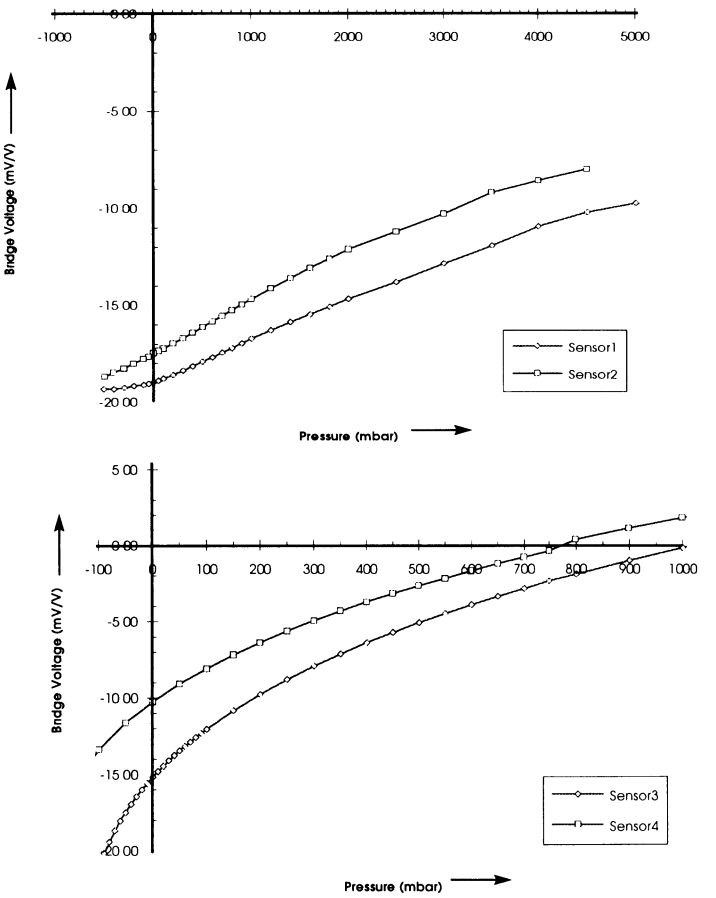

Fig. 2-4 *Measured transfer of pressure sensors developed in Dimes-01.*

Despite the fact that the sensors come from the same wafer, a significant difference in offset and sensitivity between two sensors is found, for both cases. An even larger difference can be expected when also taking into account the variation in temperature coefficients of offset and sensitivity. The large offset errors in the shown examples are mainly due to imperfections in the first resistor layout, which can easily be improved in a next version. Nevertheless, error sources such as initial stress, geometrical variations, doping concentration profiles, and resistor mismatch will result in a large error variations. The sensor construction does not allow to put resistors close together to improve matching. The source of the signal errors also explains why there is not a typical sensor-characteristic nonlinearity error but a large device-to-device variation. An overview of error contributions in piezoresistive pressure sensors can be found in [7:chapter 4] and [19]. A total error band of 30% of the full-scale can be a reasonable expectation.

Notwithstanding, one of the largest sensor markets is that for pressure transducers. Thus a strong push from that market is expected for stimulation of integrated calibration techniques. We have to conclude that in order to realize production of a pressure sensors with standard transfer from pressure range to output range, the calibration will have to compensate large error variations.

2.3 Analog Interface circuits

2.3.1 Temperature sensor readout

To enable the read-out of a temperature signal, as presented in section 2.2.1, by an AD-converter, another signal has to be generated which can be used as a reference. Hence, we will first describe the construction of a so-called bandgap reference. The temperature signal and the reference signal must be combined in such a way that a ratiometric signal is obtained which makes optimal use of the AD-converter's signal range. This will be explained next.

By summing a V_{BE} signal and a signal proportional to V_{PTAT} the first-order (linear) temperature coefficients can be cancelled, and a reference signal results, which is referred to as bandgap reference. As can be seen from equation (2-3) it relates directly to the bandgap voltage V_{BG}, although a

small offset error and second-order error are present. Bandgap references and PTAT *current* sources are well-known circuits in IC design as they are often used for biasing purposes.

The left half of the circuit displayed in Fig.2-5 shows a low-voltage PTAT source [20], which makes use of the ratio-ed transistors Q1 and Q2. These transistors are inserted in a control loop that establishes equal bias currents for both transistors. Because of the ratio in current density the difference between the base-emitter voltages is proportional to the absolute temperature, as already shown in equation (2-2). The value of the bias current is determined by the PTAT voltage at the emitter of Q2 and the value of resistor R_1. The current I_{VPTAT} inherits the proportional-to-absolute-temperature property of the voltage. The current mirror on the left-hand side only serves to generate a small start-up current to prevent a zero bias solution at start-up.

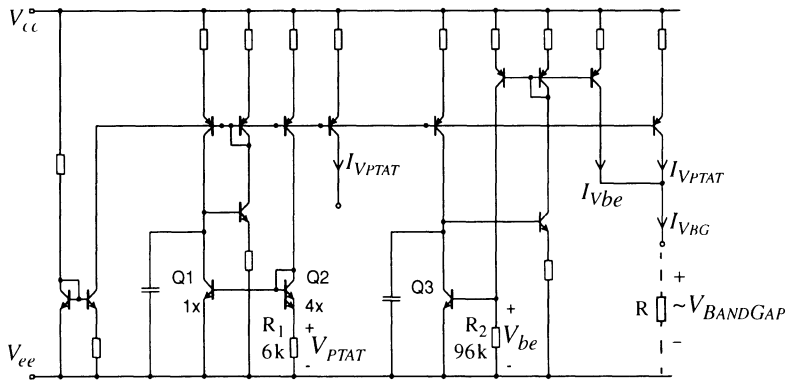

Fig. 2-5 *Bandgap reference and PTAT current generator.*

The right-hand side of the circuit, around Q3, generates a current which is determined by the base-emitter voltage of Q3 and the value of resistor R_2. The current I_{Vbe} thus inherits the V_{be} temperature characteristic, including the negative temperature coefficient.

The two current signals can easily be summed at the output, resulting in $I_{VBG}=I_{Vbe}+I_{PTAT}$. When inserting that current in a resistor R, it is converted back into a voltage signal. The voltage will then be proportional to the weighed sum of the PTAT voltage $V_{PTAT}\bullet R/R_1$ and the base-emitter voltage $V_{be}\bullet R/R_2$, which can be equalized to the silicon bandgap voltage.

A simulation of the circuit, see Fig.2-6, shows the PTAT signal with a positive temperature coefficient, the V_{BE} signal with a negative temperature coefficient, and the constant sum signal. By correctly dimensioning the ratio of the resistor values of R_1 and R_2, in this case a ratio of 16, the temperature coefficients of both current signals can be matched so that the sum of the currents, referred to as I_{VBG}, remains constant as a function of temperature.

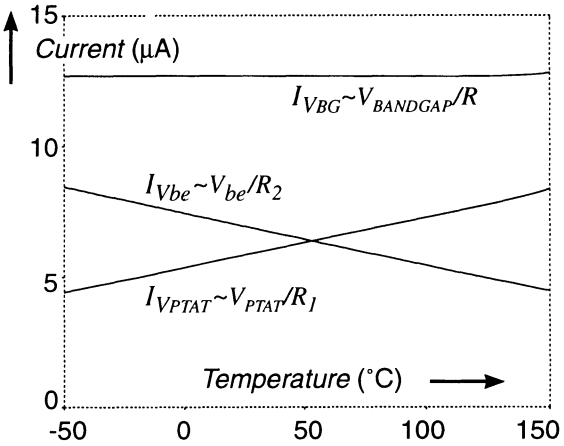

Fig. 2-6 *Current signals as function of temperature, using ideal resistors.*

The simulation shown in Fig.2-6, was done for ideal resistors, meaning that the resistance was considered independent of temperature. In reality the temperature coefficients of the resistors directly affects the curves of the *current* signals. However, when using the same kind of resistors for R, R_1, & R_2, the bandgap *voltage* signal will not be affected because it depends on the resistor ratios. Similarly, the effect of the temperature coefficients will cancel if we use the ratio of two current signals.

Temperature sensor circuit

For use in a smart temperature sensor with AD-converter we like to realize a circuit which generates two current signals of which the ratio varies approximately from 10% to 90% for the intended temperature range. Within the operating temperature range of IC technology, the ratio of the PTAT and the bandgap reference signal varies from 35% to 65%. Therefore, we prefer not to use that ratio directly, but to modify the current signals.

This can be done by combining the PTAT and bandgap currents, for example in the way shown in Fig.2-7. A fraction of the bandgap current is copied and subtracted from the PTAT current to generate a new temperature current signal I_T. A down-scaled copy of the bandgap current is used as a new reference current signal I_{REF}.

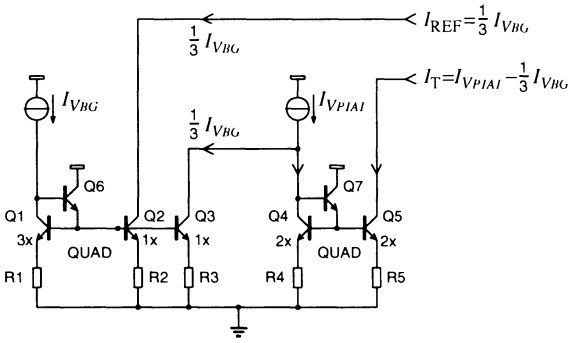

Fig. 2-7 *Temperature "sensor" circuit generating I_T and I_{REF}; I_{VBG} and I_{VPTAT} come from the circuit of* Fig.2-5.

The simulation displayed in the upper graph of Fig.2-8, shows the two currents as a function of temperature, now taking into account the temperature coefficients of the resistors in the IC process. It clearly shows

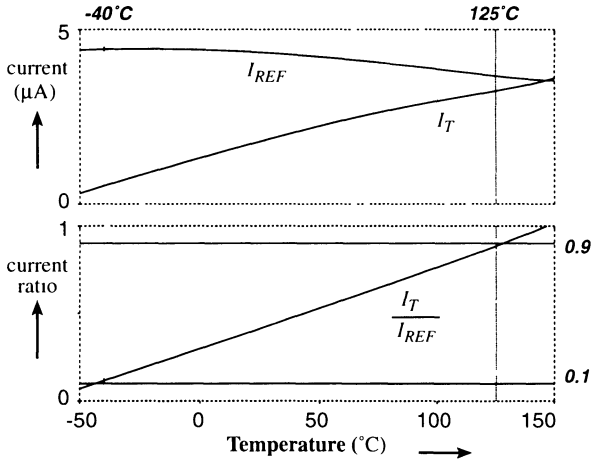

Fig. 2-8 *Ratio of I_T and I_{REF} used as measurement signal.*

that the absolute current I_{REF} is certainly not constant, and that I_T is not so linear. However, the ratiometric signal I_T/I_{REF}, displayed in the lower half of Fig.2-8, is good and is not affected by the temperature dependence of the resistors. The sensor circuit is dimensioned in such a way that the ratiometric signal range of [0.1-0.9] maps on the temperature range of -40 °C to +125 °C. The current mirrors in the sensor circuit of Fig.2-7 can be dimensioned differently to obtain a different temperature range, within the operation limits of ICs of course.

To study the effect of process variations on the signal, a simulation has been done for a worst-case relative mismatch of ±0.5% and an absolute variation of ±25%. Fig.2-9 shows the results on the ratiometric signal and the error with respect to the desired linear curve.

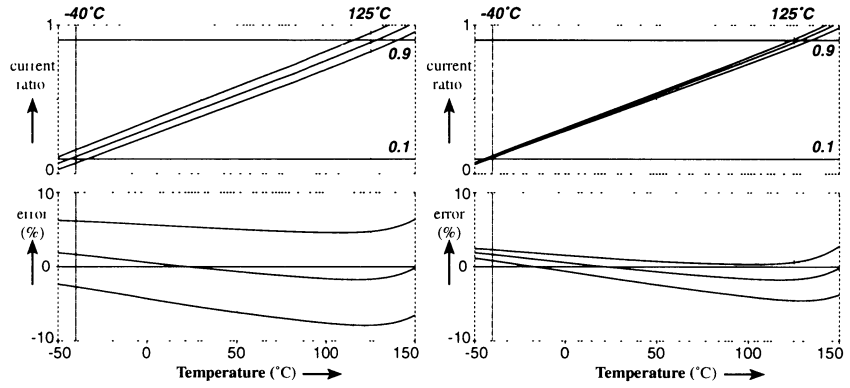

Fig. 2-9 *Effect on transfer and error curves resulting from worst-case relative (1%) and absolute (50%) variations.*

First of all, it demonstrates that the effect of relative errors is much larger. Second, it can be concluded that, in fabrication of such temperature sensors, a spread in offset and gain errors of several percents, say ±5%, should be expected. The linearity error will be relatively small, in the order of 1%, for the specified temperature range. To realize a silicon temperature sensor with exactly the desired transfer from temperature to ratiometric output, these errors will have to be calibrated. Furthermore, it has to be noticed that the nonlinearity curve has a shape that is characteristic to this type of sensor. The shape doesn't vary much from device-to-device. It is determined by the nonlinearity in the V_{BE} curve as expressed in equation (2-3). The temperature coefficient of the resistors is a second

source for nonlinearity but results only in a very small device-to-device variation of the nonlinearity error.

2.3.2 Pressure sensor readout

The piezoresistive pressure sensors based on a Wheatstone bridge configuration inherently make use of a ratiometric conversion; as explained in section 2.2.2 a pressure signal will result in an output voltage signal related to the bridge reference voltage. The AD-conversion which follows the analog readout circuitry has to realize a conversion of this ratiometric signal, by using both the bridge output voltage and the bridge reference voltage. As seen in section 2.2.3, pressure sensors may display an offset which is in the same order of magnitude as the full-scale signal range. This offset can be eliminated by using a chopping technique. As an example, Fig.2-10 gives an overview of a bridge interface circuit which fulfils these requirements [21]. A combination of standard analog cells of the DIMES-01 library and custom cells has been used for the realization of this circuit.

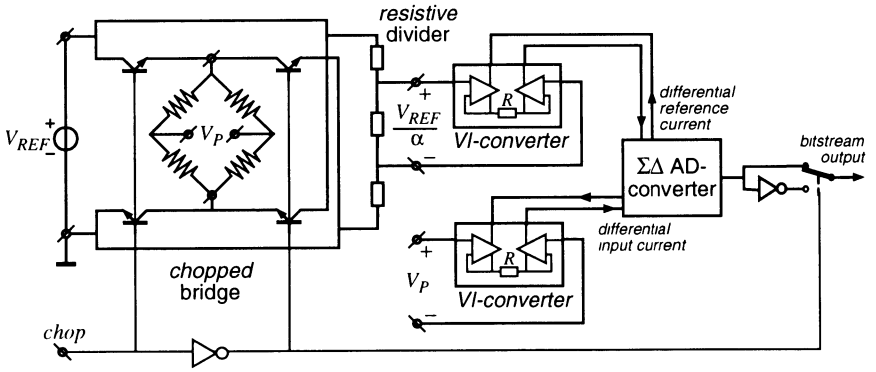

Fig. 2-10 *Pressure bridge readout circuit.*

The chopping is implemented by using saturated bipolar transistor switches which invert the polarity of the bridge reference voltage. Changing the polarity of the reference voltage, inverts the polarity of the bridge output voltage signal but not that of the bridge offset voltage. By subtracting the inverted and non-inverted signal the bridge offset is eliminated. This is preferably done at the end of the signal chain, as shown in the figure, so that all other offset contributions are removed as well.

As seen in section 2.2.3, the ratiometric bridge signal usually does not get much larger than 1-2%. To optimally use the dynamic range of the AD-converter it is necessary to scale down the bridge reference signal. In Fig.2-10 this is realized with, accurately scaled, and carefully laid-out resistors. Both the down-scaled reference voltage, and the bridge output voltage, are converted to currents, using VI-converters, and passed on to the sigma-delta AD-converter for a ratiometric conversion.

For the pressure sensor as well as for the temperature sensor we have shown how to obtain a current ratio proportional to the sensor signal. The same can be done for many types of sensors. The obtained current ratio can be accurately converted into a digital (bitstream) signal, using the continuous-time sigma-delta converter explained in the next section.

2.4 Analog-to-Digital conversion

Much effort has been, and is being put in comparing resolution, speed, and power consumption of several AD-conversion principles and architectures, however it does not fit in the scope of this work to discuss all the investigated AD-converter types. Information can be found in [22,23,24], for example. We will confine to summarizing the advantages of the preferred AD-converter type, the delta-sigma or sigma-delta converter[1]. Advantages of sigma-delta converters are:

- *serial one-bit digital clock-synchronous output*
- *simple and compact architecture which can be implemented using a small number of components*
- *a low-power consumption, especially at low sample speeds*
- *no accurate components or component matching required*
- *exchange of sample speed and resolution possible*
- *high resolution possible (16-bit)*

Disadvantageous can be the fact that the digital bitstream output needs digital post-processing in the form of an averaging, or noise-shape filter, in order to convert the one-bit output signal to multi-bit samples, which can

[1] Both names, delta-sigma and sigma-delta, are common, and refer to the same type of converter.

be used in a digital processor. Such a filter might be implemented in hardware on a separate (CMOS) chip which can be connected to the sensor bus, or in software on a microcontroller or PC bus master. This enables a shared use of the filter for all the smart sensors that produce a bitstream output, see also section 2.5.

We will first proceed by explaining the sigma-delta conversion principle.

2.4.1 Sigma-delta converter

The sigma-delta principle is based on oversampling, and on feedback and filtering (noise-shaping) of the quantization error. The operation principle in the time domain will be explained using Fig.2-11 and Fig.2-12.

The basic sigma-delta converter consists of an integrator, often implemented in a feedback configuration using an OpAmp, and a clocked comparator, mostly implemented as a master-slave flipflop.

The fact that we largely oversample the input signal,

$$f_{clock} \gg f_{Nyquist} = 2 \times bandwidth \qquad (2\text{-}4)$$

permits the assumption that the input signal is considered constant for many clock periods.

The first figure illustrates the situation that the presumably constant input current is integrated on the integration capacitor, and results at the integrator output in a ramping voltage signal, with an upward slope proportional to the input signal. The clocked comparator compares this voltage signal to the comparator's reference level V_{cmp}, and outputs a digital decision, low or high, only once each clock period, for example at the positive clock edge. In this situation the output remains low until the first clock edge after the integrated signal exceeds the comparator's reference level. Then the comparator switches the output signal to high, and turns the switch of the reference current, as illustrated in the next figure. Provided that $I_{ref} > I_{in}$, an opposite integrator input current of $I_{ref} - I_{in}$ results now in a proportional negative slope at the integrator output. The comparator output is high until the integration signal has dropped below the reference level, and a clock edge occurs. The output will become low again, and the sigma-delta converter switches back to the situation of Fig.2-11, and the procedure repeats itself.

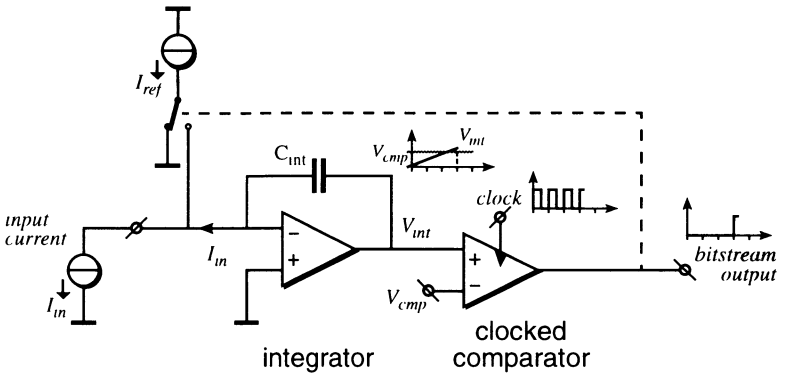

Fig. 2-11 *Sigma-delta converter principle, output low (A).*

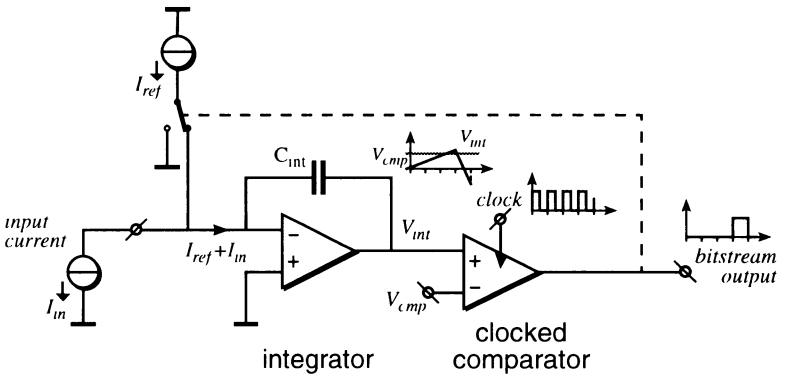

Fig. 2-12 *Sigma-delta converter principle, output high (A).*

When considering a larger number of clock periods we see that the integrator signal oscillates around the reference level, and the digital output produces a series, or pattern of ones and zeroes at the beat of the clock signal, as depicted in Fig.2-13 for an input signal of $I_{in}=0.19 \cdot I_{ref}$.

The input signal range is usually limited to the signal range from $0.1 \cdot I_{ref}$ to $0.9 \cdot I_{ref}$, to avoid very low slopes in the integrator signal. Through simple reasoning it can be found that a large input signal results in steeper upward slopes, and less steep downward slopes, and thus a large number of high outputs. The reverse applies for small input signals; the number of high outputs will be small. Hence the output pulse density seems proportional to the input signal; in fact the value of the input signal

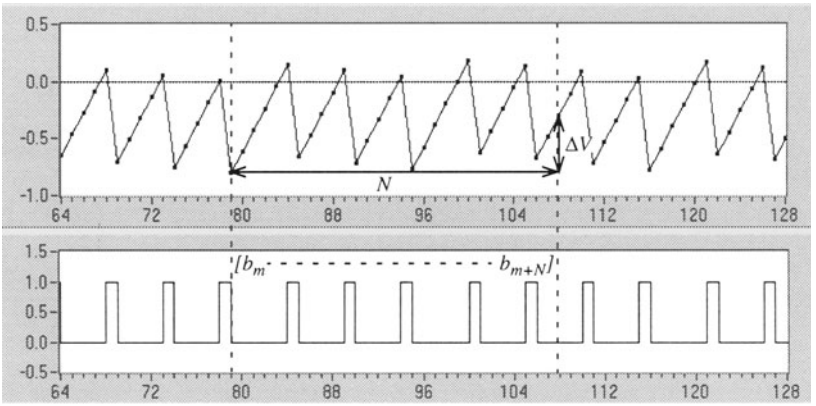

Fig. 2-13 *Sigma-delta integrator and bitstream signal.*

is encoded in the digital output bitstream. To obtain a digital number representing the input signal, the output bits will have to be counted (or otherwise processed) over a certain time interval, interpreting high outputs as *+1* and low outputs as *0*. The resolution is determined by the number of clock periods taken for the averaging, in other words by the *oversampling ratio*, which is defined as:

$$OSR = \frac{f_{clock}}{f_{Nyquist}} \tag{2-5}$$

A very high resolution AD-conversion can be obtained provided that integrator "leakage", clock jitter, delay, and hysteresis are minimized [24,...,29]. To fulfill those requirements accurate components are not required, as opposed to the requirements for other AD-converter types. Besides the *OSR* and the noise-shape order, the performance is determined by the circuit design and the invested bias power.

By realizing the sigma-delta converter in a fully differential topology, as depicted in Fig.2-14, common-mode and supply interference, important error sources in instrumentation can be strongly suppressed. This configuration allows a differential input signal limited in signal range from $-0.9 \cdot I_{ref}$ to $+0.9 \cdot I_{ref}$. High outputs should now be interpreted as *+1*, and low outputs as *-1*. As often seen in practical realizations, the two displayed reference sources can be replaced by a single reference current of $2 \cdot I_{ref}$, provided that a common-mode (CM) control loop at the input of the

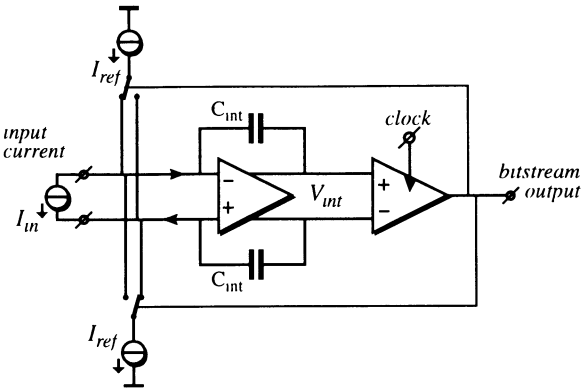

Fig. 2-14 *Differential sigma-delta converter.*

integrator takes care of fixing the input CM-level. This is necessary to obtain a *symmetrical* differential integration signal. The clocked comparator in this configuration simply decides the *polarity* of the differential signal, it compares the differential signal with the intrinsic reference of *0*. Fig.2-15 further demonstrates the operation of the (differential) sigma-delta converter. A slowly varying sine-wave input signal clearly results in a pulse-density modulated bitstream signal. In this example it is attempted to reconstruct the original signal by taking the average of the bitstream signal in clusters of 16 clock periods.

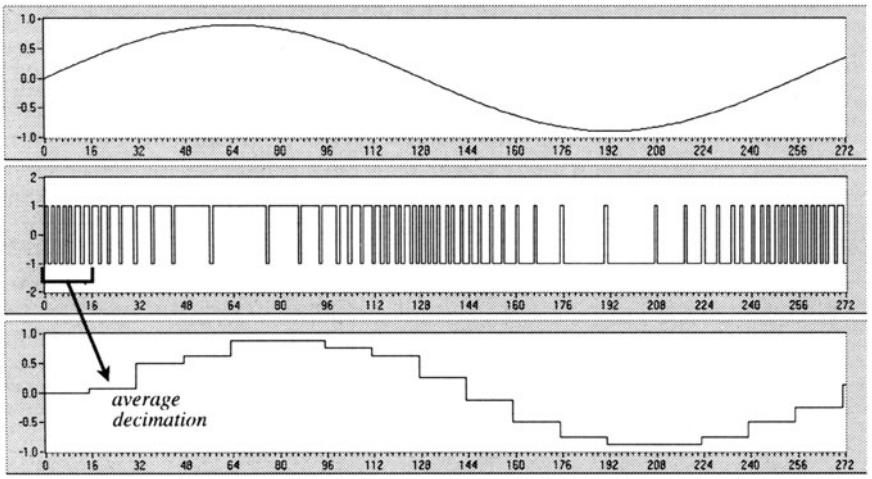

Fig. 2-15 *Sine-wave input, bitstream, and decimated output signal.*

Essentially the principle of sigma-delta conversion is based on simple (one-bit) quantization of the (filtered) input signal, whereas the quantization error is fed back to the input, and averaged (filtered) to zero (for DC) by signal integration. The output signal is composed of the digitized input signal at low frequencies, and the quantization (noise-shaped) error at high frequencies. A more elaborate explanation of the sigma-delta converter, using frequency domain analysis, will be given in *chapter 5*.

Another approach is to look at the *charge balance* which is obtained: on the long term the signal at the output of the integrator averages to zero (i.e. the remaining charge error can be neglected). This means that over a long interval the integral of the sum of all integrator input signals is zero, or in the discrete time domain:

$$\sum_{n=m+1}^{m+N} I_{in}[n] - \sum_{n=m+1}^{m+N} b_n \cdot I_{ref} = \frac{C \cdot \Delta V}{T_{clk}} \approx 0 \qquad (2\text{-}6)$$

in which N is the number of clock periods in the interval, and b_n represent the corresponding series of output bits, referring back to Fig.2-13. The remaining charge, determined by the difference ΔV between the integrator voltage, at the start and at the end of the interval, and the integrator capacitor C, can be neglected if the time interval $N \times T_{clk}$ is large with respect to the clock period T_{clk} : $N >> 1$. The maximum voltage error results when the minimum/maximum input signal is just not detected by the comparator, thus $\Delta V_{max} = I_{ref} \times T_{clk}/C$. Which means the maximum error on the right-hand side of equation (2-6) corresponds to $1 \times I_{ref}$, whereas the maximum on the left-hand side of the equation is N times larger.

Provided the input signal remains constant during the interval, we can derive for the average of the bitstream output:

$$\frac{1}{N} \sum_{n=m+1}^{m+N} b_n = \frac{I_{in}}{I_{ref}} \qquad (2\text{-}7)$$

which confirms that the output bitstream signal relates to the *ratio* of the input current and the reference current.

2.5 Digital bus or microcontroller interface

2.5.1 Microcontroller compatible interfaces

The bitstream output of a smart sensor with a sigma-delta converter is microcontroller compatible in the sense that it can easily be read in, and interpreted by a microcontroller or PC, as it is a serial, one-bit, digital, and clock-synchronous signal [30]. The appropriate sigma-delta clock signal can be generated by the microcontroller, and is sent to the sigma-delta. The digital bitstream signal is sent from the sigma-delta to the microcontroller. The microcontroller processes the bitstream in order to obtain multi-bit samples with the desired resolution. In order to read out multiple smart sensors with bitstream outputs the microcontroller needs to be equipped with a multiplexer which enables the selection of the different sensors; the clock line might be shared by several smart sensor devices. This situation is pictured on the left side of Fig.2-16.

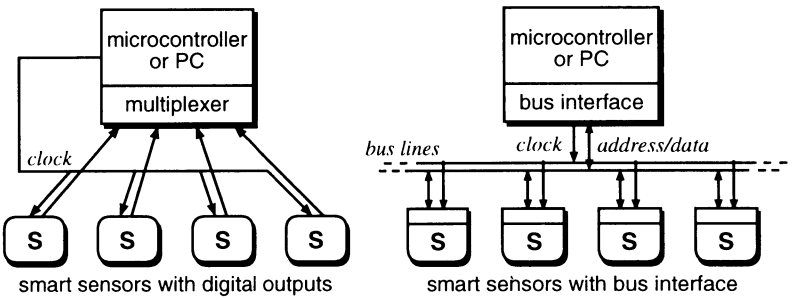

Fig. 2-16 *STAR-coupled versus BUS architecture.*

It is clear that the with the number of sensors also the wiring complexity increases. Other disadvantages of this *star-coupled* architecture are that the number of sensors is limited by the multiplexing capabilities of the microcontroller (usually 8 to 16), that the position of the sensor determines the multiplex address, and thus sensors cannot be swapped, and that only direct sensor-to-master communication is possible.

The *bus* architecture shown on the right-hand side of Fig.2-16, overcomes all these disadvantages. The sensors and the microcontroller/PC are equipped with a bus interface, and connected by common lines, a *clock line* and a *data line* for example. A *bus-slave* sensor will put its data on the bus data line only after it has been correctly *addressed* by the

microcontroller/PC *bus master* according to a *bus protocol.* The sensor data can be read by the master but also by other devices on the bus, a digital bitstream filter for example. Bidirectional communication is also possible, for example to program the calibration factors of a sensor before reading it out. Other advanced features which become available in a bus architecture are sensor identification and alarm interrupts.

2.5.2 Smart Sensor bus interfaces

Because it often is not possible to integrate complex digital circuitry with the sensor device, the first requirements for a smart sensor bus is minimum complexity at the bus-slave side. Another requirement is to have a minimum number of wires, because for use in sensor systems each connection introduces extra fabrication costs. A sensor bus which fulfills these requirements is the Inter-Integrated Circuit (I^2C) bus, which has been developed by Philips as internal bus for example for consumer products with microprocessor control. The bus has two supply wires and two wires for communication, using a simple addressing and handshake protocol on open collector (OC) lines. A flow and temperature sensor with an I^2C bus interface has been realized in a BiCMOS process [31]. Unfortunately the I^2C bus protocol allows only serial byte communications, which means that for sensors with a serial one-bit (sigma-delta or duty-cycle) signal an on-chip conversion to 8-bit or 16-bit numbers is needed which requires a considerable amount of digital circuitry.

For this reason the Integrated Smart Sensor (IS^2) bus has been invented [32]. The IS^2 bus is very similar to the I^2C: it also has two supply lines and two serial communication lines, but it has an open data transmission format [33,34,35]. In addition to the open collector technique Manchester encoding is used, so that in combination with the clock four different data states can be distinguished, as illustrated in Fig.2-17.

The clock and the data line are both pulled up by resistors, which are connected to the positive supply line. Using a strong open collector driver ($R_{clk} \approx 500\Omega$), the master puts a highly stable clock signal on the clock line, which is indispensable for the accuracy of the sensors' (time-continuous) sigma-delta converters. The data line can be pulled down by any device on the bus, using a less powerful open collector

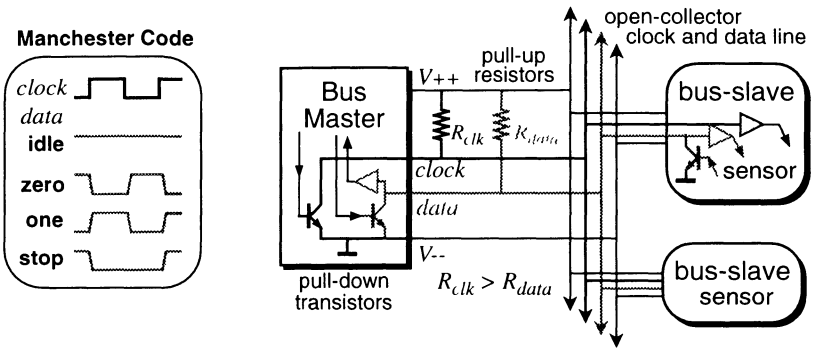

Fig. 2-17 *Using a Manchester encoding in combination with open-collector lines.*

transistor ($R_{data} \approx 5\,k\Omega$). Both the clock and the data line are read by the bus devices using high-ohmic input buffers.

When not a single bus device is active the data line remains high, and the bus is in idle state. After at least two idle states, a bus master can address a (sensor) bus slave by serially transmitting a start bit, eight address bits, and awaiting an acknowledge bit from the addressed bus slave, as explained in the bus protocol shown in Fig. 2-18. The slave can then put its data on the data line.

Digital clock-synchronous data is transmitted according to the Manchester code described in Fig. 2-17, a *zero* means pulling down the data line during the high phase of the clock, and a *one* means pulling down the data line during the low phase of the clock. When a *one* and a *zero* collide, because two sensors accidentally have responded to the same address, the line remains low during the whole clock period which corresponds to a *stop* signal which will be detected by the active bus devices, and reset the bus communication. This is also the way the master or an alarm sensor can send an interrupt. The length of a digital transmission is controlled by the master, so that it is possible to communicate bytes as well as any arbitrary number of bits, for example a long series of sigma-delta output pulses.

As mentioned before, it is also possible to put other kind of data on the bus. In that case the master keeps the clock line still (high) to prevent cross-talk distortion, and the slave can put an asynchronous digital signal (pulse-width or pulse-frequency modulated) or an analog voltage on the data line. It is up to the master to correctly interpret the data. Interruption

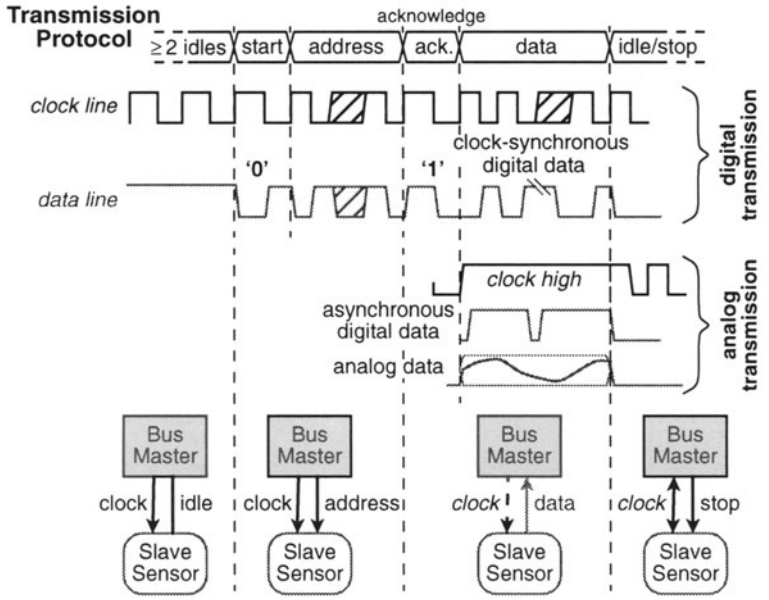

Fig. 2-18 *Explanation of the IS^2 bus communication protocol.*

is now only possible by (shortly) pulling the clock line down which should "wake up" the master, and get the clock running again.

It is also possible to make bus slaves receive data, for example to program a sensor's input range. At the side of the master the bus addresses will have to be organized in such a way that the master knows what kind of data to expect from or to send to the devices on the bus. This could be done by setting up a table with information about the sensors attached to the bus, containing address, type of data, number of samples, etc. or by splitting up the address range in sub-ranges for analog sensors, for sensors with bitstream outputs, etc. With eight address bits the maximum number of addresses is 256.

The hardware at the sensor (bus-slave) side is very simple. The scheme is shown in Fig.2-19. A Manchester decoder is needed to detect the status of the data line. After a start condition has been detected the decoded data bits are shifted in a register. A digital comparator is needed to compare the received address to the slave's own address. After positive comparison the slave immediately returns an acknowledge bit, and than puts its data on the bus. For digital data a Manchester encoder and OC driver are needed, and

for other data an analog switch and a voltage driver. The slave set-up is thus very simple, and the necessary digital circuitry is so limited (approximately 20 gates and 12 flipflops) that it can be integrated in CMOS on a very small surface, but also in bipolar technology using for example Emitter-Coupled Logic (ECL) as will be demonstrated in *chapter 4*.

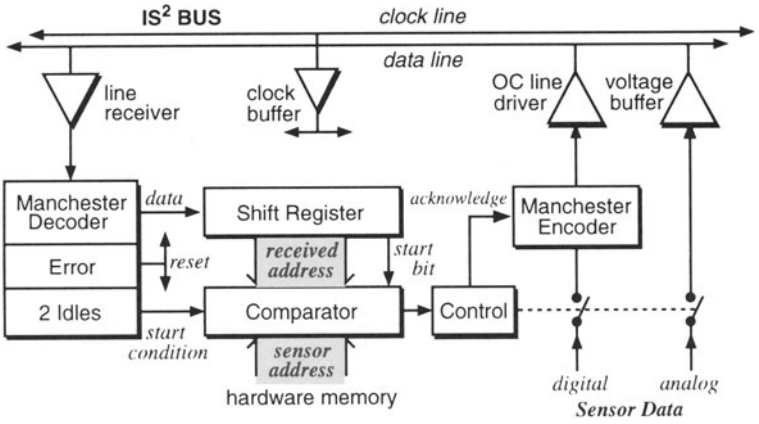

Fig. 2-19 *Configuration of an IS² bus-interface, for a bus slave.*

2.6 Integrating a calibration function in the smart sensor concept

The favored smart sensor configuration, for bipolar implementations at least, is reviewed in Fig. 2-20. Besides the (silicon) sensor it consists of an analog interface which realizes a sensor signal current and a reference current that are converted by the sigma delta converter into a digital bitstream signal. Next, the bitstream signal can easily be passed on by the IS² bus interface to the system's microcontroller or another bus master for example a PC. For many sensor types this scheme is probably the simplest way to realize a high-resolution AD-conversion and BUS interface

2.6.1 Error sources in the smart sensor signal path

Besides errors in the transfer of the sensor, from the physical input to the electrical output signal, we can also expect errors in the electrical transfer

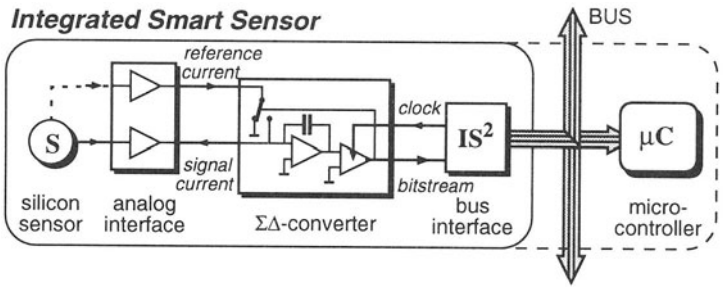

Fig. 2-20 *Signal chain of the proposed integrated smart sensor.*

of the other function blocks. Especially the analog interface may contribute offset and gain errors. However in the electrical signal domain we have methods available to reduce offset errors (chopping, auto-zero) and gain errors (dynamic element matching) to values which are much better than most sensor specifications [36,37]. Such advanced methods are not necessary in a smart sensor interface when we intend to calibrate the sensor anyway: we might as well calibrate the total error in the smart sensor signal chain. An exception has to be made when we expect considerable drift errors in the electronic circuit: in that case dynamic chopping or element matching methods will be useful.

2.6.2 Conventional sensor calibration techniques

Despite the smart sensor concept, most sensors are still fabricated (and distributed) separately from the electronic interface. Therefore, conventional calibration techniques concentrated on correction of the sensor transfer itself, during or just after fabrication. An example is the use of laser-trimmed resistors in a pressure sensor bridge, see section 3.2.1. A disadvantage of this approach is that it is difficult to automate the calibration, and that it is thus an expensive procedure in a fabrication line. Furthermore, it means that the electronic interface must match the specifications of the calibrated sensor, which could require a separate calibration or a more advanced circuit technique.

On the system level, sensor calibrations are usually performed on the systems computer. Data-acquisition programs, such as LabView, offer many possibilities for an advanced digital calibration. Disadvantage of this approach is that each new or replaced sensor in the system first has to be calibrated by the user, rather than by the manufacturer, which means the

user needs (expensive) reference equipment. Furthermore, the calibration requires computational power of the system, and the calibration information is not attached to the sensor but stored in the system's computer. Altogether it will not stimulate the use of sensors in consumer products if such a calibration technique is needed.

2.6.3 Correction of the sensor signal transfer

As the objective is to find a way to integrate a calibration function in the smart sensor concept, we will start by looking for different possibilities to change the signal transfer of one of the different function blocks that have been presented. In the smart sensor signal chain shown in Fig. 2-20 we can choose to alter the transfer in:

- *the analog signal domain*
- *the AD-converter*
- *the digital signal domain*

In all cases it is important that the calibration is made digitally programmable. This will make it possible to fully automate the calibration in a fabrication process. It is also important that the errors of the whole signal chain are calibrated, even when we apply the correction at the front of the chain. This is done by taking the final (digital) output signal when measuring the sensor transfer during the calibration phase.

The three options will be further elaborated in the succeeding chapters. The sensor signal can be passed through an analog circuit with programmable offset, gain, etc. To realize a digital programmability for analog signals Digital-to-Analog Converters (DACs) are needed. This will become clear in *chapter 4*. In the sigma-delta AD-converter we have a mixed signal circuit which offers different possibilities for a programmable correction as will be clarified in *chapter 5*. Concerning the digital signal domain, it is often not possible to integrate advanced digital circuitry on the sensor chip. Alternatively it is possible to hybridly integrate a microcontroller die in the sensor package, or to use the microcontroller bus master for a digital calibration. Therefore, *chapter 6* concentrates on the realization of an advanced calibration function in the form of microcontroller software.

Before looking at those different practical implementation forms, the important aspects of calibration, and different linearization methods will

be explained in *chapter 3*. Also an attractive polynomial calibration technique will be proposed.

2.6.4 Calibration memory

An issue that has not yet been addressed is the storage of the correction factors after calibration of the sensor. Obviously it is desirable that the correction is stored in a non-volatile memory integrated with the sensor or interface chip. Possible forms of nonvolatile memories, such as (E)PROM, zener or metal fuses, are mostly not available in standard IC processes. The development of such a memory in the used process could easily turn into a separate research project, and has not been given any attention within this project. The work in this book concentrates on the development of the circuitry needed to execute the correction. For the storage of the calibration coefficients simple volatile RAM is used, in the form of digital flipflop cells. The advantage of developing *digital* calibration circuitry is that the memory can easily be replaced with whatever digital memory is or becomes available in the used IC process.

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