A Study on Design and Simulation of 10 bit SAR ADC

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***Abstract*—This paper presents a literature review on the 10-bit Successive Approximation (SAR) Analog to Digital Convertor (ADC). The circuit is realized using the specifications 1.8 V digital voltage, 3.3 V analog voltage and 1-off chip external voltage reference. SAR is the best choice among all ADCs in terms of power consumption and area.**

I. Introduction

Data convertors act like a mediator in between the digital and analog world. They are used to convert analog signals to digital signals. They form the critical component of all the systems. The digital signals are considered dominant over analog signals as they improve the modern circuit performance. ADC is required as most signals in the physical world are analog [1].

ADC performance is measured mainly on the basis of bit resolution and sample rate. A comparison of all types of ADC as given in table 1, shows that SAR ADC is selected as it provided with a perfect balance of speed, power and area consumption [2]. Since SAR uses binary search algorithm, it consumes less power [3]. Flash ADC is fastest but it takes up a large area and has low resolution. Counter type takes maximum conversion time. There is a trade off between different parameters like resolution, sampling speed, area and others based on its application requirement.

The rest of the article is summarized below. Section II consists of block diagram and working of the circuit. Section III deals with the applications of SAR.

II. Block Diagram and Working

The block diagram of SAR ADC IP and internal block diagram is given below in fig 1.

Topology	Flash	Counter	Single Slope	Dual Slope	SAR	Sigma Delta	Pipelined	Interleaving
Resolution(Bits)	Low (6-8)	Medium (10-12)	Medium-High (12-18)	Medium-High (12-18)	Medium-High (12-18)	High (16-24)	Medium-High (12-18)	Medium-High (12-18)
Power Consumption	High	Medium-High	Low	Low	Low-Ultralow	Low	High	High
Latency	Low	Medium	Low-Medium	Low-Medium	Low	High	High	Low
Area	High	Low	Low	Low	Low	Medium	High	High
Accuracy	Low	Medium-High	Variable	High	Medium-High	High	Medium-High	Medium
Cost	High	Low	Medium	Medium	Low-High	Low	High	High

Table 1: Performance Comparison of Various Analog to Digital converters

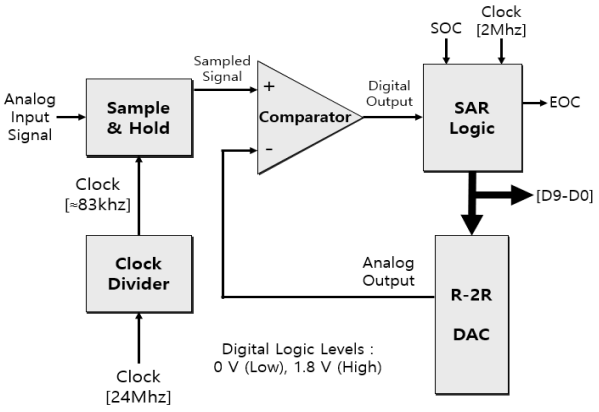

Fig.1 Internal Block Diagram of ADC IP

The block diagram of ADC consists of sample and hold circuit, comparator, SAR logic and R-2R DAC. A clock divider is used to get the required hold time for the sample and hold circuit. Initially SAR register is reset to zero. The bits of DAC are enabled one by one and the output of DAC is compared with the sampled input obtained from the output of sample and hold circuit. The output of comparator is low if the input voltage is less than the output of DAC and vice versa. The comparator output resets the bits accordingly. This process repeats until every bit of the DACs changes [4].

III. Applications

In various ADC implementation methods, the SAR ADC method is convenient to use because it has lower power consumption and smaller size and higher accuracy than other methods [5].

This method is used in medical image processing, sensors, optical communication systems, and audio signal processing. In addition, as the IoT market grows, more information needs to be collected, so the usage of ADC is expected to grow further in the future [6].

References

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