Chapter 7: Setup time and Hold time

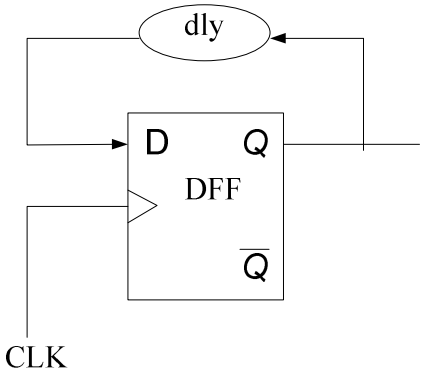
Questions:

Q1) Define (a) setup time (b) hold time (c) clock to Q delay.

Q2) Which of the following flip flops can work at maximum frequency?

	FF1	**FF2**	**FF3**
Clock to Q delay(ns)	5	6	8
Setup time(ns)	3	4	2
Hold time(ns)	2	1	1

Q3) Derive the maximum frequency of operation for the following circuit in terms of Tcq, Tsu and Th of the flip flop?



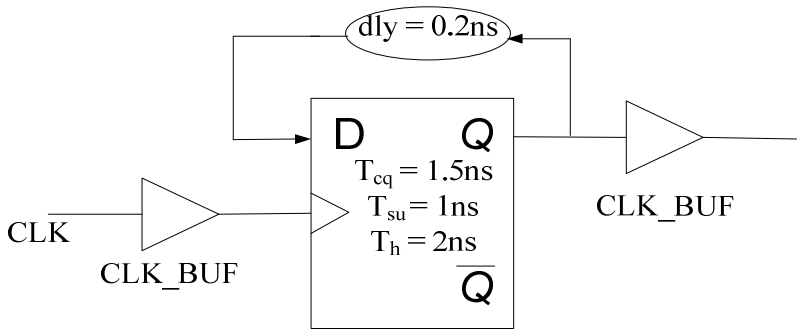
Q4) For the above configuration with dly = 0, which of the flip flops that are shown in Q2, can be used if the available clock period is (a) 5ns (b) 8ns (c) 15ns

Q5) Design a circuit for clock frequency divided by 2 using DFF. Given the following information, find the maximum clock frequency that the circuit can handle?

T_setup = 6ns , T_hold = 2ns and T_propagation = 10ns

Q6) Is there any hold violation in the above circuit? When will the hold violation occur in a given circuit and how can it be solved in circuit level? Describe in detail.

Q7)

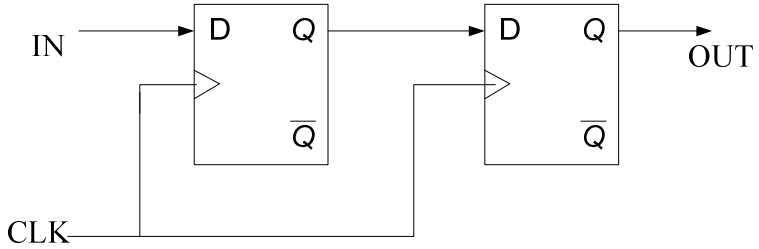


(a) Will the above circuit work without any violation?
(b) Calculate the new value of "dly" to avoid the violation, if any?
(c) Will the delay of CLK_BUF affect the maximum frequency of operation?

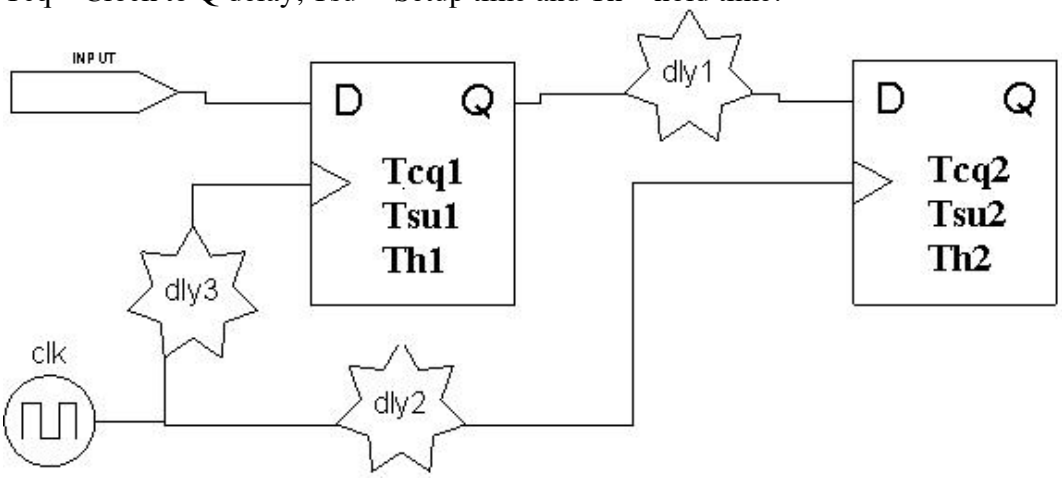
Q8) What is clock skew? Explain.

Q9) Can hold time be negative? Explain.

Q10) Among the flip flops that are shown in Q2, which combination can give maximum frequency of operation for the following circuit?

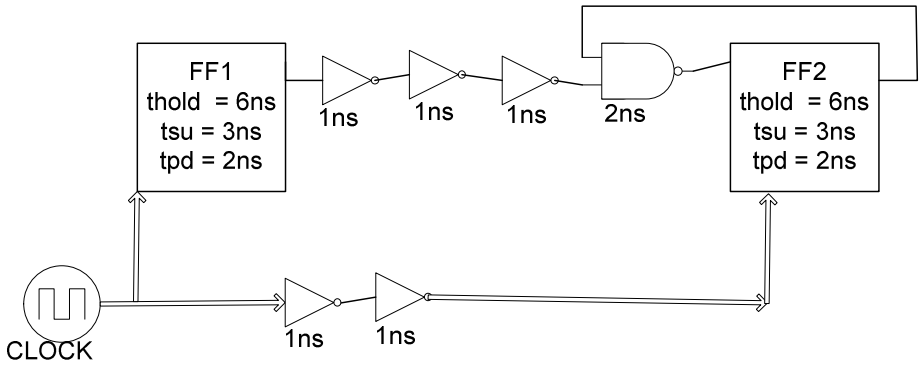


Q11) The following digital circuit shows two flops with a logic delay (dly1) in between and two clock buffer delays (dly2, dly3). Derive the conditions in terms of (dly1,dly2,dly3) to fix setup and hold timing violations at the input of second FF?
Tcq – Clock to Q delay, Tsu -- Setup time and Th – hold time.

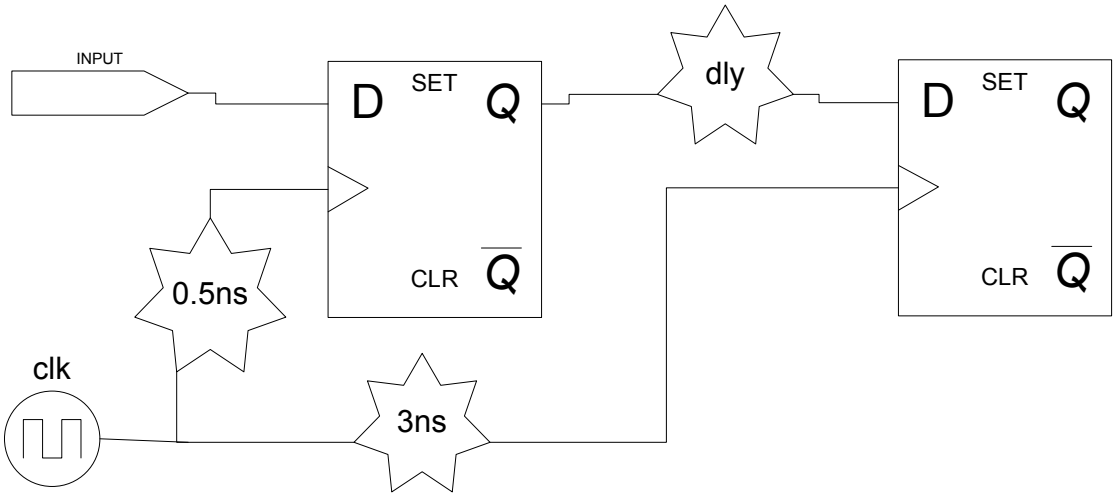


Q12)

(a) Are there any hold time violations for FF2 in the following circuit? If yes, how do you modify the circuit to avoid them?
(b) For the Circuit, what is the Maximum Frequency of Operation?

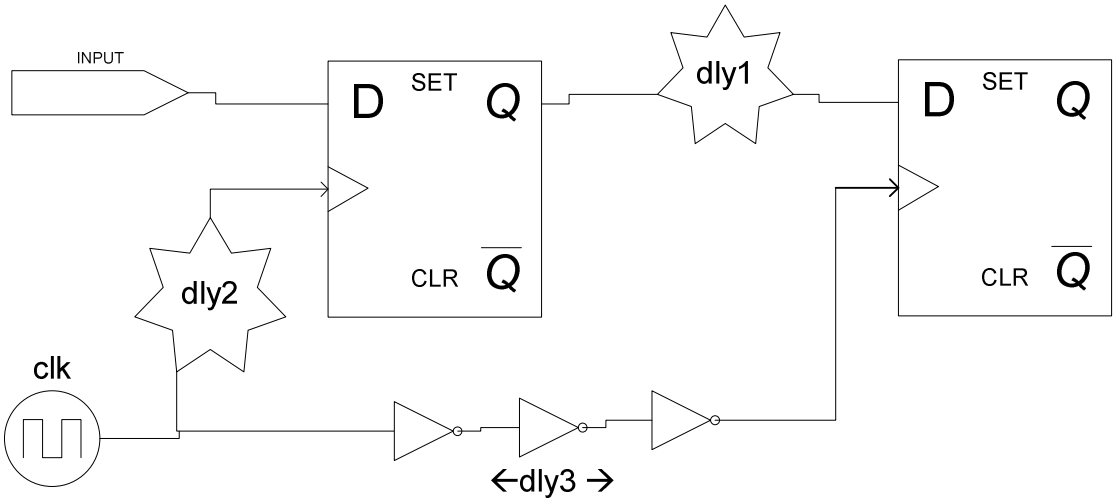


Q13)



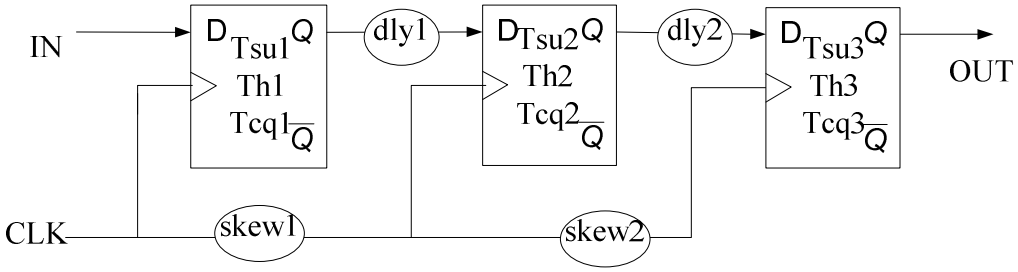
If both the flip flops have same clock to Q delay of 2.5ns, setup time of 2ns and a hold time of 1ns, what is the maximum frequency of operation for the circuit shown in the above figure?

Q14)



Repeat Q1 for the above circuit? Assume Tcq1 – Clock to Q delay, Tsu1 -- Setup time and Th1 – hold time for first FF and similarly Tcq2,Tsu2,Th2 for second FF.

Q15) What is the maximum frequency of operation for the following configuration?



Q16) What is metastability? When/why it will occur? Explain how to avoid this?

Q17) For the circuit in Q11, two identical flip flops with the following data were used: Tsu = 2ns, Th = -3ns and Tcq = 5ns. Which combination of dly1 and dly2 from the following table will give maximum frequency of operation without any violations? Given: dly3 = 0.

dly1(ns)	**dly2(ns)**
1	7
6	2
2	8

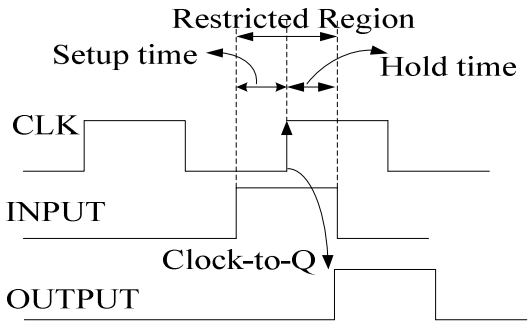
Answers:

A1)

(a) Setup time: Setup time is the minimum amount of time the data signal should be held steady before the clock event so that the data is reliably sampled by the clock.

(b) Hold time: The hold time is the minimum amount of time the data signal should be held steady after the clock event so that the data is reliably sampled by the clock.

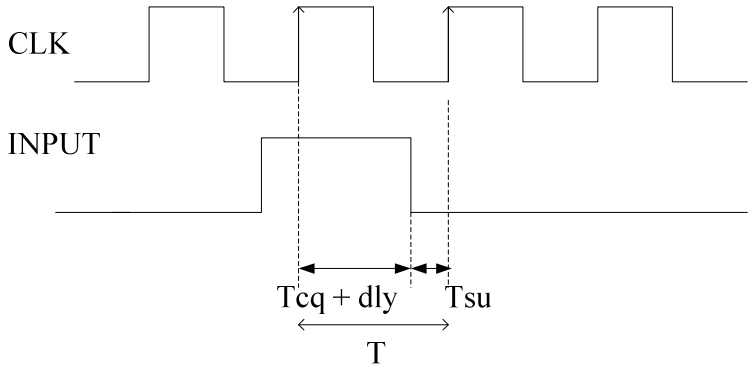
(c) Clock to Q delay: The clock to Q delay is the amount of the propagation time required for the data signal to reach the output (Q) of the flip flop after the clock event.



A2) For a single flip flop, lesser the clock-to-Q delay, more the operating frequency. However, the maximum frequency of operation may be limited by the configuration in which the flip flop is connected. This will be clear in the later parts of the chapter.

Among the 3 flops, the first one, FF1 has less clock to Q delay. So it can operate at maximum frequency which is given by 1/5ns = 200MHz

A3) After the posedge of the clock, the output will change after a delay of Tcq. The input of the flop will change after further delay of "dly". It should be available before the Tsu of the flop. So the T >= Tcq + Tsu + dly. The same thing is illustrated in the following waveform.



A4) dly = 0

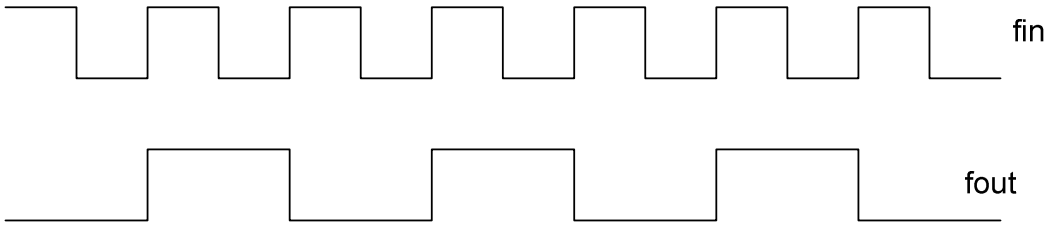
For FF1, Tsu + Tcq = 3 + 5 = 8ns
For FF2, Tsu + Tcq = 6 + 4 = 10ns
For FF3, Tsu + Tcq = 8 + 2 = 10ns

As dly = 0, Tsu + Tcq <= T

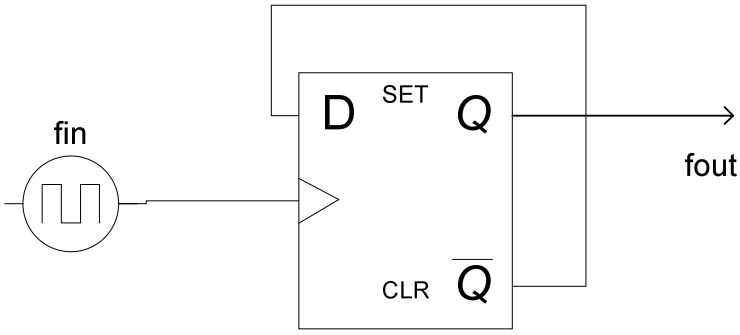
(a) T = 5ns, None of the flip flops has Tsu + Tcq <= T, so no one can be used.
(b) T = 8ns, FF1 can be used
(c) T = 15ns, Anyone can be used

A5)

Waveforms:



Design:



Using the same equation , T >= Tcq + Tsu, T >= 6 + 10. So T >= 16ns.
The maximum clock frequency = 1/16ns = 62.5MHz

A6) There are no hold violations in the above circuit. If the hold time is greater than the propagation delay then there will be hold violation for the above circuit. In that case, buffers (even number of inverters) will be used in the feedback path in order to delay the signal in reaching back to the input.

A7)

(a) Thold <= Tcq + dly. But here, 2ns > 1.5 + 0.5 = 1.7ns
So there is a hold violation in the above circuit.
(b) dly >= Thold – Tcq = 2 – 1.5 = 0.5ns
(c) The delay of the clock buffer will not effect the maximum frequency of operation of the circuit.

A8) Clock-skew: Clock skew is a phenomenon in synchronous circuits in which the clock signal (sent from the clock circuit) arrives at different components at different times.
This is typically due to two causes:

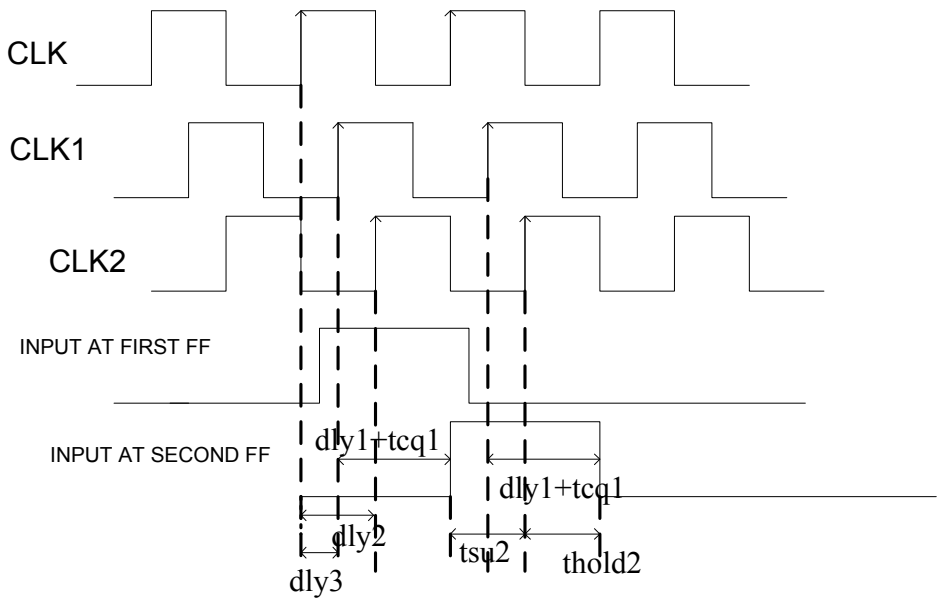
1. The first is a material flaw, which causes a signal to travel faster or slower than expected.
2. The second is distance: if the signal has to travel the entire length of a circuit, it will likely (depending on the circuit's size) arrive at different parts of the circuit at different times.

Skew is only meaningful between adjacent pairs of registers, not between any pair of registers in a clock domain.

A9) Yes, Hold time of a flip flop can be negative. Most of the modern flip flops will have either 0 or negative hold time. Assume Thold = -2ns, there should not be any transitions in the input before 2ns of the clock event.

A10) For the given circuit, T >= Tcq1 + Tsu2.
To get maximum frequency T should be less. So we should select the first flop with less clock to Q delay and second flip flop with less setup time. So FF1 and FF3 give the maximum frequency and it is equal to 1/7ns = 142.8MHz

A11)



The above waveforms show the CLK, CLK1 and CLK2. The input waveform at FF1 is assumed and the input of FF2 is shown accordingly with all the given delays and clock-to-Q delays.
From the waveforms it is clear that, to avoid setup time violation,

T >= (Tsu2 + Tcq1 + dly1 – delta) where **delta = dly2-dly3** (assuming +ve skew)

From this equation we can get maximum freq of operation.

To avoid hold time violation,

Th2 <= Tcq1 + dly1 – delta

These two equations can be used as generalized equations to solve setup time/hold time problems. This works only for synch circuits. If one clock works at pos edge and other is negative edge we need to derive one more set of equations. That also we will at later section.

A12)
(a) There is a hold time violation in the circuit, because of the feedback. Tcq2 +AND gate delay is less than thold2. To avoid this , we need to use even number of inverters(buffers). Here we need to use 2 inverters each with a delay of 1ns. Then the hold time value exactly meets.

(b) In this diagram,

dly3 = 0
dly2 = 2ns
so,delta = 2ns
tsu2 = 3ns, tcq1 = 2ns, dly1 = 5ns

Putting all these values in Eq(1) ,
T >= Tcq1 + dly1 + Tsu2 - delta

so, T >= 2 + 5 + 3 - 2, T >= 8ns, f <= 1/8
Max freq of operation is 125MHz

A13)
Tcq1 = Tcq2 = 2.5ns
Tsu1 = Tsu2 = 2ns
Thold1 = Thold2 = 1ns
delta = clock_skew = 3 - 0.5 = 2.5ns

Equation for hold-violation is,
Thold <= dly + Tcq1 - delta (Eq(2))
1 <= dly + 2.5 - 2.5
So dly >= 1ns
To obtain maximum freq, fixing it to lowest possible value, so dly = 1ns

Using this value and Eqauation (1) of setup time, we can obtain max freq.
T >= Tcq1 + dly +Tsu2 - delta
T >= 2.5 + 1 + 2 - 2.5
So T >= 3ns

Max freq of operation = 1/3ns = 333.33 MHz

A14)
Setup time:
(T/2) + delta >= Tcq1 + dly1 + Tsu2

Hold time:
Th2 <= delta + Tcq1 + dly1

where delta = dly3 - dly2, assuming positive skew
and T is clock period.

Note: The procedure is same as that of Q11.Just draw the waveforms with proper delays, you will get above equations.

A15) For FF1 and FF2, T1 >= (Tsu2 + Tcq1 + dly1 – skew1)
For FF2 and FF3, T2 >= (Tsu3 + Tcq2 + dly2 – skew2)
T >= MAX (T1,T2)

A16)
Metastable state: A un-known state in between the two known logical states is called as Metastable state.
Reason for occurrence: This will happen if the output node capacitance is not allowed to charge/discharge fully to the required logical levels. In case of flip flops, if the input changes in the restricted region, that is if there is a setup time or hold time violations, metastability will occur.

Way to avoid: To avoid this, a series of FFs is used (normally 2 or 3) which will remove the intermediate states. The extra flip flop is called the **synchronizer.**

A17) Given: Tsu = 2ns, Th = -3ns and Tcq = 5ns.
If hold time is negative and if its absolute value is less than Tsu, only thesetup violation equation without any modification will work. But if absolute value of hold time is more than setup time, we need to replace the setup time in the equation with hold time. The modified equation is shown below:

T >= Tcq1 + dly1 + Max(Tsu2, | Th2 |)
T >= 5 + dly1 + 3
T >= 8 + dly1

To get maximum frequency of operation, the minimum possible dly1 = 1ns.
So, T >= 9ns

Fmax = 1/9ns = 111MHz