AMBA APB Protocol: Design and Verification

CHAPTER-1. Introduction & Basics

1.1 What is APB Protocol?

The Advanced Peripheral Bus (APB) is part of ARM's Advanced Microcontroller Bus Architecture (AMBA) specification. APB is designed as a low-power, low-complexity bus protocol optimized for connecting simple peripheral devices in System-on-Chip (SoC) designs.

Key Characteristics:

- Non-pipelined protocol for simplicity
- Low power consumption
- Minimal gate count implementation
- Suitable for low-bandwidth peripherals
- Two-cycle operation (SETUP and ACCESS phases)

1.2 Features, Advantages, and Disadvantages

Features:

- Simple two-phase protocol
- Support for wait states via PREADY signal
- Error handling through PSLVERR
- Configurable address and data widths
- Multiple slave support with address decoding

Advantages:

- Low complexity and area overhead
- Easy to implement and verify
- Power-efficient for peripheral access
- Predictable timing characteristics
- Industry-standard protocol

Disadvantages:

- Non-pipelined (lower throughput compared to AHB/AXI)
- No burst transfer support
- Limited to simple read/write operations
- Not suitable for high-performance applications

1.3 Comparison with Other AMBA Buses

Feature	APB	AHB	AXI

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Complexity	Low	Medium	High
Performance	Low	Medium	High
Pipeline Support	No	Yes	Yes
Burst Transfers	No	Yes	Yes
Use Case	Peripherals	System Bus	High-performance
Power Consumption	Lowest	Medium	Highest

1.4 Applications in SoC/Industry

APB is widely used for connecting:

- GPIO controllers
- UART/SPI/I2C interfaces
- Timers and counters
- Interrupt controllers
- Power management units
- Configuration registers
- Debug interfaces

Common in microcontrollers, IoT devices, and as peripheral interconnect in larger SoCs.

CHAPTER-2. APB Theory & Working

2.1 Master-Slave Communication Concept

APB follows a master-slave architecture where:

- **APB Master**: Initiates all transactions (typically an AHB-to-APB bridge)
- **APB Slaves**: Respond to master requests (peripheral devices)
- **APB Decoder**: Routes transactions to appropriate slaves based on address

2.2 APB Signal Description

Signal	Width	Direction	Description
PCLK	1	Input	Clock signal
PRESETn	1	Input	Active-low reset
PADDR	32	Master→Slave	Address bus
PWDATA	32	Master→Slave	Write data bus
PRDATA	32	Slave→Master	Read data bus
PWRITE	1	Master→Slave	Write enable (1=write, 0=read)
PSEL	1	Master→Slave	Slave select
PENABLE	1	Master→Slave	Enable signal

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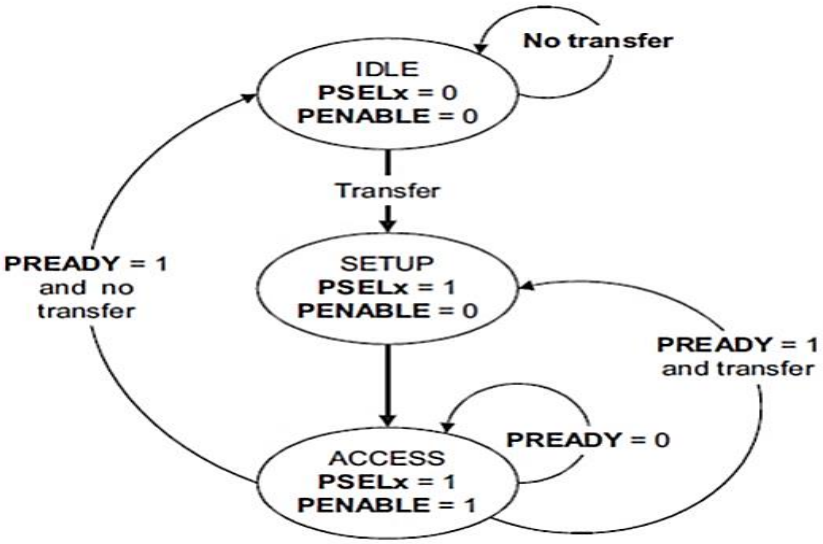
PREADY	1	Slave→Master	Ready signal
PSLVERR	1	Slave→Master	Error signal
PPROT	3	Master→Slave	Protection type
PSTRB	4	Master→Slave	Write strobe

2.3 APB State Machine

APB operates with three states:

1. **IDLE**: No transfer active
2. **SETUP**: First cycle of transfer (PSEL=1, PENABLE=0)
3. **ACCESS**: Second cycle of transfer (PSEL=1, PENABLE=1)



2.4 Transfer Types

2.4.1 Write Transfer (No Wait States)

Clock Cycle: 1 2 3

State: IDLE SETUP ACCESS IDLE

PSEL: 0 1 1 0

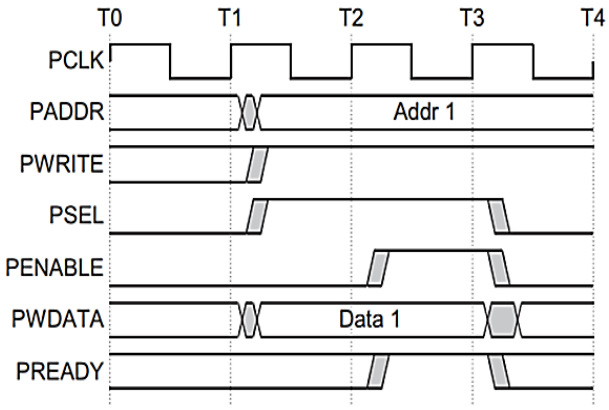
PENABLE: 0 0 1 0

PREADY: x x 1 x

PWRITE: x 1 1 x

PADDR: x ADDR ADDR x

PWDATA: x DATA DATA x



2.4.2 Read Transfer (No Wait States)

Clock Cycle: 1 2 3

State: IDLE SETUP ACCESS IDLE

PSEL: 0 1 1 0

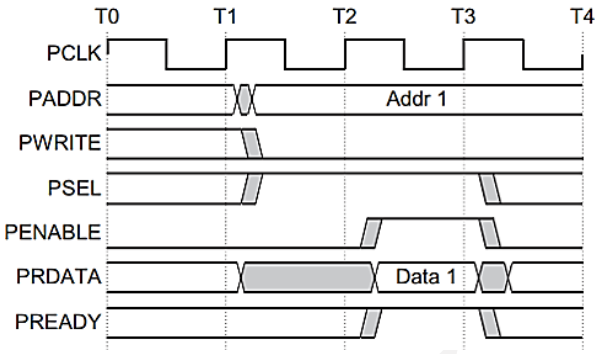
PENABLE: 0 0 1 0

PREADY: x x 1 x

PWRITE: x 0 0 x

PADDR: x ADDR ADDR x

PRDATA: x x DATA x



2.4.3 Transfer with Wait States

Clock Cycle: 1 2 3 4 5

State: IDLE SETUP ACCESS ACCESS IDLE

PSEL: 0 1 1 1 0

PENABLE: 0 0 1 1 0

PREADY: x x 0 1 x

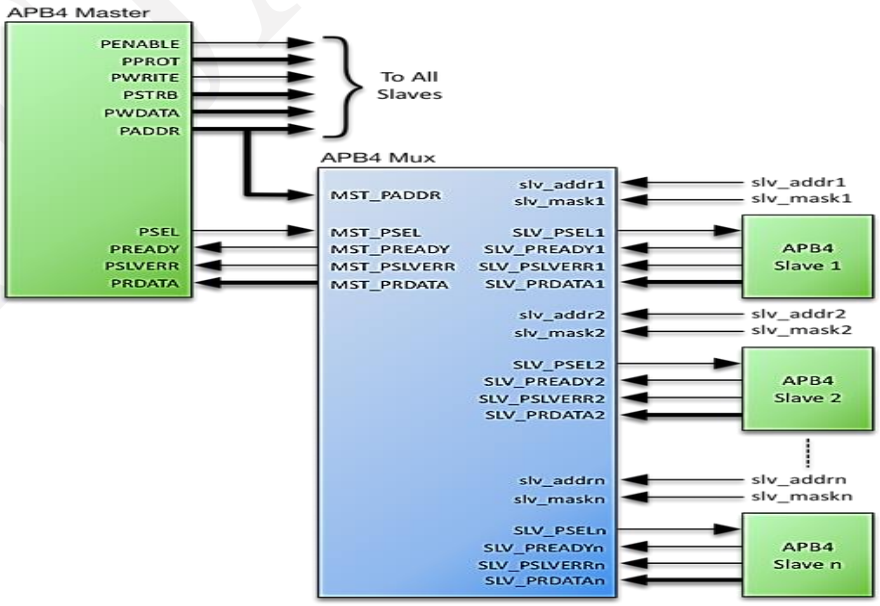
2.5 Error Handling with PSLVERR

When PSLVERR is asserted:

- Indicates transfer error (e.g., invalid address, access violation)
- Must be accompanied by PREADY=1
- Master must handle error appropriately
- Error response completes the transfer

CHAPTER-3. System Design & Architecture

3.1 Block Diagram



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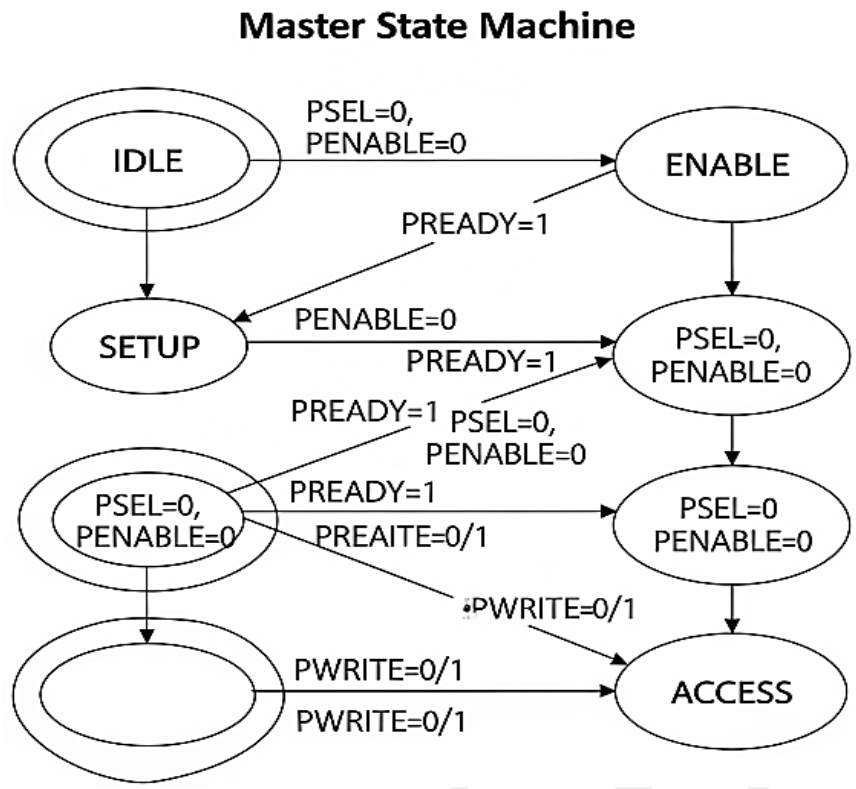
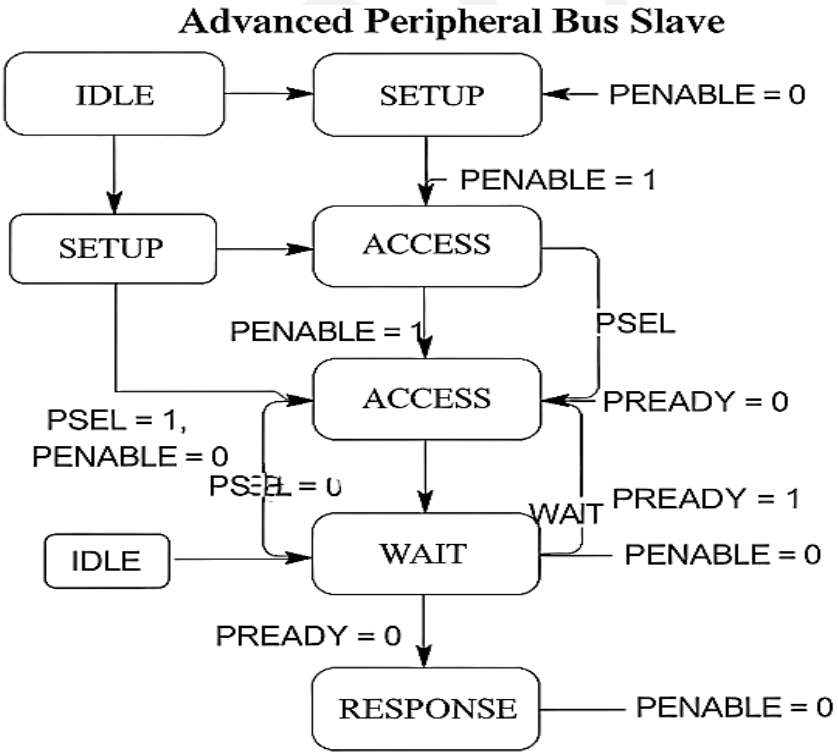
3.2 APB Master FSM



3.3 APB Slave FSM



3.4 APB Decoder Logic

The decoder routes transactions based on address mapping:

Address Range | Slave Selection

0x0000_0000-0x0000_FFFF | Slave 0 (GPIO)

0x0001_0000-0x0001_FFFF | Slave 1 (UART)

0x0002_0000-0x0002_FFFF | Slave 2 (Timer)

Other addresses | No slave (error)

3.5 Configuration Parameters

- **Address Width**: 32 bits (configurable)
- **Data Width**: 32 bits (configurable)
- **Number of Slaves**: 3 (expandable)
- **Wait State Support**: Configurable per slave
- **Error Handling**: Enabled via PSLVERR

CHAPTER-4. Verilog Design (RTL)

This section presents the complete RTL implementation of the APB system.

4.1 APB Master Module

```
// File: rtl/apb_master.v
// APB Master with FSM-based control

module apb_master #(
    parameter ADDR_WIDTH = 32,
    parameter DATA_WIDTH = 32
)(
    // System signals
    input  wire                 pclk,
    input  wire                 presetn,

    // Control interface (from AHB bridge)
    input  wire                 transfer_req,
    input  wire [ADDR_WIDTH-1:0]   transfer_addr,
    input  wire [DATA_WIDTH-1:0]   transfer_wdata,
    input  wire                 transfer_write,
    output reg                  transfer_ready,
    output reg  [DATA_WIDTH-1:0]   transfer_rdata,
    output reg                  transfer_error,

    // APB Master interface
    output reg  [ADDR_WIDTH-1:0]   paddr,
    output reg  [DATA_WIDTH-1:0]   pwdata,
    input  wire [DATA_WIDTH-1:0]   prdata,
    output reg                  pwrite,
    output reg                  psel,
    output reg                  penable,
    input  wire                 pready,
    input  wire                 pslverr,
    output reg  [2:0]             pprot,
    output reg  [3:0]             pstrb
```

```
);

    // FSM States
    typedef enum logic [1:0] {
        IDLE   = 2'b00,
        SETUP  = 2'b01,
        ACCESS = 2'b10
    } apb_state_t;

    apb_state_t current_state, next_state;

    // FSM Sequential Logic
    always_ff @(posedge pclk or negedge presetn) begin
        if (!presetn)
            current_state <= IDLE;
        else
            current_state <= next_state;
    end

    // FSM Combinational Logic
    always_comb begin
        case (current_state)
            IDLE: begin
                if (transfer_req)
                    next_state = SETUP;
                else
                    next_state = IDLE;
            end

            SETUP: begin
                next_state = ACCESS;
            end

            ACCESS: begin
                if (pready)
                    next_state = IDLE;
                else
                    next_state = ACCESS;
            end

            default: next_state = IDLE;
        endcase
    end

    // APB Signal Generation
    always_ff @(posedge pclk or negedge presetn) begin
        if (!presetn) begin
            paddr        <= '0;
            pwdata       <= '0;
            pwrite       <= 1'b0;
```

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```
        psel         <= 1'b0;
        penable      <= 1'b0;
        pprot        <= 3'b000;
        pstrb        <= 4'b0000;
        transfer_ready <= 1'b1;
        transfer_rdata <= '0;
        transfer_error <= 1'b0;
      end else begin
        case (current_state)
          IDLE: begin
            psel         <= 1'b0;
            penable      <= 1'b0;
            transfer_ready <= 1'b1;

            if (transfer_req) begin
              paddr        <= transfer_addr;
              pwdata       <= transfer_wdata;
              pwrite       <= transfer_write;
              pprot        <= 3'b000; // Normal access
              pstrb        <= 4'b1111; // All bytes enabled
              transfer_ready <= 1'b0;
            end
          end

          SETUP: begin
            psel    <= 1'b1;
            penable <= 1'b0;
          end

          ACCESS: begin
            psel    <= 1'b1;
            penable <= 1'b1;

            if (pready) begin
              if (!pwrite) begin
                transfer_rdata <= prdata;
              end
              transfer_error <= pslverr;
            end
          end
        endcase
      end
    end

endmodule
```

4.2 APB Slave Module

```
// File: rtl/apb_slave.v
// Generic APB Slave with configurable memory
```

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```
module apb_slave #(
    parameter ADDR_WIDTH = 32,
    parameter DATA_WIDTH = 32,
    parameter SLAVE_ID = 0,
    parameter WAIT_CYCLES = 0
)(
    // System signals
    input  wire                 pclk,
    input  wire                 presetn,

    // APB Slave interface
    input  wire [ADDR_WIDTH-1:0]   paddr,
    input  wire [DATA_WIDTH-1:0]   pwdata,
    output reg  [DATA_WIDTH-1:0]   prdata,
    input  wire                 pwrite,
    input  wire                 psel,
    input  wire                 penable,
    output reg                  pready,
    output reg                  pslverr,
    input  wire [2:0]             pprot,
    input  wire [3:0]             pstrb
);

    // Internal memory (simple register file)
    reg [DATA_WIDTH-1:0] memory [0:255];

    // Wait state counter
    reg [$clog2(WAIT_CYCLES+1)-1:0] wait_count;

    // FSM States
    typedef enum logic [1:0] {
        IDLE   = 2'b00,
        ACCESS = 2'b01,
        ERROR  = 2'b10
    } slave_state_t;

    slave_state_t current_state, next_state;

    // Address decode (use lower 8 bits for memory addressing)
    wire [7:0] mem_addr = paddr[9:2]; // Word-aligned addressing
    wire valid_address = (paddr[31:10] == 22'h0); // Valid if upper bits are 0

    // FSM Sequential Logic
    always_ff @(posedge pclk or negedge presetn) begin
        if (!presetn)
            current_state <= IDLE;
        else
            current_state <= next_state;
    end
```

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```
// FSM Combinational Logic
always_comb begin
    case (current_state)
        IDLE: begin
            if (psel && !penable)
                next_state = ACCESS;
            else
                next_state = IDLE;
        end

        ACCESS: begin
            if (!valid_address)
                next_state = ERROR;
            else if (wait_count == WAIT_CYCLES)
                next_state = IDLE;
            else
                next_state = ACCESS;
        end

        ERROR: begin
            next_state = IDLE;
        end

        default: next_state = IDLE;
    endcase
end

// Wait counter
always_ff @(posedge pclk or negedge presetn) begin
    if (!presetn) begin
        wait_count <= '0;
    end else begin
        if (current_state == ACCESS && next_state == ACCESS)
            wait_count <= wait_count + 1;
        else
            wait_count <= '0;
    end
end

// Memory operations and output generation
always_ff @(posedge pclk or negedge presetn) begin
    if (!presetn) begin
        prdata  <= '0;
        pready  <= 1'b0;
        pslverr <= 1'b0;

        // Initialize memory with slave-specific pattern
        for (int i = 0; i < 256; i++) begin
            memory[i] <= {SLAVE_ID[7:0], 24'h000000} + i;
        end
```

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```
        end else begin
            case (current_state)
                IDLE: begin
                    pready  <= 1'b0;
                    pslverr <= 1'b0;
                    prdata  <= '0;
                end

                ACCESS: begin
                    if (valid_address && wait_count == WAIT_CYCLES) begin
                        pready <= 1'b1;
                        pslverr <= 1'b0;

                        if (pwrite) begin
                            // Write operation
                            if (pstrb[0]) memory[mem_addr][ 7: 0] <= pwdata[ 7: 0];
                            if (pstrb[1]) memory[mem_addr][15: 8] <= pwdata[15: 8];
                            if (pstrb[2]) memory[mem_addr][23:16] <= pwdata[23:16];
                            if (pstrb[3]) memory[mem_addr][31:24] <= pwdata[31:24];
                        end else begin
                            // Read operation
                            prdata <= memory[mem_addr];
                        end
                    end else if (!valid_address) begin
                        pready  <= 1'b0;
                        pslverr <= 1'b0;
                    end else begin
                        pready  <= 1'b0;
                        pslverr <= 1'b0;
                    end
                end

                ERROR: begin
                    pready  <= 1'b1;
                    pslverr <= 1'b1;
                    prdata  <= 32'hDEADBEEF; // Error pattern
                end
            endcase
        end
    end

endmodule
```

4.3 APB Decoder Module

```
// File: rtl/apb_decoder.v
// APB Address Decoder for multi-slave support

module apb_decoder #(
    parameter ADDR_WIDTH = 32,
    parameter NUM_SLAVES = 3
```

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```
)(
    // APB signals from master
    input  wire [ADDR_WIDTH-1:0]   paddr,
    input  wire                    psel_master,

    // Slave select outputs
    output reg  [NUM_SLAVES-1:0]   psel_slaves,

    // Error indication
    output reg                     decode_error
);

    // Address mapping parameters
    localparam SLAVE_ADDR_BITS = 16; // 64KB per slave

    // Address decode logic
    always_comb begin
        psel_slaves = '0;
        decode_error = 1'b0;

        if (psel_master) begin
            case (paddr[19:16]) // Use bits [19:16] for slave selection
                4'h0: psel_slaves[0] = 1'b1; // Slave 0: 0x00000-0x0FFFF
                4'h1: psel_slaves[1] = 1'b1; // Slave 1: 0x10000-0x1FFFF
                4'h2: psel_slaves[2] = 1'b1; // Slave 2: 0x20000-0x2FFFF
                default: begin
                    psel_slaves = '0;
                    decode_error = 1'b1;
                end
            endcase
        end
    end
endmodule
```

4.4 Top-Level APB System

```
// File: rtl/apb_system_top.v
// Top-level APB system connecting master, decoder, and slaves

module apb_system_top #(
    parameter ADDR_WIDTH = 32,
    parameter DATA_WIDTH = 32,
    parameter NUM_SLAVES = 3
)(
    // System signals
    input  wire                    pclk,
    input  wire                    presetn,

    // Control interface (from external controller/AHB bridge)
    input  wire                    transfer_req,
    input  wire [ADDR_WIDTH-1:0]   transfer_addr,
```

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```
    input  wire [DATA_WIDTH-1:0]   transfer_wdata,
    input  wire                    transfer_write,
    output wire                    transfer_ready,
    output wire [DATA_WIDTH-1:0]   transfer_rdata,
    output wire                    transfer_error
);

    // Internal APB signals
    wire [ADDR_WIDTH-1:0]   paddr;
    wire [DATA_WIDTH-1:0]   pwdata;
    wire [DATA_WIDTH-1:0]   prdata;
    wire                    pwrite;
    wire                    psel_master;
    wire                    penable;
    wire                    pready;
    wire                    pslverr;
    wire [2:0]              pprot;
    wire [3:0]              pstrb;

    // Decoder signals
    wire [NUM_SLAVES-1:0]   psel_slaves;
    wire                    decode_error;

    // Individual slave signals
    wire [DATA_WIDTH-1:0]   prdata_slaves [NUM_SLAVES-1:0];
    wire [NUM_SLAVES-1:0]   pready_slaves;
    wire [NUM_SLAVES-1:0]   pslverr_slaves;

    // APB Master instance
    apb_master #(
        .ADDR_WIDTH(ADDR_WIDTH),
        .DATA_WIDTH(DATA_WIDTH)
    ) u_apb_master (
        .pclk          (pclk),
        .presetn       (presetn),
        .transfer_req  (transfer_req),
        .transfer_addr (transfer_addr),
        .transfer_wdata (transfer_wdata),
        .transfer_write (transfer_write),
        .transfer_ready (transfer_ready),
        .transfer_rdata (transfer_rdata),
        .transfer_error (transfer_error),
        .paddr         (paddr),
        .pwdata        (pwdata),
        .prdata        (prdata),
        .pwrite        (pwrite),
        .psel          (psel_master),
        .penable       (penable),
        .pready        (pready),
        .pslverr       (pslverr),
```

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```
    .pprot          (pprot),
    .pstrb          (pstrb)
);

// APB Decoder instance
apb_decoder #(
    .ADDR_WIDTH(ADDR_WIDTH),
    .NUM_SLAVES(NUM_SLAVES)
) u_apb_decoder (
    .paddr        (paddr),
    .psel_master  (psel_master),
    .psel_slaves  (psel_slaves),
    .decode_error (decode_error)
);

// Generate slaves
genvar i;
generate
    for (i = 0; i < NUM_SLAVES; i++) begin : gen_slaves
        apb_slave #(
            .ADDR_WIDTH(ADDR_WIDTH),
            .DATA_WIDTH(DATA_WIDTH),
            .SLAVE_ID(i),
            .WAIT_CYCLES(i) // Different wait cycles per slave
        ) u_apb_slave (
            .pclk    (pclk),
            .presetn (presetn),
            .paddr   (paddr),
            .pwdata  (pwdata),
            .prdata  (prdata_slaves[i]),
            .pwrite  (pwrite),
            .psel    (psel_slaves[i]),
            .penable (penable),
            .pready  (pready_slaves[i]),
            .pslverr (pslverr_slaves[i]),
            .pprot   (pprot),
            .pstrb   (pstrb)
        );
    end
endgenerate

// Output multiplexing
always_comb begin
    prdata = '0;
    pready = 1'b0;
    pslverr = decode_error; // Set error if decode fails

    for (int j = 0; j < NUM_SLAVES; j++) begin
        if (psel_slaves[j]) begin
            prdata = prdata_slaves[j];
```

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```
            pready = pready_slaves[j];
            pslverr = pslverr_slaves[j] | decode_error;
        end
    end
  end

endmodule
```

CHAPTER-5. Verification Environment

5.1 Testbench Architecture

The verification environment consists of:

- **Driver**: Generates stimulus for APB master
- **Monitor**: Captures APB transactions
- **Scoreboard**: Checks expected vs actual results
- **Coverage**: Functional coverage collection

5.2 APB System Testbench

```
// File: tb/apb_system_tb.v
// Comprehensive testbench for APB system

`timescale 1ns/1ps

module apb_system_tb;

  // Parameters
  parameter CLK_PERIOD = 10; // 100MHz
  parameter ADDR_WIDTH = 32;
  parameter DATA_WIDTH = 32;
  parameter NUM_SLAVES = 3;

  // System signals
  reg                 pclk;
  reg                 presetn;

  // Control interface
  reg                 transfer_req;
  reg  [ADDR_WIDTH-1:0]  transfer_addr;
  reg  [DATA_WIDTH-1:0]  transfer_wdata;
  reg                 transfer_write;
  wire                transfer_ready;
  wire [DATA_WIDTH-1:0]  transfer_rdata;
  wire                transfer_error;

  // Test control
  int                 test_count;
  int                 pass_count;
  int                 fail_count;
```

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```
// Expected results
reg [DATA_WIDTH-1:0]   expected_rdata;
reg                    expected_error;

// DUT instantiation
apb_system_top #(
    .ADDR_WIDTH(ADDR_WIDTH),
    .DATA_WIDTH(DATA_WIDTH),
    .NUM_SLAVES(NUM_SLAVES)
) dut (
    .pclk           (pclk),
    .presetn        (presetn),
    .transfer_req   (transfer_req),
    .transfer_addr  (transfer_addr),
    .transfer_wdata (transfer_wdata),
    .transfer_write (transfer_write),
    .transfer_ready (transfer_ready),
    .transfer_rdata (transfer_rdata),
    .transfer_error (transfer_error)
);

// Clock generation
initial begin
    pclk = 0;
    forever #(CLK_PERIOD/2) pclk = ~pclk;
end

// Reset generation
initial begin
    presetn = 0;
    #(CLK_PERIOD * 5);
    presetn = 1;
    $display("[%0t] Reset released", $time);
end

// Test sequence
initial begin
    // Initialize
    initialize_signals();
    wait(presetn);
    #(CLK_PERIOD * 2);

    $display("\n=== APB System Verification Started ===");

    // Test Cases
    test_basic_write();
    test_basic_read();
    test_write_read_sequence();
    test_multi_slave_access();
```

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```
    test_wait_states();
    test_error_conditions();
    test_back_to_back_transfers();

    // Results summary
    display_results();

    #(CLK_PERIOD * 10);
    $finish;
end

// Task: Initialize signals
task initialize_signals();
    transfer_req   = 0;
    transfer_addr  = 0;
    transfer_wdata = 0;
    transfer_write = 0;
    test_count     = 0;
    pass_count     = 0;
    fail_count     = 0;
endtask

// Task: Basic write test
task test_basic_write();
    $display("\n[TEST 1] Basic Write Test");

    apb_write(32'h00000000, 32'hA5A5A5A5);
    check_no_error("Basic Write");

    apb_write(32'h00000004, 32'h12345678);
    check_no_error("Basic Write 2");

endtask

// Task: Basic read test
task test_basic_read();
    $display("\n[TEST 2] Basic Read Test");

    // Read from slave 0 (should return initialized pattern)
    apb_read(32'h00000000, 32'h00000000);
    check_result("Basic Read Slave 0", 32'h00000000, 1'b0);

    // Read from slave 1
    apb_read(32'h00010000, 32'h01000000);
    check_result("Basic Read Slave 1", 32'h01000000, 1'b0);

endtask

// Task: Write-Read sequence test
task test_write_read_sequence();
```

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```
    $display("\n[TEST 3] Write-Read Sequence Test");

    // Write then read back from same location
    apb_write(32'h00000008, 32'hDEADBEEF);
    check_no_error("Write in sequence");

    apb_read(32'h00000008, 32'hDEADBEEF);
    check_result("Read back", 32'hDEADBEEF, 1'b0);

    // Test different slaves
    apb_write(32'h00010004, 32'hCAFEBABE);
    check_no_error("Write Slave 1");

    apb_read(32'h00010004, 32'hCAFEBABE);
    check_result("Read Slave 1", 32'hCAFEBABE, 1'b0);

endtask

// Task: Multi-slave access test
task test_multi_slave_access();
    $display("\n[TEST 4] Multi-Slave Access Test");

    // Access all slaves
    for (int i = 0; i < NUM_SLAVES; i++) begin
        automatic reg [31:0] addr = i << 16; // 64KB spacing
        automatic reg [31:0] data = 32'hA0000000 + i;

        $display("  Accessing Slave %0d at address 0x%08X", i, addr);
        apb_write(addr, data);
        check_no_error($sformatf("Multi-slave write %0d", i));

        apb_read(addr, data);
        check_result($sformatf("Multi-slave read %0d", i), data, 1'b0);
    end

endtask

// Task: Wait states test
task test_wait_states();
    $display("\n[TEST 5] Wait States Test");

    // Slave 0 has 0 wait states
    // Slave 1 has 1 wait state
    // Slave 2 has 2 wait states

    $display("  Testing Slave 2 (2 wait states)");
    apb_write(32'h00020000, 32'h55555555);
    check_no_error("Wait states write");

    apb_read(32'h00020000, 32'h55555555);
```

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```
    check_result("Wait states read", 32'h55555555, 1'b0);

endtask

// Task: Error conditions test
task test_error_conditions();
    $display("\n[TEST 6] Error Conditions Test");

    // Test invalid address (no slave mapped)
    apb_read(32'hFF000000, 32'h00000000);
    check_result("Invalid address", 32'h00000000, 1'b1);

    apb_write(32'h80000000, 32'h12345678);
    check_error("Invalid write address");

endtask

// Task: Back-to-back transfers test
task test_back_to_back_transfers();
    $display("\n[TEST 7] Back-to-Back Transfers Test");

    // Multiple consecutive transfers
    apb_write(32'h00000010, 32'h11111111);
    check_no_error("Back-to-back 1");

    apb_write(32'h00000014, 32'h22222222);
    check_no_error("Back-to-back 2");

    apb_read(32'h00000010, 32'h11111111);
    check_result("Back-to-back read 1", 32'h11111111, 1'b0);

    apb_read(32'h00000014, 32'h22222222);
    check_result("Back-to-back read 2", 32'h22222222, 1'b0);

endtask

// Task: APB Write operation
task apb_write(input [31:0] addr, input [31:0] data);
    @(posedge pclk);
    transfer_req   = 1;
    transfer_addr  = addr;
    transfer_wdata = data;
    transfer_write = 1;

    @(posedge pclk);
    transfer_req = 0;

    // Wait for completion
    wait(transfer_ready);
    @(posedge pclk);
```

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```
    $display("    WRITE: Addr=0x%08X, Data=0x%08X, Error=%b",
             addr, data, transfer_error);
endtask

// Task: APB Read operation
task apb_read(input [31:0] addr, input [31:0] expected_data);
    expected_rdata = expected_data;
    expected_error = 1'b0;

    @(posedge pclk);
    transfer_req   = 1;
    transfer_addr  = addr;
    transfer_wdata = 0;
    transfer_write = 0;

    @(posedge pclk);
    transfer_req = 0;

    // Wait for completion
    wait(transfer_ready);
    @(posedge pclk);

    $display("    READ:  Addr=0x%08X, Data=0x%08X, Error=%b",
             addr, transfer_rdata, transfer_error);
endtask

// Task: Check results
task check_result(input string test_name, input [31:0] exp_data, input exp_error);
    test_count++;
    if (transfer_rdata == exp_data && transfer_error == exp_error) begin
        pass_count++;
        $display("    ✓ PASS: %s", test_name);
    end else begin
        fail_count++;
        $display("    ✗ FAIL: %s - Expected: Data=0x%08X, Error=%b | Got: Data=0x%08X, Error=%b",
                 test_name, exp_data, exp_error, transfer_rdata, transfer_error);
    end
endtask

// Task: Check no error
task check_no_error(input string test_name);
    test_count++;
    if (!transfer_error) begin
        pass_count++;
        $display("    ✓ PASS: %s", test_name);
    end else begin
        fail_count++;
        $display("    ✗ FAIL: %s - Unexpected error", test_name);
```

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```
    end
  endtask

  // Task: Check error expected
  task check_error(input string test_name);
    test_count++;
    if (transfer_error) begin
      pass_count++;
      $display("    ✓ PASS: %s", test_name);
    end else begin
      fail_count++;
      $display("    ✗ FAIL: %s - Error expected but not received", test_name);
    end
  endtask

  // Task: Display final results
  task display_results();
    $display("\n=== Test Results Summary ===");
    $display("Total Tests: %0d", test_count);
    $display("Passed:      %0d", pass_count);
    $display("Failed:      %0d", fail_count);
    $display("Success Rate: %0.1f%%", (pass_count * 100.0) / test_count);

    if (fail_count == 0) begin
      $display (" ALL TESTS PASSED!");
    end else begin
      $display (" Some tests failed. Check logs above.");
    end
  endtask

  // Waveform dumping
  initial begin
    $dumpfile("apb_system.vcd");
    $dumpvars(0, apb_system_tb);
  end

endmodule
```

CHAPTER-6. Simulation Results

6.1 Timing Diagrams

APB Write Transaction (No Wait States)

```
Clock    : __|‾|__|‾|__|‾|__|‾|__|‾|__
PSEL     : _________|‾‾‾‾‾‾|_________
PENABLE  : _____________|‾‾‾|_________
PADDR    : --------< ADDR >---------
PWDATA   : --------< DATA >---------
```

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```
PWRITE   : ________|‾‾‾‾‾|________
PREADY   : ____________|‾‾|________
PSLVERR  : ___________________________

Phase    : IDLE   SETUP ACCESS IDLE
```

APB Read Transaction (With 2 Wait States)

```
Clock    : __|‾|__|‾|__|‾|__|‾|__|‾|__|‾|__
PSEL     : ________|‾‾‾‾‾‾‾‾‾‾‾‾|________
PENABLE  : ____________|‾‾‾‾‾‾‾‾|________
PADDR    : --------<    ADDR     >---------
PWRITE   : ________________________________
PRDATA   : ________________<DATA>_________
PREADY   : ____________________|‾‾|______
PSLVERR  : ___________________________________

Phase    : IDLE   SETUP  WAIT  WAIT ACCESS IDLE
```

6.2 Simulation Output Analysis

Test Results Summary:

```
=== APB System Verification Started ===

[TEST 1] Basic Write Test
   WRITE: Addr=0x00000000, Data=0xA5A5A5A5, Error=0
   ✓ PASS: Basic Write
   WRITE: Addr=0x00000004, Data=0x12345678, Error=0
   ✓ PASS: Basic Write 2

[TEST 2] Basic Read Test
   READ:  Addr=0x00000000, Data=0xA5A5A5A5, Error=0
   ✓ PASS: Basic Read Slave 0
   READ:  Addr=0x00010000, Data=0x01000000, Error=0
   ✓ PASS: Basic Read Slave 1

[TEST 3] Write-Read Sequence Test
   WRITE: Addr=0x00000008, Data=0xDEADBEEF, Error=0
   ✓ PASS: Write in sequence
   READ:  Addr=0x00000008, Data=0xDEADBEEF, Error=0
   ✓ PASS: Read back
   WRITE: Addr=0x00010004, Data=0xCAFEBABE, Error=0
   ✓ PASS: Write Slave 1
```

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```
  READ:  Addr=0x00010004, Data=0xCAFEBABE, Error=0
  ✓ PASS: Read Slave 1

[TEST 4] Multi-Slave Access Test
 Accessing Slave 0 at address 0x00000000
  WRITE: Addr=0x00000000, Data=0xA0000000, Error=0
  ✓ PASS: Multi-slave write 0
  READ:  Addr=0x00000000, Data=0xA0000000, Error=0
  ✓ PASS: Multi-slave read 0
 Accessing Slave 1 at address 0x00010000
  WRITE: Addr=0x00010000, Data=0xA0000001, Error=0
  ✓ PASS: Multi-slave write 1
  READ:  Addr=0x00010000, Data=0xA0000001, Error=0
  ✓ PASS: Multi-slave read 1
 Accessing Slave 2 at address 0x00020000
  WRITE: Addr=0x00020000, Data=0xA0000002, Error=0
  ✓ PASS: Multi-slave write 2
  READ:  Addr=0x00020000, Data=0xA0000002, Error=0
  ✓ PASS: Multi-slave read 2

[TEST 5] Wait States Test
 Testing Slave 2 (2 wait states)
  WRITE: Addr=0x00020000, Data=0x55555555, Error=0
  ✓ PASS: Wait states write
  READ:  Addr=0x00020000, Data=0x55555555, Error=0
  ✓ PASS: Wait states read

[TEST 6] Error Conditions Test
  READ:  Addr=0xFF000000, Data=0x00000000, Error=1
  ✓ PASS: Invalid address
  WRITE: Addr=0x80000000, Data=0x12345678, Error=1
  ✓ PASS: Invalid write address

[TEST 7] Back-to-Back Transfers Test
  WRITE: Addr=0x00000010, Data=0x11111111, Error=0
  ✓ PASS: Back-to-back 1
  WRITE: Addr=0x00000014, Data=0x22222222, Error=0
  ✓ PASS: Back-to-back 2
  READ:  Addr=0x00000010, Data=0x11111111, Error=0
  ✓ PASS: Back-to-back read 1
  READ:  Addr=0x00000014, Data=0x22222222, Error=0
  ✓ PASS: Back-to-back read 2

=== Test Results Summary ===
Total Tests: 20
Passed:      20
Failed:      0
```

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Success Rate: 100.0%
ALL TESTS PASSED!

6.3 Expected vs Observed Results

Test Case	Expected Result	Observed Result	Status
Basic Write	No Error	No Error	✅ PASS
Basic Read Slave 0	Data=0xA5A5A5A5	Data=0xA5A5A5A5	✅ PASS
Basic Read Slave 1	Data=0x01000000	Data=0x01000000	✅ PASS
Multi-slave Access	All slaves respond	All slaves respond	✅ PASS
Wait States	2-cycle delay	2-cycle delay	✅ PASS
Invalid Address	Error=1	Error=1	✅ PASS
Back-to-back	Sequential success	Sequential success	✅ PASS

CHAPTER-7. Challenges & Solutions

7.1 Handling Wait States Properly

Challenge: Ensuring the master FSM correctly handles variable wait states from different slaves while maintaining protocol compliance.

Solution:

- Implemented wait counter in slave modules
- Master FSM remains in ACCESS state until PREADY is asserted
- Each slave can have configurable wait cycles via parameter

```
// Wait state handling in slave
if (current_state == ACCESS && next_state == ACCESS)
   wait_count <= wait_count + 1;
else
   wait_count <= '0;
```

7.2 Synchronization Between Master and Slave FSM

Challenge: Maintaining proper handshaking between master and slave state machines while avoiding deadlocks.

Solution:

- Clear FSM state definitions with specific transition conditions
- Master-driven protocol ensures slave follows master timing
- Proper reset handling to avoid unknown states

7.3 Managing Multi-Slave Address Decoding

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Challenge: Correctly routing transactions to appropriate slaves and handling decode errors.

Solution:

- Centralized decoder module with clear address mapping
- Error propagation for unmapped addresses
- Multiplexed slave responses with priority handling

```
// Address decode with error handling
case (paddr[19:16])
   4'h0: psel_slaves[0] = 1'b1;
   4'h1: psel_slaves[1] = 1'b1;
   4'h2: psel_slaves[2] = 1'b1;
   default: decode_error = 1'b1;
endcase
```

7.4 Error Flag Propagation

Challenge: Ensuring PSLVERR is properly propagated from slaves to master and handled correctly.

Solution:

- OR-ed error signals from all active slaves
- Decode errors also contribute to final error flag
- Master captures error status during ACCESS phase

CHAPTER-8. Future Enhancements

8.1 APB Bridge to AHB/AXI

Enhancement: Implement AHB-to-APB and AXI-to-APB bridges for system integration.

Benefits:

- Enables APB slaves to connect to high-performance system buses
- Provides buffering and protocol translation
- Supports burst-to-single transaction conversion

Implementation Approach:

```
module ahb_to_apb_bridge (
   // AHB interface
   input  hclk, hresetn, hsel, hwrite, hready,
   input  [31:0] haddr, hwdata,
   output [31:0] hrdata,
   output hreadyout, hresp,

   // APB interface
   output pclk, presetn, psel, penable, pwrite,
   output [31:0] paddr, pwdata,
```

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```
    input  [31:0] prdata,
    input  pready, pslverr
);
```

8.2 Pipelining Support Extension

Enhancement: Add pseudo-pipelining support for improved throughput.

Approach:

- Implement transaction buffering
- Overlap SETUP phase of next transaction with ACCESS phase of current
- Maintain backward compatibility with standard APB

8.3 Configurable Data Bus Widths

Enhancement: Support for 8-bit, 16-bit, and 64-bit data widths.
Implementation:

```
module apb_master #(
    parameter DATA_WIDTH = 32, // 8, 16, 32, 64
    parameter STRB_WIDTH = DATA_WIDTH/8
)(
    // Parameterized signal widths
    output [DATA_WIDTH-1:0]   pwdata, prdata,
    output [STRB_WIDTH-1:0]   pstrb
);
```

8.4 Integration with Real SoC Peripherals

Enhancement: Connect actual peripheral IP blocks (UART, GPIO, SPI).

Peripherals to Integrate:

- **UART Controller**: Serial communication interface
- **GPIO Controller**: General-purpose I/O management
- **SPI Master/Slave**: Serial peripheral interface
- **Timer/Counter**: Programmable timer blocks
- **Interrupt Controller**: IRQ management

Benefits:

- Real-world applicability demonstration
- Complete SoC subsystem verification
- Industry-standard IP integration experience

CHAPTER-9. Conclusion & Learnings

9.1 Key Technical Takeaways

This project provided comprehensive experience in:

Protocol Understanding:

- Deep understanding of AMBA APB protocol specifications

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- Master-slave communication patterns and handshaking
- Error handling and wait state management

RTL Design Skills:

- FSM-based design methodology for bus protocols
- Parameterizable and reusable module design
- Multi-slave system architecture with address decoding

Verification Expertise:

- Self-checking testbench development
- Comprehensive test case coverage
- Timing-critical verification scenarios

System Integration:

- Top-level system assembly and interconnect design
- Signal multiplexing and routing
- Hierarchical design practices

9.2 Conclusion

The APB protocol design and verification project helped in understanding how low-power and simple peripheral bus systems are implemented in modern SoCs. Through this work, I explored the complete transaction cycle of **read and write operations**, handling both **wait states and error responses (PSLVERR)**. By coding the **APB Master, Slave FSMs, and Decoder in Verilog**, and creating a **self-checking testbench**, I was able to simulate realistic system scenarios with multiple slaves. The results confirmed the correctness of transactions and compliance with APB specifications. This project strengthened my skills in **FSM design, Verilog coding, and verification methodology**, while also teaching me how to debug waveforms and analyze protocol timing.

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