Computer Architecture

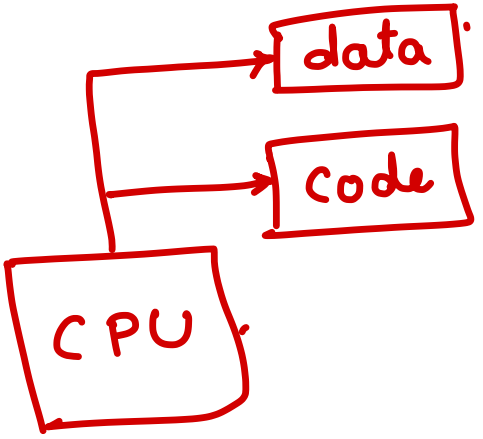
Von Neumann architecture

- The Von Neumann architecture consists of a single, shared memory for programs and data, a single bus for memory access, an arithmetic unit, and a program control unit

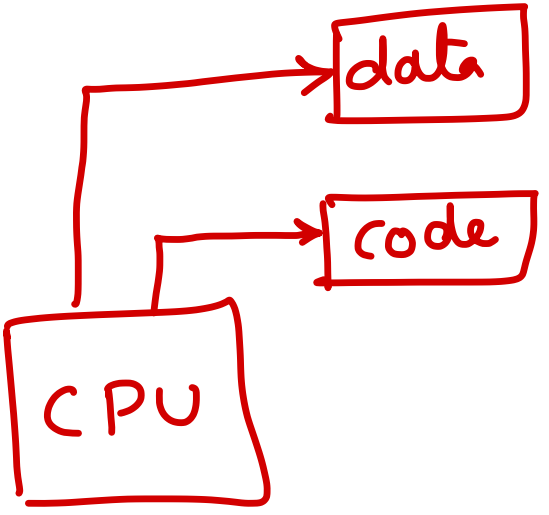
Harvard architecture

- The Harvard architecture has two separate memory spaces dedicated to program code and to data. respectively, two corresponding address buses, and two data buses for accessing two memory spaces.

Von Neu



Har Arch.



Computer Architecture

CISC Processor

- It is known as Complex Instruction Set Computer.
- Large set of instructions with variable formats
- In this instructions are not register based.
- Instructions cannot be completed in one machine cycle that is it requires multiple cycle.
- Data transfer is from memory to memory.
- Examples of CICS are 8085,8086,80386,80486 etc

RISC Processor

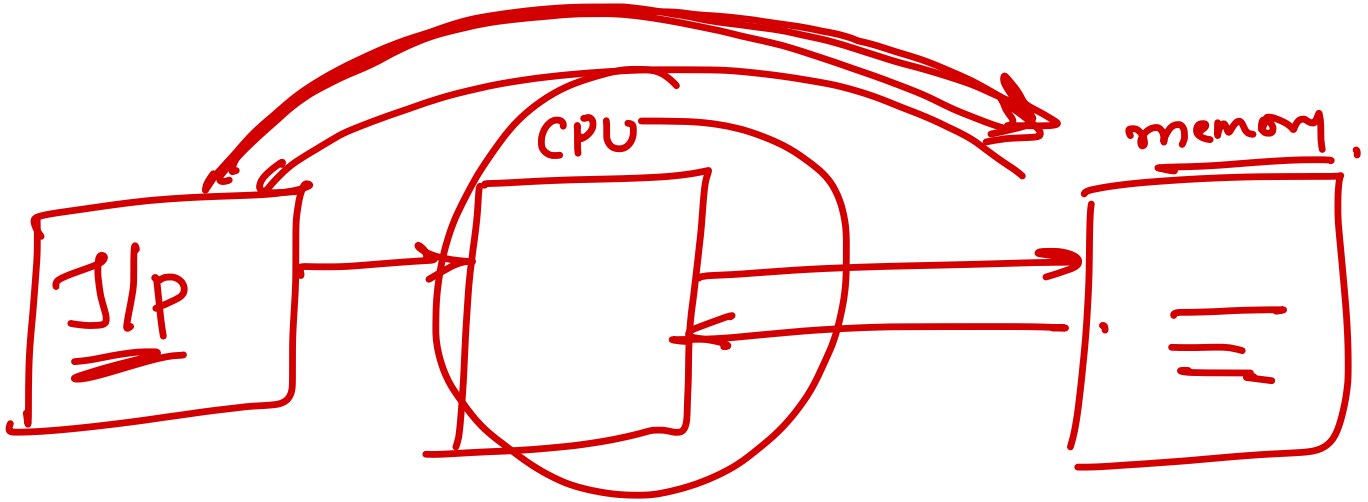
- It is known as Reduced Instruction Set Computer
- Small set of instructions with fixed format
- In this instructions are register based.
- Instructions can be completed in one machine cycle.
- Data transfer is from Register to Register.
- They can execute their instructions very fast because instructions are very small and simple
- Examples of Harvard architecture are AVR, ARM, Sun SPARC, Power PC.

memory → LDA & STA

Load and store Arch.

Direct Memory Access(DMA)

- Removing the CPU from the path and letting the peripheral device manage the memory buses directly would improve the speed of transfer. This technique is known as **DMA**.
- In this, the interface transfer data to and from the memory through memory bus. A DMA controller manages to transfer data between peripherals and memory unit.
- Many hardware systems use DMA such as disk drive controllers, graphic cards, network cards and sound cards etc. It is also used for intra chip data transfer in multicore processors.



Interrupt

- Data transfer between the CPU and the peripherals is initiated by the CPU. But the CPU cannot start the transfer unless the peripheral is ready to communicate with the CPU. When a device is ready to communicate with the CPU, it generates an interrupt signal.
- The main job of the interrupt system is to identify the source of the interrupt.

Priority Interrupt

- A priority interrupt is a system which decides the priority at which various devices, which generates the interrupt signal at the same time, will be serviced by the CPU.
- For example, devices with high speed transfer such as *magnetic disks* are given high priority and slow devices such as *keyboards* are given low priority.
- When two or more devices interrupt the computer simultaneously, the computer services the device with the higher priority first.

Computer Architecture

Types of Interrupts:

Hardware Interrupts

- When the signal for the processor is from an external device or hardware then this interrupts is known as **hardware interrupt**.
- Let us consider an example: when we press any key on our keyboard to do some action, then this pressing of the key will generate an interrupt signal for the processor to perform certain action.
  - **Maskable Interrupt**
    - The hardware interrupts which can be delayed when a much high priority interrupt has occurred at the same time.
  - **Non Maskable Interrupt**
    - The hardware interrupts which cannot be delayed and should be processed by the processor immediately.

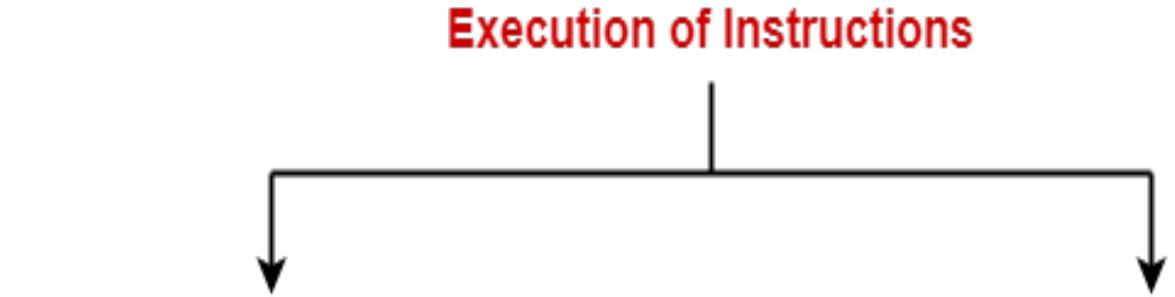
Software Interrupts

- The interrupt that is caused by any internal system of the computer system is known as a **software interrupt**.
  - **Normal Interrupt**
    - The interrupts that are caused by software instructions are called **normal software interrupts**.
  - **Exception**
    - Unplanned interrupts which are produced during the execution of some program are called **exceptions**, such as division by zero.

Computer Architecture

- A program consists of several number of instructions.
- These instructions may be executed in the following two ways

1) Accept 1 F D E .
2) Accept 2 F D E .
3) A + B . F D E .
4) Result .



8085.

8086.

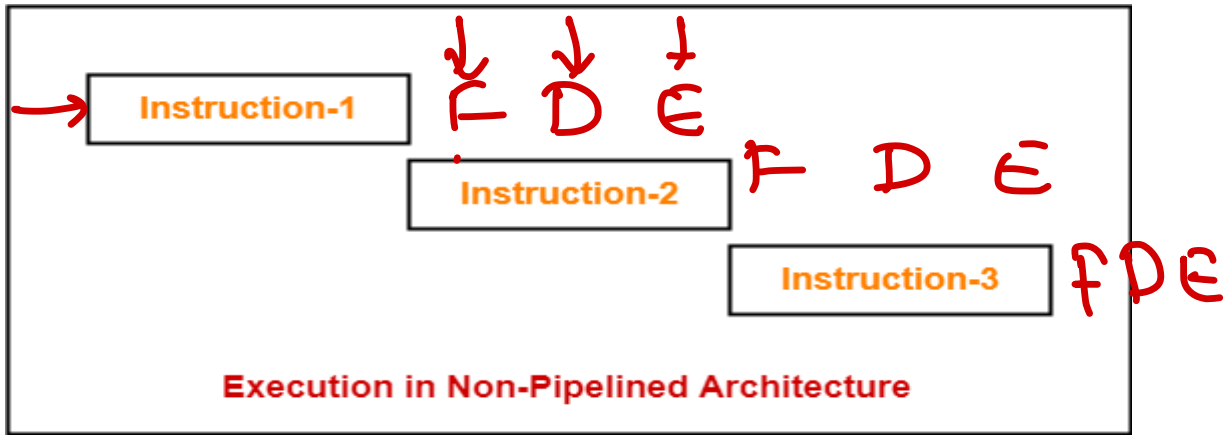
Non-Pipelined Execution

- In non-pipelined architecture, All the instructions of a program are executed sequentially one after the other.
- A new instruction executes only after the previous instruction has executed completely.

Example

- Consider a program consisting of three instructions.
- In a non-pipelined architecture, these instructions execute one after the other as-

- If time taken for executing one instruction = t, then-
- Time taken for executing 'n' instructions = n x t



- No. of cycle required to execute = K x N
- Where K → Number of stages
  N → Number of Instruction

no of stages. F D E 3.

Instruction - 4

4 x 3 = 12.

For Example :

- If we have 5 number of instruction and 4 number of stages then total how many cycle are required in non-pipelining ?

N x K.

= 5 x 4

= 20 cycle.

5 stages → 8 instn.

No of cycle = 8 x 5 = 40

accept
Add.

Pipelined Execution-

- In pipelined architecture, Multiple instructions are executed parallelly.
- Pipelining is the process of accumulating instruction from the processor through a pipeline. It allows storing and executing instructions in an orderly process. It is also known as pipeline processing.

Four-Stage Pipeline-

- In four stage pipelined architecture, the execution of each instruction is completed in following 4 stages-
- Instruction fetch (IF)
- Instruction decode (ID)
- Instruction Execute (IE)
- Write back (WB)

Read Back (RB)

4 Stages..

1 instn → 9 stage . = 4 Stages.

clk clk clk clk .

	Stage 1	Stage2	Stage 3	Stage 4	Stage 5	Stage 6	Stage 7	Stage 8
Instruction 1	IF	ID	IE	WB				
Instruction 2		IF	ID	IE	WB			
Instruction 3			IF	ID	IE	WB		
Instruction 4				IF	ID	IE	WB	
Instruction 5					IF	ID	IE	WB

No. of cycle required to execute = K +(N -1)

Where K → Number of stages

N → Number of Instruction

1 instn = K stages.

1 + (N-1)

K + (N-1)

For Example :

If we have 5 number of instruction and 4 number of stages then total how many cycle are required in pipelining ?

K + ((N - 1)

4 + (5 - 1)

4 + 4 = 8 clk.

8 instn — 5 stages. non pipeling.
pipeling.

Non-Pipeling. K × N,

8 × 5 = 40 cycle;

Pipeline.

K + (N - 1)

5 + (8 - 1)

5 + 7 = 12 cycle

Advantages of Pipelining

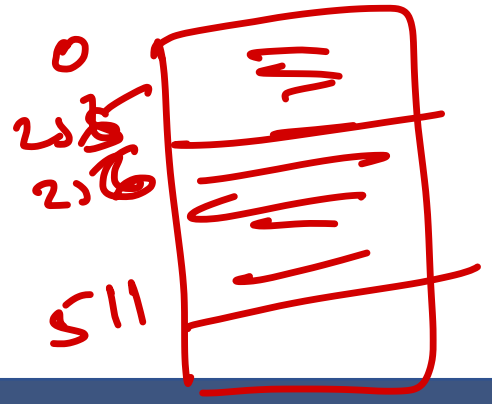
- The cycle time of the processor is reduced.
- It increases the throughput of the system
- It makes the system reliable.

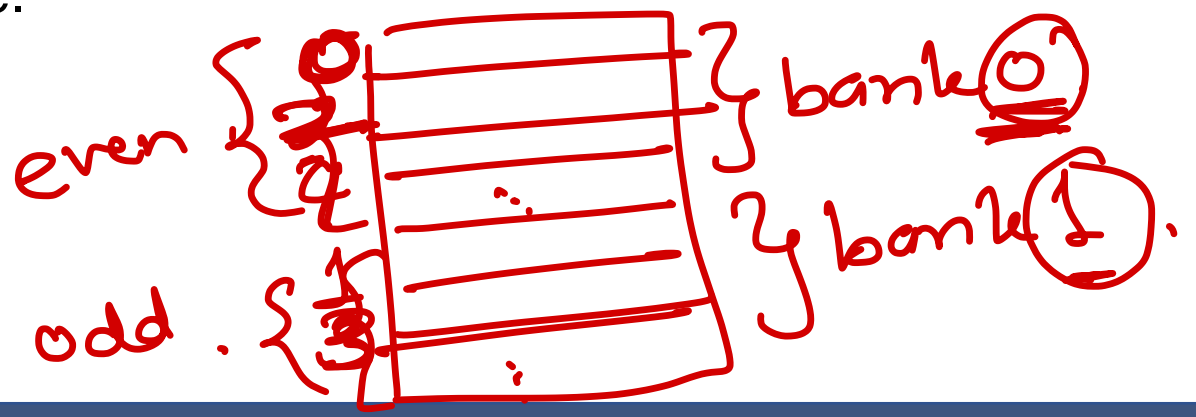
Disadvantages of Pipelining

- The design of pipelined processor is complex and costly to manufacture.

What is Interleaved Memory?

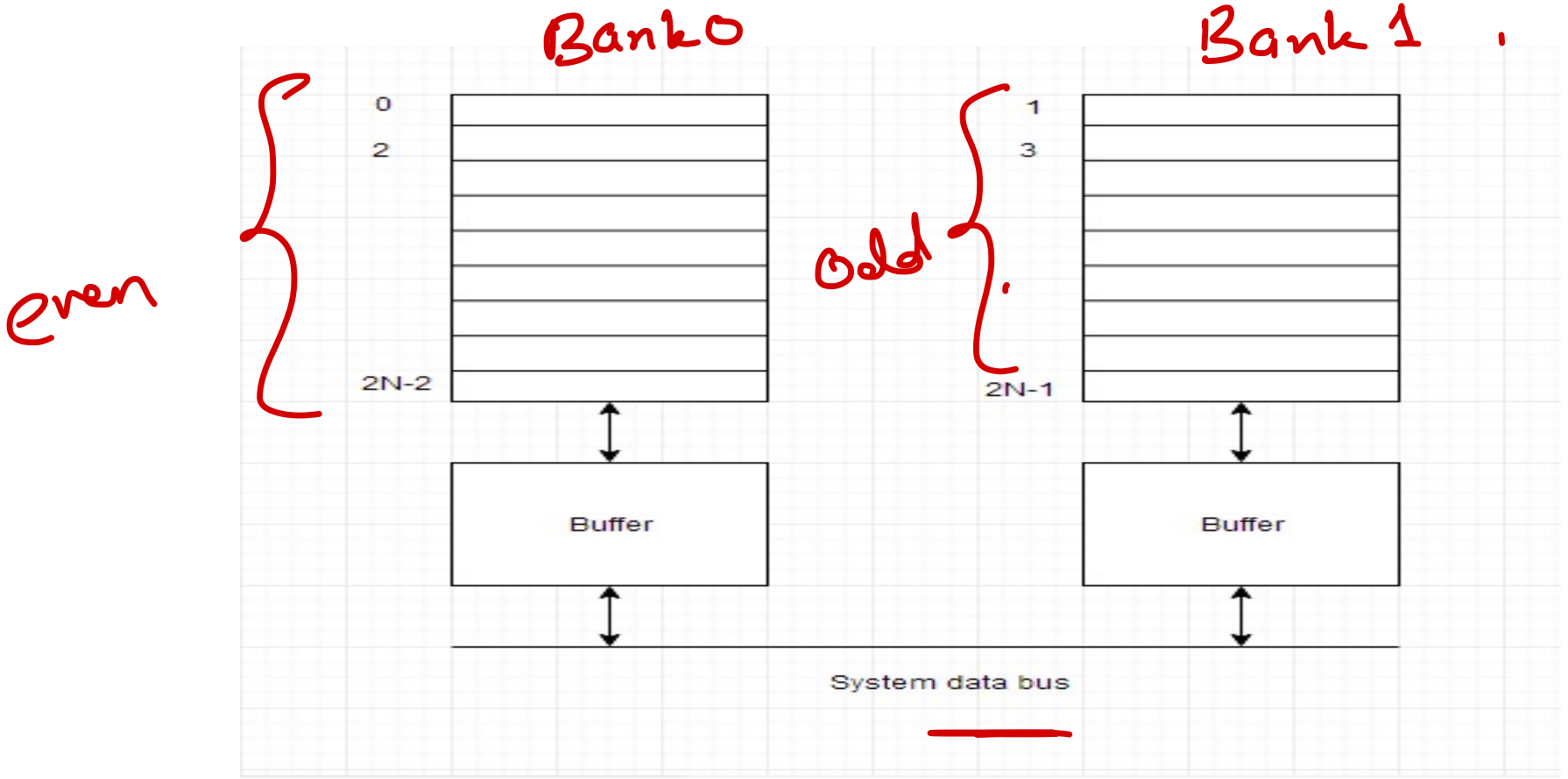
- In this technique, the main memory is divided into memory banks which can be accessed individually without any dependency on the other.
- **For example:** If we have 4 memory banks(4-way Interleaved memory), with each containing 256 bytes, then, the Block Oriented scheme(no interleaving), will assign virtual address 0 to 255 to the first bank, 256 to 511 to the second bank. But in Interleaved memory, virtual address 0 will be with the first bank, 1 with the second memory bank, 2 with the third bank and 3 with the fourth.
- CPU can access alternate sections immediately without waiting for memory to be cached.
- Memory interleaving is a technique for increasing memory speed. It is a process that makes the system more efficient, fast and reliable.





Computer Architecture

- The organization of two physical banks of n long words. All even long words of logical bank are located in physical bank 0 and all odd long words are located in physical bank 1.



μP → Micro computer on chip.

μP → ALU, Control. Unit, Reg.

1st μP → 4004 → 4-bit → Intel.

2nd → 8008 → 8-bit.

8080 → 8-bit →

1974 → 8085 → 8-bit → Intel.

+5V, NMOS. 3MHz

HMOS. 5MHz.

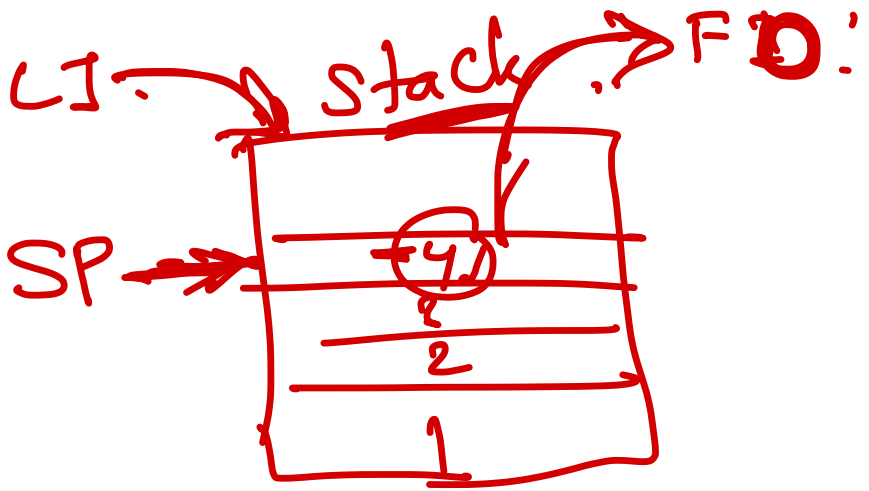
1978 → 8086 → 16-bit → Intel.

+5V, CMOS., 5MHz.

HCMOS.

Microprocessor 8085

- 8085 architecture generally called as "eighty-eighty-five" microprocessor. It is an 8-bit microprocessor which was introduced by Intel in the year 1976 using NMOS technology.
- It has the following configuration –
- 8-bit data bus
- 16-bit address bus, which can address up to 64KB
- A 16-bit program counter
- A 16-bit stack pointer
- Six 8-bit registers arranged in pairs: BC, DE, HL
- Requires +5V supply to operate at 3 MHZ single phase clock



Bus Structure in 8085

- There are three buses in Microprocessor: 1. Address Bus 2. Data Bus 3. Control Bus

Data Bus

- The data bus width is 8-bit i.e. 2^8 = 256 combination of binary digits, identified as D_0– D_7. Data bus is bidirectional since it carries data in binary form between microprocessor and other external units such as memory. It is used to transmit data. As it is 8-bit wide then largest number is 11111111.

Address Bus

- 8085 microprocessor contains 16-bit address bus i.e. 2^{16}= 65536= 64KB memory location it can access, identified as A_0 - A_{15}. Address bus is unidirectional. The address bus carries addresses from microprocessor to the memory or other devices. The higher order address lines are A8 – A15 and the lower order lines (A0 – A7) are multiplexed with the eight bits data lines (D0 – D7).

Control Bus

- Control bus are various lines which have specific functions for coordinating and controlling microprocessor operations. The control bus carries control signals partly unidirectional and partly bidirectional.

Data Bus.

Bidirectional – 8-bit → $2^8 = 256$ (0-255)

11111111

$D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7$

$D_0 D_1 D_2 D_3$ – Lower order

$D_4 D_5 D_6 D_7$ – higherderd

Address Bus. – Unidirectional.

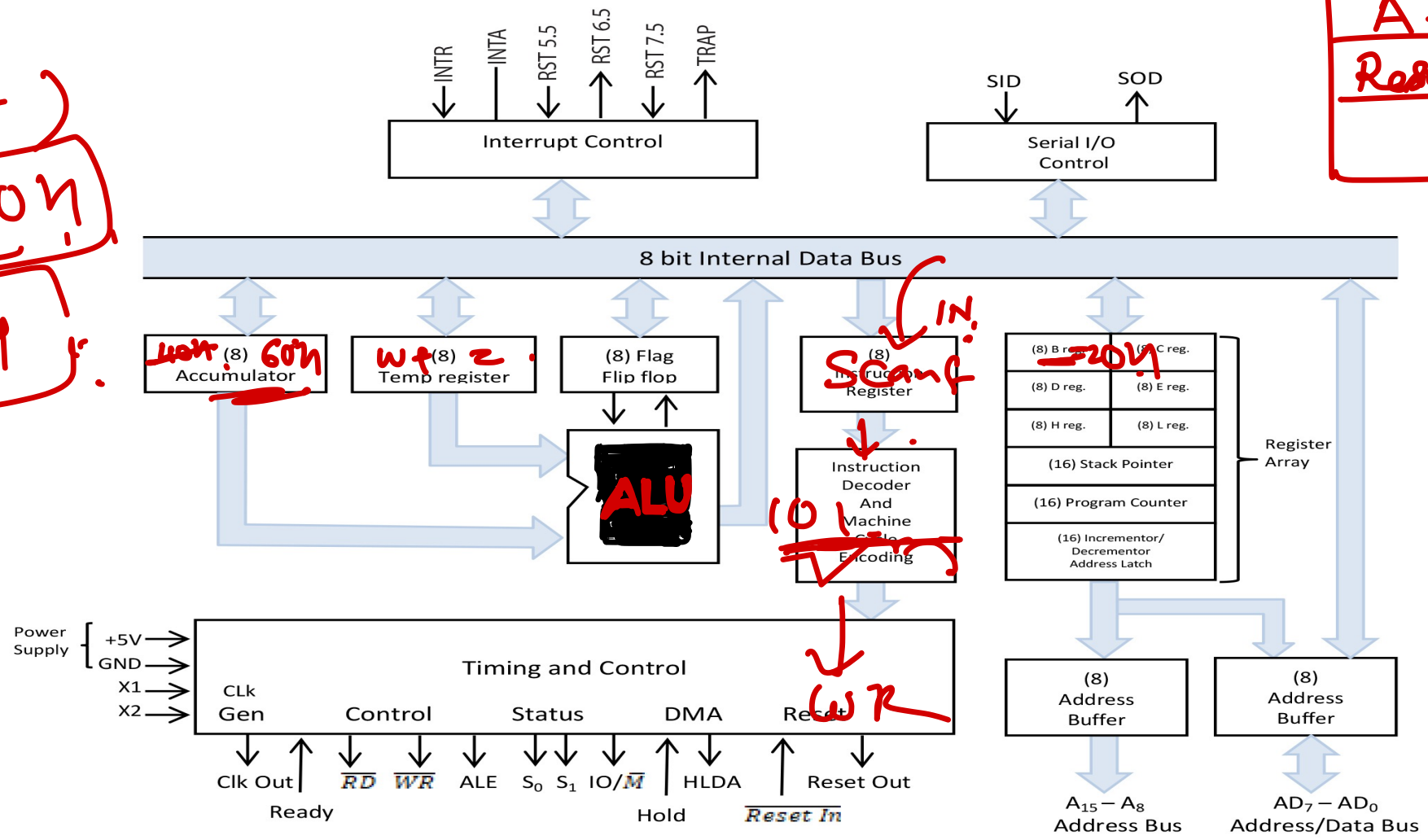
16-bit → $2^{16} = 64KB$

$A_0 A_1 A_2 \ldots A_7$ $A_8 A_9 \ldots A_{15}$

$A_0 A_1 A_2 \ldots A_7$ – lower order Add.

$A_8 A_9 \ldots A_{15}$ – High order Add.

8085 Architecture



Microprocessor 8085

Accumulator

- It is an 8-bit register used for general purposes. It also helps in arithmetic, logical, I/O & LOAD/STORE operations. It is connected to internal data bus & ALU. The data is stored in this register.

Arithmetic and logic unit

- It is helpful in arithmetic and logical operations like Addition, Subtraction, AND, OR, etc. on 8-bit data.

General purpose register

- There are 6 general purpose registers in 8085 processor, i.e. B, C, D, E, H & L. Each register can hold 8-bit data.
- These registers can work in pairs in order to hold 16-bit data and their pairing combination looks like B-C, D-E & H-L.

Program counter

- It is a type of 16-bit register used to store the address of the instructions that is to be executed. Whenever each instruction gets fetched from the program counter its store value is increased by 1.

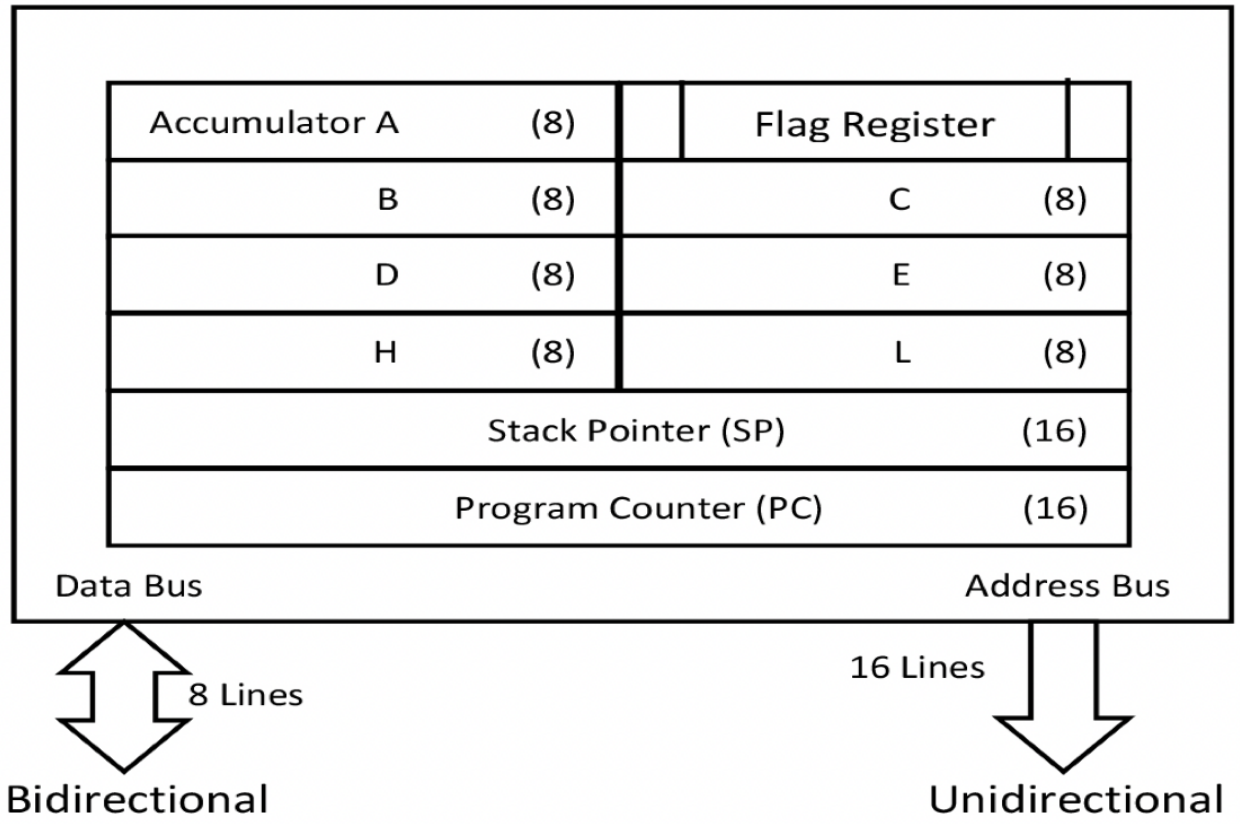
Stack pointer

- It is also a 16-bit register works like stack, which is always incremented/ decremented by 2 during push & pop operations.

Temporary register

- It is an 8-bit register, as the name suggests it holds the temporary data of arithmetic and logical operations. W and Z are temporary register.

Microprocessor 8085

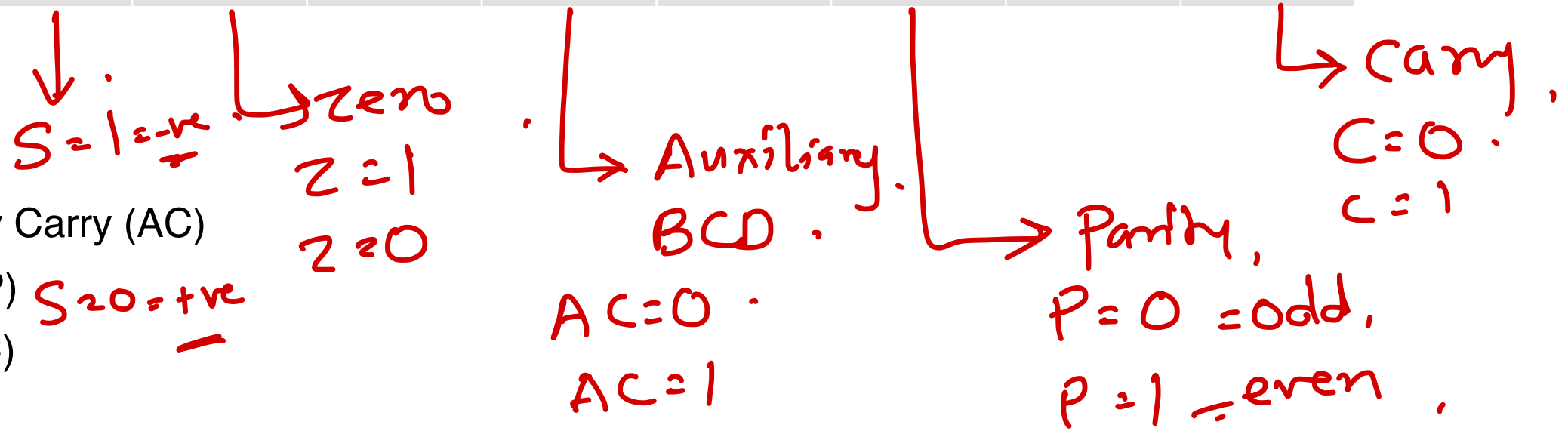


Flag register

- It is an 8-bit register which has five 1-bit flip-flops, which contains either 0 or 1 based on the result data that is stored in the accumulator.

D7	D6	D5	D4	D3	D2	D1	D0
S	Z	×	AC	×	P	×	C

- Sign (S)
- Zero (Z)
- Auxiliary Carry (AC)
- Parity (P)
- Carry (C)



8-bit:

MSB.

$D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0$

20H → 0 0 1 0 0 0 0 0

\+

40H → 0 1 0 0 0 0 0 0

0 1 1 0 0 0 0 0

AC = 0

P = 1

C = 0

Z = 0

S = 0

60H

MSB. D_3

1 1 1 0 1 0 1 0

\+ 1 0 0 1 0 1 0 1

1 0 1 1 1 1 1 1

C = 1

P = 0

AC = 0

Z = 0

S = 0

Microprocessor 8085

Instruction register and decoder

- the instructions that is fetched from the memory. Instruction decoder decodes the information present in the Instruction register.

Timing and control unit

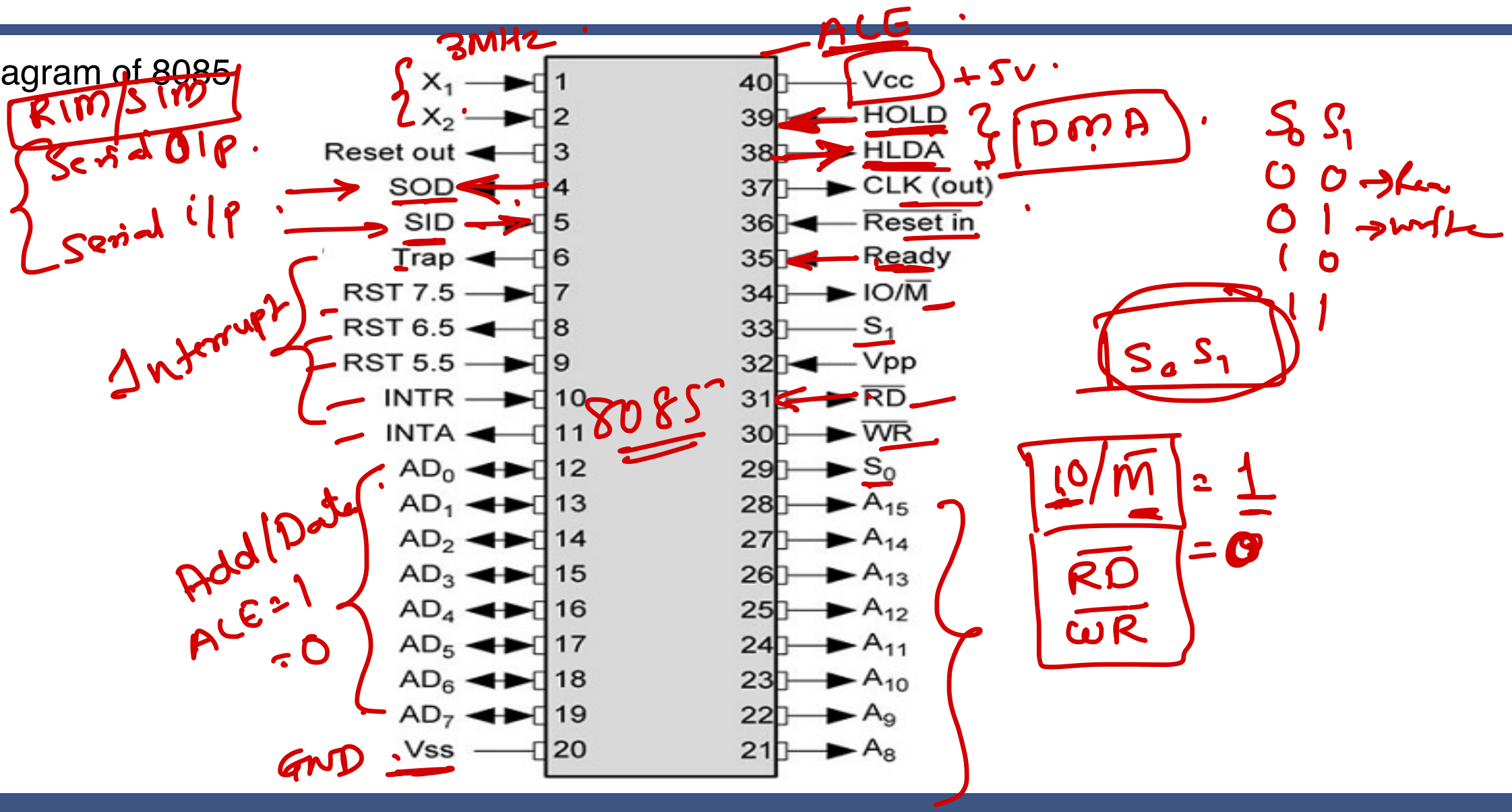
- It supplies timing and control signal to the microprocessor to perform certain operations. Following are the timing and control signals, which control external and internal circuits –
- Control Signals: READY, RD', WR', ALE
- Status Signals: S0, S1, IO/M'
- DMA Signals: HOLD, HLDA
- RESET Signals: RESET IN, RESET OUT

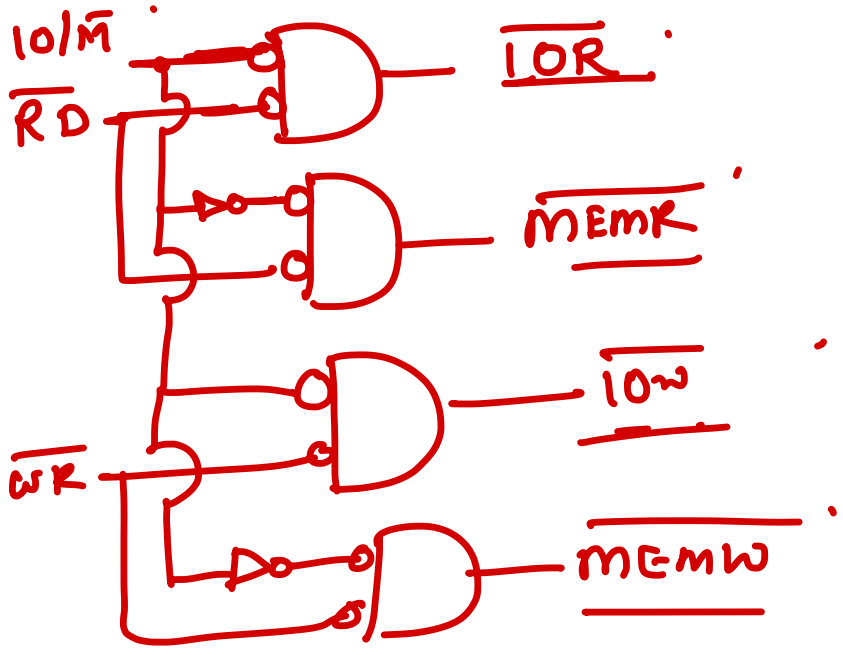
Microprocessor 8085

- 8085 is a 40pin IC. Works on +5v power supply with 3MHz frequency. 8085 signals are classified into six groups:
- Address bus
- Data bus
- Control & status signals
- Power supply and frequency signals
- Externally initiated signals
- Serial I/O signals

Microprocessor 8085

- Pin Diagram of 8085




IO/M
RD
IOR
MEMR
IOW
WR
MEMW

Microprocessor 8085

Address bus

- A15-A8, it carries the most significant 8-bits of memory/IO address.

Data bus

- AD7-AD0, it carries the least significant 8-bit address and data bus.

Control and status signals

- These signals are used to recognize the nature of operation. There are 3 control signal and 3 status signals.

Three control signals are RD, WR & ALE.

- **RD** – This signal signifies the selected IO or memory device that is to be read and helps in accepting data readily available on the data bus.
- **WR** – This signal indicates that the data on the data bus is to be written into a selected memory or IO location.
- **ALE** – It is Address Latch Enable signal.It is a positive going pulse produced when a new operation is started by the microprocessor. When the pulse goes high, it indicates address. When the pulse goes down it indicates data.

Microprocessor 8085

Three status signals are IO/M, S0 & S1.

IO/M

- This signal is used to distinguish between IO and Memory operations, i.e. when it is high indicates IO operation and when it is low then it indicates memory operation.

S1 & S0

- These signals are used to identify the type of current operation.

Power supply

- There are 2 power supply signals – VCC & VSS. VCC indicates +5v power supply and VSS indicates ground signal.

There are 3 clock signals, i.e. **X1, X2, CLK OUT.**

X1, X2 – A crystal is connected at these two pins and is used to set frequency of the internal clock generator. This frequency is internally divided by 2.

CLK OUT – This signal is used when the system clock for devices connected with the microprocessor.

Interrupts & externally initiated signals

- Interrupts are the signals produced by external devices to request the microprocessor to perform a specific task. There are 5 interrupt signals, i.e. TRAP, RST 7.5, RST 6.5, RST 5.5, and INTR.
- **INTA –** It is an interrupt acknowledgment signal.
- **RESET IN** – This signal is used to reset the microprocessor by setting the program counter to zero.
- **RESETOUT–** This signal is used to reset all the connected devices when the microprocessor is reset.
- **READY** – This signal indicates that the device is ready to send or receive data. If READY is low, then the CPU has to wait for READY to go hig**h.**
- **HOLD** – This signal gives hint that another master is requesting the use of the address and data buses.
- **HLDA (HOLD Acknowledge) –** It indicates that the CPU has received the HOLD request and it will relinquish the bus in the next clock cycle. HLDA is set to low after the HOLD signal is removed.

Serial I/O signals

- There are 2 serial signals, i.e. SID and SOD and these signals are used for serial communication.
- **SOD (Serial output data line)** – According to the SIM instruction the output SOD is set/reset.
- **SID (Serial input data line)** - Whenever the data instruction is executed the data on this line is loaded into accumulator.