प्रगत संगणन विकास केन्द्र

Paper Code

C4

CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING

C-DAC's Common Admission Test (C-CAT) – DECEMBER 2014

INSTRUCTIONS TO CANDIDATES

Candidate should read the following instructions before attempting the question paper.

1. **DO NOT CLOSE THE BROWSER ANYTIME DURING THE EXAM.**
2. Candidate **should check his/her name and hall ticket number** being displayed on the screen. In case of any discrepancy, it should be reported to Invigilator immediately.
3. Candidate should ensure that he/she has marked attendance on the attendance sheet and also ensure that session id has also been recorded. Any other session id which has not been mentioned in the attendance sheet would not be considered and all responses on that session id would be treated as null and void.
4. Do not start the exam (do not click **Next** button) before instructed to do so by the Invigilator.
5. **Every Section has 50 objective-type questions.** Each objective-type question has four choices of which only one is correct. Candidate should select the radio button, given below the question, corresponding to his/her correct choice.
6. Marking scheme of C-CAT is as follows:
   a. +3 (plus three) marks for each correct answer.
   b. -1 (minus one) mark for each wrong answer.
   c. 0 (zero) mark for each un-attempted question.
7. **Duration of each Section is ONE hour**. No candidate will be allowed to leave the examination hall before the completion of exam duration.
8. On clicking the **Next** button given at the bottom of the Instructions page, candidate will be directed to the question display screen.
9. Candidate should **note down the Session ID** that is displayed on the question screen after clicking on **Next** button.

10. Once the exam is started:-

    a. **Candidate should not close the browser. In case the browser is closed accidentally, it SHOULD BE reported to the Invigilator immediately.**
    b. **Candidate should not open any other software application on the computer system.**
    c. Candidate should neither shut down the machine nor fiddle with allocated hardware or software.
    d. In case of any problem it should be reported to Invigilator.

11. Candidate can navigate through questions using scroll bar or directly through the question number grid.

12. C-CAT screen contains the following buttons with the below specified functionality:

Button	Functionality
Examination Instruction	This link will open the instructions for the exam. After reading the instructions candidate has to click on [Back] button to move back to the questions interface.
Mark for Review	In case a candidate is not sure about the answer, then he/she can use this Button to mark the question for a visit later. It will be shown with a **?** against the question (in the question number grid) if the question has not been answered but has marked it for review. In case candidate has answered the question and marked it for review, then **√?** will be displayed against the question in the question number grid.
Clear Answer	This button will clear the option marked and the question will be shown as un-answered.

13. Each candidate will be provided one A4 size sheet for rough work. Candidates have to record their Name, hall ticket number and session ID on the rough sheet. They have to return the rough sheet to the Invigilator before leaving the exam hall.
14. Calculators, mobile phones, pagers and electronic gadgets in any form are not allowed to be used in the Exam Hall.

15. Candidate will be disqualified if found indulging in any kind of malpractice.

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1. The average time required to reach a storage location in memory and obtain its content?

   A. Latency time
   B. Access time
   C. Turnaround time
   D. Response time

2. BSA instruction is_____

   A. Branch and store accumulator
   B. Branch and save return address
   C. Branch and shift address
   D. Branch and show accumulator

3. In computers, subtraction is carried out generally by_____

   A. 1's compliment method
   B. 2's compliment method
   C. Signed magnitude method
   D. BCD subtraction method

4. When CPU is executing a program that is part of the operating system, it is said to be in_____

   A. Interrupt mode
   B. System mode
   C. Half mode
   D. Simplex mode

5. In a program if a subroutine call instruction is executed, it is necessary to_____

A. Initialize program counter
B. Clear the accumulator
C. Reset the microprocessor
D. Clear the instruction register

6. The idea of cache memory is based_____

A. On the property of locality of reference
B. On the heuristic 90-10 rule
C. On the fact that reference generally tend to cluster
D. All of the above

7. DMA interface unit eliminates the need to use CPU registers to transfer data

A. MAR to MBR
B. MBR to MAR
C. I/O units to memory
D. Memory to I/O units

8. How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes

A. 8
B. 16
C. 24
D. 32

9. After reset CPU begins execution of instruction from memory address

A. 0101 h
B. 8000 h

C. 0000 h
D. FFFF h

10. When an instruction is read from the memory, it is called?

A. Memory read cycle
B. Fetch cycle
C. Instruction cycle
D. Memory write cycle

11. Which flag of the 8085 flag register is not accessible to programmer directly?

A. Zero flag
B. Carry flag
C. Auxiliary carry flag
D. Parity flag

12. Which of the following is a pseudo instruction?

A. SPHL
B. LXI
C. NOP
D. END

13. Cycle stealing technique is used in

A. Interrupt based data transfer
B. Polled mode data transfer
C. DMA based data transfer
D. None of these

14. Associative memory is sometimes called as

A. Virtual memory
B. Cache memory
C. Main memory
D. Content addressable memory

15. Interrupts which are generated by an instruction are

A. Internal
B. External
C. Hardware
D. Software

16. What does MESI stands for?

A. Mandatory Extension, Shared, Invalid
B. Modified, Exclusive, Shared, Invalid
C. Multi, Extensive, Sharing, Invalid
D. Multiple, Exclusive, Shared, Invalid

17. For a magnetic disk with concentric circular tracks, the seek latency is not linearly proportional to the seek distance due to

A. non-uniform distribution of requests
B. arm starting and stopping inertia
C. higher capacity of tracks on the periphery of the platter
D. use of unfair arm scheduling policies

18. when we move from the outermost track to the innermost track in a magnetic disk, the the density(bits per linear inch)

    A. increases
    B. decreases
    C. remains the same
    D. either remains same or decreases

19. A ROM is used to store the table for multiplication of two 8-bit unsigned integer, the size of the ROM required is

    A. 256K × 16
    B. 64K × 8
    C. 4K × 16
    D. 64 K × 16

20. Let the page fault service time be 10 ms in a computer with memory access time being 20 ns. If one page fault is generated for every 106 memory accesses, what is the effective access time for the memory?

    A. 21ns
    B. 30ns
    C. 23ns
    D. 35ns

21. 'snooping' cache coherency protocol

    A. updates cached value after memory update
    B. invalidates cached value after memory update
    C. invalidates cached value then updates memory
    D. updates cached value and memory location

22. Assuming a memory has 32 blocks and a cache consists of 8 blocks. Where the 13^{th} memory block will be mapped for a direct mapped cache?

    A. 5^{th} cache block
    B. 13^{th} cache block
    C. 6^{th} cache block
    D. none of the above

23. TLB is used for

    A. physical address to virtual address translation
    B. virtual address to physical address translation
    C. store evicted cache lines
    D. none of the above

24. Throughput defines…

    A. No. of task executed per unit time
    B. Ratio of the actual speed-up to the maximum speed-up
    C. Task start time to exit time
    D. Task moved out forcibly

25. The technique of prefetching of instructions and executing them during a pipeline stall due to instruction dependency is called …….

    A. Branch folding
    B. Dispatch unit
    C. Branch delay

D. None of the above

26. How many classifications are there in Flynn's Taxonomy for Computer Architecture

A. 2
B. 3
C. 4
D. 5

27. Consider the Facts and answer:

I.Address Bus is unidirectional
II.Data bus is bi-directional
III Control Bus is Uni-directional

A. I and II are correct , III is incorrect
B. I and III are correct , II is incorrect
C. II and III are correct , I is incorrect
D. I , II and II are correct

28. In computer architecture, a disk storage medium (floppy disk) contains…

A. Sectors only
B. Both circular tracks and sectors
C. Circular tracks only
D. None of the above

29. Optical fibre bandwidth is in the order of …..

A. Order of KHz

B. Order of GHz
C. Order of Hz'
D. None of the above

30. …… provides aefficient connection for a computers in a wide geographical area.

A. Coaxial cables
B. Twisted pair lines
C. Communications satellites
D. None of the above

31. If (2.3)base 4 + (1.2)base 4 = (y)base 4 ; what is the value of y?

A. 10.1
B. 10.01
C. 10.2
D. 1.02

32. The number of 1 in 8-bit representation of -127 in 2's complement form is m and that in 1's complement form is n. What is the value of m:n ?

A. 1 : 2
B. 2 : 1
C. 3 : 1
D. 1 : 3

33. The number of ones in 8-bit 1's complement form of -10

A. 3
B. 5
C. 2

D. 6

34. The octal representation of 11001100 is

A. 314
B. 630
C. 614
D. none of above

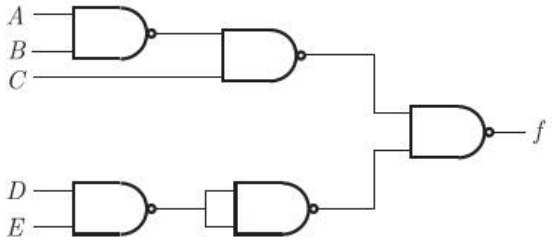
35. When four 1s are taken as a group on a Karnaugh map, the number of variables eliminated from the output expression is _____.

A. 2
B. 3
C. 4
D. 1

36. Determine the values of A, B, C, and D that make the sum term $\overline{A} + B + \overline{C} + D$ equal to zero.

A. A = 1, B = 0, C = 0, D = 0
B. A = 0, B = 1, C = 0, D = 0
C. A = 1, B = 0, C = 1, D = 0
D. A = 1, B = 0, C = 1, D = 1

37. Which one of the following functions is realized by the circuits shown below ?



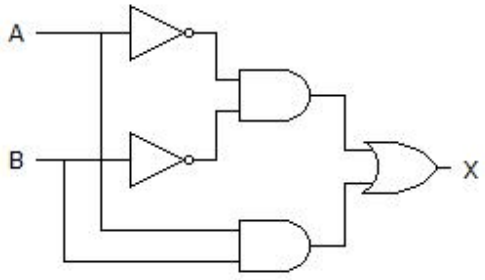
A. $(\overline{A}+\overline{B})C+\overline{DE}$

B. $(A+B)C+D+E$

C. $AB+C+DE$

D. $AB+C(D+E)$

38. What type of logic circuit is represented by the figure shown below?



A. XOR

B. XNOR

C. XAND

D. XNAND

39. How many 4-bit parallel adders would be required to add two binary numbers each representing decimal numbers up through 300_{10}?

A. 1

B. 2

C. 3

D. 4

40. The carry propagation can be expressed as _____.

A. $C_p = AB$
B. $C_p = A + B$
C. $C_{p=} A \oplus B$
D. $C_{p=} A + \overline{B}$

41. Which of the following statements correctly defines the full-adder ?

An adder circuit

A. Having two inputs used to add two binary digits. It produces their sum and carry as input.
B. Having three inputs used to add two binary digits plus a carry. It produces their sum and carry as outputs.
C. Used in the least significant position when adding two binary digits with no carry-in to consider. It produces their sum and carry as outputs.
D. Having two inputs and two outputs.

42. _____ is a correct combination for an ODD-parity data transmission system.

A. data = 1101 1011
   parity = 1
B. data = 1101 0010
   parity = 0

C. data = 0001 0101
   parity = 1
D. data = 1010 1111
   parity = 0

43. An 8-bit serial in/serial out shift register is used with a clock frequency of 2 MHz to achieve a time delay (td) of _____

A. 16 us
B. 8 us
C. 4 us
D. 2 us

44. A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. The Q output is _____

A. constantly LOW
B. constantly HIGH
C. a 20 kHz square wave
D. a 10 kHz square wave

45. When two counters are cascaded, the overall MOD number is equal to the _____ of their individual MOD numbers

A. product
B. sum
C. log
D. reciprocal

46. A MOD-12 and a MOD-10 counter are cascaded. Determine the output frequency if the input clock frequency is 60 MHz.

A. 500 kHz
B. 1,500 kHz
C. 6 MHz
D. 5 MHz

47. An asynchronous 4-bit binary down counter changes from count 2 to count 3. How many transitional states are required?

A. None
B. One
C. Two
D. Fifteen

48. Which of the following best describes static memory devices?

A. memory devices that are magnetic in nature and do not require constant refreshing
B. memory devices that are magnetic in nature and require constant refreshing
C. semiconductor memory devices in which stored data will not be retained with the power applied unless constantly refreshed
D. semiconductor memory devices in which stored data is retained as long as power is applied

49. How many storage locations are available when a memory device has 12 address lines?

A. 144

B. 512

C. 2048

D. 4096

50. How many address lines would be required for accessing 4 memory chips of 2Kbytes each. Memory chips has 8 bits data bus ?

A. 11

B. 12

C. 13

D. 14