S	R
0	0
0	1
1	0
1	1

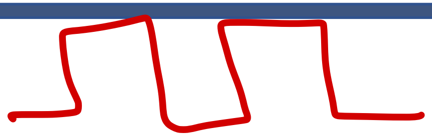
K-Map

SR \ Q		
00		1
01		
11	X	X
10	1	1

	clk	S	R
1			
$\uparrow$	$\downarrow$ 0		—

Counter

- Counters will count the number of pulses applied to the count input



- Counter is a sequential circuit.
- Counters are constructed using Flipflops and logic gates
- An ‘N’ bit binary counter consists of ‘N’ flip-flops

$n = n$ FF

- **Up/Down counter**
  - If the counter counts from 0 to 2^n – 1(zero-max), then it is called as binary up counter.
    - Example : 4- bit counter has 4 FF and counter counts from 0000 to 1111
  - Similarly, if the counter counts down from 2^n – 1 to 0(max-zero), then it is called as binary down counter.
    - Example : 4- bit counter has 4 FF and counter counts from 1111 to 0000

MOD 4 $\rightarrow 2^2 \rightarrow$ 2bit – 2FF

- **Modulus Counter/ MOD – N Counter**
  - The number of states that a counter can count is known as the modulus or MOD of the counter
  - The 2-bit ripple counter is called as MOD-4 counter and 3-bit ripple counter is called as MOD-8 counter
  - So in general, an n-bit ripple counter is called as modulo-N counter. Where, MOD number = 2^n .

$2^3 = 8$

up.

000

incr.
Binary
up.

111

down.

111

decre
Binary
down.

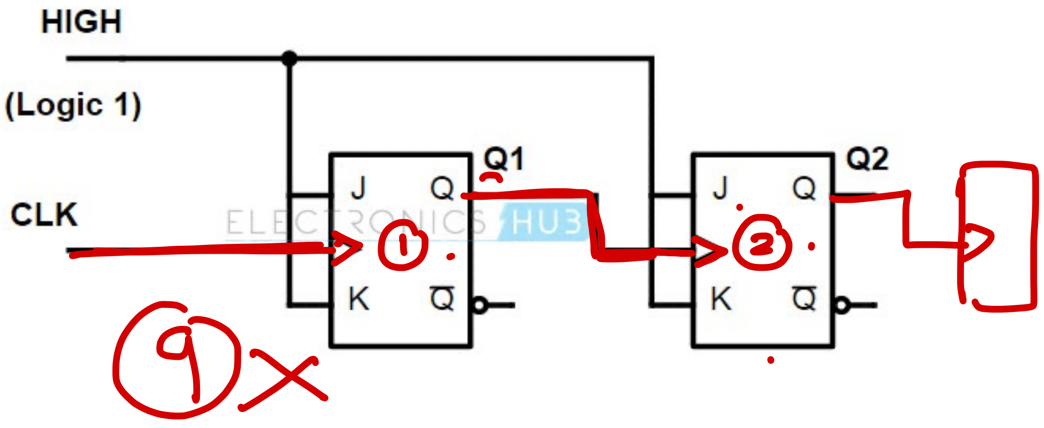
000

Counter

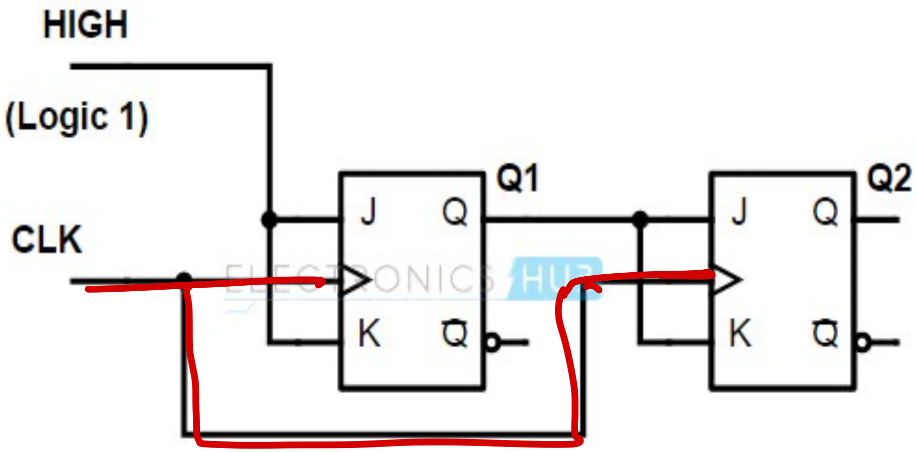
- Counters are of two types.
  - **Asynchronous or ripple counters**
    - The first flip-flop is clocked by the external clock pulse and then each successive flip-flop is clocked by the output of the preceding flipflop.
    - Asynchronous counters are also called as Truncated counters.

Mod 5
~~Mod 16~~
Mod 3

$2^2 = 4$ $2^3 = 8$



  - **Synchronous counters**
    - In synchronous counters, the clock input is connected to all of the flip-flops so that they are clocked simultaneously.

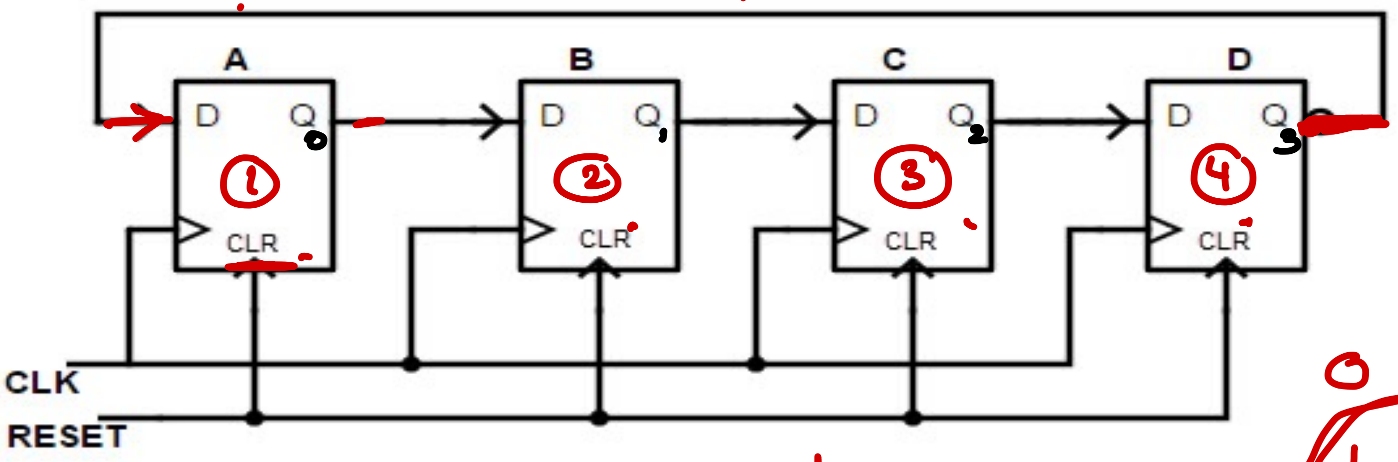


Counter

- Application of counters
  - Frequency counters
  - Digital clock
  - Time measurement
  - A to D converter
  - Frequency divider circuits
  - Digital triangular wave generator

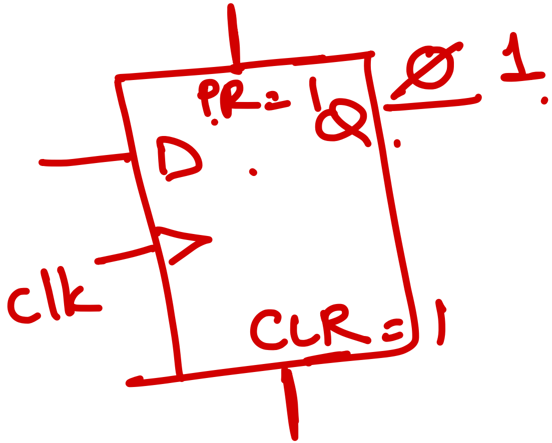
Ring Counter

- The ring counter is a cascaded connection of flip flops, in which the output of last flip flop is connected to input of first flip flop.
- Ring counter is called a divide by N counter, where N is the number of flip-flops.



TT

	Q_0	Q_1	Q_2	Q_3
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	0
		0	0	0

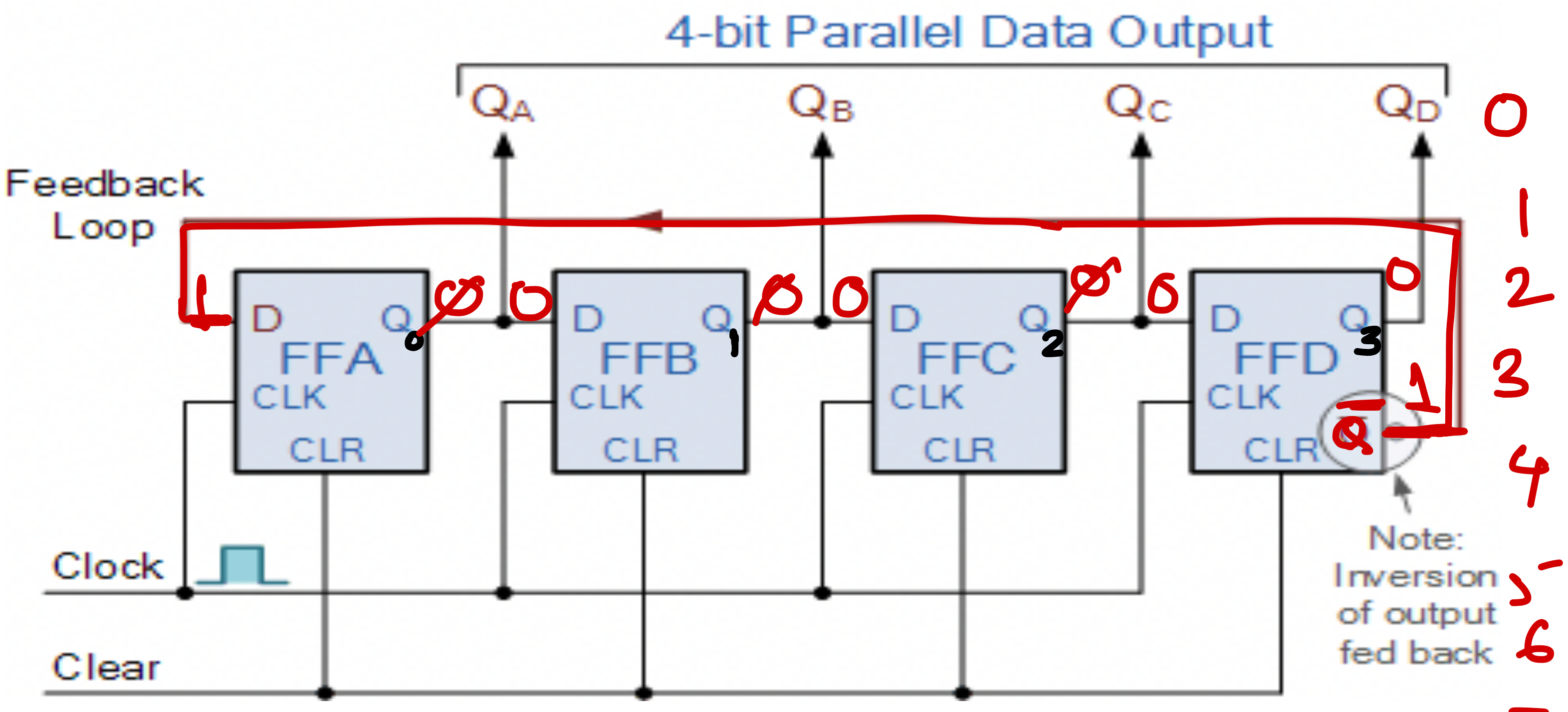


PR	$\overline{CLR}$	
0	0	Normal FF.
0	1	0 (Reset)
1	0	1 (set).
1	1	None.

Johnson counter

Mod = $\boxed{2N}$ → FF.

- The complement output of final flip-flop is connected to the input of first flip-flop.
- Johnson counter is also called Twisted ring counter or divide by $\boxed{2N}$ counter. TT



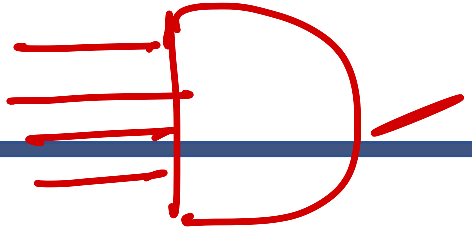
	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
	0	0	0	0

	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1

Logic Families

0 - 5v

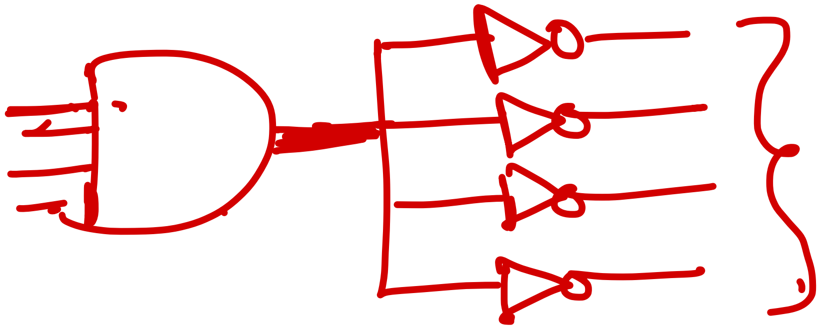
low high



- **Fan In**
  - The fan-in defined as the maximum number of inputs that a logic gate can accept. If number of input exceeds, the output will be undefined or incorrect.

- **Fan Out**
  - The fan-out is defined as the maximum number of inputs (load) that can be connected to the output of a gate without degrading the normal operation.
  - Fan Out is calculated from the amount of current available in the output of a gate and the amount of current needed in each input of the connecting gate.
  - Exceeding the specified maximum load may cause a malfunction because the circuit will not be able supply the demanded power.

i/p



Noise Margin

- Ability of the gate to tolerate fluctuations of the voltage levels.
- Stray electric and magnetic fields may induce unwanted voltages, known as noise, on the connecting wires between logic circuits
- Noise margin is the amount of noise that a circuit could withstand without compromising the operation of circuit.

Power Dissipation

Power dissipation is the amount of heat (in mill watts) that the IC dissipates in the form of heat.

Propagation Delays:

The delay change in output after applying the input.

- t_{pHL} : delay time in going from logic 1 to logic 0 (turn-off delay).
- t_{pLH} : delay time in going from logic 0 to logic 1(turn-on delay)

Logic Families

R

(RTL)

- In **Resistor-transistor logic** which uses a resistor as input and a transistor as switching device.

- **Diode-transistor logic(DTL)** which uses a diode for logic functions while a transistor for amplifying functions.

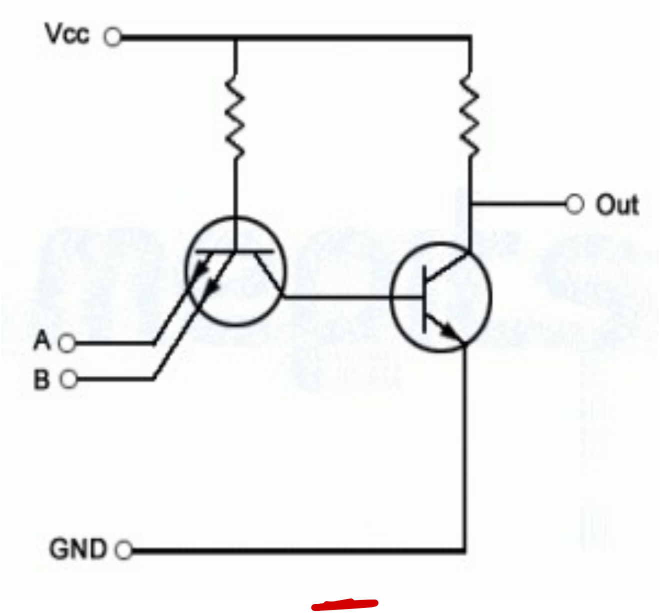
Transistor-Transistor Logic Families(TTL)

- It is the modified form of DTL(Diode Transistor Logic), invented in 1961 by James L Buie. The diodes were replaced by transistor to improve the circuit operation. It is called transistor-transistor logic because transistor performs both the logic function and the amplifying function.

Logic Families

Advantages of TTL Logic Families

- TTL has a strong drive capability.
- It is least susceptible to electrical damage.
- Lesser immune to noise when compared to ECL, but more than CMOS.
- Fastest saturation, when compared to other logic families
- Low output impedance for all states



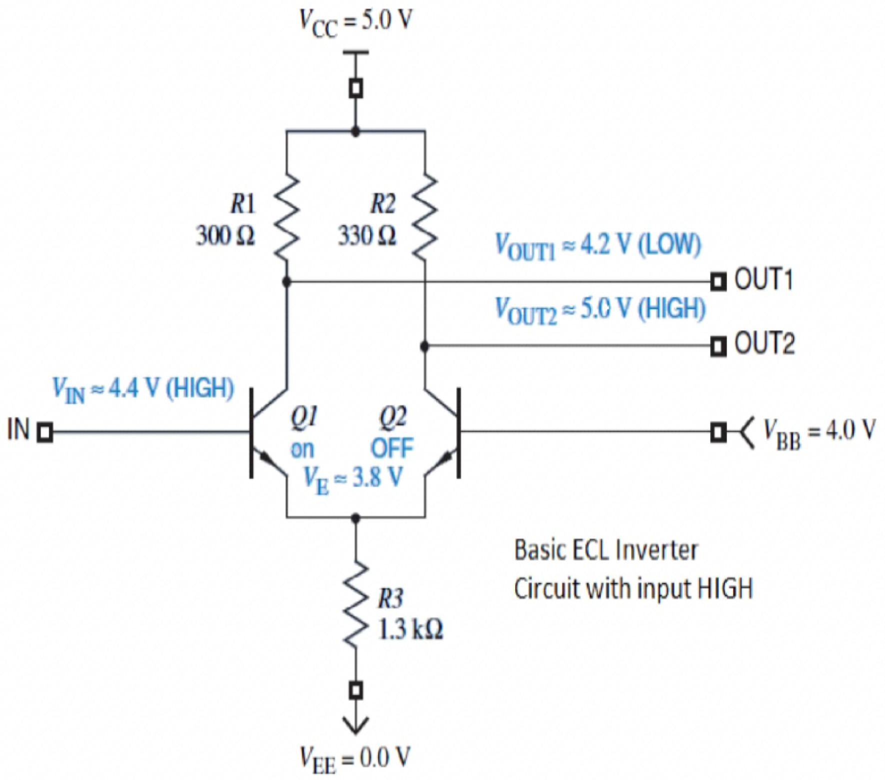
Disadvantages of TTL Logic Families

- TTL dissipates a lot of power, thus not making it suitable for battery-powered devices.
- Expensive compared to MOSFETs

Logic Families

Emitter – Coupled Logic Families (ECL).

- The emitters of the transistors are connected all together, hence the name 'emitter-coupled' logic families.
- It provides highest speed digital circuits. It is used in systems such as supercomputers and signal processors where high speed is required. ECL uses overdriven BJT in its circuit.



Basic ECL Inverter Circuit with input HIGH

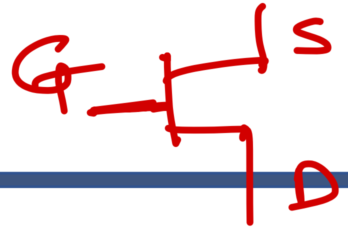
Advantages of ECL Logic Families

- Has a fan-out better than the TTL Logic family
- Offers the highest speed in operation
- Parameters do not vary much with temperature

Disadvantages of ECL Logic Families

- Worst noise immunity compared to TTL and CMOS
- Highest power consumption, when compared with TTL and CMOS
- Capacitive loading reduces the fan-out capacity

Logic Families

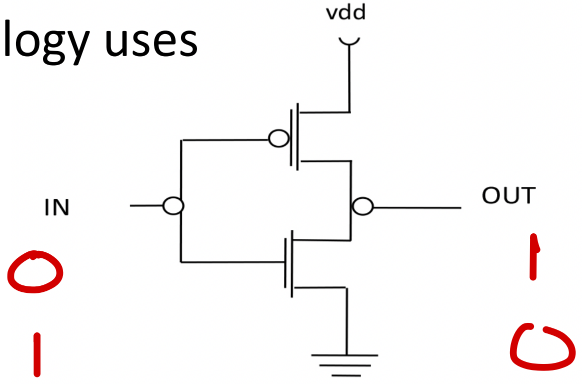


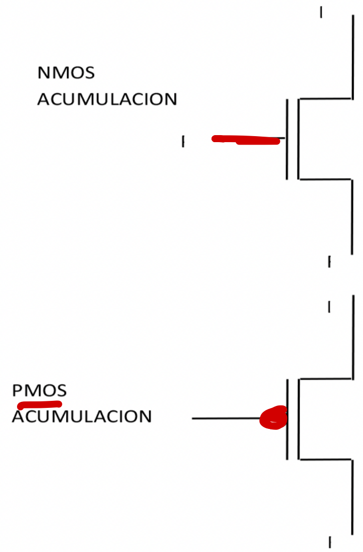
CMOS

MOS stands for Metal Oxide Semiconductor and this technology uses FETs.

MOS can be classified into three sub-families:

1) PMOS (P-channel)
2) NMOS (N-channel)
3) CMOS (Complementary MOS)





Advantages of CMOS Logic Families

The highest fan-out, when compared with TTL and ECL

Noise immunity is better than TTL and ECL

Power dissipation is low.

Waste heat production is very less as compared to other logic families.

Disadvantages of CMOS Logic Families

Average propagation delay is the least in comparison with TTL and ECL a

b   b

c

d

Questions

Question 1

The Universal gate is ________

a) NAND gate
b) OR gate
c) AND gate
d) None of the above

Question 2

An OR gate has 6 inputs. The number of input words in its truth table are

no of comb.

OR → 6 i/p.

$2^6 = 64$.

a) 6
b) 32
c) 64
d) 128

Question 3

In which of the following base systems is 123 not a valid number?

a) Base 10 → 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.
b) Base 16 → 0-9, A-F.
c) Base 8 → 0 – 7
d) Base 3 → 0, 1, 2

Question 4

In case of OR gate, no matter what the number of inputs

a) 1 at any input causes the output to be at logic 1
b) 1 at any input causes the output to be at logic 0
c) 0 at any input causes the output to be at logic 1
d) 0 at any input causes the output to be at logic 0

1 1

0 0 0

Question 5

The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called _________________

a) Combinational circuits
b) Sequential circuits
c) Latches
d) Flip-flops

Question 6

Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?

a) Low input voltages
b) Synchronous operation
c) Gate impedance
d) Cross coupling

Question 7

One example of the use of an S-R flip-flop is as ____________

a) Transition pulse generator
b) Racer
c) Switch de-bouncer
d) Astable oscillator

Question 8

The characteristic equation of J-K flip-flop is ________________

a) Q(n+1)=JQ(n)+K'Q(n)

b) Q(n+1)=J'Q(n)+KQ'(n)

c) Q(n+1)=JQ'(n)+KQ(n)

d) Q(n+1)=JQ'(n)+K'Q(n)

$\boxed{J\bar{Q} + \bar{K}Q_n}$

Question 9

Propagation delay time, tPLH, is measured from the _________.

a) triggering edge of the clock pulse to the LOW-to-HIGH transition of the output
b) triggering edge of the clock pulse to the HIGH-to-LOW transition of the output
c) preset input to the LOW-to-HIGH transition of the output
d) clear input to the HIGH-to-LOW transition of the output

Question 10

A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?

a) Tristate
b) End around
c) Universal
d) Conversion

Question 11

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first)

a) 1100

b) 0011

c) 0000

d) 1111

4-bit SISO → Right

LSB

1100

	Q_0	Q_1	Q_2	Q_3
	0	0	0	0
1	0	0	0	0
2	0	0	0	0

Question 12

A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains ________ (Right most bit).

a) 0000

b) 1111

c) 0111

d) 1000

Question 13

A register is defined as ____________

a) The group of latches for storing one bit of information
b) The group of latches for storing n-bit of information
c) The group of flip-flops suitable for storing one bit of information
d) The group of flip-flops suitable for storing binary information

Question 14

right / $\overline{Left} = 0$

A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing ________

Low → Left

a) 1110

b) 0111

c) 1000

d) 1001

	Q_0	Q_1	Q_2	Q_3	MSB Serial 0 1 1 1
	1	1	1	0	
1	1	1	0	0	
2	1	0	0	1	

Question 15

The terminal count of a typical modulus-10 binary counter is ____________

a) 0000

b) 1010

c) 1001

d) 1111

0

9 → 1001

mod 4

0

3 → 011

mod 6

0

5 → 0101

Question 16

A modulus-10 counter must have ________

a) 10 flip-flops
b) 4 Flip-flops
c) 2 flip-flops
d) Synchronous clocking

$2^n \geq \text{Mod}\,N.$

$4 = 2^2 \geq 10$

$8 = 2^3 \geq 10$

$16 = 2^{\boxed{4}} \geq 10$

4bit - 4FF

N-bit $\rightarrow$ N FF.

Question 17

Which is ~~not~~ an example of a truncated modulus?

2^3

a) 8
b) 9
c) 11
d) 15

Question 18

DeMorgan's theorem states that __________

a) (AB)' = A' + B'
b) (A + B)' = A' * B
c) A' + B' = A'B'
d) (AB)' = A' + B

$$\overline{A+B} = \bar{A}\cdot\bar{B}$$

$$\overline{A\cdot B} = \bar{A}+\bar{B}$$

$(AB)'$

$\overline{AB}$

Question 19

ECL is a way of achieving higher speed of gate.

a) True
b) False

Question 20

Which logic is the fastest of all the logic families?

a) TTL
b) ECL
c) HTL
d) DTL

Question 21

CMOS behaves as a/an _____________

a) Adder
b) Subtractor
c) Inverter
d) Comparator

Question 22

Two important characteristics of CMOS devices are ____________

a) High noise immunity
b) Low static power consumption
c) High resistivity
d) Both high noise immunity and low static power consumption

Question 23

A ___________ gate gives the output as 1 only if all the inputs signals are 1.

a) AND
b) OR
c) EXOR
d) NOR

1 1 1 1

Question 24

Convert binary to octal: (110110001010)2 =?

6 6 1 2

a) (5512)8

b) (6612)8

c) (4532)8

d) (6745)8

Question 25

Which of the following correctly describes the distributive law.

$A + (B.C) = (A+B).(A+C)$

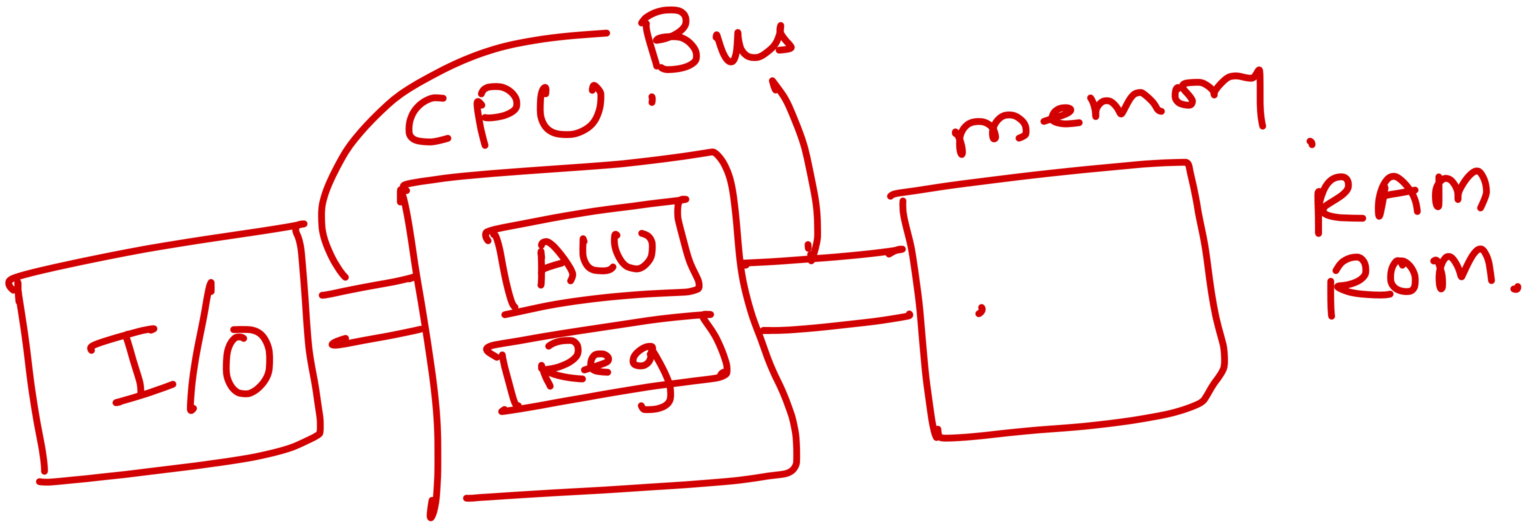
$(A+B).C = AC + BC$

a) (A+B)(C+D)=AB+CD

b) (A+B).C=AC+BC

c) (AB)(A+B)=AB

d) (A.B)C=AC.AB



Computer Architecture

3 - Buses.
Add
control.
Data

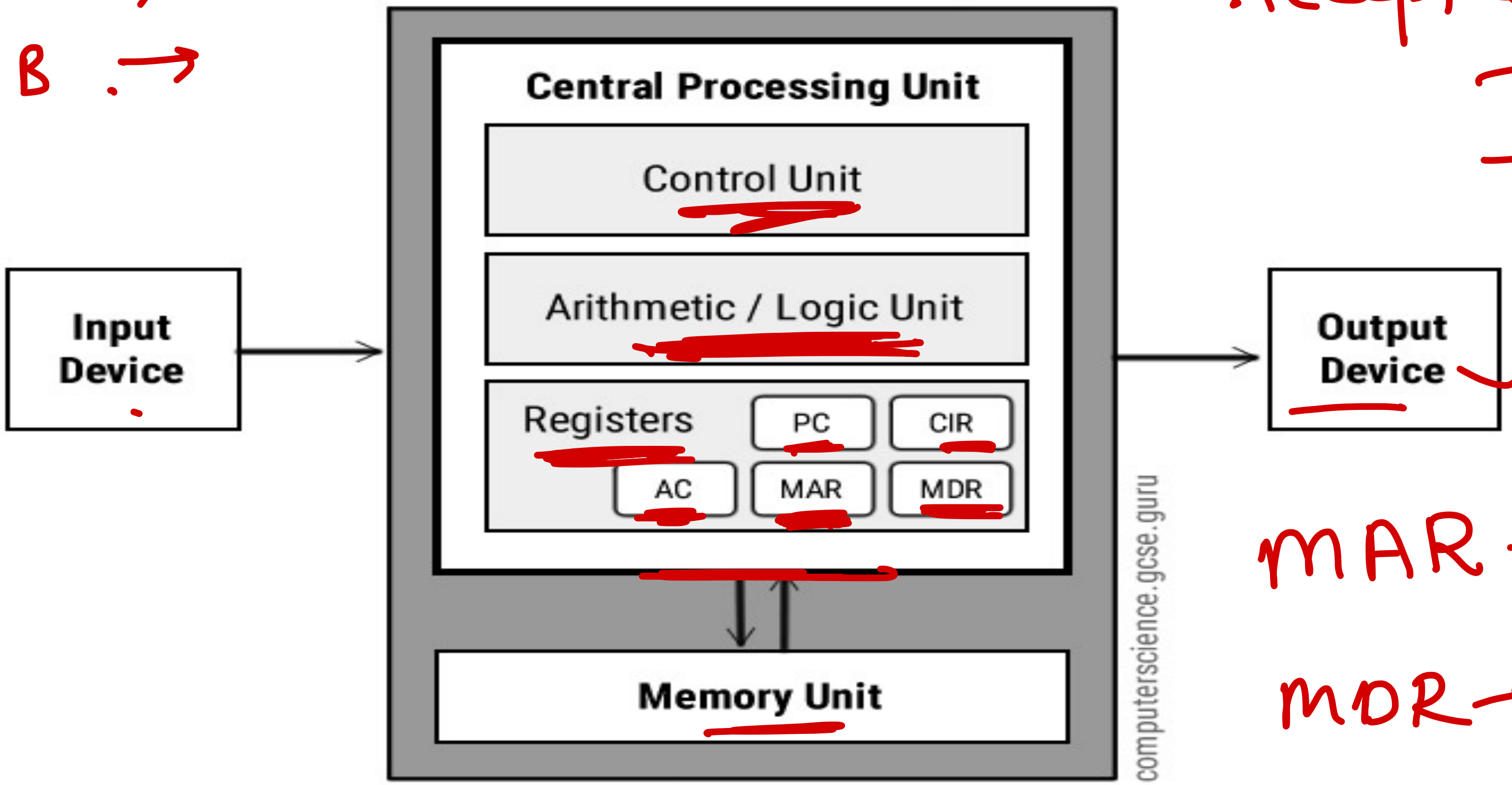
Computer Architecture

Volatile – RAM
Non-Volatile – ROM

- Computer is an electronic machine that perform any task very easy. In computer, the CPU executes each instruction provided to it, in a series of steps, this series of steps is called **Machine Cycle.**
- One machine cycle involves *fetching of instruction*, *decoding the instruction, executing the instruction*

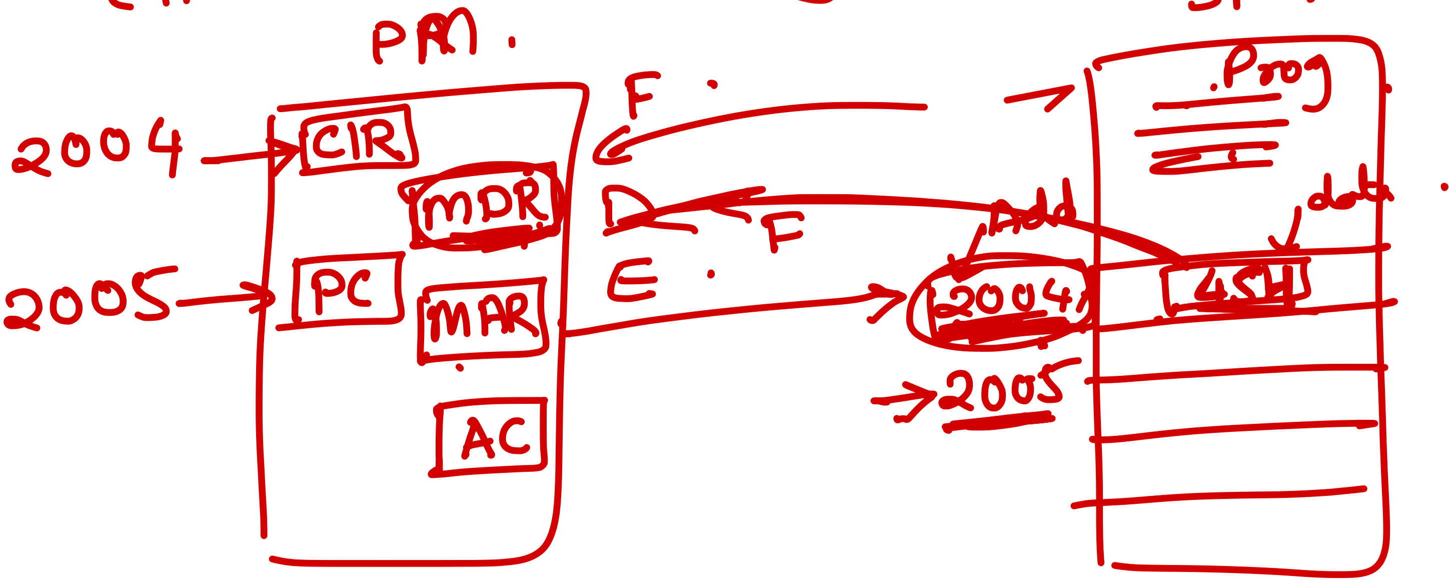
CIR
1) Accept 1st A →
PC
2) Accept 2nd B →
3) A+B
4) Result

Accept → F D E



MAR → memory Addr Reg.
MDR → memory data Reg.

CIR → Current Inst Reg



AC → 1.

PC - Prog Counter.

A+B → ALU

Computer Architecture

- Computer architecture design consists of a Control Unit, Arithmetic and Logic Unit(ALU), Memory Unit, Register and Inputs/Outputs.
- **Central Processing Unit (CPU)**
  - The CPU is the electronic circuit responsible for executing the instructions of a computer program.
  - It is sometimes referred to as the microprocessor or processor.
- **Registers**
  - Registers are high speed storage areas in the CPU. All data must be stored in a register before it can be processed.
  - MAR - Memory Address Register
    - Holds the memory location of data that needs to be accessed
  - MDR - Memory Data Register
    - Holds data that is being transferred to or from memory
  - AC – Accumulator
    - Where intermediate arithmetic and logic results are stored
  - Program Counter
    - Contains the address of the next instruction to be executed

Computer Architecture

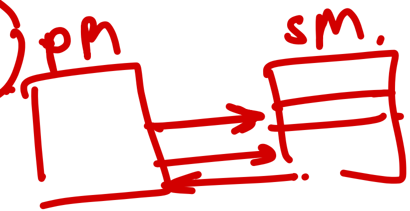
- **CIR – Current Instruction Register**
  - Contains the current instruction during processing
- **Arithmetic and Logic Unit (ALU)**
  - The ALU allows arithmetic (add, subtract etc) and logic (AND, OR, NOT etc) operations to be carried out.
- **Control Unit (CU)**
- The control unit controls the operation of the computer's ALU, memory and input/output devices, telling them how to respond to the program instructions it has just read and interpreted from the memory unit.
- The control unit also provides the timing and control signals required by other computer components.
- **Buses**
  - Buses are the means by which data is transmitted from one part of a computer to another, connecting all major internal components to the CPU and memory.
  - **Address Buses**
    - Carries the addresses of data (but not the data) between the processor and memory
  - **Data Buses**
    - Carries data between the processor, the memory unit and the input/output devices
  - **Control Buses**
    - Carries control signals/commands from the CPU in order to control and coordinate all the activities within the computer

Address Bus.

$A_0 A_1 A_2 - A_{15}$ Unidirectional.

μP: $\boxed{4}$

$2^4 = 16$



Data Bus.

$D_0 D_1 D_2 D_3$. Bidirectional.

Control Bus.

$\overline{RD}$

$\overline{WR}$

Input/Output Devices

- Program or data is read into main memory from the *input device* or secondary storage under the control of CPU input instruction. *Output devices* are used to output the information from a computer.

Memory Unit

- A **Memory Unit** is a collection of storage cells together with associated circuits needed to transfer information in and out of storage.
- Two major types of memories are used in computer systems: **Random Access Memory(RAM)** and **Read Only Memory(ROM)**.
- The memory unit consists of RAM, sometimes referred to as primary or main memory. Unlike a hard drive (secondary memory), this memory is fast and also directly accessible by the CPU.
- RAM is split into partitions. Each partition consists of an address and its contents

Computer Architecture

- **RAM**: Random Access Memory
  - **DRAM**: Dynamic RAM, is made of capacitors and transistors, and must be refreshed every 10~100 ms. It is slower and cheaper than SRAM.
  - **SRAM**: Static RAM, has a six transistor circuit in each cell and retains data, until powered off.
  - **NVRAM**: Non-Volatile RAM, retains its data, even when turned off. Example: Flash memory.
- **ROM**: Read Only Memory, is non-volatile and is more like a permanent storage for information.

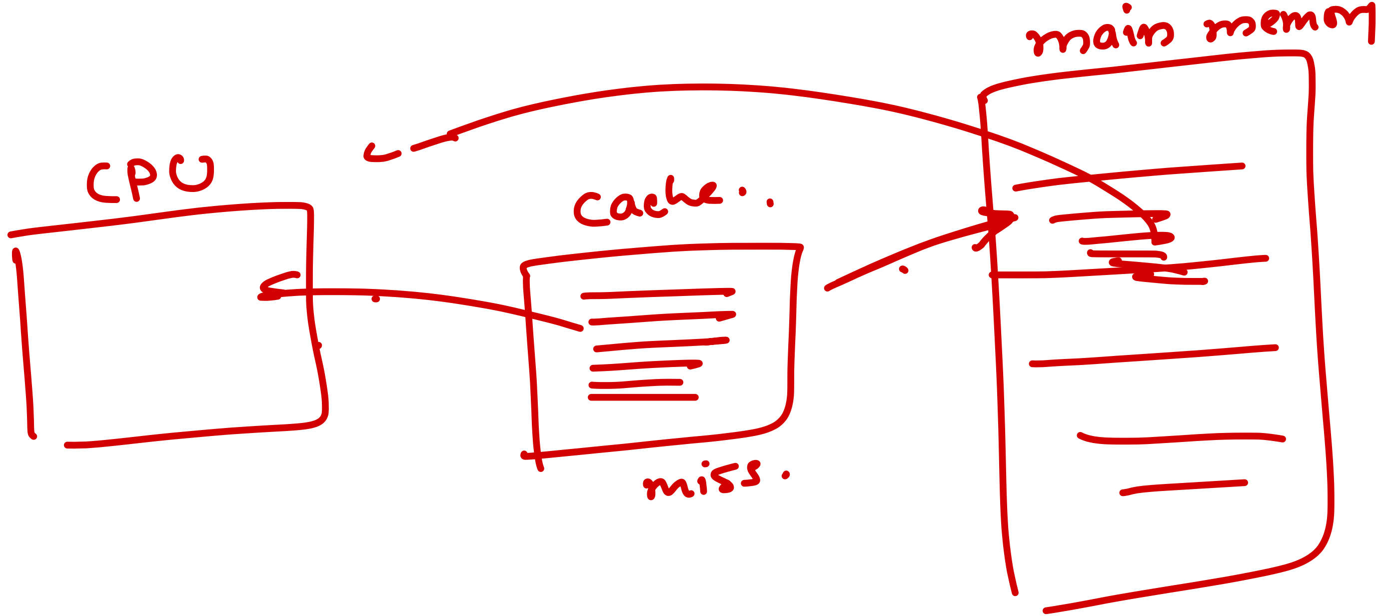
PROM(Programmable ROM), **EPROM**(Erasable PROM) and **EEPROM**(Electrically Erasable PROM) are some commonly used ROMs.

Auxiliary Memory

- Devices that provide backup storage are called auxiliary memory. **For example:** Magnetic disks and tapes are commonly used auxiliary devices. Other devices used as auxiliary memory are magnetic drums, magnetic bubble memory and optical disks.

Cache Memory

- The data or contents of the main memory that are used again and again by CPU, are stored in the cache memory so that we can easily access that data in shorter time.
- Whenever the CPU needs to access memory, it first checks the cache memory. If the data is not found in cache memory then the CPU moves onto the main memory
- The performance of cache memory is measured in terms of a quantity called **hit ratio**. When the CPU refers to memory and finds the word in cache it is said to produce a **hit**. If the word is not found in cache, it is in main memory then it counts as a **miss**.
- Hit Ratio = Hit/(Hit + Miss)


main memory.
CPU
cache.
miss.

8-bit → 1 byte
16-bit → 2 byte.
32-bit → 4 bytes.

Word

- The memory stores **binary information(1's and 0's)** in groups of **bits** called **words**.
- A memory word is a group of 1's and 0's and may represent a number, an instruction code, one or more alphanumeric characters, or any other binary coded information.

16-bit → 1 word
32-bit → 2 word.

Byte

- A group of **eight bits** is called a **byte**. Most computer memories use words whose number of bits is a multiple of 8. Thus a 16-bit word contains two bytes, and a 32-bit word is made up of 4 bytes.
- The capacity of memories in computers is usually stated as the total number of bytes that can be stored.

K(Kilo) is equal to 1024bytes = 2^{10}. = 1K.

M(Mega) is equal to 1024Kbytes = 2^{20} = 1MB.

G(Giga) is equal to1024Mbytes = 2^{30} = 1GB.

1024 GBytes = 1TB.