प्रगत संगणन विकास केन्द्र

Paper Code

C3

CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING

C-DAC's Common Admission Test (C-CAT) – DECEMBER 2014

INSTRUCTIONS TO CANDIDATES

Candidate should read the following instructions before attempting the question paper.

1. **DO NOT CLOSE THE BROWSER ANYTIME DURING THE EXAM.**
2. Candidate **should check his/her name and hall ticket number** being displayed on the screen. In case of any discrepancy, it should be reported to Invigilator immediately.
3. Candidate should ensure that he/she has marked attendance on the attendance sheet and also ensure that session id has also been recorded. Any other session id which has not been mentioned in the attendance sheet would not be considered and all responses on that session id would be treated as null and void.
4. Do not start the exam (do not click **Next** button) before instructed to do so by the Invigilator.
5. **Every Section has 50 objective-type questions.** Each objective-type question has four choices of which only one is correct. Candidate should select the radio button, given below the question, corresponding to his/her correct choice.
6. Marking scheme of C-CAT is as follows:
    a. +3 (plus three) marks for each correct answer.
    b. -1 (minus one) mark for each wrong answer.
    c. 0 (zero) mark for each un-attempted question.
7. **Duration of each Section is ONE hour**. No candidate will be allowed to leave the examination hall before the completion of exam duration.
8. On clicking the **Next** button given at the bottom of the Instructions page, candidate will be directed to the question display screen.
9. Candidate should **note down the Session ID** that is displayed on the question screen after clicking on **Next** button.

10. Once the exam is started:-

    a. **Candidate should not close the browser. In case the browser is closed accidentally, it SHOULD BE reported to the Invigilator immediately.**
    b. **Candidate should not open any other software application on the computer system.**
    c. Candidate should neither shut down the machine nor fiddle with allocated hardware or software.
    d. In case of any problem it should be reported to Invigilator.

11. Candidate can navigate through questions using scroll bar or directly through the question number grid.

12. C-CAT screen contains the following buttons with the below specified functionality:

Button	Functionality
Examination Instruction	This link will open the instructions for the exam. After reading the instructions candidate has to click on [Back] button to move back to the questions interface.
Mark for Review	In case a candidate is not sure about the answer, then he/she can use this Button to mark the question for a visit later. It will be shown with a **?** against the question (in the question number grid) if the question has not been answered but has marked it for review. In case candidate has answered the question and marked it for review, then **√?** will be displayed against the question in the question number grid.
Clear Answer	This button will clear the option marked and the question will be shown as un-answered.

13. Each candidate will be provided one A4 size sheet for rough work. Candidates have to record their Name, hall ticket number and session ID on the rough sheet. They have to return the rough sheet to the Invigilator before leaving the exam hall.
14. Calculators, mobile phones, pagers and electronic gadgets in any form are not allowed to be used in the Exam Hall.

15. Candidate will be disqualified if found indulging in any kind of malpractice.

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1. What do you mean by interrupt latency

   A. Interrupt error
   B. Time elapsed to service the ISR of the interrupt
   C. Time elapsed between generation of two interrupt
   D. None of the above

2. In memory mapped I/O system which of the following instruction will not be there?

   A. LDA
   B. STA
   C. ADD
   D. OUT

3. Consider the following program segment

```
MVI B,00
MVI A,1C
DCR B
DAA
STA TEMP
HLT
```

content of TEMP after execution of above program

   A. 10h
   B. 22h
   C. 82h
   D. 12

4. In the program segment

```
LXI H,0106 H
DCR L
loop: DCX H
        NZ loop
        HLT
```

loop will be executed?

A. 115 times
B. 261 times
C. 0 times
D. Infinite times

5. In order to compliment the lower order nibble of the accumulator, one can use

A. ANI of H
B. XRI of H
C. ORI of H
D. CMA

6. Maximum number of bits required to represent any character from ASCII code set is

A. 10
B. 8
C. 7
D. 3

7. Consider the following program segment

```
8000:START: LXI H,0001 H
            LXI D,8010 H
            XCHG
            DCXD
            JZ 800 C
            PCHL
800C: JMP8000
      NOP
      HLT
```

referring to the above program which statement is true

A. The program will loop infinitely
B. The program will reach halt state after first pass
C. Program will reach halt state after 8010 h

D. None of the above

8. In virtual memory system the address space specified by address lines of CPU must be _____than physical memory size and_____than secondary storage size

A. Smaller, larger
B. Smaller, smaller
C. Large, smaller
D. Larger, larger

9. Which of the following is true with micro programmed control unit

A. It is faster than hardwired unit
B. Facilitates easy implementation of a new instruction
C. Is useful when small programs are run
D. All of the above

10. The maximum number of I/O devices that can be addressed by intel 8085?

A. 65536
B. 255
C. 512
D. 256

11. Assembly language directive is

A. The same as an instruction
B. Used to define space for variables
C. Used to start a program
D. To give commands to an assembler

12. The output of the linker(LINK command) is stored in a file with the extension

A. .lis
B. .obj
C. .exe
D. .ink

13. Which of the following is not an MASM directive?

A. .stack
B. .model
C. .db
D. Call

14. Which of the following defines a constant Max?

A. Max db 80
B. Max equ 80
C. Max dw 80
D. Mov max,80

15. MIMD stands for_____

A. Multiple instruction multiple data
B. Multiple instruction memory data
C. Memory instruction multiple data
D. Multiple information memory data

16. Pipelining is more common in which architecture?

A. CISC
B. Microprogrammed
C. RISC
D. Multiprocessor

17. Which of the following techniques is used to minimize data-dependency hazard in pipeline?

A. Operand forwarding
B. Instruction prefetching
C. Branch Prediction
D. none of the above

18. In a dependency graph of instruction scheduling for a pipeline, an edge E(u,v) signifies that

A. instruction u must be executed before instruction v
B. instruction u must be executed after instruction v
C. instruction u and v shares input data
D. none of the above

19. if(R1) R2 = R3 + R4 else R5 = R6 + R7which of the following hazards can happen in this kind of instruction execution?

A. Data hazard
B. Control hazard
C. Structural hazard
D. Memory hazard

20. What is the highest possible speedup of an n-stage pipeline?

A. n
B. n^2
C. √n
D. n – 1

21. IF(5ns) → ID(4ns) → EX(5ns) → MEM(10ns) → WB(4ns)
for the above pipeline with single memory access channel, what is the time after which the third instruction in the pipe will be completed?

A. 48ns
B. 38ns
C. 50ns
D. 12ns

22. A pipeline achieves 9.9 speedup for 90 instructions. Assuming every pipeline stages requires equal time to complete what is the number of stages in the pipeline?

A. 10
B. 11
C. 12
D. 9

23. The function f(x,y,z)= Σ(1,2,6,7) can be implemented using :

A. 8 to 1 MUX
B. 2 to 1 MUX
C. 4 to 1 MUX
D. None of these

24. What is the average access time of a system having three levels of memory with access times of 20 ns, 100 ns, and 1 ms, respectively. The cache hit ratio is 90% and the main memory hit ratio is 95%.

A. 5 µs
B. 503 ns
C. 0.5ms

D. 10ns

25. The number of records contained within a block of data on magnetic tape is defined by the

A. block definition
B. record container
C. blocking factor
D. record per block factor

26. Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20 bit address for a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively

A. 9,6,5
B. 7,7,6
C. 7,5,8
D. 9,5,6

27. Consider a pipelined processor with 4 stages, IF,ID,EX and WB with following time-
cost:

IF = 1 cycle, ID = 1 cycle, EX = (ADD = 1 cycle; SUB = 1 cycle; MUL = 3 cycle), WB = 1 cycle
Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

ADD R2, R1, R0 (R2 ← R1 + R0)
MUL R4, R3, R2 (R4 ← R3 * R2)
SUB R6, R5, R4 (R6 ← R5 – R4)

A. 7
B. 8

C. 10

D. 14

28. Which of the following are NOT true in a pipelined processor?

i. Bypassing can handle all RAW hazards
ii. Register renaming can eliminate all register carried WAR hazards
iii. Control hazards penalties can be eliminated by dynamic branch prediction

A. I and II only

B. I and III only

C. II and III only

D. I, II and III

29. Consider a disk with the following characteristics:
Track size : 10000 bytes
Rotational latency: 10ms/revolution
Block size: 1000 bytes
What is the maximum transfer rate per track measured in bits per second?

A. 400Mbps

B. 8Mbps

C. 6400Mbps

D. 4250Mbps

30. Consider a 4-way set associative cache with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks is in the following order:
0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155
which one of the following memory block will NOT be in cache if LRU replacement policy is used?

A. 3

B. 8

C. 129

D. 216

31. In the negative logic system,

A. The more negative of the two logic levels represents a logic '1' state
B. The more negative of the two logic levels represents a logic '0' state
C. All input and output voltage levels are negative
D. The output is always complement of the intended logic function

32. F's complement (2BFD)Hex is

A. E304
B. D403
C. D402
D. C403

33. In signed magnitude representation, the binary equivalent of 22.5625 is (the bit before comma represents the sign)

A. 0, 10110.1011
B. 0, 10110.1001
C. 1, 10101.1001
D. 1, 10110.1001

34. Which of the following represents $E3_{16}$?

A. $(1CE)_{16} + (A2)_{16}$
B. $(1BC)_{16} - (DE)_{16}$
C. $(2BC)_{16} – (1DE)_{16}$
D. $(200)_{16} – (11D)_{16}$

35. What is the minimum number of NAND gates (2-input or 3-input or both) required to implement $A + A\overline{B} + A\overline{B}C$?

A. 0

B. 4

C. 5

D. 7

36. The standard SOP form of the expression $\overline{A}B + \overline{A}C$ is _____.

A. $\overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + A\overline{B}C$

B. $\overline{A}\overline{B}C + \overline{A}B\overline{C} + \overline{A}BC$

C. $\overline{A}\overline{B}C + \overline{A}BC + A\overline{B}\overline{C}$

D. $\overline{A}\overline{B}C + A\overline{B}C + AB\overline{C}$

37. Which of the following is true for a 5-variable Karnaugh map?

A. There is no such thing

B. It can be used only with the aid of a computer.

C. It is made up of two 4-variable Karnaugh maps.

D. It is made up of a 2-variable and a 3-variable Karnaugh map.

38. Assertion (A): A look-ahead carry adder is a fast adder.
Reason (R): A parallel carry adder generates sum digits directly from the input

digits.

A. Both A & R are true and R is the correct explanation of A

B. Both A & R are true but R is NOT the correct explanation of A

C. A is true but R is false

D. A is false but R is true

39. What is the number of selector lines required in a single input n-output demultiplexer ?

A. 2

B. n

C. 2^n

D. $\log_2 n$

40. When two 16-input multiplexers drive a 2-input MUX, what is the result ?

A. 2-input MUX

B. 4-input MUX

C. 16-input MUX

D. 32-input MUX

41. On a master-slave flip-flop, when is the master enabled?

A. when the clock is LOW

B. when the clock is HIGH

C. both of the above

D. neither of the above

42. When adding an even parity bit to the code 110010, the result is _____.

A. 1110010
B. 1111001
C. 0110010
D. 1001101

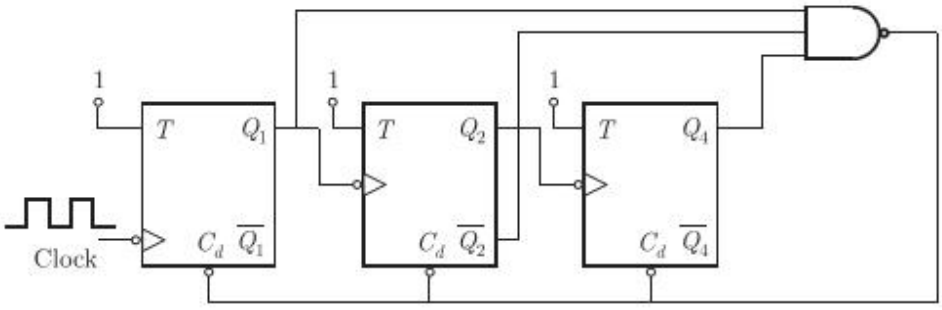
43. Consider the following statements regarding registers and latches :

1. Registers are made of edge-triggered FFs, whereas latches are made from level-triggered FFs.
2. Register are temporary storage devices whereas latches are not.
3. A latch employs cross-coupled feedback connections.
4. A register stores a binary word whereas a latch does not.

Which of the statements given above are correct ?

A. 1 and 2
B. 1 and 3
C. 2 and 3
D. 3 and 4

44. The circuit given above is that of a



A. Mod-5 counter

B. Mod-6 counter

C. Mod-7 counter

D. Mod-8 counter

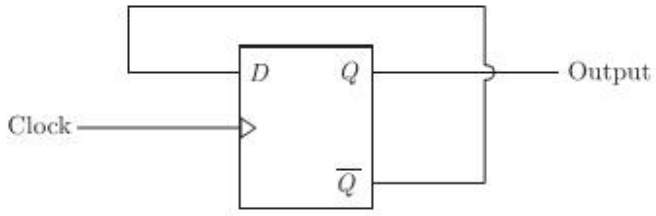
45. Match List - I(Circuit) with List - II(Application) and select the correct answer using the code given below the lists :

List-1	List-2
a. Ripple up counter	1. Division
b. Synchronous down counter	2. Multiplication
c. Shift lest register	3. To create delay
d. Shift right register	4. Transient states

Codes :

	a	b	c	d
A.	2	3	4	1
B.	4	1	2	3
C.	2	1	4	3
D.	4	3	2	1

46. For the circuit shown in the figure, what is the frequency of the output Q?



A. Twice the input clock frequency

B. Half the input clock frequency

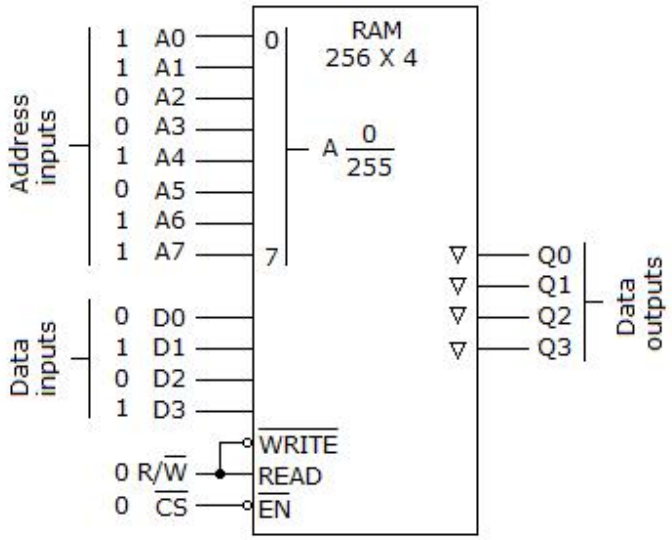
C. Same as the input clock frequency

D. Inverse of the propagation delay of the FF

47 . On the third clock pulse, a 4-bit Johnson sequence is Q0 = 1, Q1 = 1, Q2 = 1, and Q3= 0. On the fourth clock pulse, the sequence is _____.

A. Q0 = 1, Q1 = 1, Q2 = 1, Q3 = 1
B. Q0 = 1, Q1 = 1, Q2 = 0, Q3 = 0
C. Q0 = 1, Q1 = 0, Q2 = 0, Q3 = 0
D. Q0 = 0, Q1 = 0, Q2 = 0, Q3 = 0

48. For the given circuit, which of the following is correct?

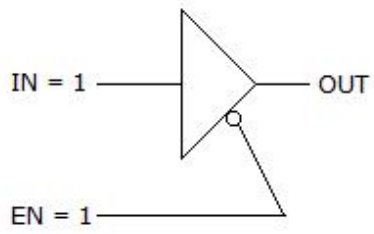


A. The number 5 is being written to the memory at address location 203.
B. The chip has not been enabled, since the EN terminal is 0; therefore, nothing will be written to the chip and the output is tri-stated.
C. Decimal 10 is being written into memory location 211.
D. The read/write line is LOW; therefore, decimal 5 is being stored at memory location 211

49. Which of the following best describes random-access memory (RAM)?

A. a type of memory in which access time depends on memory location
B. a type of memory that can be written to only once but can be read from an infinite number of times
C. a type of memory in which access time is the same for each memory location
D. mass memory

50. The device shown in the given figure is checked with a logic probe and the output is HIGH.



A. The device is working properly.
B. For the input conditions shown the output should be LOW; the input is shorted to ground.
C. For the input conditions shown the output should be neither HIGH nor LOW; the device output has got shorted to Vcc.
D. The device is probably alright; the problem is most likely caused by the stage connected to the output of the device.