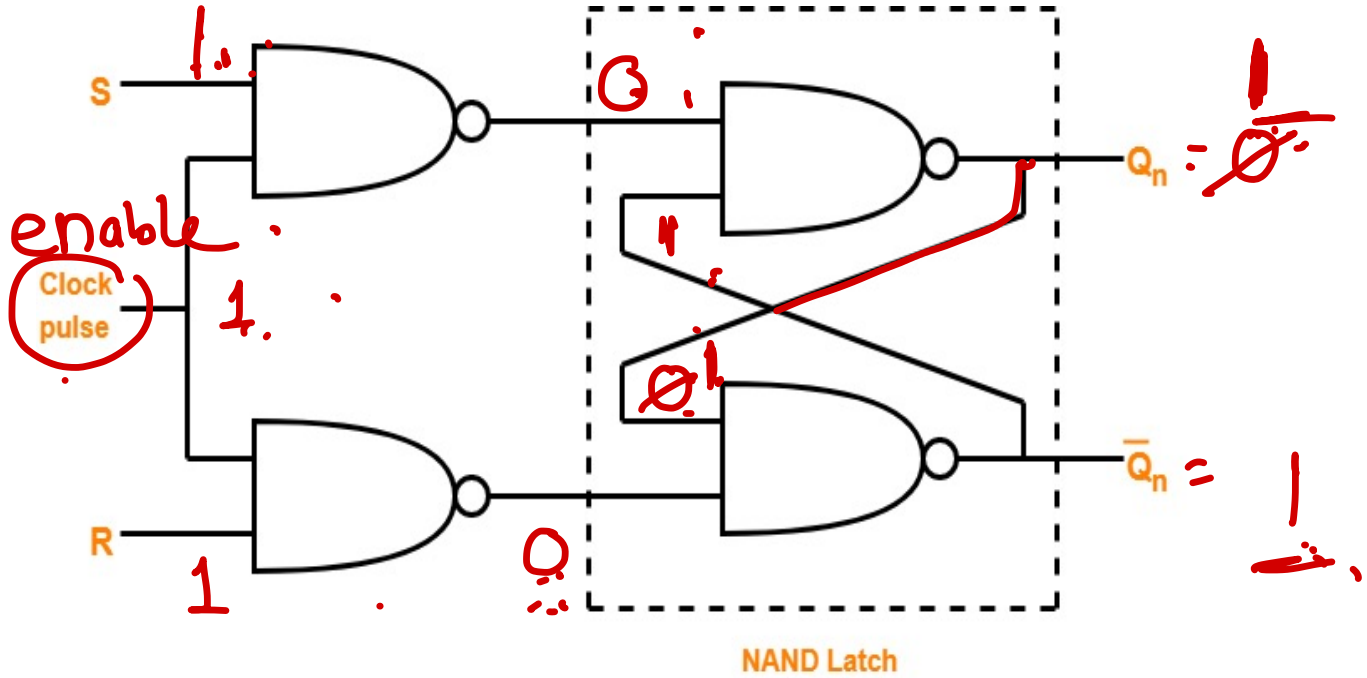
SR-Flip-Flop

- SR flip flop is the simplest type of flip flops.
- It stands for **Set Reset flip flop.**
- It is a clocked flip flop.

en=1 +ve } Latch
en=0 -ve }
clk-↑ +ve } FF
clk-↓ -ve }



SR Flip Flop Using NAND Latch

Application of SR

- SR flip-flops are used to eliminate mechanical bounce of switches in digital circuits

SR Flip-Flop

SR
0 0 → no change
0 1 → Reset
1 0 → Set
1 1 → Indetermine

Truth Table of SR Flip-Flop

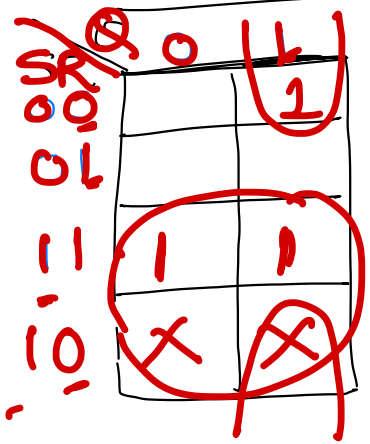
prev present

Clk	S	R	Q_n	Q_{n+1}	State
↑	0	0	0	0	no change
↑	0	0	1	1	
↑	0	1	0	0	Reset
↑	0	1	1	0	
↑	1	0	0	1	Set
↑	1	0	1	1	
↑	1	1	0	X	Indetermine
↑	1	1	1	X	

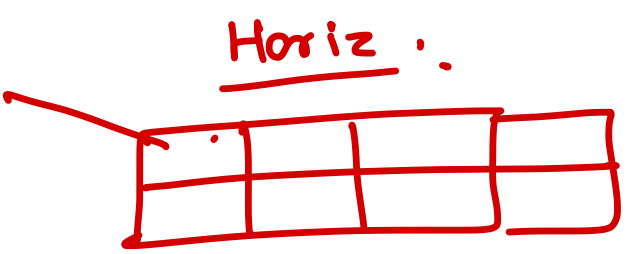
Excitation Table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

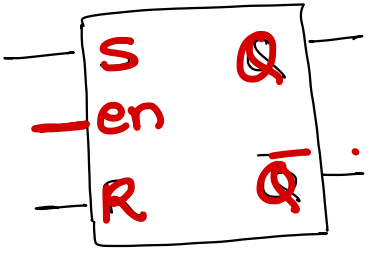
Characteristic Eqn.



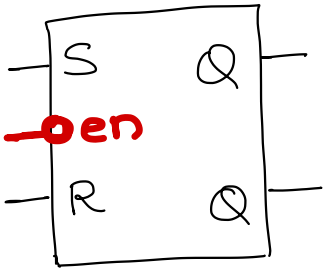
$S + Q\bar{R}$.


Horiz

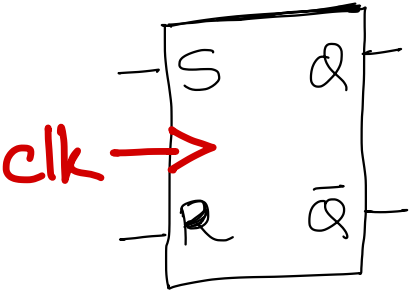
positive SR Latch.



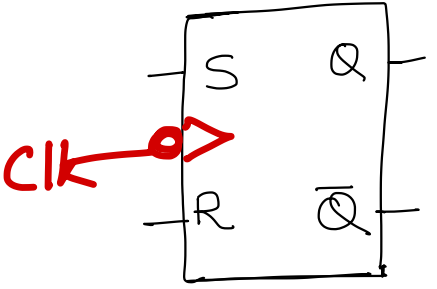
Negative SR Latch:



Positive SR FF.

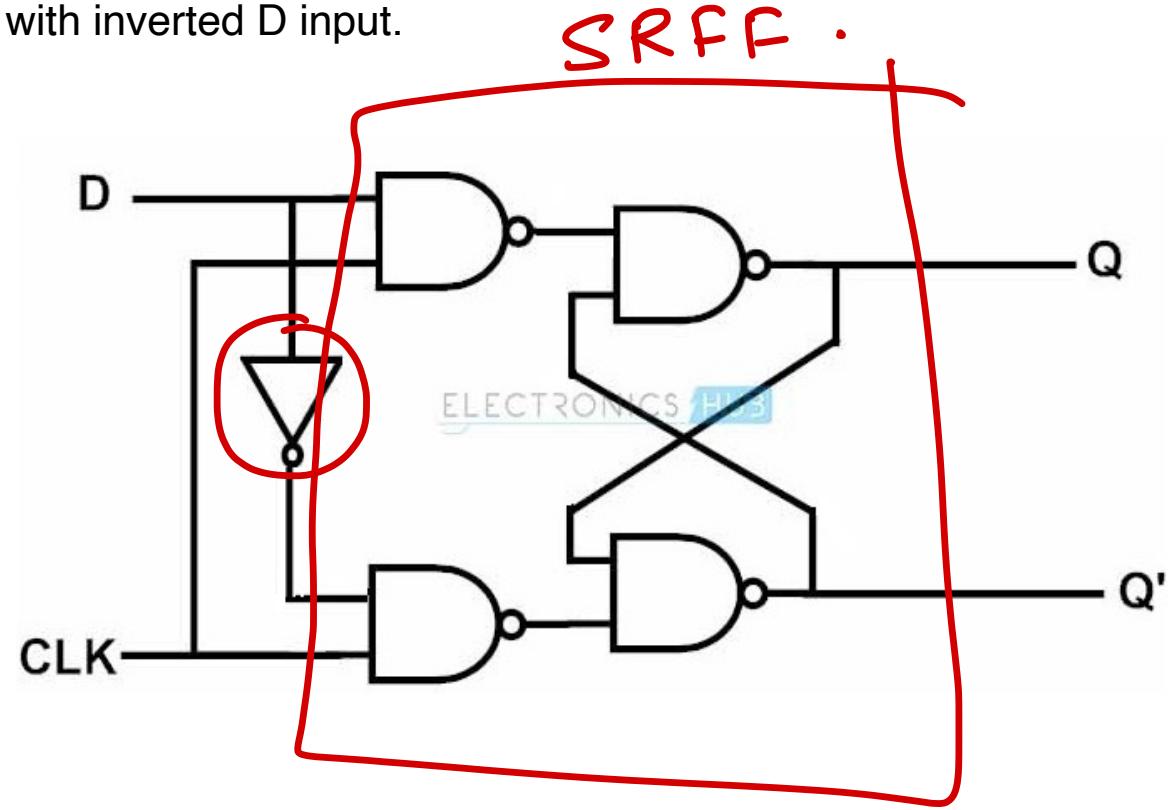


Negative SR FF:



D-Flip-Flop

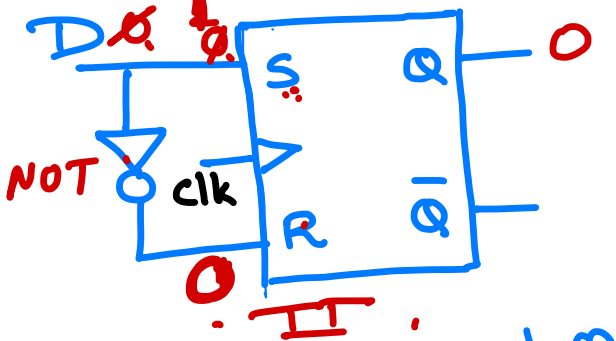
- D flip-flops are also called as **Delay** flip–flop or **Data** flip–flop. They are used to store 1–bit binary data.
- The S input is given with D input and the R input is given with inverted D input.
- D Flip-flop is also called as transparent latch.



Applications of D

- Data storage registers.
- Data transferring as shift registers.
- Frequency division circuits.

D-FF



clk	D	Q_n	Q_{n+1}
↑	0	0	0
↑	0	1	0
↑	1	0	1
↑	1	1	1

S	R	
0	0	no change
0	1	Reset
1	0	Set
1	1	x

Characteristic Eqn D

D	Q_n = 0	Q_n = 1
0	0	0
1	1	1

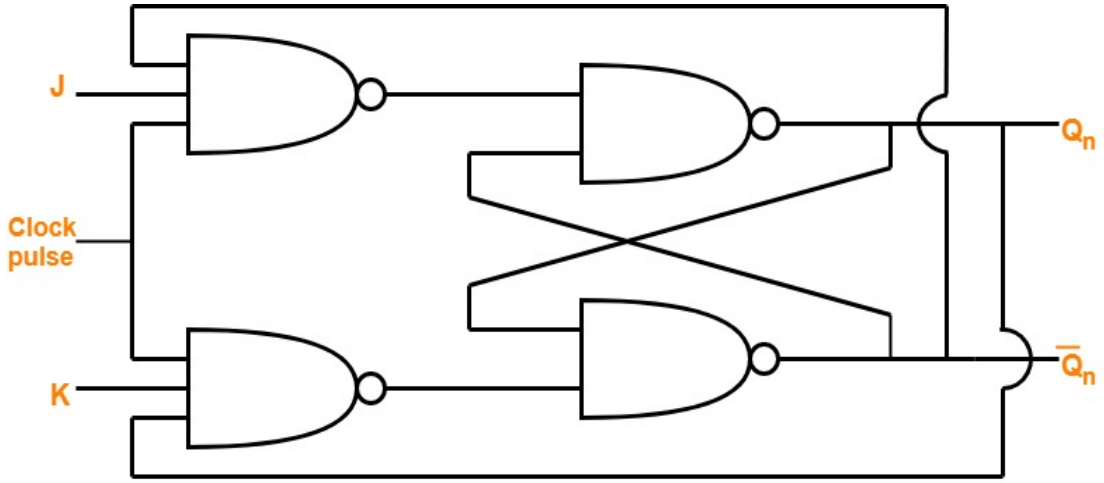
$= D$

Excitable table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

JK-Flip-Flop

- Input J behaves like input S of SR flip-flop which was meant to set the flip-flop.
- Input K behaves like input R of SR flip-flop which was meant to reset the flip flop.



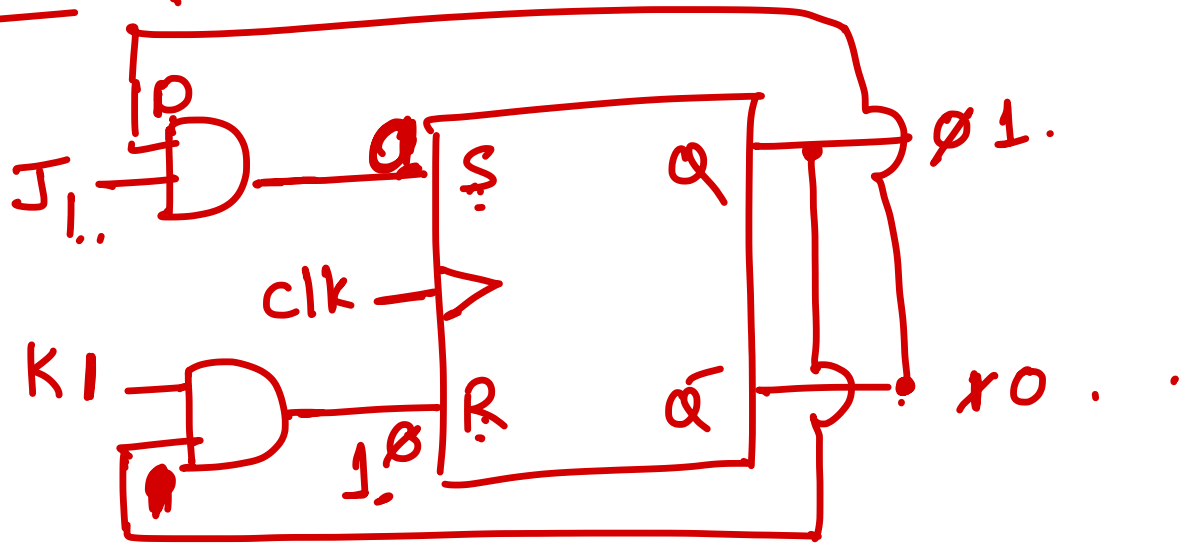
Logic Circuit For JK Flip Flop Using SR Flip Flop

(Constructed Using NAND Latch)

Applications

- Shift Registers
- Frequency Dividers
- Switching Applications
- Parallel Data Transfer
- Serial Data Transfer
- Binary Counter
- Sequence Detector

JK-FF.



S	R	
0	0	no change.
→ 0	1	Reset
→ 1	0	Set
1	1	X

JK Flip-Flop

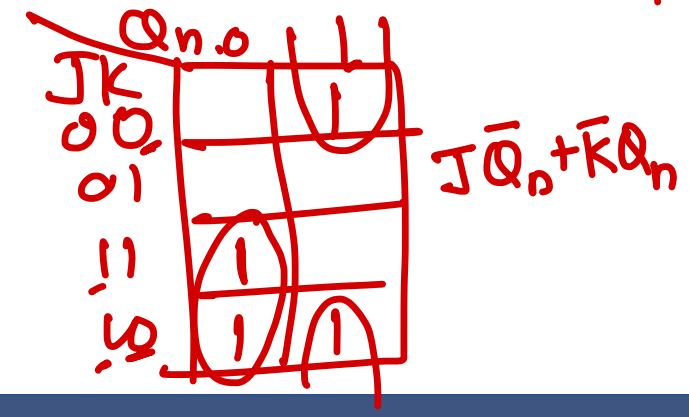
Truth Table of JK Flip-Flop

Clk	J	K	Q_n	Q_{n+1}	State
↑	0	0	0	0	no change
↑	0	0	1	1	
↑	0	1	0	0	Reset
↑	0	1	1	0	
↑	1	0	0	1	Set
↑	1	0	1	1	
↑	1	1	0	1	toggle
↑	1	1	1	0	

Excitation Table

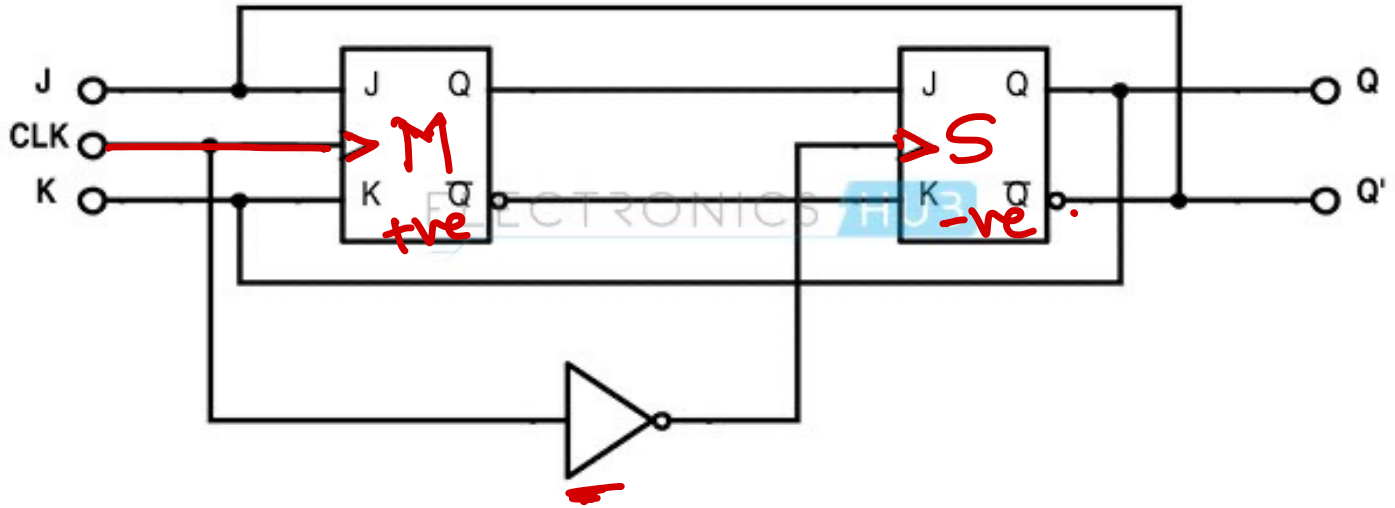
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Characteristic Eqn.



MASTER SLAVE J-K FLIP-FLOP

- Race around condition occur in JK flip-flop when both J and K input is high. If you keep this condition for longer period of time and then flip-flops are disable we cannot predict the output
- We can remove race around condition by Master and Slave JK flip-flop. The Master-Slave Flip-Flop is basically two gated JK flip-flops connected together in a series configuration with the slave having an inverted clock pulse
- Where “Master” works on, the rising edge of the clock pulse while the “Slave” works on the falling edge of the clock pulse

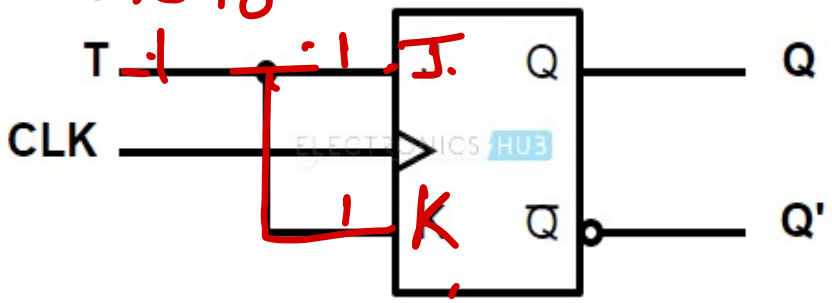


T-Flip-Flop

- T flip–flop is also known as “Toggle Flip–flop”

Clk	T	Q_n	Q_{n+1}	State
↑	0	0	0	no change
↑	0	1	1	
↑	1	0	1	toggle
↑	1	1	0	

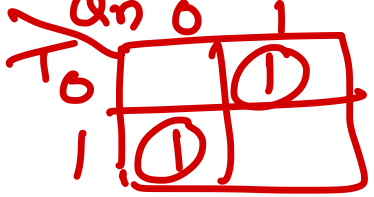
JK
0 0 — no change.
0 1 — Reset
1 0 — Set
1 1 — toggle.



Excitation table.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic Eqn.



$\Rightarrow \bar{T}Q_n + T\bar{Q}_n$

$= T \oplus Q_n$

Application of T-Flip-Flop

- Frequency Division Circuit

Flip-Flop

- **Setup Time**

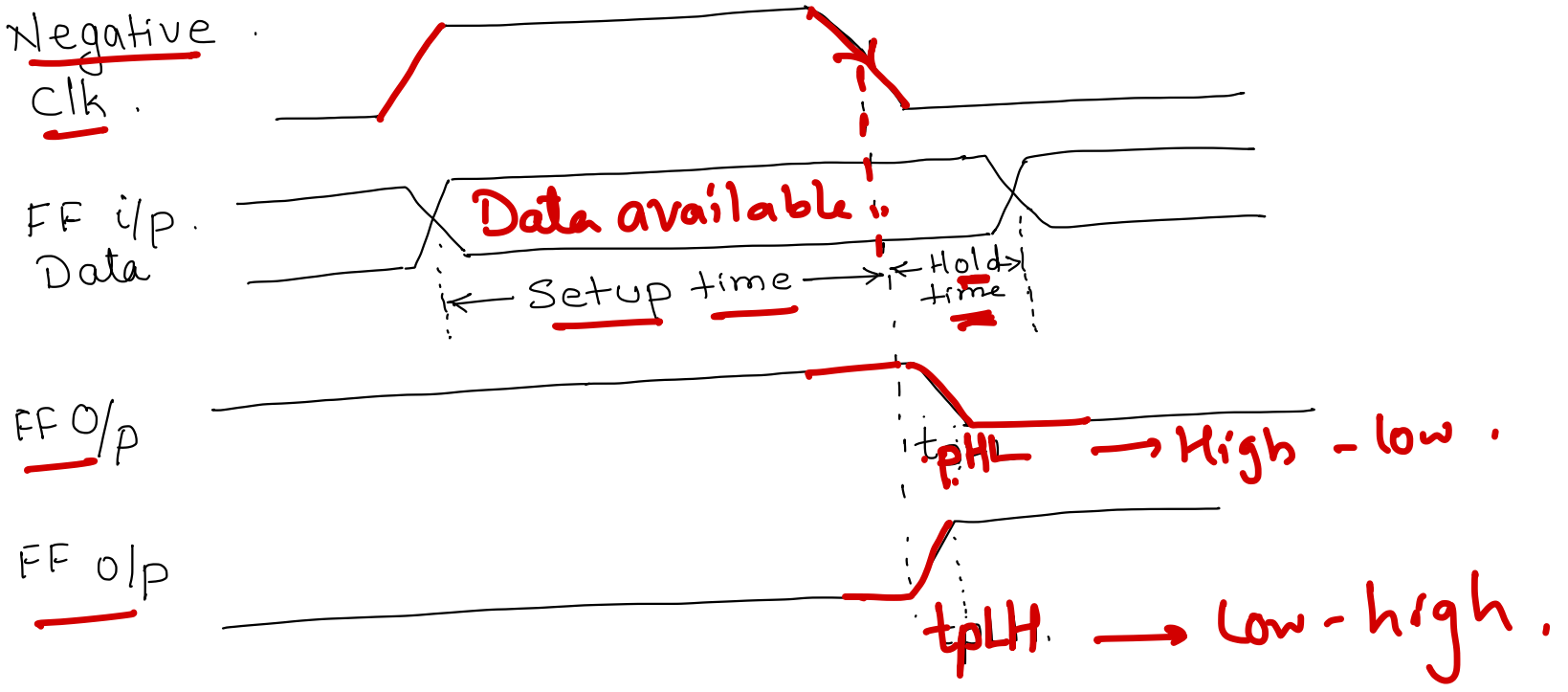
Setup time is the minimum time required to maintain a constant voltage level at the excitation input of flipflop before the triggering edge of the clock pulse

- **Hold Time**

Hold time is the minimum time for which the voltage level at the excitation input must remain constant after the triggering edge of the clock pulse

- **Propogation Delay**

A propogation delay is the time required to change the output after application of input.

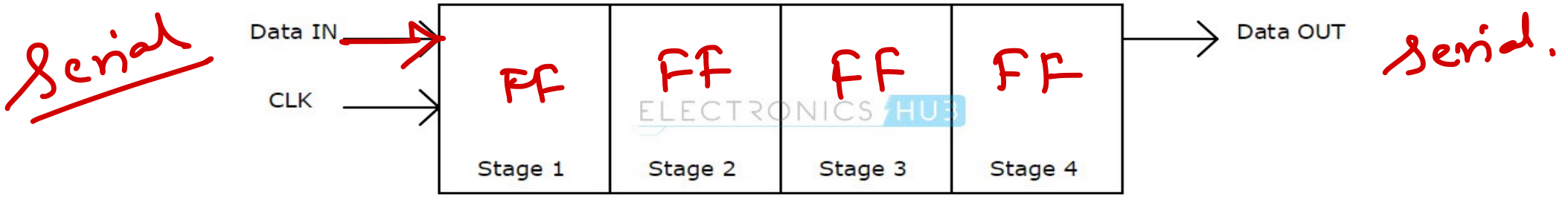

Negative clk.
FF i/p Data
Data available
Setup time
Hold time
FF O/p
tpHL → High - low.
FF O/p
tpLH → Low - high.

Shift Register

- Flip flops can store a single bit of binary data i.e. 1 or 0.
- Register is a group of flip flops used to store multiple bits of data
- When a number of flip flops are connected in series, this arrangement is called a Register.
- The stored information can be transferred within the registers; these are called as 'Shift Registers'.
- Shift registers are of 4 types
  - Serial In Serial Out shift register — SISO.
  - Serial In parallel Out shift register — SIPO.
  - Parallel In Serial Out shift register — PISO.
  - Parallel In parallel Out shift register — PIPO.
- The registers which will shift the bits to left are called "Shift left registers".
- The registers which will shift the bits to right are called "Shift right registers".

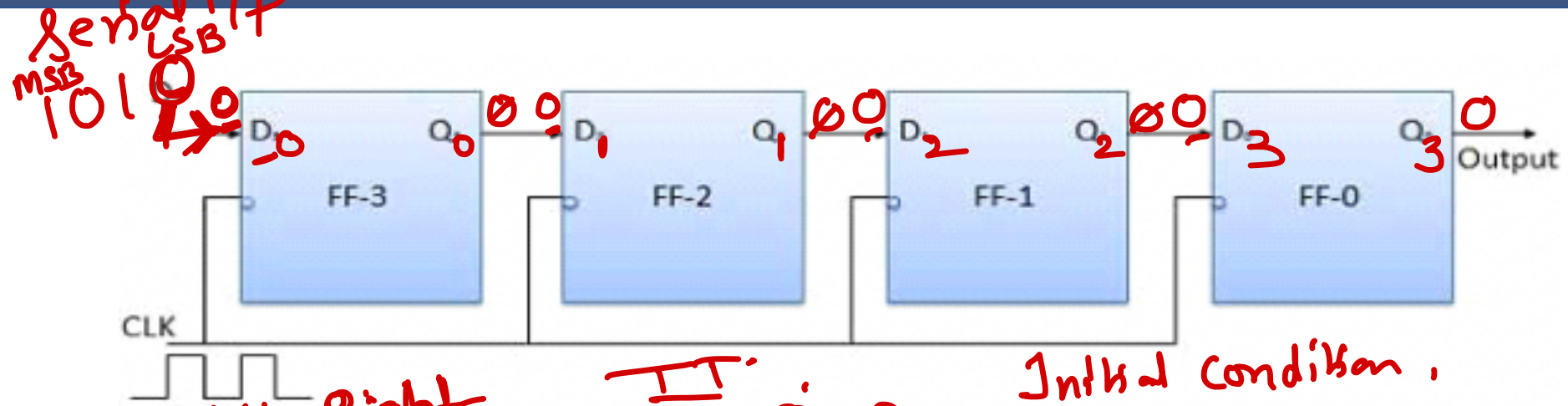
Serial In Serial Out

- The input to this register is given in serial fashion i.e. one bit after the other through a single data line and the output is also collected serially.
- SISO shift register is use as temporary data storage device.
- SISO shift register is also use as a delay element.

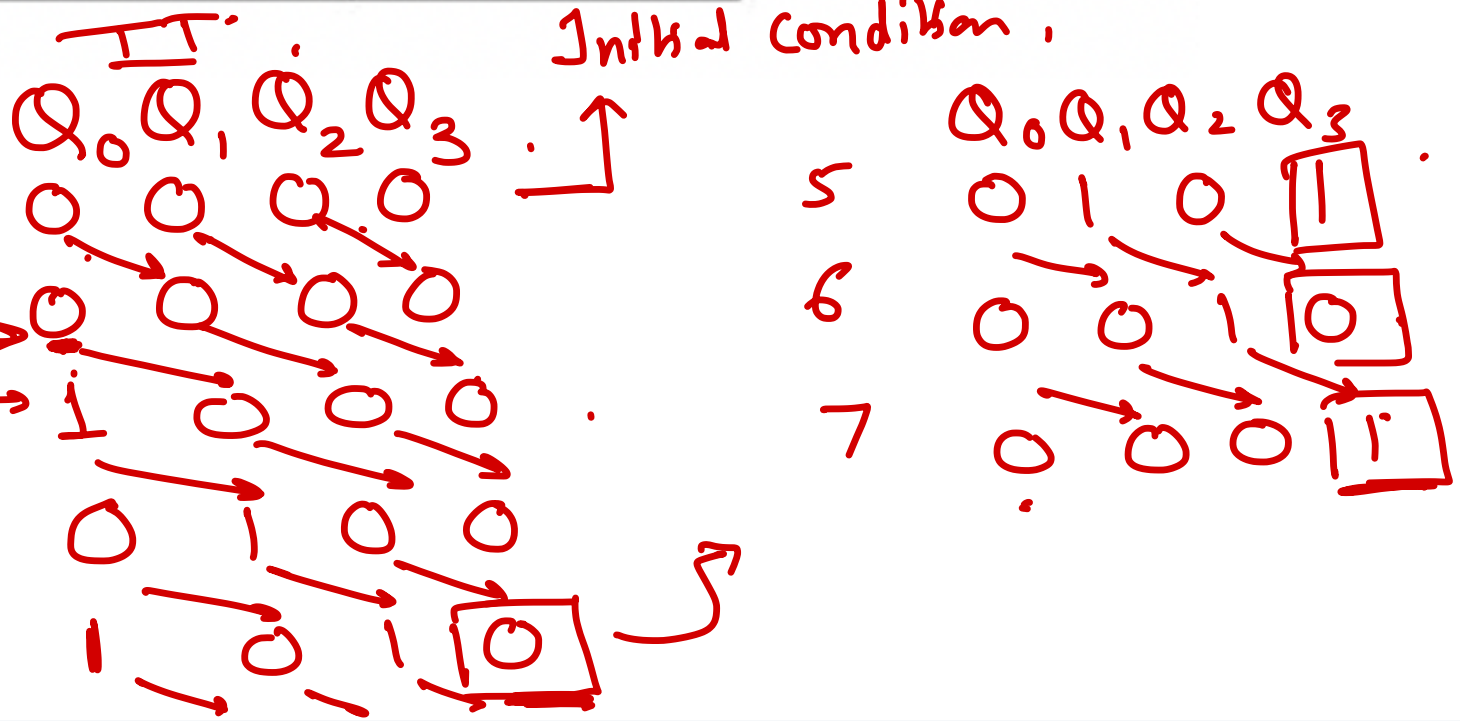


Serial In Serial Out

Right.

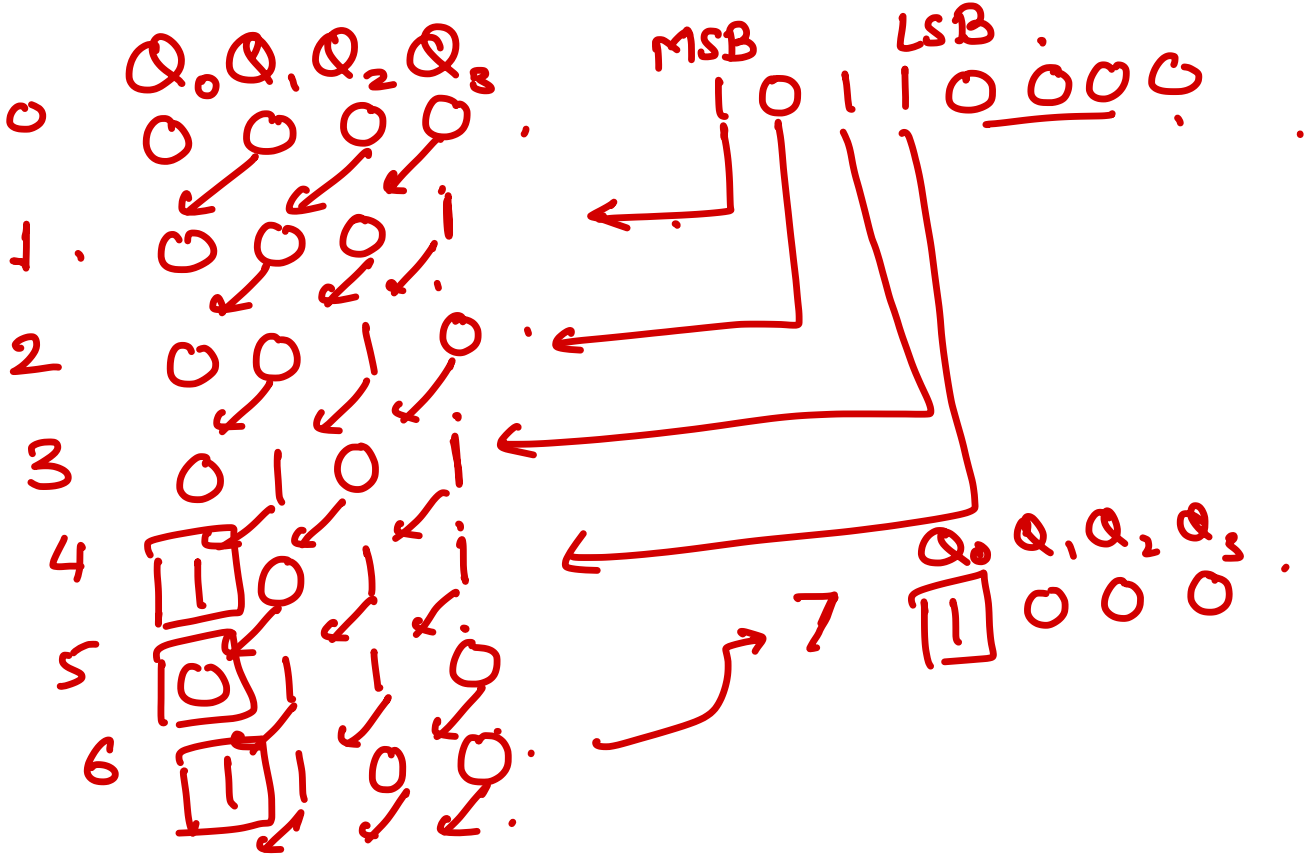


Serial i/p Right
MSB
LSB
0 0 1 0 1 0 . 0



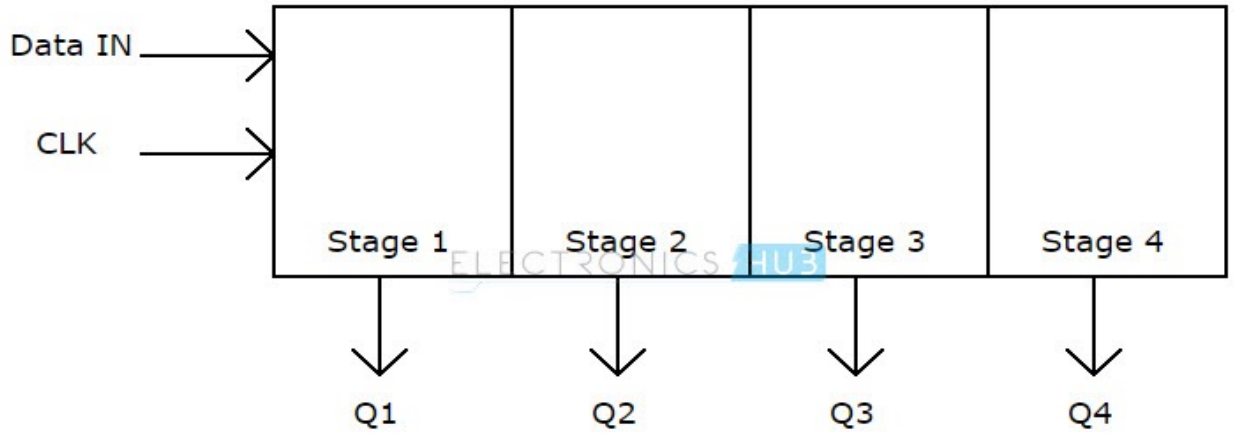
Serial I/P. → 1 0 1 1 Left.

Initial cond → 0 0 0 0.

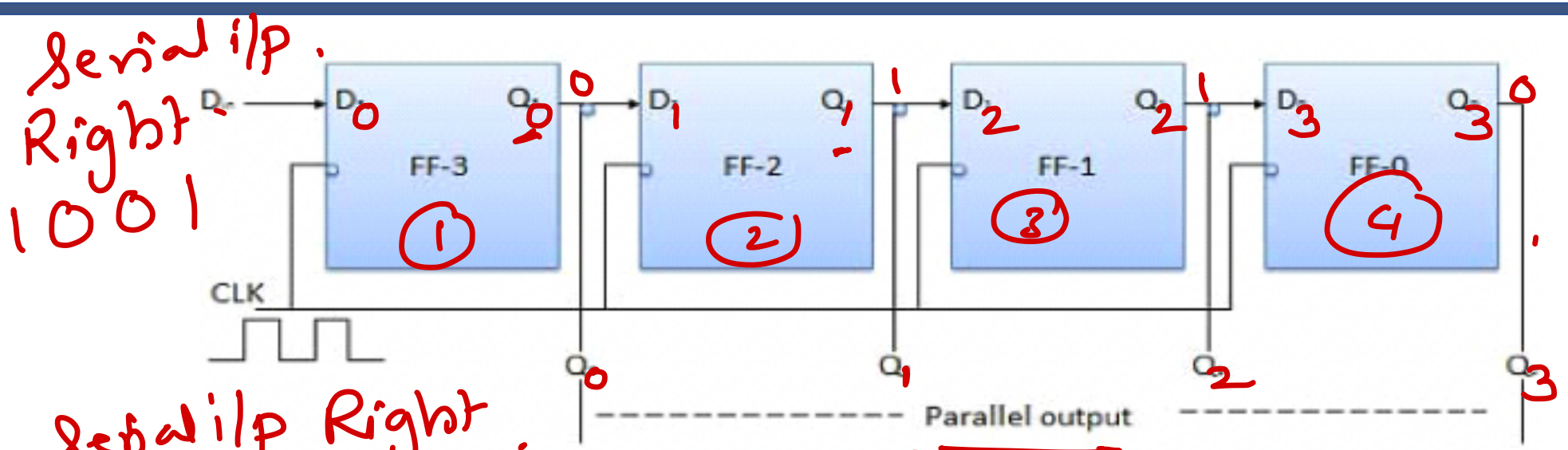


Serial In Parallel Out

- The input to this register is given in serial and the output is collected in parallel.
- The main application of Serial in Parallel out shift register is to convert serial data into parallel data.
- Hence they are used in communication lines where demultiplexing of a data line into several parallel line is required.

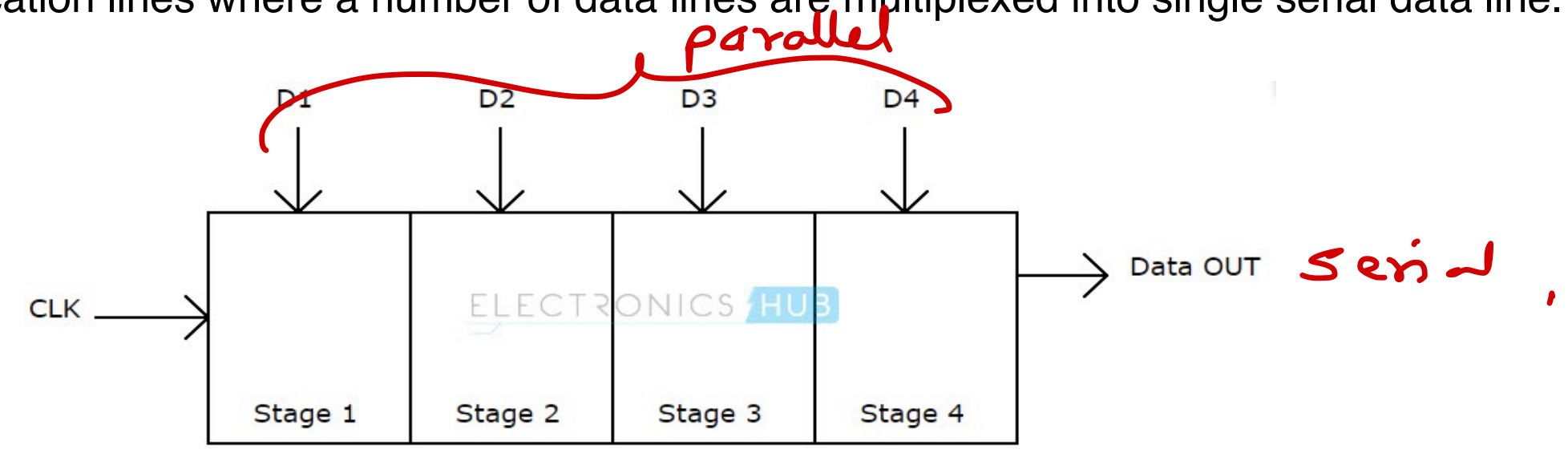


Serial In Parallel Out



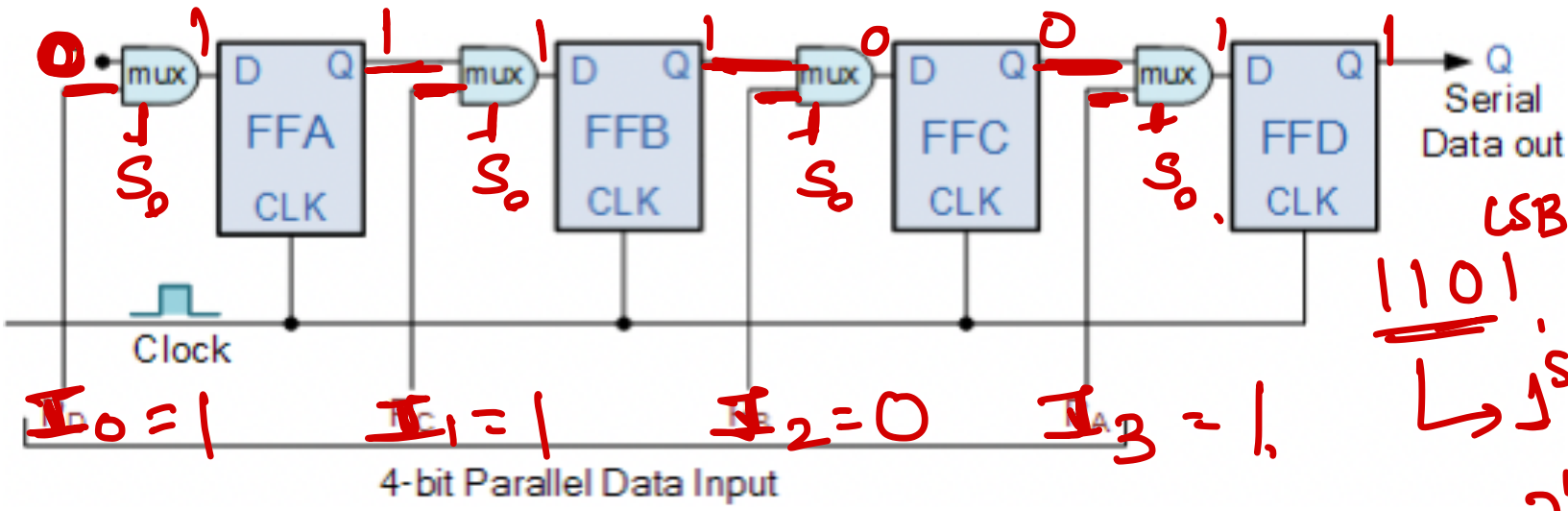
Parallel In Serial Out

- The output of the previous flip flop and parallel data input are connected to the input of the MUX and the output of MUX is connected to the next flip flop.
- A Parallel in Serial out (PISO) shift register converts parallel data to serial data. Hence they are used in communication lines where a number of data lines are multiplexed into single serial data line.



Parallel In Serial Out

S	Y
0	I0
1	I1

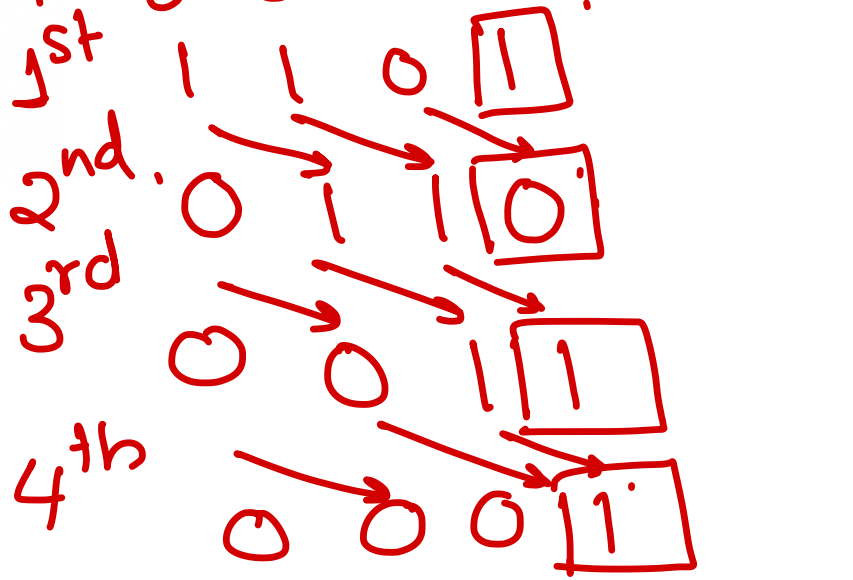


$S_0 = 1 \rightarrow$ parallel i/p.

$S_0 = 0 \rightarrow$ shift

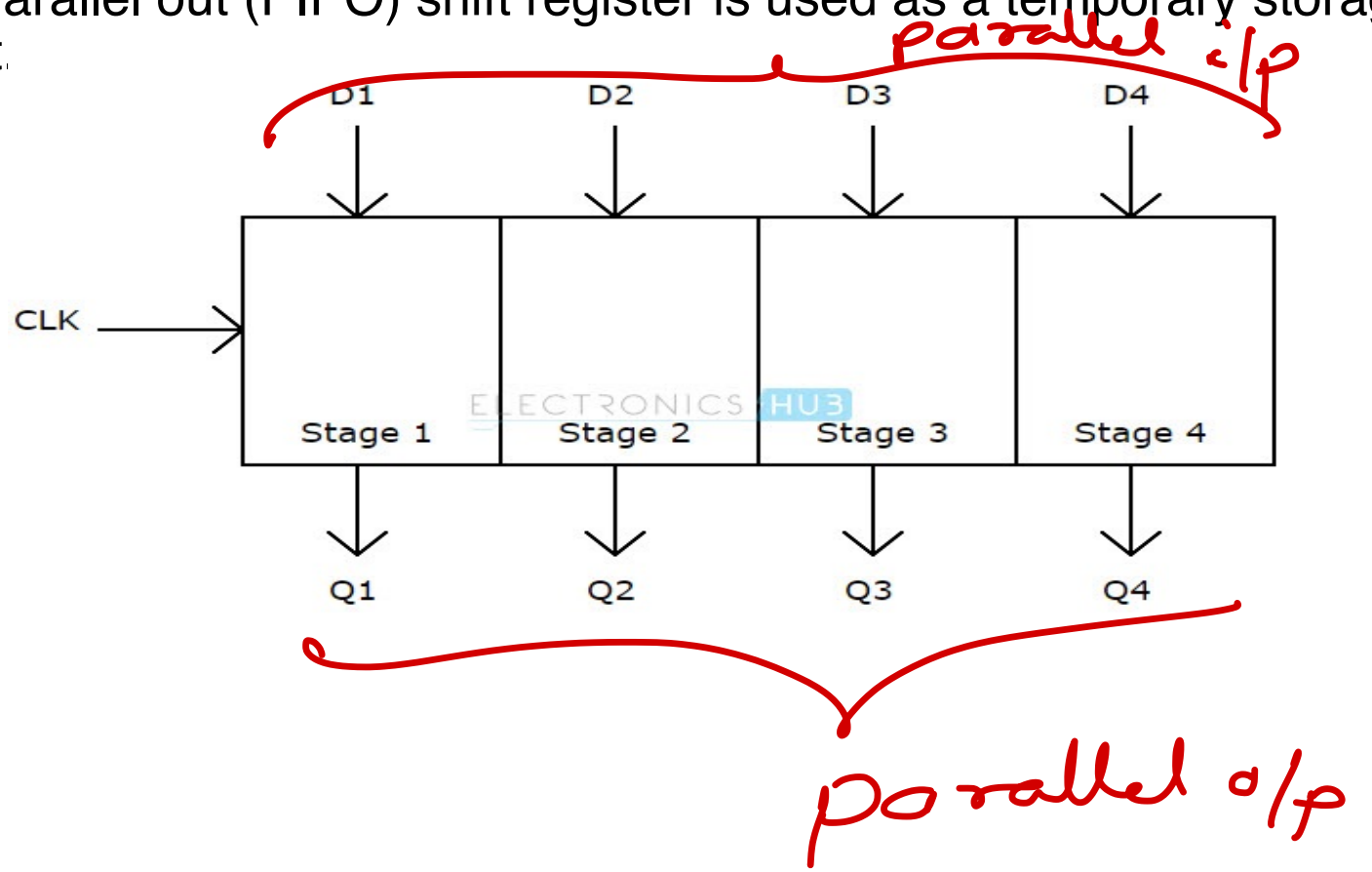
1101

LSB $Q_0\ Q_1\ Q_2\ Q_3$

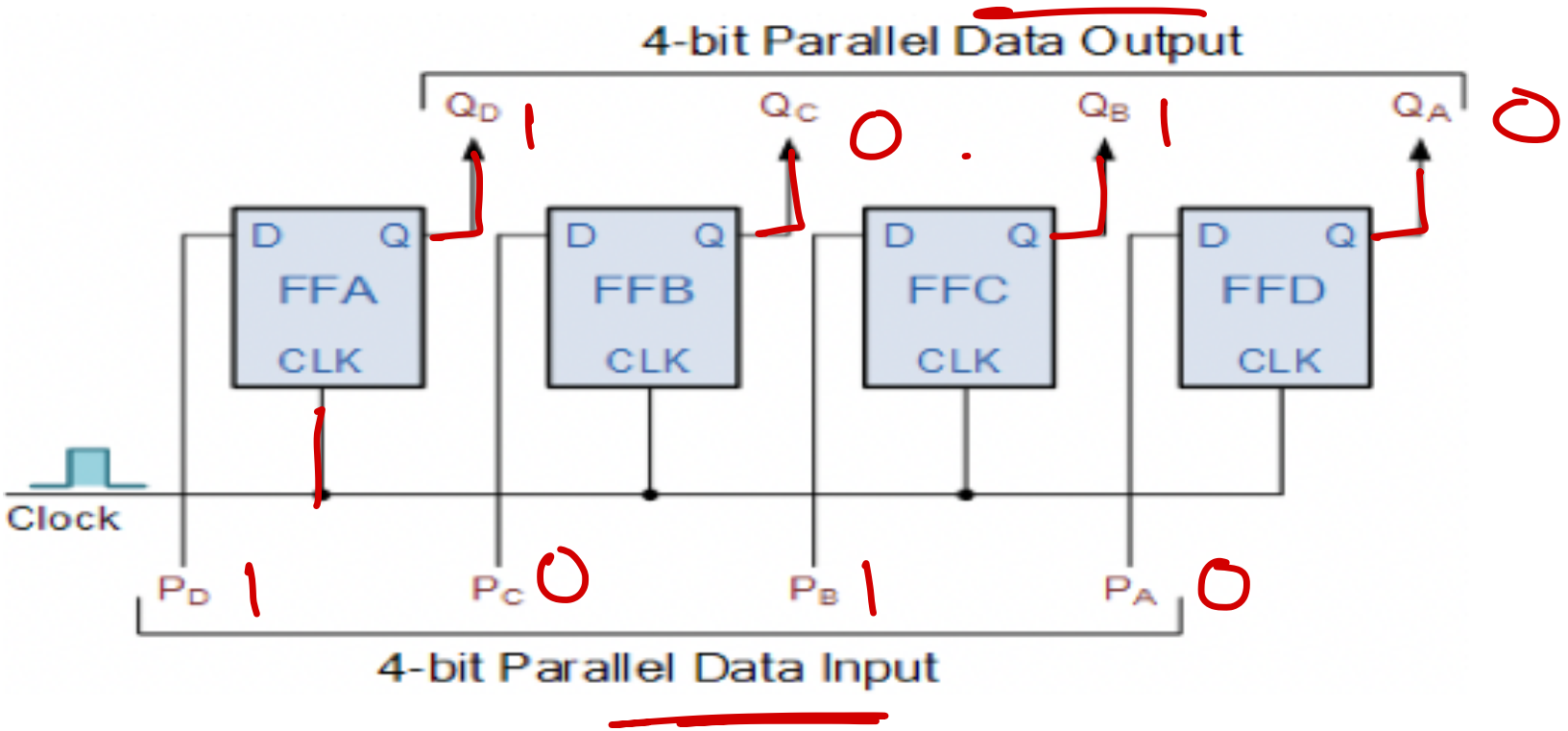


Parallel In Parallel Out

- The input is given in parallel and the output also collected in parallel.
- A Parallel in Parallel out (PIPO) shift register is used as a temporary storage device and also as a delay element.



Parallel In Parallel Out



Bidirectional and Universal Shift Register

- **Bidirectional Shift Register**
  - The bidirectional shift register can be defined as the register in which the data can be shifted either left of right
  - Right /Left is the mode signal. When Right /Left is a 1, the logic circuit works as a right shift register. When Right /Left is a 0, the logic circuit works as a left shift register.
- **Universal Shift Register**
  - The universal shift register can be defined as the register which can be used to shift the data in both the directions like left, right and can load parallel data as well.
  - It is called Universal Shift Register as it can be used for left shift, right shift, serial to serial, serial to parallel, parallel to serial and parallel to parallel operations.

Shift Register

- **Application of Shift Register**
- Registers are used in digital electronic devices like computers as
  - Temporary data storage
  - Data transfer
  - Data manipulation
  - As counters.