International Journal of VLSI System Design and Communication Systems

ISSN 2322-0929
Vol.02, Issue.08,
October-2014,
Pages:0624-0629

www.ijvdcs.org

Design of High Speed Low Power 32-Bit Multiplier using Reversible Logic: A Vedic Mathematical Approach

R.VASIM AKRAM[1], MOHAMMED RAHMATULLAH KHAN[2], B.RAJKUMAR[3]

[1]PG Scholar, Dept of ECE, Shadan College of Engineering and Technology, Hyderabad, India, Email: Vasim487@gmail.com.
[2]Asst Prof, Dept of ECE, Shadan College of Engineering and Technology, Hyderabad, India, Email: mrkmudassir@gmail.com.
[2]Asst Prof, Dept of ECE, Shadan College of Engineering and Technology, Hyderabad, India, Email: rajkumarnany@gmail.com.

Abstract: Multipliers are vital components of any processor or computing machine. More often than not, performance of microcontrollers and Digital signal processors are evaluated on the basis of number of multiplications performed in unit time. Hence better multiplier architectures are bound to increase the efficiency of the system. Vedic multiplier is one such promising solution. It's simple architecture coupled with increased speed forms an unparalleled combination for serving any complex multiplication computations. Tagged with these highlights, implementing this with reversible logic further reduces power dissipation. Power dissipation is another important constraint in an embedded system which cannot be neglected. In this paper we bring out a 32-bit Vedic multiplier implemented using reversible logic, and comparing with 32-bit Array multiplier implemented using reversible logic. This multiplier may find applications in Fast Fourier Transforms (FFTs), and other applications of DSP like imaging, software defined radios, wireless communications.

Keywords: Vedic Multiplier, Reversible Logic, Urdhva Tiryakbhayam, Quantum Cost, Total Reversible Logic Implementation Cost.

I. INTRODUCTION

Vedic mathematics [2] is the ancient Indian system of mathematics which mainly deals with Vedic mathematical formulae and their application to various branches of mathematics. Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Sri Bharati Krsna Tirtha after his research on Vedas. He constructed 16 sutras and 16 upa sutras after extensive research in Atharva Veda. The most famous among these 16 are Nikhilam Sutram, Urdhva Tiryakbhayam, and Anurupye. It has been found that Urdhva Tiryakbhayam is the most efficient among these. The beauty of Vedic mathematics lies in the fact that it reduces otherwise cumbersome looking calculations in conventional mathematics to very simple ones. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Hence multiplications in DSP blocks can be performed at faster rate. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering. Digital signal processing (DSP) is the technology that is omnipresent in almost every engineering discipline. Faster additions and multiplications are the order of the day.

Multiplication is the most basic and frequently used operations in a CPU. Multiplication is an operation of scaling one number by another. Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Trans forms, etc. With ever increasing need for faster c10ck frequency it becomes imperative to have faster arithmetic unit. Hence Vedic mathematics can be aptly employed here to perform multiplication. Reversible logic is one of the promising fields for future low power design technologies. Since one of the requirements of all DSP processors and other hand held devices is to minimize power dissipation multipliers with high speed and lower dissipations are critical. This paper proposes an implementation of Reversible Urdhva Tiryakbhayam Multiplier which consists of two cardinal features. One is the fast multiplication feature derived from Vedic algorithm Urdhva Tiryakbhayam and another is the reduced heat dissipation by the virtue of implementing the circuit using reversible logic gates. The paper is partitioned into six sections. Section II gives Vedic Mathematics Section III deals with Compressor Adder. Section IV explains the Results, Analysis and Comparison. Section V Conc1usions and references follow.

II. VEDIC MATHEMATICS

Mathematics is a mother of all sciences. Mathematics is full of magic and mysteries. The ancient Indians were able to understand these mysteries and develop simple keys to solve these mysteries. Thousands of years ago the Indians used these techniques in different fields like construction of temples, astrology, medicine, science etc, due to which INDIA emerged as the richest country in the world. The Indians called this system of calculations as "The Vedic

Mathematics". Vedic Mathematics is much simpler and easy to understand than conventional mathematics. Vedic Mathematics introduces the wonderful applications to Arithmetical computations, theory of numbers, compound multiplications, algebraic operations, factorizations, simple quadratic and higher order equations, simultaneous quadratic equations, partial fractions, calculus, squaring, cubing, square root, cube root, coordinate geometry and wonderful Vedic Numerical code. Conventional mathematics is an integral part of engineering education since most engineering system designs are based on various mathematical approaches. All the leading manufacturers of microprocessors have developed their architectures to be suit-able for conventional binary arithmetic methods. The need for faster processing speed is continuously driving major improvements in processor technologies, as well as the search for new algorithms.

The Vedic mathematics approach is totally different and considered very close to the way a human mind works. A multiplier is one of the key hardware blocks in most of applications such as digital signal processing, encryption and decryption algorithms in cryptography and in other logical computations. With advances in technology, many researchers have tried to design multipliers which offer either of the following- high speed, low power consumption, regularity of layout and hence less area or even combination of them in multiplier. The Vedic multiplier is considered here to satisfy our requirements. The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital Hardware.

III. REVERSIBLE LOGIC

Reversible logic is a promising computing design paradigm which presents a method for constructing computers that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. Specifically the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in dose proximity. The basic principle of reversible computing is that a objective device with an identical number of input and output lines will produce a computing environment where the electrodynamics of the system allow for prediction of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation
A reversible logic gate is an N-input N-output logic device that provides one to one mapping between the input and the output. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. Garbage outputs are those which do not contribute to the reversible logic realization of the design. Quantum cast refers to the cost of the circuit in terms of the cost of a primitive gate. Gate count is the number of reversible gates used to realize the function. Gate level refers to the number of levels which are required to realize the given logic functions.

The following are the important design constraints for reversible logic circuits.

1. Reversible logic gates do not allow fan-outs.
2. Reversible logic circuits should have minimum quantum cost.
3. The design can be optimized so as to produce minimum number of garbage outputs.
4. The reversible logic circuits must use minimum number of constant inputs.
5. The reversible logic circuits must use a minimum logic depth or gate levels.

The basic reversible logic gates encountered during the design are listed below:

1. Feynman Gate [5]:

It is a 2x2 gate and its logic circuit is as shown in the figure. It is also known as Controlled Not (CNOT) Gate. It has quantum cost one and is generally used for Fan Out purposes.

2. Peres Gate [17]:

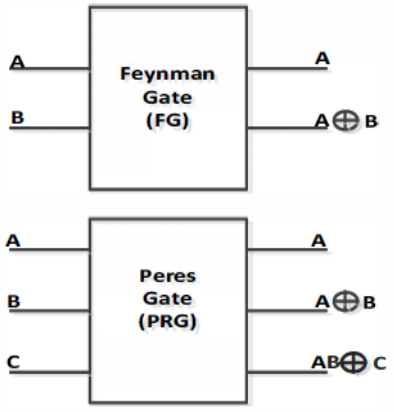
It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost four. It is used to realize various Boolean functions such as AND, XOR.

3. Fredkin Gate [16]:

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost five. It can be used to implement a Multiplexer.

4. HNG Gate[7]:

It is a 4x4 gate and its logic circuit is as shown in the figure. It has quantum cost six. It is used for designing ripple carry adders. It can produce both sum and carry in a single gate thus minimizing the garbage and gate counts.



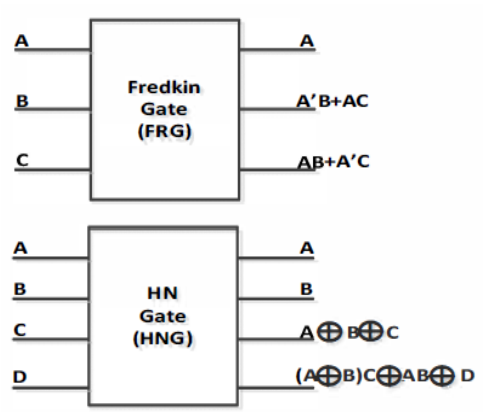
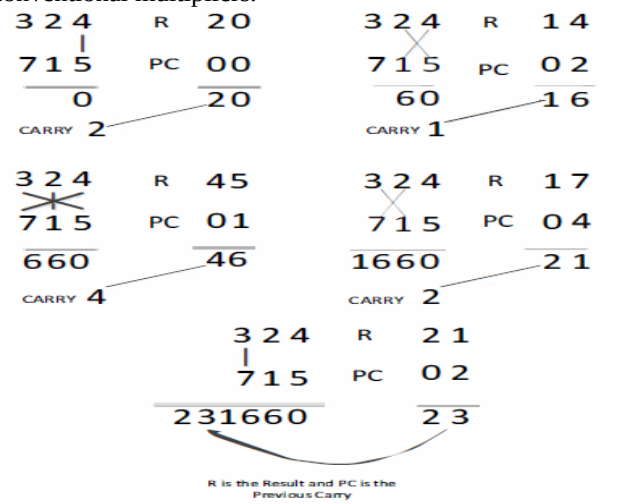


Fig1: Reversible Loglc Gates [5][7][16][17].

IV. URDHVA TRRYAKBHAYAMMULTIPLICATION ALGORITHM

Urdhva Tiryakbhayam CUT) is a multiplier based on Vedic mathematical algorithms devised by ancient Indian Vedic mathematicians. Urdhva Tiryakbhayam sutra can be applied to all cases of multiplications viz. Binary, Hex and also Decimals. It is based on the concept that generation of all partial products can be done and then concurrent addition of these partial products is performed. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhayam. Unlike other multipliers with the increase in the number of bits of multiplicand and/or multiplier the time delay in computation of the product does not increase proportionately. Because of this fact the time of computation is independent of c10ck frequency of the processor. Hence one can limit the c10ck frequency to a lower value. Also, since processors using lower c10ck frequency dissipate lower energy, it is economical in terms of power factor to use low frequency processors employing fast algorithms like the above mentioned. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases at a slow pace as compared to other conventional multipliers.



Flgure2: Urdhva Tlryakbhayam Algorithm For decimal Mul Tlpltca Tlon.

The algorithm can be iIlustrated using the following visual walkthrough. Fig2 shows the application of the algorithm for decimal multiplication and Figure 3 for binary multiplication.

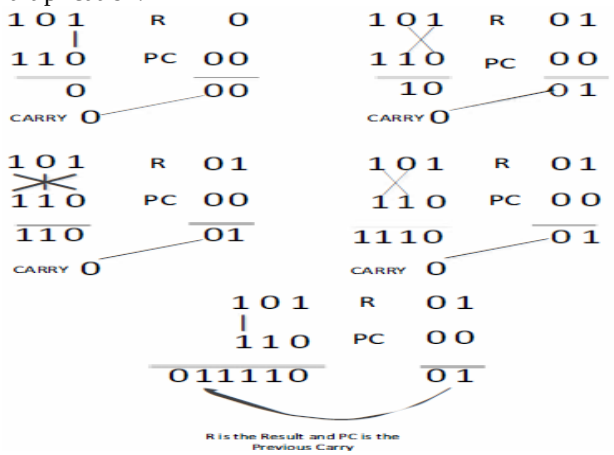


Fig3: Urdhva Tlryakbha Yam Algortthm for Blnary Multlpltcatlon

V. ARCHIRECRURE OF REVERSIBLE URDHV A TIR Y AKBHA Y AM MULTIPLIER

The digital logic implementation of the 2X2 Urdhva Tiryakbhayam multiplier using the conventional logic gates [19] is as shown in figure 4. The expressions for the four output bits are given under. The reversible implementation is as shown in figure 5. This design does not consider the fanouts. The circuit requires a total of six reversible logic gates out of which five are Peres gates and remaining one is the Feynman Gate. The quantum cost of the 2X2 Urdhva Tiryakbhayam Multiplier is enumerated to be 21. The number of garbage outputs is 9 and number of constant inputs is 4. The Reversible 4X4 Urdhva Tiryakbhayam Multiplier design emanates from the 2X2 multiplier. The block diagram of the 4X4 Vedic Multiplier is presented in the figure 6. It consists of four 2X2 multipliers each of which procures four bits as inputs; two bits from the multiplicand and two bits from the multiplier. The lower two bits of the output of the first 2X2 multiplier are entrapped as the lowest two bits of the final result of multiplication. Two zeros are concatenated with the upper two bits and given as input to the four bit ripple carry adder.

The other four input bits for the ripple carry adder are obtained from the second 2X2 multiplier. Likewise the outputs of the third and the terminal 2X2 multipliers are given as inputs to the second four bit ripple carry adder. The outputs of these four bit ripple carry adders are in turn 5 bits each which need to be summed up. This is done by a five bit ripple carry adder which generates a six bit output. These six bits form the upper bits of the final result. The ripple carry adder is consummated (realized) using the HNG Gate. The number of bits that need to be ripple carried verdicts the number of HNG gates to be used. Thus a 4-bit ripple carry adder needs 4 HNG gates and the 5 bit adder requires 5

HNG gates. This design also does not take into consideration the fan out gates. For this design the quantum cost is computed to be 162, the total number of gates used will be 37, the number of garbage outputs will be 62 and the number of constant inputs will be 29.

The Algorithm: Multiplication of 101 by 110.

1. We will take the right-hand digits and multiply them together. This will give us LSB digit of the answer.
2. Multiply LSB digit of the top number by the second bit of the bottom number and the LSB of the bottom number by the second bit of the top number. Once we have those values, add them together.
3. Multiply the LSB digit of bottom number with the MSB digit of the top one, LSB digit of top number with the MSB digit of bottom and then multiply the second bit of both, and then add them all together.
4. This step is similar to the second step, just move one place to the left. We will multiply the second digit of one number by the MSB of the other number.
5. Finally, simply multiply the LSB of both numbers together to get the final product.

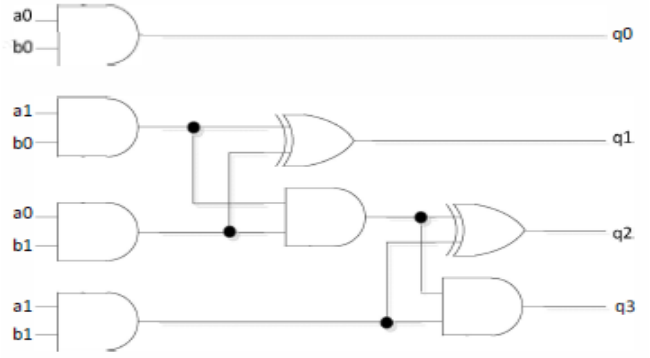


Fig4. Conventional Logic Implementation of 2x2 UT Multiplier [19].

q0= a0.b0
q1= (a1.b0) xor (a0.b1)
q2= (a0.a1.b0.b1) xor (a1.b1)
q3= a0.a1.b0.b1

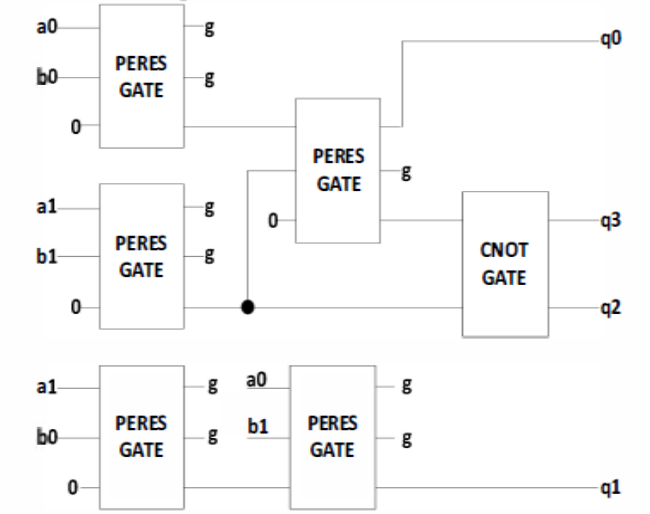
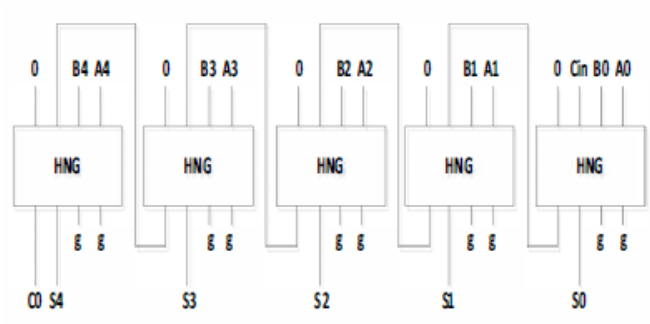
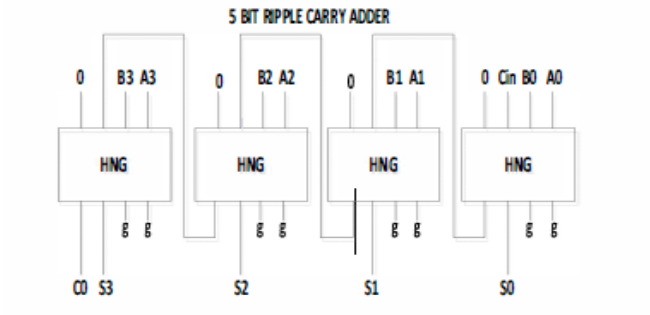


Fig5: Reversible Implementation of 2x2 UT Multiplier.



5 BIT RIPPLE CARRY ADDER



4 BIT RIPPLE CARRY ADDER

Fig6: Ripple Carry Adder.

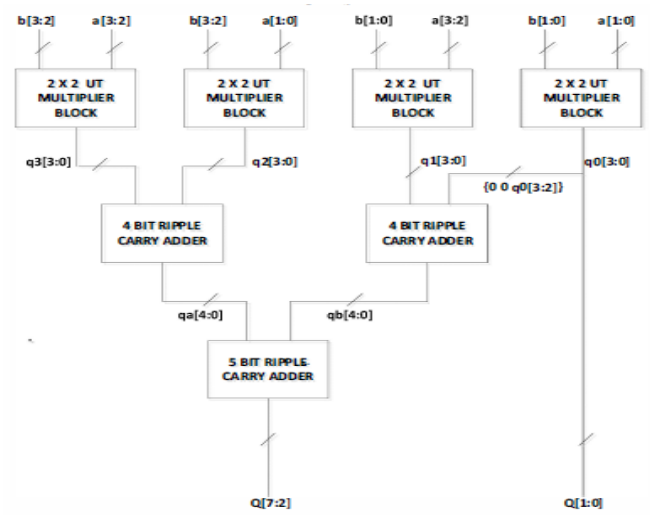


Fig7: Block Diagram of 4x4 UT Multiplier.

IV. RESULTS, ANALYSIS AND COMPARISON

The Reversible 32X32 Urdva Tiryakbhayam Multiplier design emanates from the 16X16 multiplier. The block diagram of 32X32Vedic multiplier is presented in the Fig.5. It consists of four 16X16 multipliers each of which produce 32 bits as inputs; 16 bits from the multiplicand and 16 bits from the multiplier. The lower 16 bits of the output of the first 16X16 multiplier are entrapped as the lowest 16 bits of the final result of multiplication. 16 zeros are concatenated with the upper 16 bits and give as input to the 32 bit ripple carry adder. The center two multipliers which produce 32 bits each as a outputs and these outputs are concatenated to 32 bit ripple carry adder, which produces an output of 33 bit, these 33 bits is given as input to 33 bit ripple carry adder

which produces 34 bits, of these LSB 16 bits is taken as output. Then remaining 18 bits is given to 32 bit ripple carry adder, which is having 32 bits as input from the last multiplier, then 32 ripple carry adder generates 32 bits as output.

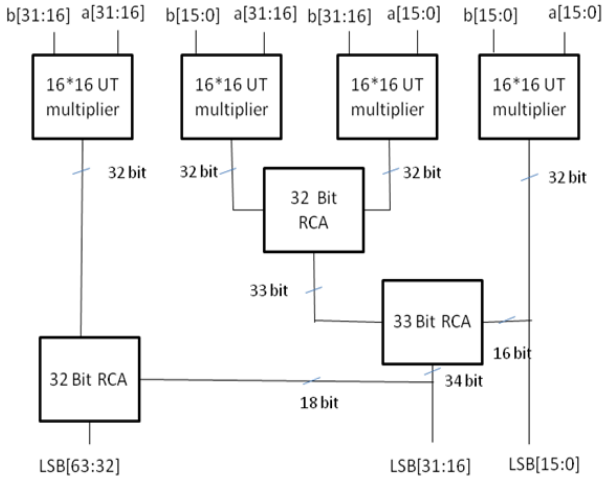


Fig5: Block Diagram of 32X32 UT multiplier

MULTIPLIER	MAXIMUM COMBINATIONAL PATH DELAY
4 Bit Vedic Multiplier using Reversible Logic gates	15.363 ns
32 Bit Array Multiplier using Reversible Logic gates	126.335 ns
32 Bit Vedic Multiplier using Reversible Logic gates	87.587 ns

Fig6: Speed comparisons between the multipliers.

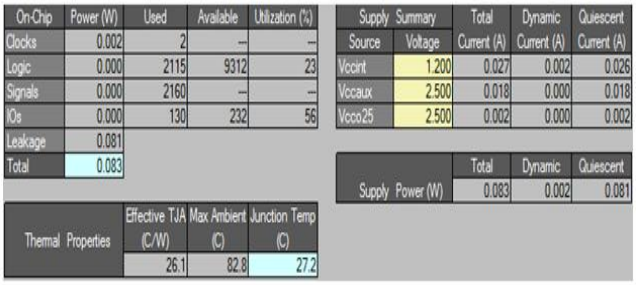


Fig7: Power analyzer of 32- bit array multiplier using reversible logic.

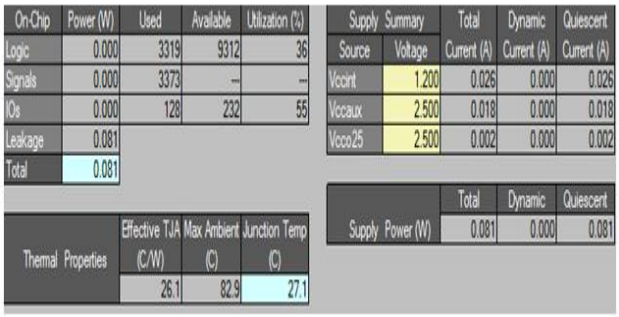


Fig8: Power analyzer of 32- bit Vedic multiplier using reversible logic.

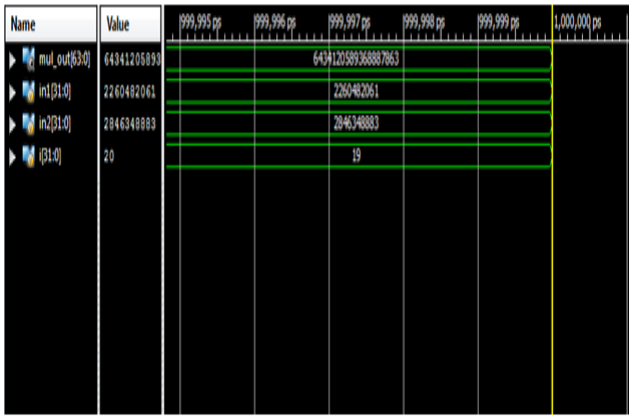


Fig9: Simulation results of reversible 32X32 UT multiplier.

V. CONCLUSION

This paper presents the Urdhva Tiryakbhayam 32-bit Vedic multiplier realized using reversible logic gates. Firstly a basic 2X2 UT multiplier is designed. This design stems from the conventional logic implementation. After this, the 2X2 UT multiplier block is cascaded to obtain 4X4 multiplier. After this, 16X16 multiplier blocks is cascaded to obtain 32X32multiplier. The ripple carry adders which were required for adding the partial products were constructed using HNG gates. Design of 4 bit Vedic multiplier implemented using reversible logic has maximum combinational path delay of 15.363ns. The proposed design of 32-bit Vedic multiplier implemented using reversible logic has maximum combinational path delay of 87.587ns.the design of 32 bit array multiplier implemented using reversible logic has maximum combinational path delay of 126.335ns. Thus on increase in number of bits of multiplicand and multiplier the speed does not decrease with high pace. The power analyze of proposed design of 32 bit Vedic multiplier implemented using reversible logic has 81mW, and the power analyze of proposed design of 32 bit array multiplier implemented using reversible logic has 83mW.

VI. REFERENCES

[1] Rakshith TR., Rakshith Saligram, "Design of High Speed Low Power 32-Bit Multiplier Using Reversible Logic: A Vedic Mathematical APPROACH", 2013 International Conference on Circuits, Power and Computing Technologies.

[2] Swami Bharati Krsna Tirtha, Vedic Mathematics. Delhi: Motilal Banarsidass publishers 1965.

[3] Rakshith Saligram and Rakshith T.R. "Design of Reversible Multipliers for linear filtering Applications in DSP" International Journal of VLSI Design and Communication systems, Dec-12.

[4] R. Landauer," Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp.183-191, 1961.

[5] C.H. Bennett, "Logical reversibility of Computation", IBM J. Research and Development, pp.525-532, November 1973.

[6] R. Feynman, "Quantum Mechanical Computers," Optics News, Vol.1l, pp. 11-20, 1985.
[7] H. Thapliyal and M.B. Srinivas, "Novel Reversible Multiplier Architecture Using Reversible TSG Gate", Proc. IEEE International Conference on Computer Systems and Applications, pp. 100-103, March 20 06.
[8] Shams, M., M. Haghparast and K. Navi, Novel reversible multiplier circuit in nanotechnology. World Appl. Sci. J., 3(5): 806-810.
[9] Somayeh Babazadeh and Majid Haghparast, "Design of a Nanometric Fault Tolerant Reversible Multiplier Circuit" Journal of Basic and Applied Scientific Research, 2012.
[10] Thapliyal, H., M.B. Srinivas and H.R. Arabnia, 2005, A Reversible Version of 4x4 Bit Array Multiplier with Minimum Gates and Garbage Outputs, Int. Conf. Embedded System, Applications (ESA'05), Las Vegas, USA, pp: 106 114.
[11] H. Thapliyal and M.B. Srinivas, "Reversible Multiplier Architecture Using TSG Gate", Proc. IEEE International Conference on Computer Systems and Applications, pp. 241-244, March 20 07.
[12] M. Haghparast et al. , "Design of a Novel Reversible Multiplier Circuit using HNG Gate in Nanotechnology," in World Applied Science Journal, Vol. 3, No. 6, pp. 974-978, 2008.