







The image shows a detailed PCB layout for an ADXL345 module. The central component is the ADXL345 digital accelerometer, which is connected to a microcontroller via I2C (SDA and SCL lines). The layout includes various passive components such as resistors and capacitors, and a VREF circuit. The pinout for the ADXL345 is shown at the top, with labels for DRAM addresses, data, and control signals. The layout also shows the placement of decoupling capacitors, a VREF circuit, and a pull-up resistor for the I2C SDA line.

ADXL345 Pinout:

Pin	Signal	Pin	Signal	Pin	Signal
1	DRAM_ADDR0	18	DRAM_DATA0	35	DRAM_DATA15
2	DRAM_ADDR1	19	DRAM_DATA1	36	DRAM_DATA16
3	DRAM_ADDR2	20	DRAM_DATA2	37	DRAM_DATA17
4	DRAM_ADDR3	21	DRAM_DATA3	38	DRAM_DATA18
5	DRAM_ADDR4	22	DRAM_DATA4	39	DRAM_DATA19
6	DRAM_ADDR5	23	DRAM_DATA5	40	DRAM_DATA20
7	DRAM_ADDR6	24	DRAM_DATA6	41	DRAM_DATA21
8	DRAM_ADDR7	25	DRAM_DATA7	42	DRAM_DATA22
9	DRAM_ADDR8	26	DRAM_DATA8	43	DRAM_DATA23
10	DRAM_ADDR9	27	DRAM_DATA9	44	DRAM_DATA24
11	DRAM_ADDR10	28	DRAM_DATA10	45	DRAM_DATA25
12	DRAM_ADDR11	29	DRAM_DATA11	46	DRAM_DATA26
13	DRAM_ADDR12	30	DRAM_DATA12	47	DRAM_DATA27
14	DRAM_ADDR13	31	DRAM_DATA13	48	DRAM_DATA28
15	DRAM_ADDR14	32	DRAM_DATA14	49	DRAM_DATA29
16	DRAM_ADDR15	33	DRAM_DATA15	50	DRAM_DATA30
17	DRAM_ADDR16	34	DRAM_DATA16	51	DRAM_DATA31
18	DRAM_ADDR17	35	DRAM_DATA17	52	DRAM_DATA32
19	DRAM_ADDR18	36	DRAM_DATA18	53	DRAM_DATA33
20	DRAM_ADDR19	37	DRAM_DATA19	54	DRAM_DATA34
21	DRAM_ADDR20	38	DRAM_DATA20	55	DRAM_DATA35
22	DRAM_ADDR21	39	DRAM_DATA21	56	DRAM_DATA36
23	DRAM_ADDR22	40	DRAM_DATA22	57	DRAM_DATA37
24	DRAM_ADDR23	41	DRAM_DATA23	58	DRAM_DATA38
25	DRAM_ADDR24	42	DRAM_DATA24	59	DRAM_DATA39
26	DRAM_ADDR25	43	DRAM_DATA25	60	DRAM_DATA40
27	DRAM_ADDR26	44	DRAM_DATA26	61	DRAM_DATA41
28	DRAM_ADDR27	45	DRAM_DATA27	62	DRAM_DATA42
29	DRAM_ADDR28	46	DRAM_DATA28	63	DRAM_DATA43
30	DRAM_ADDR29	47	DRAM_DATA29	64	DRAM_DATA44
31	DRAM_ADDR30	48	DRAM_DATA30	65	DRAM_DATA45
32	DRAM_ADDR31	49	DRAM_DATA31	66	DRAM_DATA46
33	DRAM_ADDR32	50	DRAM_DATA32	67	DRAM_DATA47
34	DRAM_ADDR33	51	DRAM_DATA33	68	DRAM_DATA48
35	DRAM_ADDR34	52	DRAM_DATA34	69	DRAM_DATA49
36	DRAM_ADDR35	53	DRAM_DATA35	70	DRAM_DATA50
37	DRAM_ADDR36	54	DRAM_DATA36	71	DRAM_DATA51
38	DRAM_ADDR37	55	DRAM_DATA37	72	DRAM_DATA52
39	DRAM_ADDR38	56	DRAM_DATA38	73	DRAM_DATA53
40	DRAM_ADDR39	57	DRAM_DATA39	74	DRAM_DATA54
41	DRAM_ADDR40	58	DRAM_DATA40	75	DRAM_DATA55
42	DRAM_ADDR41	59	DRAM_DATA41	76	DRAM_DATA56
43	DRAM_ADDR42	60	DRAM_DATA42	77	DRAM_DATA57
44	DRAM_ADDR43	61	DRAM_DATA43	78	DRAM_DATA58
45	DRAM_ADDR44	62	DRAM_DATA44	79	DRAM_DATA59
46	DRAM_ADDR45	63	DRAM_DATA45	80	DRAM_DATA60
47	DRAM_ADDR46	64	DRAM_DATA46	81	DRAM_DATA61
48	DRAM_ADDR47	65	DRAM_DATA47	82	DRAM_DATA62
49	DRAM_ADDR48	66	DRAM_DATA48	83	DRAM_DATA63
50	DRAM_ADDR49	67	DRAM_DATA49	84	DRAM_DATA64
51	DRAM_ADDR50	68	DRAM_DATA50	85	DRAM_DATA65
52	DRAM_ADDR51	69	DRAM_DATA51	86	DRAM_DATA66
53	DRAM_ADDR52	70	DRAM_DATA52	87	DRAM_DATA67
54	DRAM_ADDR53	71	DRAM_DATA53	88	DRAM_DATA68
55	DRAM_ADDR54	72	DRAM_DATA54	89	DRAM_DATA69
56	DRAM_ADDR55	73	DRAM_DATA55	90	DRAM_DATA70
57	DRAM_ADDR56	74	DRAM_DATA56	91	DRAM_DATA71
58	DRAM_ADDR57	75	DRAM_DATA57	92	DRAM_DATA72
59	DRAM_ADDR58	76	DRAM_DATA58	93	DRAM_DATA73
60	DRAM_ADDR59	77	DRAM_DATA59	94	DRAM_DATA74
61	DRAM_ADDR60	78	DRAM_DATA60	95	DRAM_DATA75
62	DRAM_ADDR61	79	DRAM_DATA61	96	DRAM_DATA76
63	DRAM_ADDR62	80	DRAM		

VREF circuit should
be placed close between
proc and dram





