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CMS ECAL Off-detector Electronics

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Abstract

This report summarizes the architecture and functionality of the Off-detector electronics system of the Compact Muon Solenoid (CMS) Electromagnetic Calorimeter (ECAL). The ECAL readout and trigger architecture is organized in two physical layers: the On-detector electronics and the Off-detector electronics. At the On-detector boards crystal signals are amplified, digitized and pipelined waiting for the first level trigger decision. In parallel, the On-detector system sends to the Off-detector trigger boards the trigger data, and after final calculation and synchronization of the trigger primitives, these data are sent to the Regional Trigger system. If the event passes the level 1 trigger, the On-detector sends the crystal data to the Off-detector readout electronics where, among other operations, data integrity is verified, reduced (through the combination of Selective Readout and Zero Suppression algorithms) and finally, data are formatted and transmitted to the CMS Data Acquisition system.

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1 Introduction

The CMS ECAL [1] is a high-resolution calorimeter made of the order of 80000 lead tungstate (PbWO$_4$) crystals. The On-detector electronics is organized following arrays of 5x5 crystals called Trigger Towers in the barrel and Super-crystals in the end-caps. The Trigger Towers are organized in Super-modules (1700 crystals) and the Super-crystals are organized in Dees (3662 crystals). Bi-di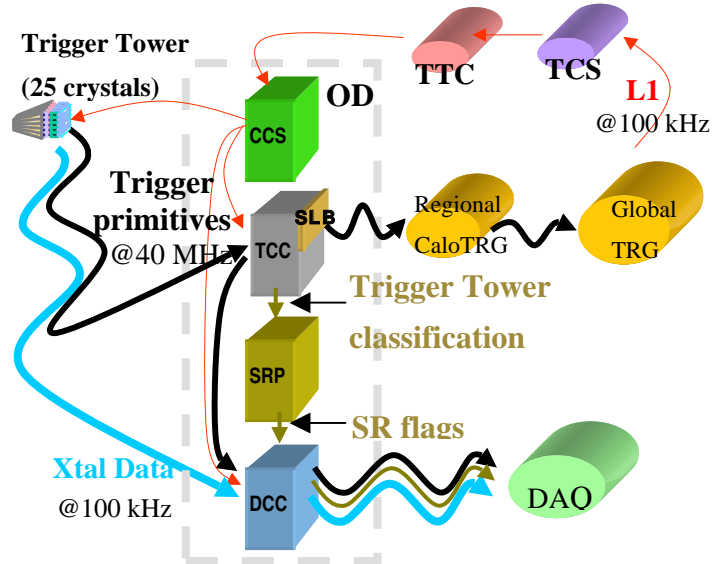rectional optical links connect the On-detector system and the Off-detector Clock and Control System (CCS) board. Those links carry clock and control signals and the trigger level 1 accepts signal (L1A) from the Timing, Trigger and Control (TTC) board [2] and the Trigger Control System (TCS) [3]. Crystal signals collected by an Avalanche Photodiode (APD) in the barrel or a Vacuum Phototriode (VPT) in the end-caps, are amplified, sampled at 40 MHz, digitized and finally, pipelined during the first level trigger L1A latency. In parallel, sophisticated Trigger Primitives are computed and sent to the Off-detector Trigger Concentrator Card (TCC) at 40 MHz using high-speed optical links (800 Mbits/s). After final calculation of the Trigger Primitives in the TCC and synchronization by the Synchronization and Link mezzanine Board (SLB), the trigger data are sent to the Regional Calorimeter Trigger and then to the Global Trigger. On reception of a first level trigger decision signal, crystal data are formatted and transmitted to the Off-detector Data Concentrator Card (DCC) using another set of high-speed optical links (800 Mbits/s). There data integrity is verified, reduced (through the combination of Selective Readout and Zero Suppression algorithms) and finally, data are formatted and transmitted to the CMS Data Acquisition (DAQ) system through an S-link 64 [4]. The schematic layout of the Off-detector system and its interfaces are shown in Figure 1.

Figure 1. Off-detector system and its interfaces with the On-detector and the Data Acquisition and Trigger System.

2 The Clock and Control System (CCS)

The CCS is a VME 9U module, VME64x compliant, responsible for:

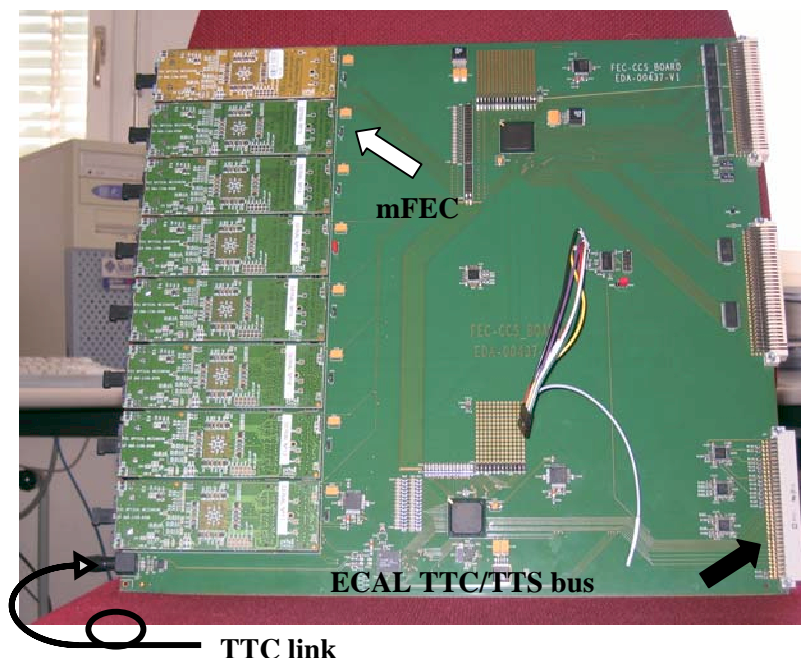- interfacing the On- and Off-detector electronics to the TCS and Trigger Throttling System (TTS);

Figure 2. The CCS board prototype designed by the CERN group.

- distribution of clock, L1A and control signals (e.g. BC0) to the TCC, the DCC and the On-detector electronics;
- fan-in the TTS signals from the DCC and TCC, and transmission to the TTS;
- configuration and setup of the On-detector electronics.

3   The Trigger Concentrator Card (TCC) and the Synchronization and Link Board (SLB)

The Trigger Primitives are sent at 40 MHz from the On-detector Trigger Primitive Generator (TPG) to the TCC. The Trigger Primitive is computed for each Trigger Tower and consists of the total transverse energy of the Trigger Tower (E_T) and a bit called the Fine Grain Veto bit. This bit reflects the lateral extension of the electromagnetic shower, and it is used to improve the rejection of background in the electromagnetic trigger. It relies on the fact that on average 80% of the energy deposited by an electron is contained in one crystal. Bunch-crossing identification is also performed in the TPG.

The TCC is a VME 9U module, VME64x compliant, which functions are the following:
1. opto-electronic conversion and deserialization of the input Trigger Primitives;
2. completing the Trigger Primitives calculation for the end-caps performing the geometrical mapping between the Trigger Towers ($\eta\phi$) and the Super-crystals (xy);
3. classifying the Trigger Towers in three categories depending on the total E_T and on adjustable Low and High Energy Thresholds:
   a) $E_T <$ Low Energy Threshold (LET ~1 GeV);
   b) LET $< E_T <$ High Energy Threshold (HET ~2.5 GeV);
   c) $E_T >$ HET;
   and transmits this classification at the L1A frequency to the Selective Readout Processor;
4. storing the Trigger Primitives during the L1A latency for subsequent reading by the DCC upon reception of the L1A.

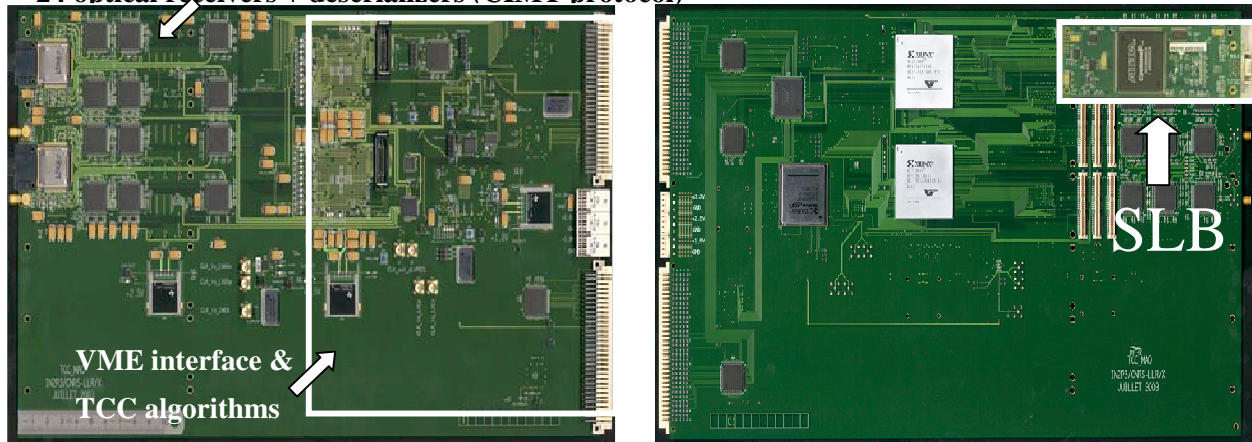**24 optical receivers + deserializers (CIMT protocol)**

Figure 3. The TCC24 prototype designed by LLR (CNRS/IN2P3), and the SLB designed by the LIP (Lisbon) group.

The SLB is a custom mezzanine board implemented in the TCC that plays the role of the interface between the Off-detector and the Regional Calorimeter Trigger. The SLB is responsible for performing the synchronization of the trigger data that arrives @40 MHz (with the granularity of a Trigger Tower) using synchronization circuits. Those circuits build online histograms to survey the LHC bunch crossing structure. Each Trigger Tower time structure is aligned with respect to the BC0. Once the trigger data are synchronized, the serial transmission to the Regional Calorimeter Trigger at 1.2 Gbits/s takes place.

4 The Selective Readout Processor (SRP)

If there is a positive first level trigger decision the Trigger Tower classification made by the TCC is sent to the SRP to compute the Selective Readout (SR) flags. The processor uses a sliding window method to combine the information of different Trigger Towers of different Super-modules on a 3x3 Trigger Tower matrix basis. The Trigger Towers are scanned in pseudorapidity and in phi directions on the full detector including end-caps. The Selective Readout criteria are the following:

1. <u>High energy e/γ criterium</u>: If the E_T in a Trigger Tower is above HET, then the Trigger Tower is labeled as *centre state (11)* and all the others around in a 3x3 Trigger Tower matrix are labeled as *neighbor states (01)*. Upon reception of these flags the DCC will read the 10 time samples per crystal for that window of 3x3 Trigger Towers centered on the *centre state* tower.

2. <u>Low energy e/γ criterium</u>: If the E_T in a Trigger Tower is larger than LET, and lower than HET, then the Trigger Tower state is set to *single state (10)*. Upon reception of the flag the DCC will read the 10 time samples of the crystals of that Trigger Tower. The information of the neighboring Trigger Towers is supplied by the coarse grain data.

3. <u>Not-read state</u>: If E_T is below LET and the Trigger Tower is not a neighbor state, it will be set in a *not-read state (00)*.

The SR algorithm is not suitable for low energy electromagnetic clusters (< 1 GeV). They contribute, however, in a significant way to the measurement of jets and E_T^{miss}. In consequence the SR must be complemented with coarse grain data of the entire calorimeter. The coarse grain data are the Trigger Primitives when the event passes the first level trigger. In all cases, the coarse grain data will be readout for all Trigger Towers providing a complete map of calorimeter energy flow.

The SR flags must arrive to the DCC before the crystal data because the DCC will readout or not a Trigger Tower depending on the SR flags. The time budget of SR flags calculation is then 3-4 μs. The SRP consists of a single VME 6U crate with twelve algorithm boards that compute the SR flags.

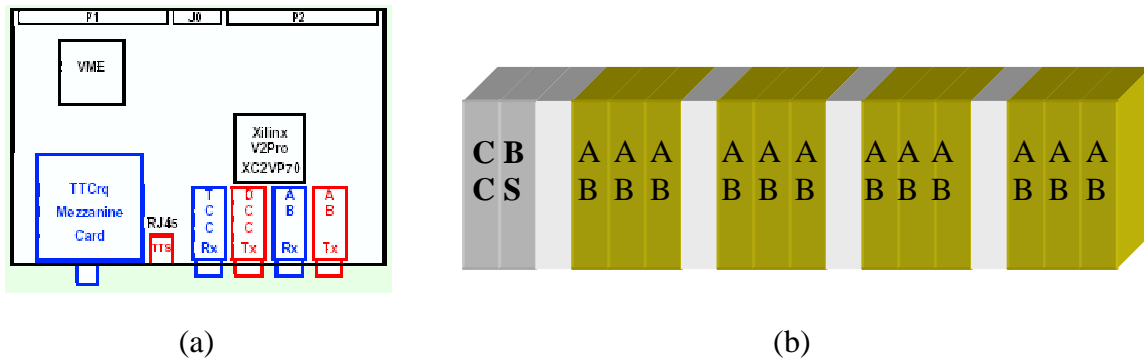(a)   (b)

Figure 4. (a) Layout of the Algorithm Boards (AB) of the SRP designed by the DAPNIA - CEA Saclay group.

(b) The SRP is a collection of AB placed in a single 6U VME crate.

5 The Data Concentrator Card (DCC)

The last piece of the Off-detector architecture is the DCC. The DCC is implemented on a VME 9U board, VME64x compliant. It receives 68 optical data links from the On-detector boards (one link per Trigger Tower; one DCC reads one Super-module), two additional optical links from the Monitoring Electronic Module (MEM), one SR link to get the SR flags and up to four links from the TCC. The DCC also includes a TTC and a TTS interface.

The DCC performs the opto-electronic conversion and deserialization of the serial input data streams. The input event fragments integrity and synchronization are also verified at the input handler side.

5.1 Data volume reduction on-line

The input event fragments correspond to ~40 Kbytes per DCC, however the DAQ system limits the size of the events to 2 Kbytes or, equivalently, to an average transmission data flow of 200 Mbytes/s. In order to achieve this average suppression factor of 20, two complementary methods are used on-line by the DCC: **Zero Suppression (ZS) and Selective Readout (SR)**. Under the control of the input handler, crystal data are analyzed

on a channel-by-channel basis by the ZS FIR (Finite Impulse Response) filter. Crystal signals from Trigger Towers that pass the high or low energy e/γ criteria and that are, nevertheless, below a certain programmable ZS energy threshold are suppressed. The threshold in this case is kept at a low level, typically below 2σ of the noise distribution. Further suppression would imply a degradation of the energy resolution and linearity. Trigger Towers in *not-read* state either will not be readout by the DCC, or optionally, they will be readout applying another higher and programmable ZS energy threshold.

Only event fragments that pass ZS and SR are moved into the DCC Event Manager to be formatted and sent to the DAQ system.
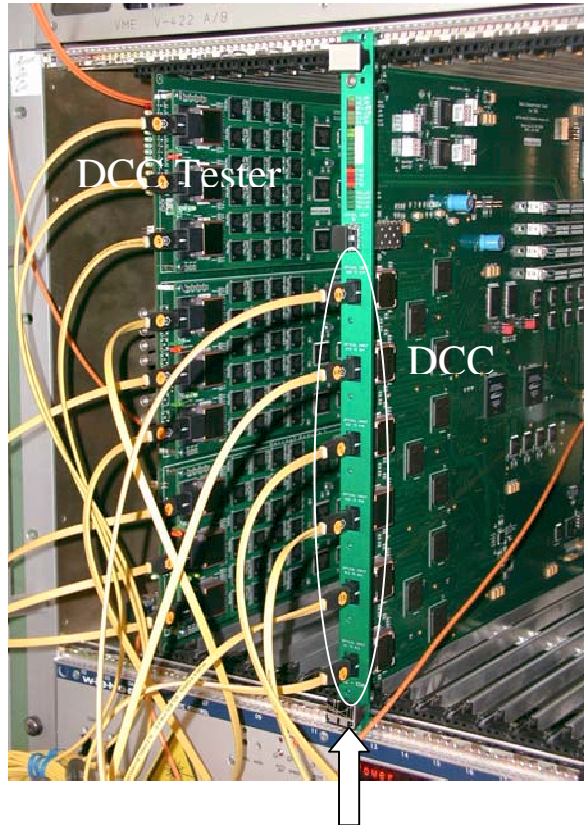

70 Optical links

Figure 5. The DCC with 70 high-speed optical links working, and the DCC Tester card as designed by LIP.

5.2   Buffer handling

The DCC implements a double protection mechanism to avoid overflow in the data buffers and the consequent loss of synchronization. The mechanism consist on first using a TTS feedback, and secondly, storing empty events. The available free space in the buffers is monitored and compared to two programmable thresholds. When the **Almost Full Level 1** is reached the TTS signal **Warning Overflow** is issued, requesting a reduction in trigger rate. If the **Almost Full Level 2** is reached the TTS signal **Busy** is issued, inhibiting new triggers, and in parallel empty events are stored. If the **Full** condition is reached the DCC enters in **Error state** and waits for a **Reset**.

5.3   Event Format

The DCC formats together the TCC information (coarse grain data), the SRP flags and the crystal data (fine grain data) of selected Trigger Towers according to the SR processor flags. Words of 64 bits are formed and sent to the DAQ through a S-Link 64 (the maximum rate by design is 528 Mbytes/s) at L1A rate provided by the trigger system.

5.4   Event types

The event types received by the DCC are of two kinds: physics events (the result of a p-p collision), and monitoring events like laser, pedestals, MEM test pulse and test pulses applied on the very front-end electronics. Some kind of events are stored in the VME spy memory and sent only to the local DAQ.

6   Crate layout

The Super-module readout unit in the barrel consists of one CCS, one DCC and one double-width TCC. A total of twelve 9U VME64x crates are needed to contain the trigger and readout electronics of the whole barrel.

The 40º readout unit in the End-Caps consists of one CCS, one DCC and four single-width TCC. A total of six 9U VME64x crates are needed to contain the trigger and readout electronics of the two End-Caps.

7   Software

The software built to operate all the Off-detector components has been based on a toolkit that supports the development of distributed data acquisition systems in a network environment. The toolkit XDAQ [5,6] has been completely developed by the CMS Data Acquisition System and Detector Control group at CERN. It facilitates the use of communication mechanisms (TCP/IP and GM) and protocols (SOAP [7] and i2o [8]). It offers

pluggable modules providing a W3C standard DOM [9] interface to read/write information from/to persistent data storage like ORACLE, MySQL and XML [10]. XDAQ implements a high level interface hardware access library, which allows for user-friendly hardware access to VME or PCI modules.

The software [11] has been organized in three main parts: crate configuration, run control and data acquisition. The crate configuration takes care of the setting up of the crate and of all the electronic modules present in the crate. First of all, the entire crate, which is VME64x compliant, is scanned in order to perform a plug and play configuration, i.e. the memory map of the crate is automatically created and the base addresses are automatically set for all the VME64x devices placed in. In a second step, the stored information concerning the crate and the devices inside the crate (except the configurable parameters) is retrieved from the database and compared with the currently scanned one. If there are differences, the stored data can be updated on-line with the new layout.

Once the crate has been set up, the second part controls the operation of the crate. To accomplish this task the software implements a state machine pattern to configure (write into the device registers the configurable parameters retrieved from the database), start, stop, pause, etc the current run of the system.

The last part is related to the acquisition and storing of the data. For the acquisition, the software offers two possibilities. In the first one, the data are read out from the DCC S-Link64 interface using the FEDkit [12] delivered by the EP/CMD group at CERN and sent to the DAQ. In the second one, the data are read out from the DCC spy memory via VME and sent to the local data monitoring.

8   Conclusions

The CMS ECAL Off-detector electronics architecture and functionality and its interface with the On-detector electronics and the DAQ and Trigger systems have been presented. Among its features the following ones should be emphasized:
1. it is the first time a sub-detector will operate with ~9000 high-speed (800 Mbits/s) optical links;
2. the Trigger system will run at 40 MHz and will compute sophisticated Trigger Primitives;
3. a data volume reduction factor of ~20 needed to cope with the CMS DAQ specification of 200 Mbytes/s of data flow, will be achieved on-line with Selective Readout algorithms and Zero Suppression filters;
4. all the boards make extensive use of very large FPGA (Field Programmable Gate Array).

Prototypes of all the Off-detector boards have been produced and initial tests are successful. The SRP system is currently under design.

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