Driver Board V5.3, DB2 Test Results

1. Driver Board Initial Test
    a. Do visual inspection to make sure that all parts are on the board (Pass
    b. Check the input pins to make sure they are not shorted
    c. Plug into power, turn it on, check for smoke
    d. Measure 5V, ±15V, 24V, 2.5V, 3.3V, -50 voltages and current draw (when possible).

Table 1: Power Supply Voltages

	+5V	+15V	-15V	+24V	1.5V	2.5 V	3.3	-50
Voltage	4.857	14.93	-15.03	23.95	1.500	2.255	3.268	-52.45
Current	348mA	109mA	101mA	.001				

    e. Use the thermal image to look for hot spots
    f. Hook up JTAG (interface) to FPGA and program. FlashPro will give pass/fail on programming.
2. Hook up camera link interface. Type "lse_term". Pass/fail is seeing LSE prompt on GSE after power cycle.
3. Type "$vdm60f.fpg" to load "vdm60f" to set the DAC voltages and set up and start the sequencer in timer mode.
4. Check DACs: set DAC voltage (record set value in Table 2), measure output at DAC (record in Table 3). Value should be within 1% of full scale of expected values.

Table 2: DAC Set Values

DAC SET	Set (Hex)	Set (Dec)	/4096	Expected Value
PP (DAC 0)	0900	2304	.5625	.856
PN (DAC 1)	09C4	2500	.61035	2.014
SP (DAC 2)	04A6	1190	.29052	0.959
SN (DAC 3)	0A0A	2570	.62744	2.076
RP (DAC 4)	0280	640	.15625	0.516
RN (DAC 5)	0995	2453	.59888	1.976
IDP (DAC 6)	0CE4	3300	.80566	2.659
IDN (DAC 7)	0CE4	3300	.80566	2.659

Table 3: DAC Voltages

DAC	1	2	3	4
VREF	3.304	3.304	3.304	3.304
PP (DAC 0)	1.851	1.853	1.852	1.870
PN (DAC 1)	2.003	2.026	2.030	2.014
SP (DAC 2)	0.953	0.965	0.969	0.987
SN (DAC 3)	2.062	2.070	2.055	2.060
RP (DAC 4)	0.522	0.509	0.528	0.522
RN (DAC 5)	1.997	1.980	1.97	1.983
IDP (DAC 6)	2.647	2.662	2.659	2.661
IDN (DAC 7)	2.663	2.675	2.668	2.655

5. Measure the voltages of the clock regulators associated with each CCD.

Table 4: Regulator Voltages

CCD	PP	PN	SP	SN	RP	RN	IDP	IDN
CCD1	2.095	-8.02	6.034	-3.956	9.81	-3.424		
CCD2	1.977	-8.13	5.848	-4.114	9.92	-3.294		
CCD3	1.988	-8.13	5.862	-3.939	9.68	-3.268		
CCD4	2.151	-8.08	5.617	-3.940	9.81	-3.325		

6. Using the LSE, query each of the housekeeping values for each of the driver board voltages and record below.

Table 5: Housekeeping Voltages

CCD	PP	PN	SP	SN	RP	RN	IDP	IDN
CCD1	2.03	-7.95	6.10	-3.95	9.90	-3.51	12.06	12.10
CCD2	1.97	-8.10	5.74	-4.18	9.86	-4.18	12.09	12.19
CCD3	1.98	-8.06	5.86	-4.00	9.69	-4.00	12.09	12.16
CCD4	2.06	-8.08	5.66	-4.04	9.77	-4.04	12.07	12.05

7. With the sequencer running in timer mode, measure clock timing and amplitude with oscilloscope. Clocks to measure: parallel (framestore and imaging, 3 clocks each), serial (3 clocks), CI gate (1), reset gate (1): 11 clocks. Any visible jitter on the 'scope is a problem, as the sequencer is better than the 'scope. Attach scope photos for each clock to the end of this document.

8. Connect a known good video board and, while the sequencer is running, and verify that each of the four ADC's are functioning by observing each of the 6 signals associated with the ADC's and record this functioning below.

Table 6: Video Board ADC Functionality

CCD	SCLK	CNV	SDO-A	SDO-B	SDO-C	SDO-D
CCD1	OK	OK	OK	OK	OK	OK
CCD2	OK	OK	OK	OK	OK	OK
CCD3	OK	OK	OK	OK	OK	OK
CCD4	OK	OK	OK	OK	OK	OK

9. Using the SW available, obtain and observe the video files that are created by the board set and verify that all sixteen channels produce a valid video image.

CCD, Channel	Valid Image?
1, A	OK
1, B	OK
1, C	OK
1, D	OK
2, A	OK
2, B	OK
2, C	OK
2, D	OK
3, A	OK
3, B	OK
3, C	OK
3, D	OK
4, A	OK
4, B	OK
4, C	OK
4, D	OK

Scope Images of Clocks

Figure 1: CCD1 FS

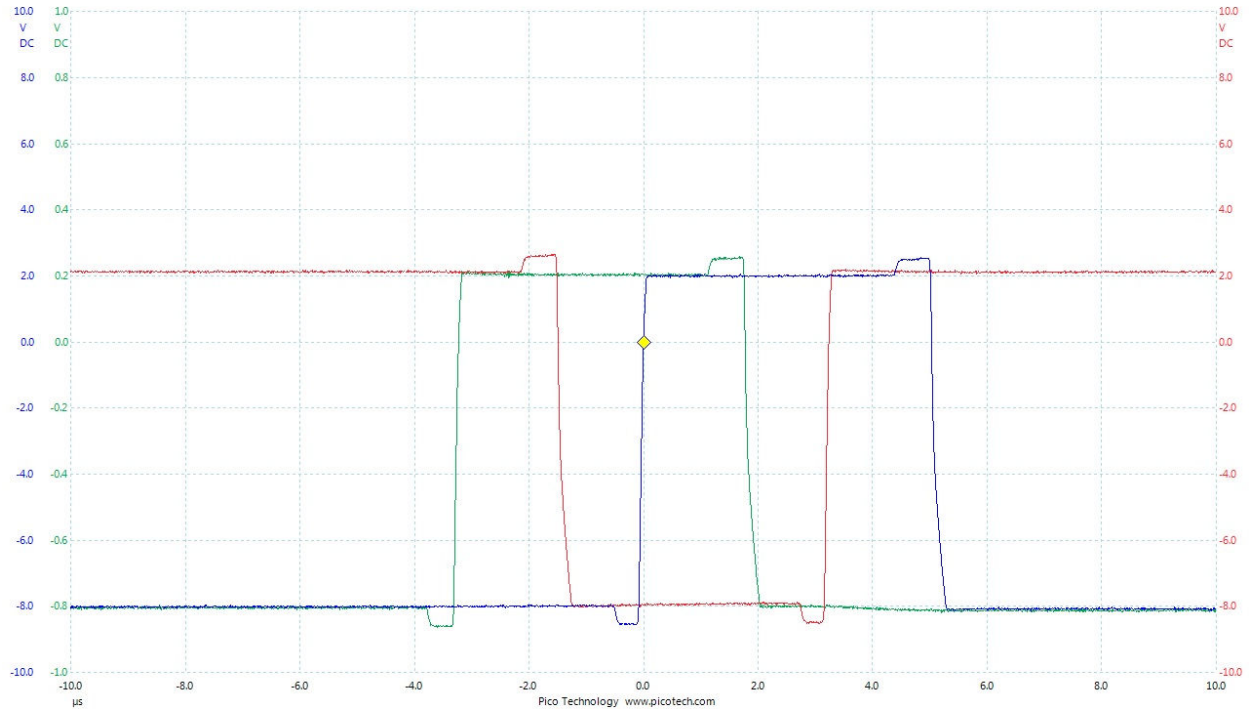

Figure 2: CCD1 IA

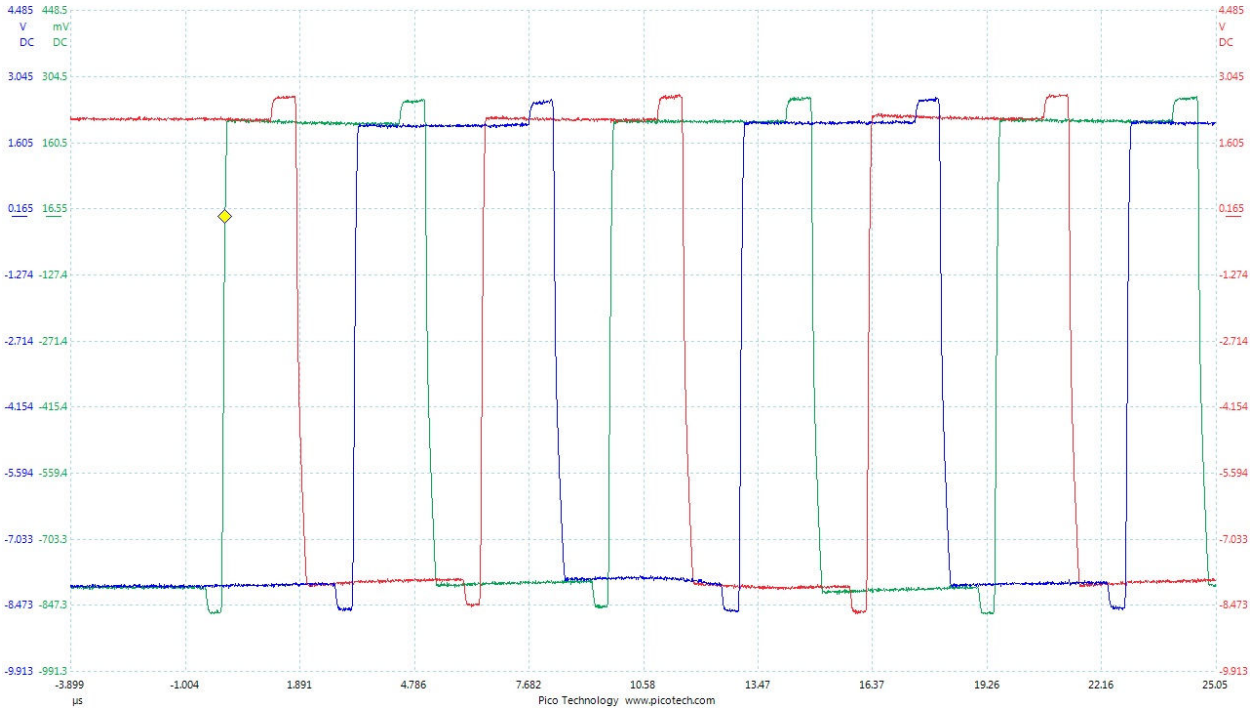

Figure 3: CCD1 OR

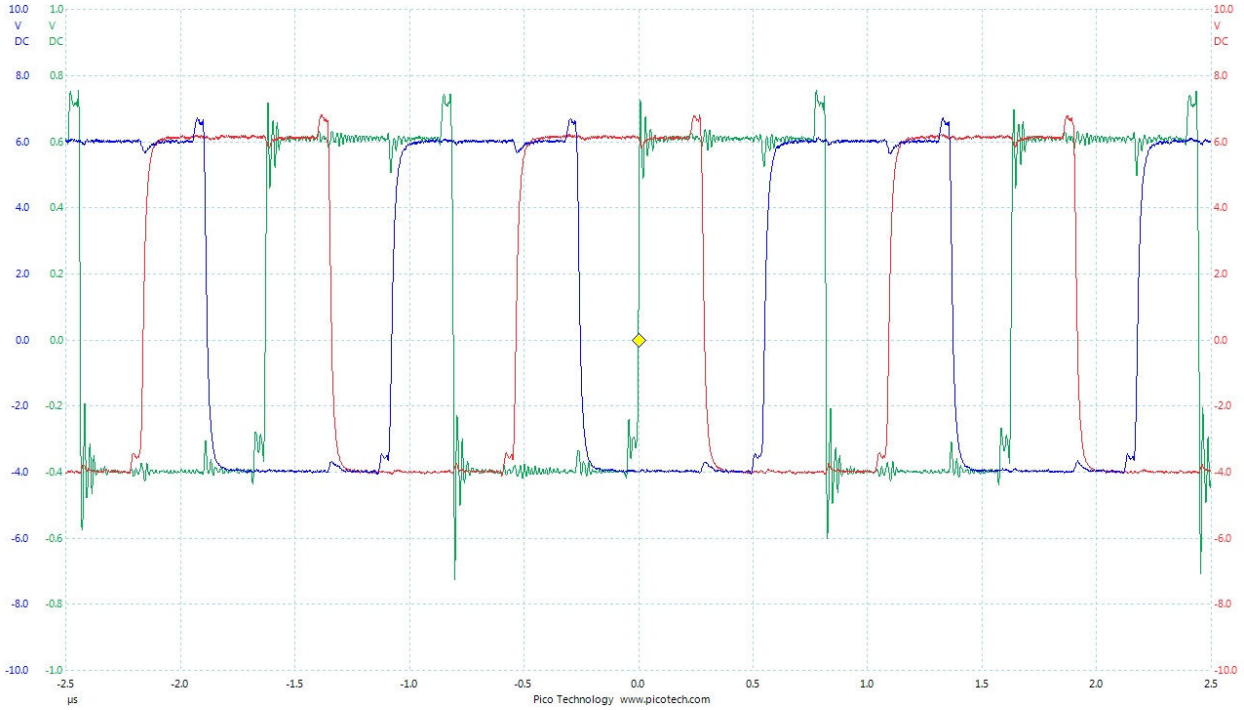

Figure 4: CCD1 RG

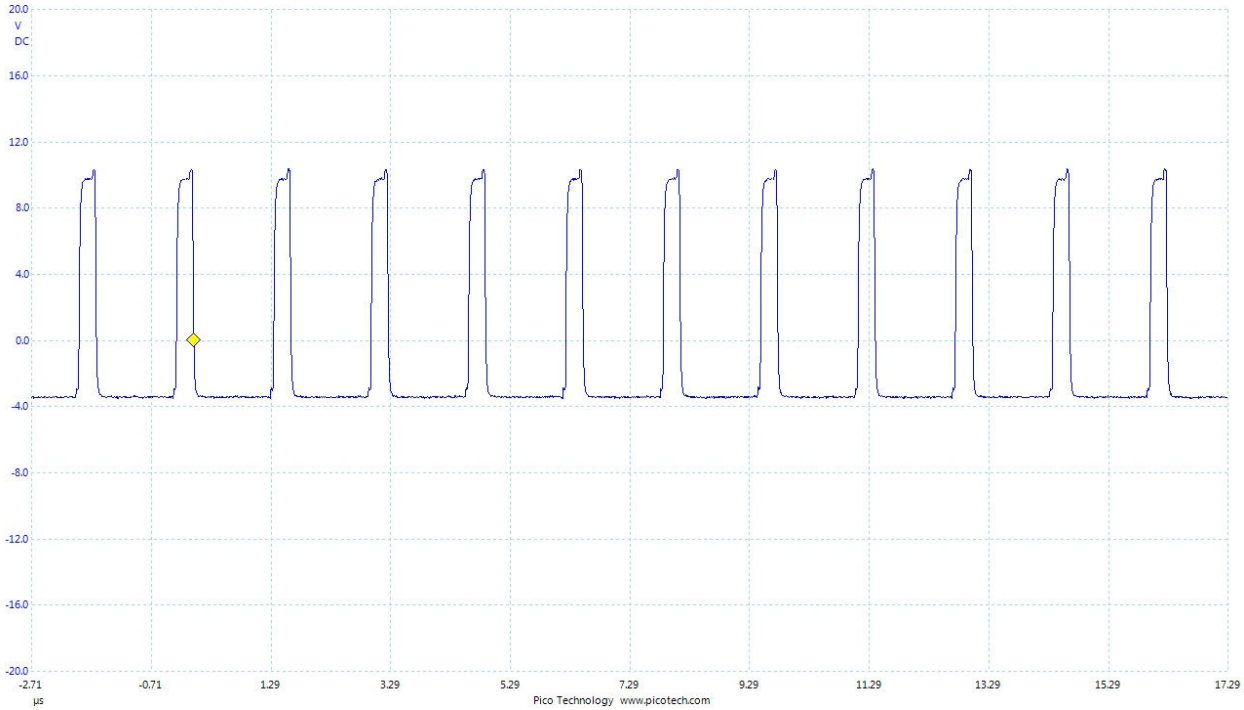

Figure 5: CCD2 FS

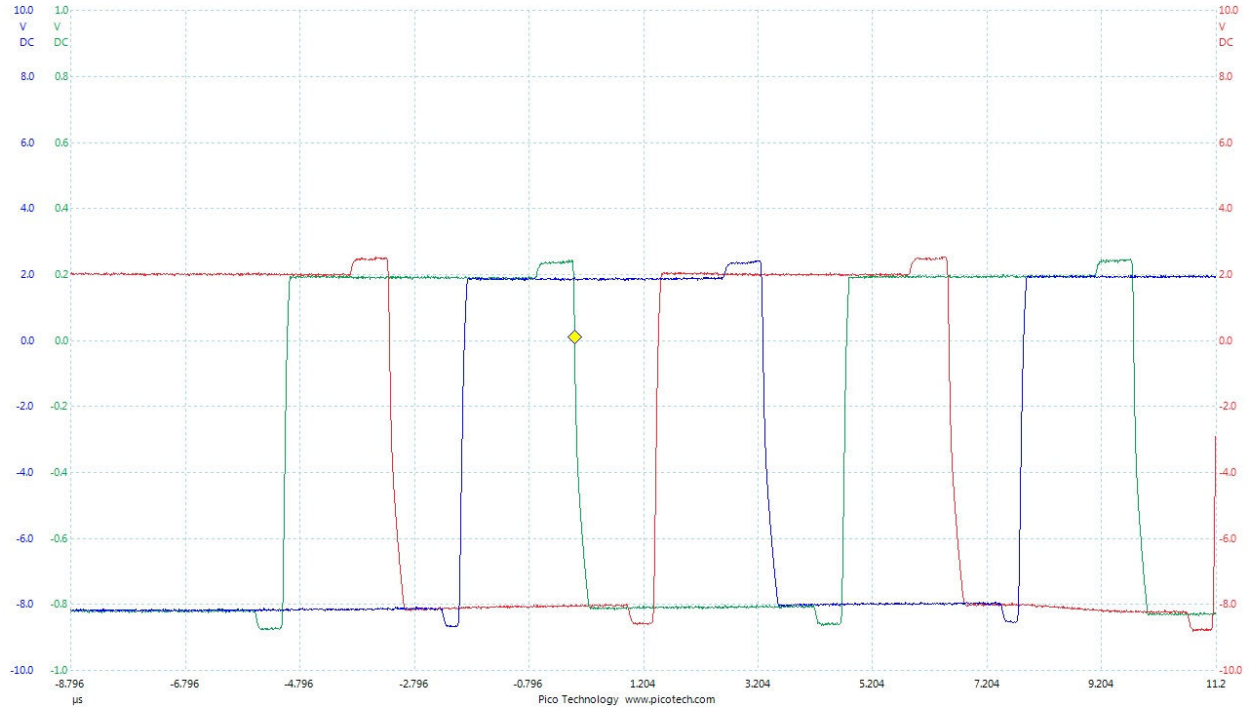

Figure 6: CCD2 IA

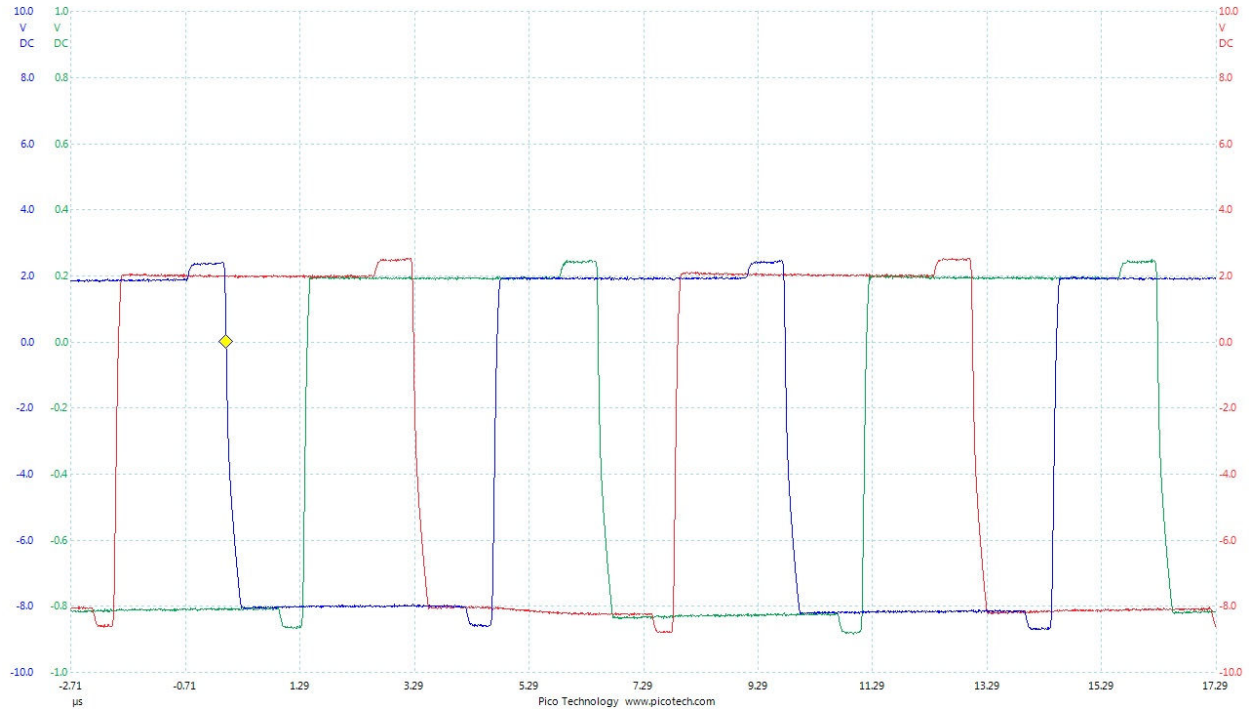

Figure 7: CCD2 OR

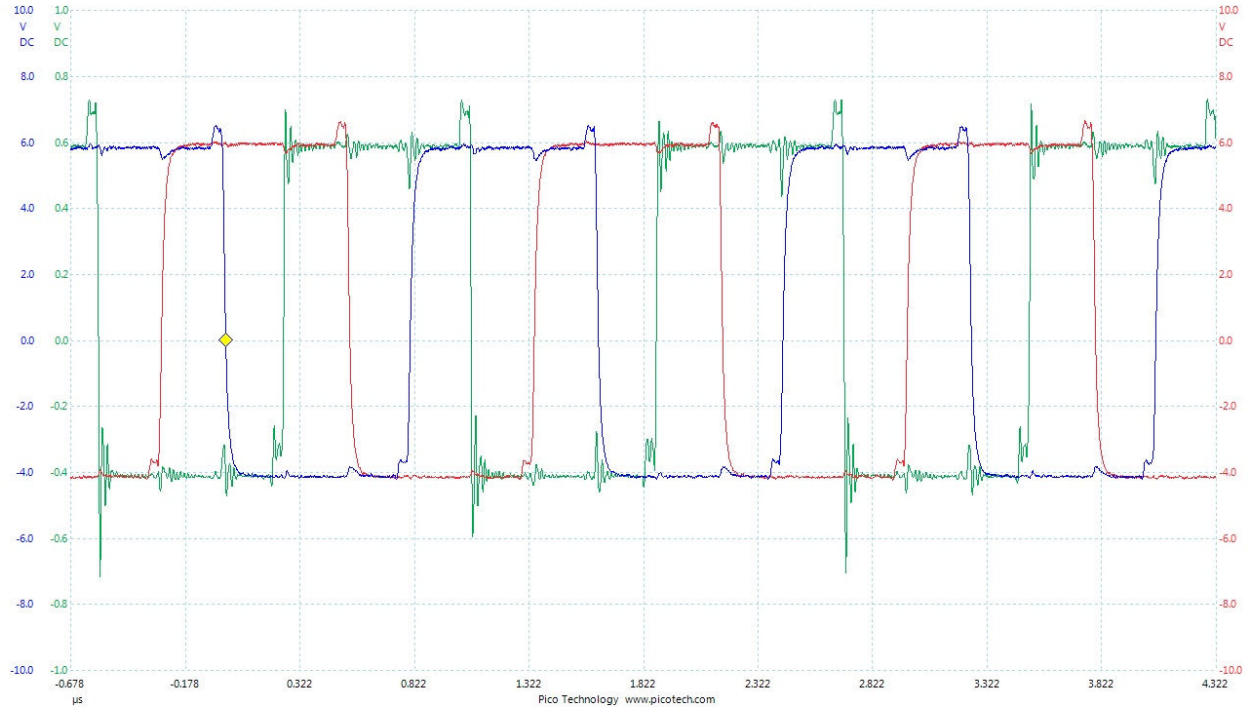

Figure 8: CCD2 RG

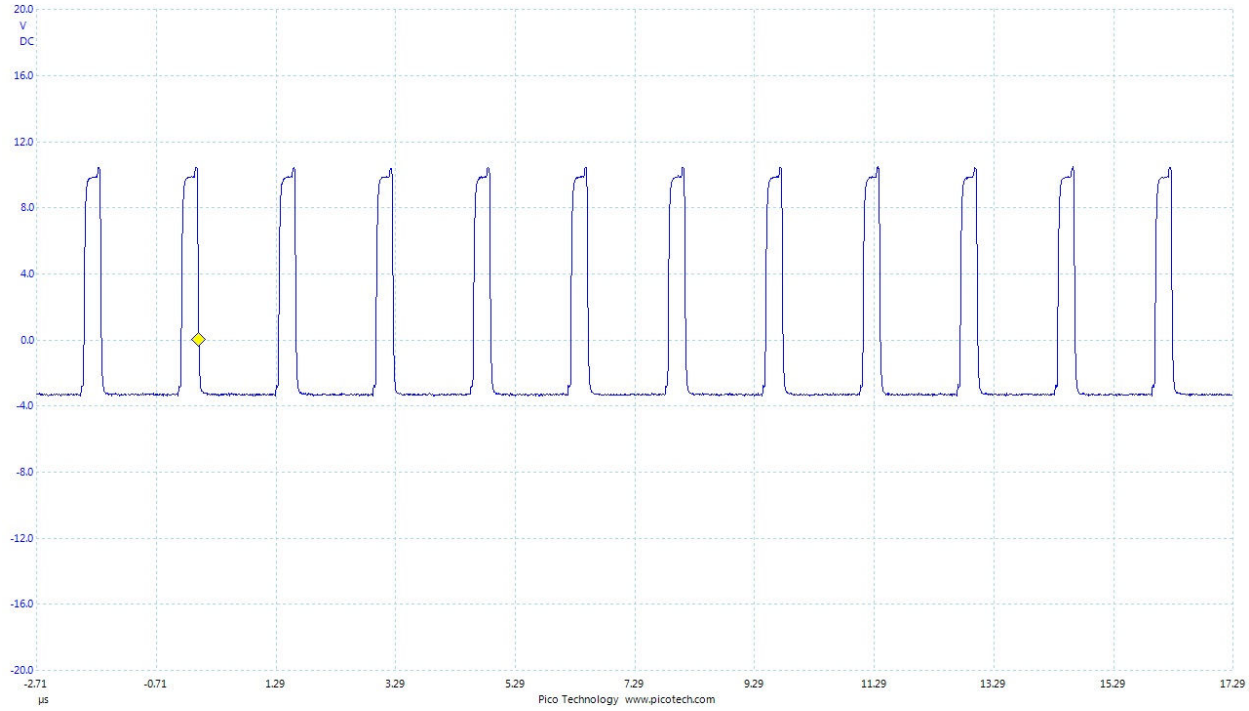

Figure 9: CCD3 FS

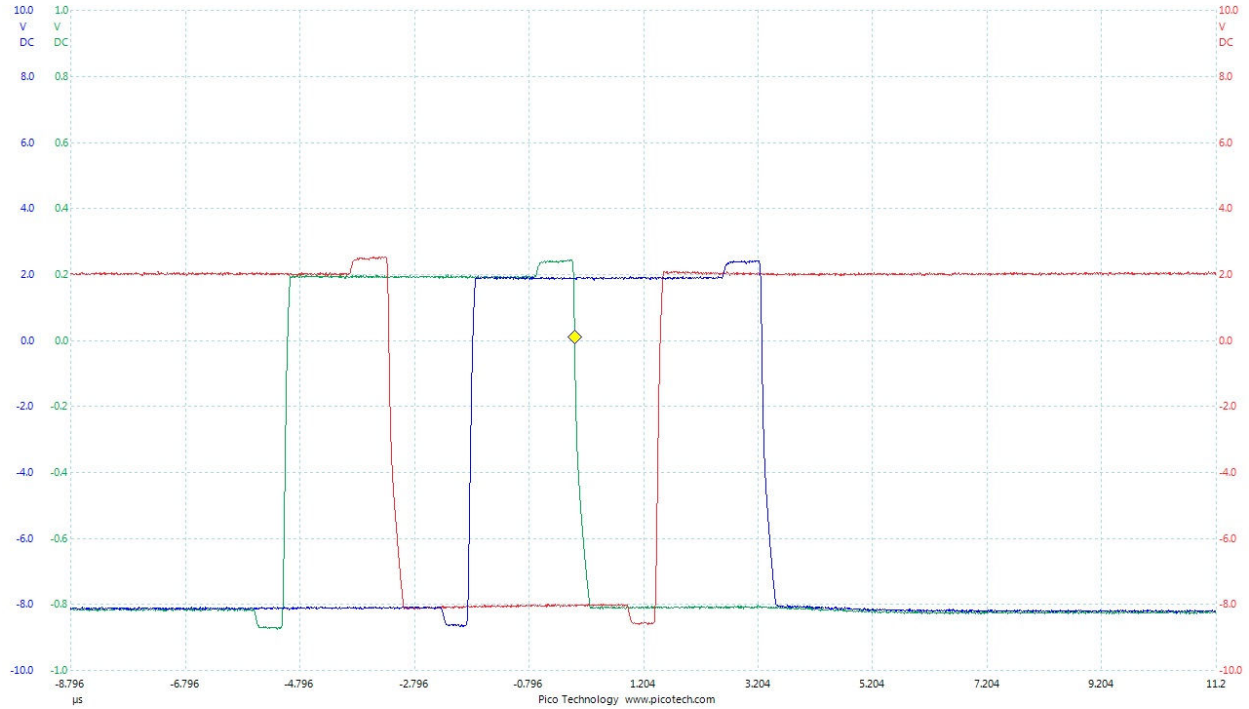

Figure 10: CCD3 IA

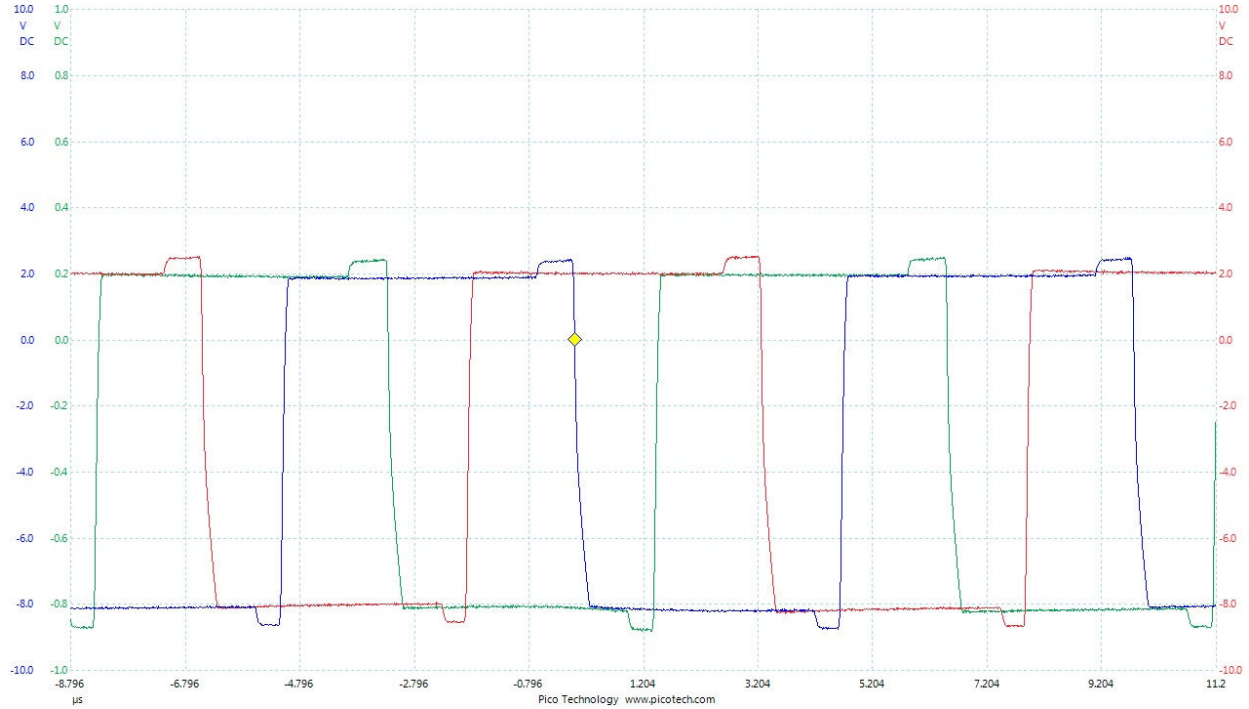

Figure 11: CCD3 0R

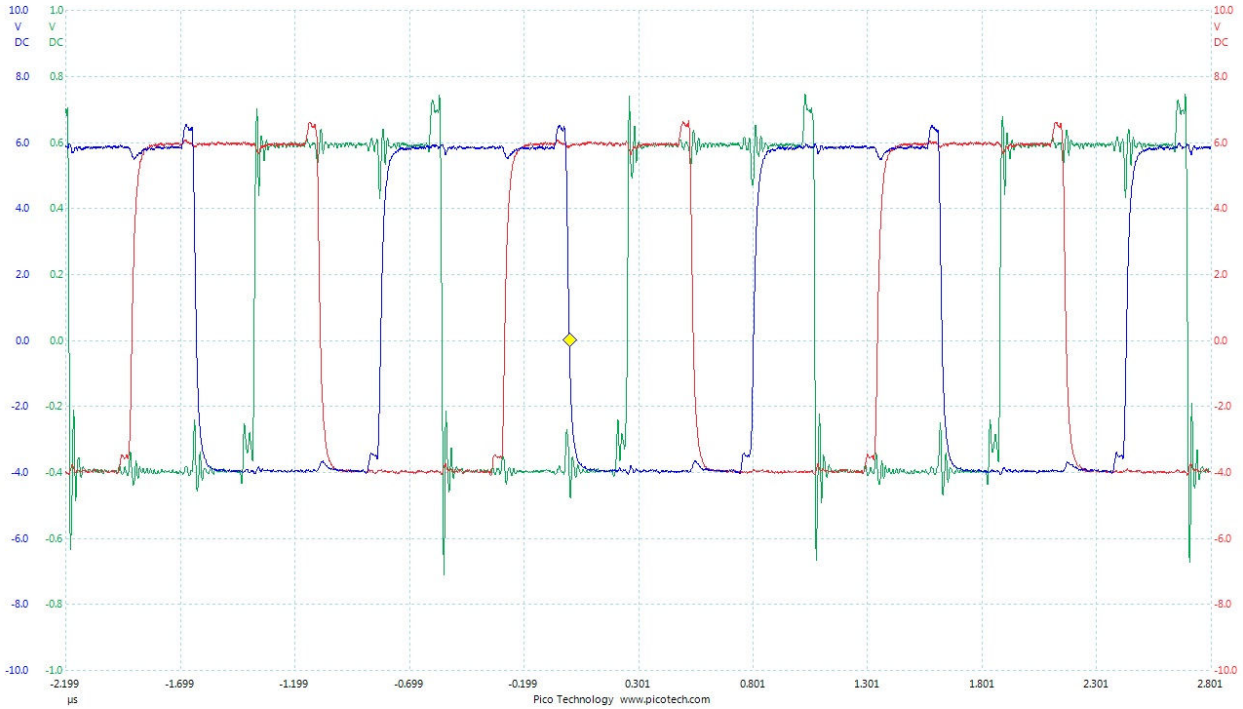

Figure 12: CCD3 RG

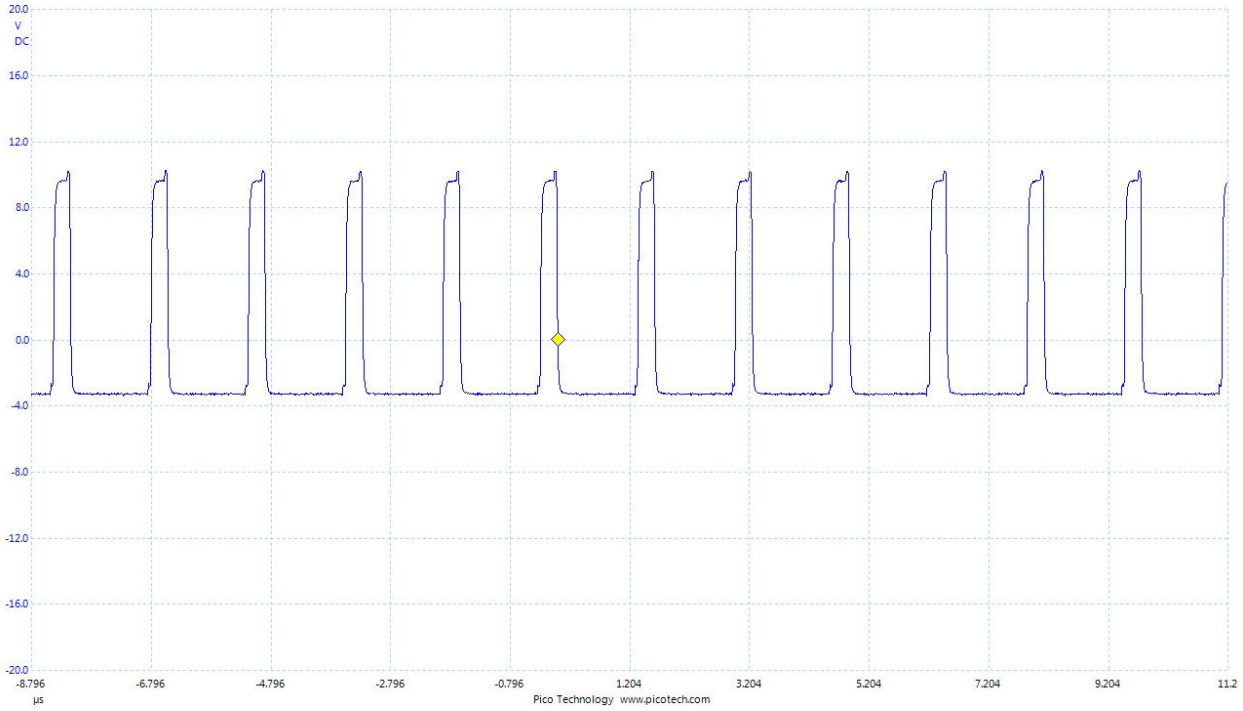

Figure 13: CCD4 FS

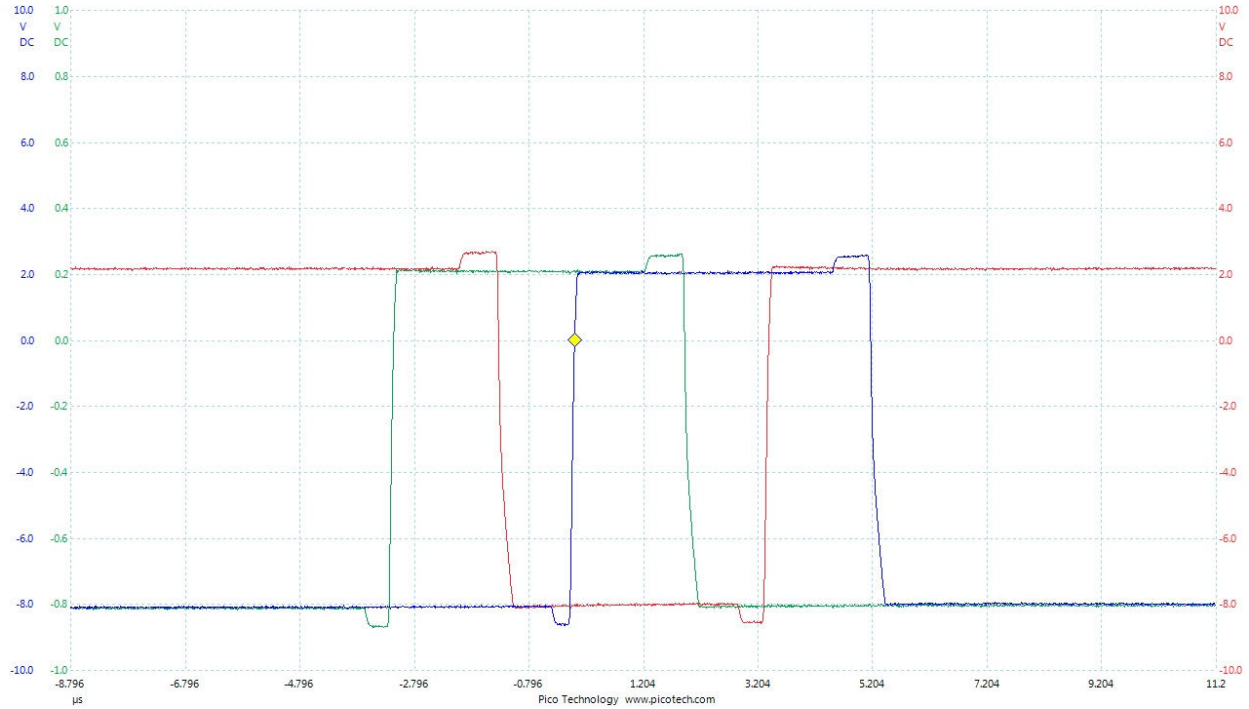

Figure 14: CCD4 IA

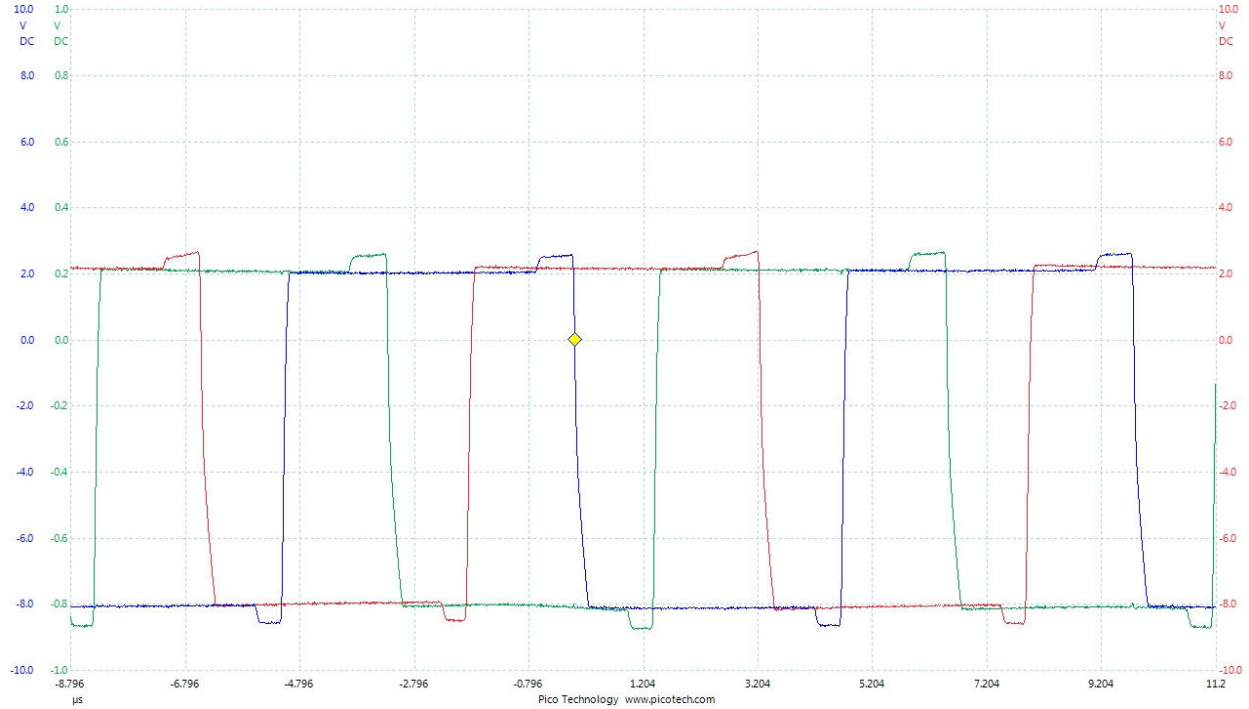

Figure 15: CCD4 OR

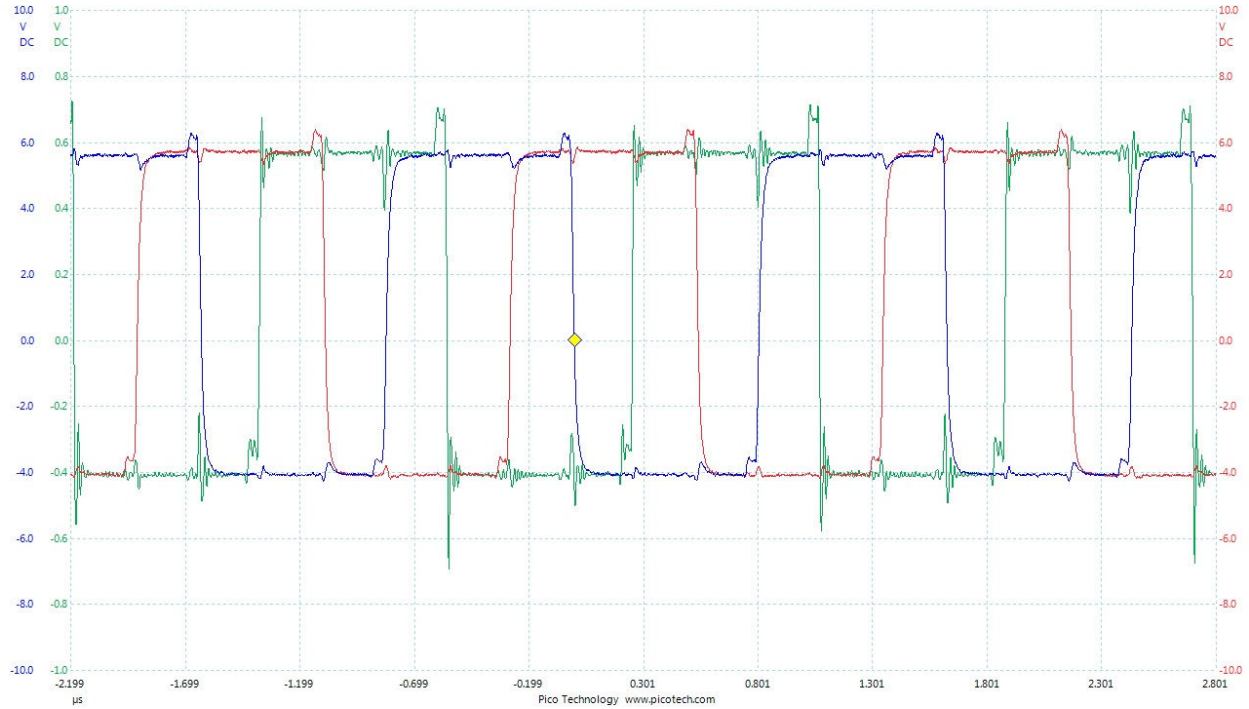

Figure 16: CCD4 RG