The comparator with the positive feedback resistor is a Schmitt trigger and the hysteresis is caused by the positive feedback signal V_f

$$V_f = \frac{R_{eqv}}{R_f + R_{eqv}} V_{cout} \quad (1)$$

where R_{eqv} is the equivalent resistance in the positive input of the comparator. We suppose that at the initial state the output of the comparator is high and the heating resistor begins to heat the chip. As a result, the temperature of the chip increases and V_1 will decrease until the output of the comparator switches low. Then the chip temperature will decrease owing to the heating exchange with the fluid until the output of the comparator is high again. The cycle is repeated. The waveforms of the sensor are depicted in Fig. 2. Because of the hysteresis and the very high gain of the comparator, the output is a square wave and the oscillation of the chip temperature is approximately a triangle wave. In the experiments the temperature oscillation amplitude ($T_h - T_l$) was chosen to be about 1 K, therefore the average chip temperature $T_{ave} = \frac{1}{2}(T_h + T_l)$ is almost constant.

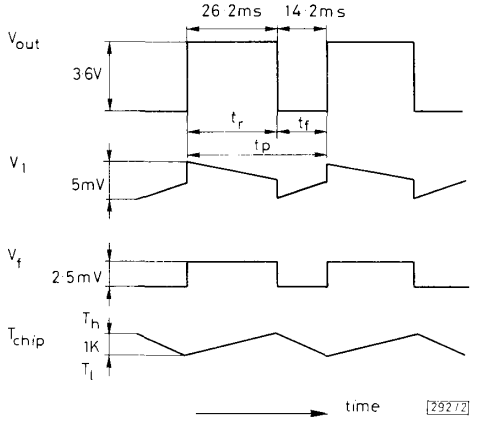

Fig. 2 *Waveforms of the sensor*
($U = 2$ m/s)

The average heating power can therefore be written as

$$P_{ave} = P_{max} \frac{t_r}{t_p} = AC(T_{ave} - T_f)(U)^{1/2} \quad (2)$$

where P_{ave} is the average heating power, P_{max} is the maximum heating when the output of the comparator is at high level, t_r/t_p is the duty cycle, A is the area of the heated surface and C is a constant depending on the size of the chip and several flow parameters.

Therefore, we can conclude from eqn. 2 that the duty cycle is proportional to the heating power and therefore to the square root of the flow velocity for a laminar flow. The duty cycle output is an accurate and well-defined measurement result. Moreover, it can be delivered to a microprocessor directly.[5] The measuring time can be reduced to one period time, which may be in the order of tens of milliseconds.

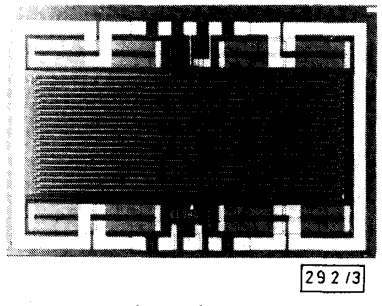

Fig. 3 *Integrated circuit layout*

Experiments: The sensor chip is mounted on a ceramic substrate carrying a gold interconnection pattern. This assembly is mounted upside-down in a printed circuit board which is placed in the mouth of a small wind tunnel. A photograph of the sensor chip is shown in Fig. 3. It contains a diode, a heating resistor and a Seebeck sensor (the Seebeck sensor is not used in our configuration). The experimental results are depicted in Fig. 4. The average sensitivity is 13·5%/(m/s) in

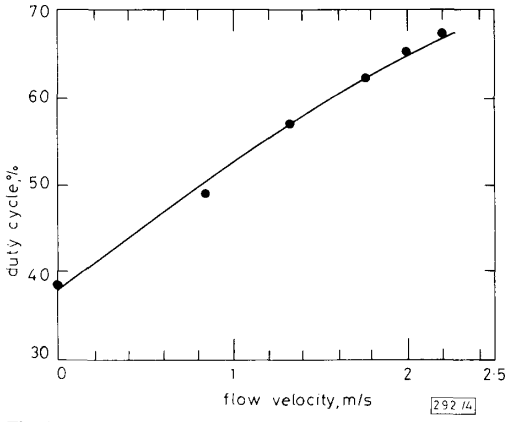

Fig. 4 *Duty cycle as a function of flow velocity*

the range 0–2 m/s. Further work will concentrate on integrating all of the external elements on a single chip, leading to a so-called 'smart sensor'.

Y. PAN
J. H. HUIJSING

Electronic Instrumentation Laboratory
Dept. of Electrical Engineering
Delft University of Technology
Mekelweg 4, 2628CD Delft, The Netherlands

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NEW METHOD FOR THE EXTRACTION OF MOSFET PARAMETERS

Indexing terms: Semiconductor devices and materials, Semiconductor devices and materials testing, Field-effect transistors

A new method for the extraction of the MOSFET parameters is presented. The method, which relies on combining drain current and transconductance transfer characteristics, enables reliable values of the threshold voltage V_t, the low field mobility μ_0 and the mobility attenuation coefficient θ to be obtained.

Introduction: In recent years, different methods for the extraction of MOSFET parameters have been proposed.[1–6] These methods are based primarily on the premise that the threshold voltage V_t can be obtained by extrapolating the linear region of the transfer characteristics $I_d(V_g)$ to zero drain current. In an alternative approach, Chu Hao *et al.*[5] proposed a method in which this limitation was bypassed by extracting the threshold voltage from the transconductance characteristics $g_m(V_g)$.

In this case, the extracted threshold voltage was found to be roughly equal to the gate voltage at which the transconductance was maximum. In addition, the low field mobility parameter μ_0 was taken to be equal to the maximum field effect mobility.

This letter presents a new method for the extraction of MOSFET parameters based on the combined exploitation of the $I_d(V_g)$ and $g_m(V_g)$ characteristics. In this way, it is possible to avoid the effects of mobility reduction with gate voltage on the determination both of the threshold voltage and of the low field mobility parameter.

Principle of the method: The MOSFET parameter extraction is conducted, as is usual, within the strong inversion regime of the MOSFET linear region and, therefore, relies on the following well known drain current expression:

$$I_d = \frac{WC_{ox}}{L} \frac{\mu_0}{[(1 + \theta(V_g - V_t)]} \cdot (V_g - V_t) \cdot V_d \qquad (1)$$

where W and L are the effective channel width and length, C_{ox} is the gate oxide capacitance, μ_0 is the low field mobility, θ is the mobility reduction coefficient, V_t is the charge threshold voltage[7] and V_g and V_d are the gate and drain voltages respectively.

It is worth noting that the charge threshold voltage V_t is not to be confused with the extrapolated threshold voltage V_{text}. As a result, when the mobility reduction factor θ is not equal to zero, V_{text} becomes smaller than the charge threshold voltage V_t.[7] V_{text} is strictly equal to V_t only when the mobility is gate voltage independent. In this case, the threshold voltage V_t is determined from the linear variation of the inversion charge with gate voltage.

The transconductance g_m of the MOSFET is readily obtained by differentiation from eqn. 1 as

$$g_m = \frac{W}{L} C_{ox} \frac{\mu_0}{[1 + \theta(V_g - V_t)]^2} V_d \qquad (2)$$

The basic idea of our method consists in constructing a function, through a proper combination of eqns. 1 and 2, which eliminates the influence of the mobility attenuation with gate voltage. This can readily be achieved by dividing the current expression by the square root of the transconductance:

$$\frac{I_d}{g_m^{1/2}} = \left(\frac{W}{L} C_{ox} \mu_0 V_d\right)^{1/2} (V_g - V_t) \qquad (3)$$

It is clear from eqn. 3 that in strong inversion, the quantity $I_d/g_m^{1/2}$ should be linear in gate voltage with intercept and slope giving the charge threshold voltage V_t and the low field mobility parameter μ_0 (when W, L and C_{ox} are known), respectively.

It is worth emphasising that the present method allows a separate determination of the threshold voltage V_t and the mobility μ_0 which is not the case in previous works.[1–6] With our method, the value of V_t is not needed *a priori* to deduce the value of μ_0 or vice versa.

Now, knowing the threshold voltage V_t enables the determination of the mobility reduction factor θ. To do this, we combine eqns. 1 and 2 in such a way as to eliminate the prefactor $WC_{ox}\mu_0/L$ obtaining

$$\theta = [I_d/(g_m \cdot (V_g - V_t)) - 1]/(V_g - V_t) \qquad (4)$$

In strong inversion, this function is expected to be a constant equal to the value of the mobility reduction coefficient θ. It is to be noted that the values of θ appearing in eqns. 1 and 2 and given by eqn. 4 are effective mobility reduction coefficients that include the effects of the source/drain series resistance R_{sd}: $\theta = \theta_0 + R_{sd} C_{ox} \mu_0 W/L$ (θ_0 being the intrinsic mobility reduction factor).[8] The corrected value, θ_0, can thus be deduced if the series resistance R_{sd} is separately measured, using for instance the method of Reference 5.

In addition, as in Reference 5, the effective channel length L can be obtained from the plot of the inverse of the transconductance parameter ($G_m = WC_{ox}\mu_0/L$) as a function of gate length. In our method, G_m can be directly deduced from eqn. 3 from the slope of the $I_d/g_m^{1/2}(V_g)$ characteristics rather than from the maximum experimental transconductance (as in Reference 5) which is always smaller than $G_m V_d$.[7] In the same way, the source/drain series resistance R_{sd} can be assessed by plotting the inverse of the MOSFET conductance as a function of G_m^{-1}.[5]

Results: The above method of parameter extraction has been tested on *n*-channel MOSFETs fabricated at the Naval Research Laboratory with a technology providing a gate oxide thickness of 22 nm and a surface channel doping of about $10^{16}\,cm^{-3}$. The gate width of the devices is about 100 μm and the channel lengths range over 2–7 μm. The electrical measurements were performed using a computerised HP 4145B system.

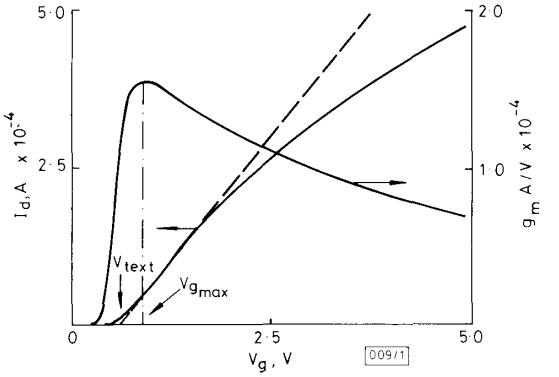

Fig. 1 *Typical drain current $I_d(V_g)$ and transconductance $g_m(V_g)$ MOSFET characteristics*
$L = 5\,\mu m$ $V_d = 50\,mV$

Fig. 1 shows typical plots of the transfer characteristics $I_d(V_g)$ and $g_m(V_g)$. Note the sublinear dependence of the drain current above threshold owing to the decrease of the mobility (or transconductance) at high gate voltages.

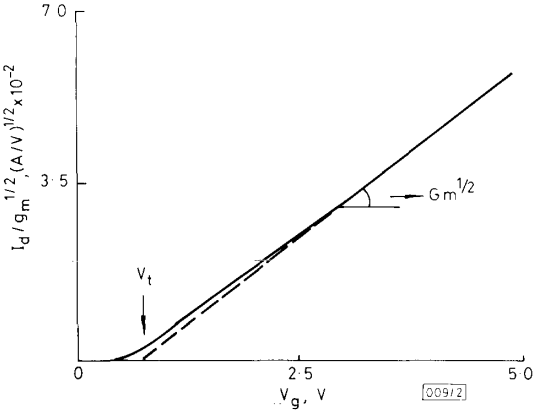

Fig. 2 *Typical $I_d/g_m^{1/2}(V_g)$ MOSFET characteristic illustrating the parameter extraction method*
$L = 5\,\mu m$ $V_d = 50\,mV$

Fig. 2 shows the corresponding plot of the $I_d/g_m^{1/2}(V_g)$ characteristics for the same gate voltage range. As expected from eqn. 3, a linear dependence with gate voltage is clearly observed at high gate voltages. The intercept of this straight line on the x-axis gives a charge threshold voltage: $V_t = 0{\cdot}71$ V. The low field mobility μ_0 deduced from the slope is in this case, equal to $515\,cm^2/Vs$. Note that, in contradiction to Reference 5, V_t is actually well below the gate voltage at which g_m is maximum ($V_{gmax} = 0{\cdot}95$ V) and also that μ_0 is greater than the maximum field effect mobility ($\mu_{FEmax} = 424\,cm^2/Vs$). Moreover, in agreement with Reference 7, the extrapolated threshold voltage, $V_{text} = 0{\cdot}57$ V, is found to be smaller than the charge threshold voltage V_t.

Likewise, the values of the mobility attenuation coefficients θ have been obtained by applying eqn. 4 to our data, giving a typical value of θ of $0{\cdot}16\,V^{-1}$ (see Fig. 3). Since for our devices, the series resistance R_{sd} is about $20\,\Omega$, an intrinsic attenuation coefficient θ_0 of $0{\cdot}11\,V^{-1}$ has been deduced. It is worth noting that, for a correct determination of V_t, μ_0 and θ, the linear regression extraction method has to be performed at high gate voltages to be in a sufficiently strong inversion region to avoid the proximity effects of the transconductance maximum region. This can be checked experimentally by the occurrence of a plateau in the $\theta(V_g)$ characteristics.

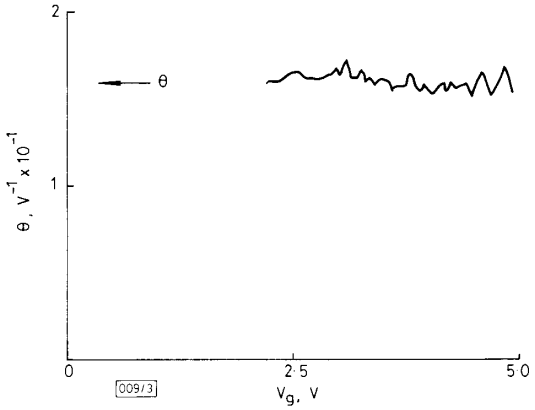

Fig. 3 *Typical variation of* $[I_d/(g_m \cdot (V_g - V_t)) - 1]/(V_g - V_t)$ *with gate voltage providing the value of* θ

$L = 5\,\mu m$ $V_d = 50\,mV$

Finally, it is to be mentioned that the method has also been successfully applied at liquid nitrogen temperatures, demonstrating thereby the validity of eqn. 1 for this temperature range.

Conclusion: A new and simple method for the extraction of the MOSFET parameters has been proposed. The method, based on the combined exploitation of the drain current and transconductance transfer characteristics, provides reliable values of the threshold voltage V_t, the low field mobility μ_0 and the mobility attenuation coefficient θ both for room and liquid nitrogen temperatures.

It is worthwhile to note that, because of its simplicity, the present extraction method can easily be implemented on semiconductor parameter analysers (such as the HP 4145B) where the drain current and the transconductance data are simultaneously available. Therefore, such a simple method should be very useful not only for MOSFET characterisations in research but also for the control of fabrication in semiconductor production lines.

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G. GHIBAUDO* *15th February 1988*

Sachs and Freeman Associates, Inc.
1401 McCormick Drive, Landover, MD 20785, USA

* Permanent address: Laboratoire de Physique des Composants a Semiconducteurs, UA-CNRS 840, ENSERG, 23 rue des Martyrs, 38031 Grenoble, France

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NEW INTEGRATED OPTIC SWITCH FOR CROSSBAR SWITCHING ARRAYS

Indexing terms: Integrated optics, Optical switching, Networks, Optical waveguide components

A new electro-optic switch is described which is insensitive to parameter tolerances and allows switching arrays with the same switching voltage for each element in the bar state and 0 V in the cross state, respectively. Measurements on a preliminary device are presented.

Optical switching becomes an attractive alternative to electronic switching when there is a high data rate and a low switching speed, e.g. local area networks (LANs).[1] To fabricate a switching matrix it is necessary that all switches have the same switching characteristics. A switching matrix with a strictly nonblocking crossbar structure, as shown in Fig. 1, is considered. With this matrix it is possible to switch the light from any input port a_i ($i = 1, n$) to any output port b_j ($j = 1, n$) via the crosspoint S_{ij}.

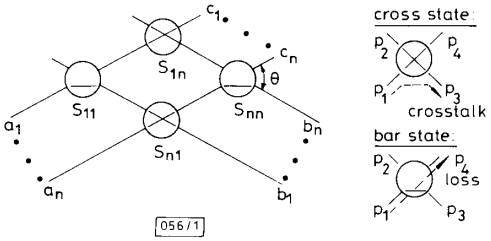

Fig. 1 *$n \times n$ crossbar switching matrix with both switching states*

It is thus desirable to design a switch which is in the cross state if it is not activated (corresponding to zero voltage at the respective switch). For switching from an input port a_i to an output port b_j it is then necessary to activate only the switch S_{ij} by applying a suitable voltage, so that the switch S_{ij} is driven into the bar state.

It is important to note that the bar state need not be perfect, since light which leaves the switch at the wrong output port only contributes to a light output at the port c_i which is not used. Therefore, an imperfect bar state does not yield crosstalk, but only some loss, since then not all incoming light from the port a_i appears at port b_j.

We thus require an electro-optic switch with low crosstalk ($< -30\,dB$) in the cross state, which should be achieved for zero voltage, whereas the crosstalk in the bar state is not critical.[2]

Following these guidelines a switch is designed as shown in Fig. 2. It consists of two intersecting waveguides 1 and 2. The waveguides 1 and 2 are tapered at the intersection point, to achieve low crosstalk. The crosstalk contribution from the intersection point alone has been measured to be lower than $-31\,dB$ for a taper width $W = 22{\cdot}5\,\mu m$ and a crossing angle $\theta = 6°$.