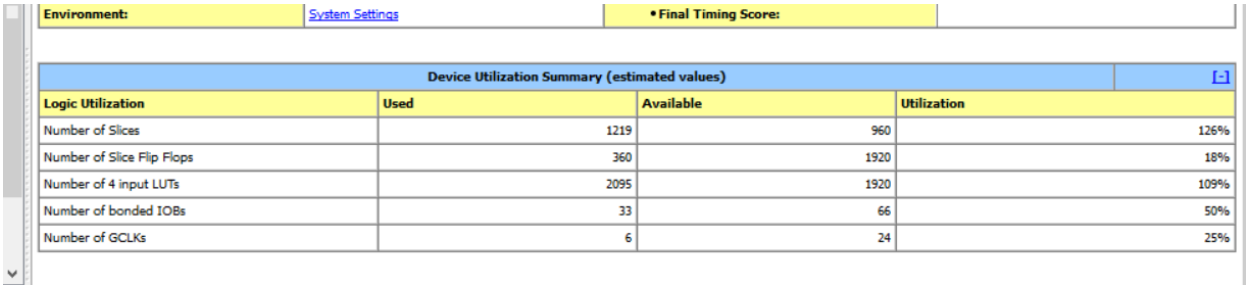
CHAPTER 9

XILINX SYNTHESIS REPORT

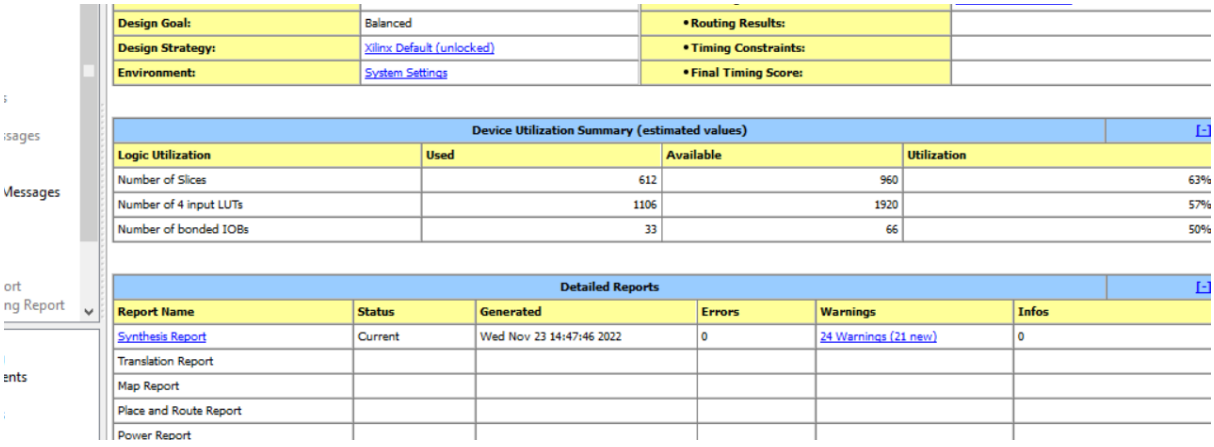
Existing system:



Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1219	960	126%
Number of Slice Flip Flops	360	1920	18%
Number of 4 input LUTs	2095	1920	109%
Number of bonded IOBs	33	66	50%
Number of GCLKs	6	24	25%

Proposed System:



Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	612	960	63%
Number of 4 input LUTs	1106	1920	57%
Number of bonded IOBs	33	66	50%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed Nov 23 14:47:46 2022	0	24 Warnings (21 new)	0
Translation Report					
Map Report					
Place and Route Report					
Power Report					

The proposed has been simulated and the synthesis report can be obtained by using Xilinx ISE 12.1i. The various parameters used for computing existing and proposed systems with Spartan-3 processor are given in the table.

Table:1

s.no	Parameter	Existing	Proposed
1	Slice	1219	2095
2	LUT	612	1106