ABSTRACT

Multi-digit multiplication is widely used for various applications in recent years, including numerical calculation, chaos arithmetic, primality testing. Systems with high performance and low energy consumption are demanded, especially for image processing and communications with cryptography using chaos. In this project,hardware design of multi-digit multiplication is described, and its VLSI realisation is evaluated in terms of the cost and performance. A configurable Karatsuba multiplier is proposed for low power application. The results obtained by this study will help system designers for applications requiring multi-digit multiplication to select design alternatives including ASIC realisation. Multiplications are very expensive and slows the over all operation. Theperformance of many computational problems are often dominated by the speed at which a multiplication operation can be executed. In this project, a low-error and area-efficient fixed-width Karatsuba multiplier is presented. As compared with the state-of-the-art design, the proposed fixed-width multiplier performs not only with lower compensation error but also with lower hardware complexity, especially as multiplier input bits increase.