THARAN S M

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Executive Summary

I am a motivated and dedicated Electronics and Communication Engineering student with a strong academic foundation in Digital Electronics, Analog Communication, and Semiconductor fundamentals. I am developing my expertise in VLSI and chip design with hands-on knowledge of Verilog HDL, Digital System Design, and EDA tools. I possess strong analytical thinking, problem-solving skills, and a disciplined work ethic. I am seeking opportunities in the semiconductor industry where I can apply my technical knowledge, contribute to high-performance design environments, and grow as a hardware engineer.

Education

2027 B.E ECE at **SRM Valliammai Engineering College** CGPA: 8.945
2023 HSC **Shree Niketan Matric Hr. Sec School** Percentage: 90

PROJECTS

16-Bit Multicycle Processor with Adaptive ALU and Booth MAC Unit Jan 2026-Present

Developed a 16-bit multi-cycle RISC processor with Adaptive ALU and Radix-4 Booth MAC unit in Verilog HDL. Implemented a five-stage FSM control unit with clock gating to minimize dynamic power dissipation. Realized a maximum of 40% power saving through operand-based ALU optimization and minimized partial product generation in the multiplication process. Tested the design using testbenches and synthesized at 25 MHz.

Low-Power Clock Gating Implementation in Sequential Circuits Nov 2025-Dec 2025

- Implemented clock gating methods in sequential digital circuits using Verilog HDL to minimize unnecessary switching transitions and dynamic power dissipation.
- Developed gated clock logic for flip-flop and register modules to disable clock signals during idle periods while ensuring functional correctness.
- Conducted functional verification using structured testbenches and analyzed switching activity through simulation-based comparison, verifying the effectiveness of dynamic power reduction.

SKILLS

Languages & Scripting

- Verilog HDL
- Python
- C Programming
- Tcl Scripting
- Linux (CLI & Shell)

EDA Tools

- Cadence Virtuoso
- Xilinx Vivado

CERTIFICATIONS

- **VLSI For Beginners** – National Institute of Electronics & Information Technology (NIELIT), July 2025
- **VLSI Design and Verification: Integrating Analog and Digital Systems with Vivado and Cadence** – SRM Valliammai Engineering College (VAC), April 2025