Table1: 16 bit hybrid adders with enable

Adder Name	**Dynamic power** (W)	**Static power (W)**	**Total Power (W)**	**Delay (ns)**	**Power delay product** (W.ns)	**Slice logic**	**LUT logic**
LING+BKA	7.131	0.105	7.236	14.120	102.172	9	30
LING+KSA	7.217	0.106	7.323	13.639	99.8783	12	38
BKA+SKSA	7.204	0.106	7.31	13.974	102.1499	12	36
LING+SKSA (Proposed)	**7.131**	**0.105**	**7.236**	**13.423**	**97.1288**	**9**	**30**

Table2: 32 bit hybrid adders with enable

Adder Name	**Total Power (W)**	**Delay (ns)**	**Power delay product**	**Slice logic**	**LUT logic**
LING+BKA	14.878	22.121	329.116	26	72
LING+KSA	15.225	21.822	332.239	30	95
BKA+SKSA	14.764	24.430	360.684	26	71
LING+KSA+KSA SKSA	14.791	22.412	331.495	21	70
LING8+SKSA8+ LING8+SKSA8	14.795	26.431	391.046	26	72
LING+SKSA (Proposed)	**15.095**	**20.807**	**314.081**	**31**	**80**