32 bit adders

Type	Adder Name	Total Power (W)	Delay (ns)	Power delay product	Slice logic	LUT logic
Conventional Adders	BKA	22.991	22.469	516.584	24	64
	KSA	24.034	17.409	418.407	41	134
	LING	22.742	25.407	577.805	23	55
	SKSA	**22.744**	**24.585**	**559.161**	**23**	**55**
Hybrid Adders	LING+BKA	14.878	22.121	329.116	26	72
	LING+KSA	15.225	21.822	332.239	30	95
	BKA+SKSA	14.764	24.430	360.684	26	71
	LING+KSA+ KSA SKSA	14.791	22.412	331.495	21	70
	LING8+SKSA8+ LING8+SKSA8	14.795	26.431	391.046	26	72
	LING+SKSA (Proposed)	**15.095**	**20.807**	**314.081**	**31**	**80**
	LING+SKSA _withclk out reg	21.085	16.045	338.308	47	48 reg:67
	LING+SKSA _withclk with XDC	0.078	15.221	1.187	34	48 reg:67
	SIGNED LING+SKSA _withclk with XDC	0.078	16.113	1.256	41	58 reg:66

MULTIPLIER 16

Type	MULTIPLIER	Total Power (W)	Delay (ns)	Power Delay Product	Slice Logic	LUT logic
Conventional multipliers	Dadda	37.424	25.773	964.528	102	350
	Karatsuba	34.168	21.154	722.789	149	465
	Wallace	39.189	23.546	922.744	110	387
	Vedic	32.122	19.527	627.246	109	334
Hybrid multipliers	Hybrid multiplier Parallel addition with all 4 adders	33.827	25.573	865.057	183	644
	Hybrid multiplier Serial addition with all 4 adders	13.898	42.897	596.182	231	778
	Hybrid multiplier 4 chain tree addition with all 4 adders	13.355	29.783	397.751	216	743
	Hybrid multiplier 4 chain tree addition with LKSA	13.118	28.400	372.551	228	774
	Hybrid multiplier 4 chain tree addition with LBKA	32.572	25.490	830.260	156	543
	Hybrid multiplier 2 chain tree addition with all	13.555	31.761	430.520	224	780
	Hyd_4chain_LSKSA (Proposed)	**12.073**	**30.375**	**366.717**	**158**	**529**
	Hyd_4chain_LSKSA_withclk Signed (pp clk)	36.58	10.470	382.992	184 memory: 18	422 reg:833
	Hyd_4chain_LSKSA_withclk Signed (pp no clk)	37.447	12.907	483.328	195 memory: 18	543 reg:580
	Hyd_4chain_LSKSA_withclk Signed (pp clk) with XDC	0.084	5.391		185 memory: 18	423 reg:833

16bit i/p 16 tap lowpass FIR FILTER

Type	Lowpass FIR Filter 16tap	Tot Power (w)	Delay (ns)	Power Delay Product	Slice logic	LUT logic	Slice Register
Without timing constraints	Fir Direct arithmetic	36.929	35.436	1308.616	78	104	234
	Fir_parallel_addition	26.076	30.127	785.591	269	883	265
	Fir_serial_addition	23.806	38.870	925.339	285	970	267
	Fir_tree_addition	23.316	31.102	725.174	279	913	265
	Enhanced FIR filter tree addition	**5.975**	**30.928**	**184.794**	**267**	**903**	**265**
With timing constraints	FIR Direct arithmetic with timing constraints 28.571 MHz (35ns period)	0.081	33.177	2.687	75	104	234
	Enhanced FIR filter With timing constraints 33.333 MHz (30nsperiod)	**0.075**	**22.065**	**1.654**	**201**	**921**	**265**