Conclusion table

Component	Metric	Conventional Design	Proposed Hybrid Design Improvement
16- bit adders	Power Consumption	Ling adder	25.79% reduction
	Delay	Ling adder	6.797% reduction
	Power delay product	Ling adder	30.836% reduction
32-bit Adder	Power Consumption	Ling adder	33.63% reduction
	Delay	Ling adder	18.6% reduction
	Power delay product	Ling adder	45.64% reduction
	Power Consumption	Sparse Kogge–Stone adder	33.63% reduction
	Delay	Sparse Kogge–Stone adder	15.36% reduction
	Power delay product	Sparse Kogge–Stone adder	43.82% reduction
16-bit Multiplier	Power Consumption	Vedic Multiplier	62.415% reduction
	Power delay product	Vedic Multiplier	41.535% reduction
	Power Consumption	Wallace Tree Multiplier	69.192% reduction
	Power delay product	Wallace Tree Multiplier	60.257%
16-bit 16 tap FIR Filter	Power Consumption	FIR_Arithmetic Operators	83.82% reduction
	Delay	FIR_Arithmetic Operators	12.721% reduction
	Power-Delay Product (PDP)	FIR_Arithmetic Operators	85.87% reduction