MAKAUT ODD SEMESTER PRACTICAL EXAMINATION, 2020-21
ACADEMY OF TECHNOLOGY

Subject: Analog and Digital Electronics Laboratory **Subject Code: ESC 391**
Discipline: CSE/IT **Full Marks: 60**

Time: 3 Hours (Execution time: 45 minutes)

Marks Distribution

Execution--20
Lab copy--20 (Logical expression + Circuit Diagram + Experimental Table+ Conclusion)
Viva--20

Questions:

1. Simplify the given expression using K-Map and implement the minimized form using only NOR gates : $F(A, B, C, D) = \sum(0,2,3,4,8,12) + d(1,14,15)$.
2. Simplify the given expression using K-Map and implement the minimized form using only NOR gates : $F(A, B, C, D) = \sum(0,1,2,3,4,6,9,11) + d(5,7,8, 10)$.
3. Simplify the given expression using K-Map and implement the minimized form using only NAND gates : $F(A, B, C, D) = \sum(1,2,5,9,13) + d(6,14,15)$.
4. Simplify the given expression using K-Map and implement the minimized form using only NAND gates: $F(A, B, C) = \sum(3,6,7)$.
5. Simplify the given expression using K-Map and implement the minimized form using only NAND gates : $F(A, B, C) = \sum(3,4,7) + d(5,6)$.
6. Simplify the given expression using K-Map and implement the minimized form using only NOR gates : $F(A, B, C,D) = \Pi(0,4,8,12,13,14,15)$.
7. Simplify the given expression using K-Map and implement the minimized form using universal gate : $F(A, B, C,D) = \Pi(1, 4,6,11,12) + d(3,8,9,14)$.
8. Simplify the given expression using K-Map and implement the minimized form using only NAND gates : $F(A, B, C,D) = \sum(0,2,5,10,13,15) + d(7,8, 14)$.

9. Implement the function F= A + B using a 2x4 decoder with logic low outputs and required logic gates (if required).

10. Design an Half Adder using 2 x 4 decoder with active high output and required logic gates. Also verify the result with a Half Adder truth table.

11. Implement the function F= A' + B' using a 2x4 decoder with logic high outputs and required logic gates(if required).

12. Design an Full Adder using two 2 x 4 decoders with active low outputs and required logic gates with active high output and also verify the result with an Full Adder truth table.
13. Implement the function F= A + B using a 2x4 decoder with logic high outputs and required logic gates (if required). Explain the function of Enable input line of a decoder chip.
14. Design a Half Adder circuit using NAND gates only. Also verify the result with a Half Adder truth table.
15. Design a Full adder circuit using suitable logic gates and verify the result with a Half Adder truth table.
16. Design a Full Subtractor circuit using suitable logic gates and verify the result with a Half Adder truth table.

17. Implement the function using 4:1 MUX : Y (A, B, C) = ∑ m (1, 2, 5, 7)

18. Realize the function F (A, B, C) = ∑ m (1, 3, 4, 5, 7) using 4:1 MUX.

19. Implement the function F (A, B, C) = (A + B'). (A + B). (A' + C') using 4:1 MUX.

20. Implement XOR, OR gates using 4:1 MUX.

21. Realize the function F (A, B, C) = A´B+B´+BC´ using a 4:1 MUX and extra logic gate if necessary.
22. Design HALF-ADDER using 4:1 MUX.
23. Design a clocked S-R flip-flop using NAND gates only. Write the truth table of it mentioning forbidden inputs.
24. Design and verify the truth table of a J-K flip-flop using NAND gates.
25. Design and verify the truth table of a D flip-flop using NAND gates.
26. Design and verify the truth table of a D flip-flop using S-R flip-flop.
27. Design and verify the truth table of a T flip-flop using J-K flip-flop.
28. Design and verify the truth table of a D flip-flop using T flip-flop.
29. Design and verify the truth table of S-R latch using both NAND and NOR gate.
30. Design and verify a 2bit synchronous up counter using j-k flip flop.
31. Design and verify a 2bit synchronous counter using d flip flop.

32. Design and verify a 3bit synchronous up counter using t flip flop.

33. Design and verify a mod 6 asynchronous counter.

34. Design an Half Adder using 2 x 4 decoder with active low outputs and also verify the result with an Half Adder truth table.

35. Design and implement schmitt trigger circuit using Op-Amp (Use R_1 = 10kΩ, R_2 = 15kΩ and input frequency = 50Hz). Draw input output wave form and hence draw the hysteresis curve for the circuit. Use the following link for the experiment – http://vlabs.iitb.ac.in/bootcamp/labs/ic/exp10/exp/
36. Design the Astable Multivibrator Circuit using 555 Timer IC. Verify its output with the theoretical values. Calculate frequency and duty cycle of the output. Use R_a = 10 kΩ, R_b = 11.5 kΩ and C = 1μf. Use the following link for the experiment – http://vlabs.iitb.ac.in/bootcamp/labs/ic/exp9/exp/index.php
37. Design a Phase Shift Oscillator using Op-Amp. Draw input output wave form and and calculate phase shift. Use C = 0.1 μf and output frequency 500Hz. Use the following link for the experiment – http://vlabs.iitb.ac.in/bootcamp/labs/ic/exp6/exp
38. Design and implement schmitt trigger circuit using Op-Amp (Use R_1 = 10kΩ, R_2 = 12kΩ and input frequency = 60Hz). Draw input output wave form and hence draw the hysteresis curve for the circuit. Use the following link for the experiment – http://vlabs.iitb.ac.in/bootcamp/labs/ic/exp10/exp/
39. Design the Astable Multivibrator Circuit using 555 Timer IC. Verify its output with the theoretical values. Calculate frequency and duty cycle of the output. Use R_a = 10 kΩ, R_b = 13 kΩ and C = 1μf. Use the following link for the experiment – http://vlabs.iitb.ac.in/bootcamp/labs/ic/exp9/exp/index.php

40. Design a Phase Shift Oscillator using Op-Amp. Draw input output wave form and and calculate phase shift. Use C = 0.2 µf and output frequency 250 Hz. Use the following link for the experiment – http://vlabs.iitb.ac.in/bootcamp/labs/ic/exp6/exp
41. Design and verify a 2bit synchronous down counter using j-k flip flop.
42. Realize two inputs XOR gate and XNOR, gate using a 2x4 decoder with logic high outputs and required logic gates(if required).
43. Design and verify a 3bit asynchronous up counter.
44. Design and verify a 3bit asynchronous down counter.
45. Design and verify a MOD-4 synchronous up counter using D flip flop.
46. Design and verify a MOD-4 synchronous down counter using T flip flop.
47. Design and verify a MOD-4 synchronous up counter using T flip flop.
48. Design and verify a MOD-4 synchronous down counter using D flip flop.
49. Design and verify a MOD-5 asynchronous down counter.
50. Design and verify a MOD-5 asynchronous up counter.