The Technical Reference Manual for the Full-Spatial Median-Free-Liquid Photonic bit(s) Transfer Module 276,480-bit analog/digital Computer Processor Architecture.
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Draft number 1
Drafted by Dr. Thomas Catalano
<tomcatalano@outlook.com>
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This working draft will outline the full-spatial 276,480-bit computer processor architecture with the newly
designed median-free-liquid via photonic bit transfer module processor computer system from design, engineering and programming.
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Diversity:
As we continued into the 21st century yearning for seamless interconnectivity and quasi-operational machines new designs were needed. One such designed utility was invented and engineered by Dr. Thomas Catalano in AD 2014, the Full-Spatial median-free-liquid photonic bit(s) transfer module 276,480-bit analog/digital computational processor/computer so to the design,
engineering and guidelines to coherently run arbitrary instruction sets to the architecture and system.
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Design:
A core processing unit runs single and/or overlayed data stream(s) as RGB color spectrum number sequencing as one "channeled" stream like a thread in a "silica" based microprocessor. The
"channeled" stream is sequencing data numerically by referencing the RGB color spectrum. A one standalone complete center-cycling semiconductor at the central switching module hubed to the I/O spectra on each side of the
U-shaped unit embedding the 276,480 "pins".
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Engineering:
The how, what and where of it.
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How do we now handle/define units of bit(s)-to-precession float number counts as hardware architecture is not limited to bit transfer unit.

/
We need new and add to current structured binary translations to define spunit as per independent of 360_degree area cavity trace route.
/
No matter the size of cavity, defining measurable rate is compared by data rate (d rate) to "defined" transmitting median(tm rate).
/
############The "spectra unit" ############
/
-requires unit of measurement for RGB color/spectrum(by)data stream coverage to compute rate() per time/frame at actual area computing
-A required unit of measurement for one(1) "spectra unit" as per a "IEEE Std" would define the scale to calculate 0-100% cofactor of continuous bit transfer rate..
-()3×256=768×360=(276,480-bit spectral cavity processor); spectra by one(n area) cavity or multi(n area) per cavities spectrums total area of calculating/actual area used =
-now we have one "276,480-bit "spectra(s)"" in (n) area;
data at()
×
per second of ON time=(n)
/
*
*
*
Programming:
We will contextualize current programming languages to building a stand alone language.
/
Arithmetic…
IE. Floating point numbers...
/
=
([(Floating-Point*/0×
Floating-Point*/0)])
=
((3×256)[x*])(k*))]
/
new programming language/packaging required for pragmatic system requirements needed for operations/conversions to...
Now;
-we fill in with architecture hardware specifications..
/
[]
[]
[]

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[]
[]
/
All (spectral areas(undetermined defined range) by(×)×(the cavity(x)) are deterministic[x] and accountable (per unit(xOFn)) of(per unit filled(xOFn)=(spectral range(3×256)×(n))...
/
Defined area of spectral area as standard;
-material per unit sq. ?...
/
then-
/
-we know we can not use the ranges defined by present standards or programming languages required to define the future approved ranges of grouped numbers then to be translated into current silica microprocessor architecture.
/
/
Example- progmatic inference;
/
"it" lang for the Full-Spatial Quantum Computer);
-Due to new architecture non-restrictions setting implicit charters are required…
1. Looped verification of spectral timed events
2. Bounds vs. Latency = ~0~
3. Numbered/naming power of (n) number sequensing in blocks named(x)
/
!Level of standard!...machine always ON or always OFF…
...okay let's GO!
/
Example-
/
/
Formatting/Transfer from the "it" lang programming language to…
-Registry requirements per area of available spectral cohesion rate..
-library's to systemically w/ Floating-Point
File format and/or runing sums to target architecture whether dependent to specific output of Full-Spatial computer processor(ie. operating system specific to FSPC) and/or available architecture.
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-on continuing this working draft the emphasis will be maximum hardware output with a stand alone standardized operating system to utilize structured semantics in programming language/base unit packaging the new 276,480-bit computer processor architecture.
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