Proposal for IEEE Standard Full-Spatial Floating-Point Arithmetic.

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Proposal for IEEE Std n-2020 for Full-Spatial Floating-Point Arithmetic is draft no. 01 for a working standard.

This standard proposes formats and operations for full-spatial floating-point arithmetic in the newly designed full-spatial(median-free liquid via photonic bit transfer) processors/computer systems.

Diversity: The 1960's were the flowering of the mainframe era, epitomized by IBM 360 and CDC 6600 and DEC 10, but with many other contenders as well. The 1970's saw a corresponding boom in minicomputers, epitomized by the DEC PDP-11 and, again, many others. These systems all had
floating-point arithmetic, usually programmed with Fortran compilers. But that was about all one could generalize. Each arithmetic was different in greater or lesser ways, sometimes even within the same instruction-set architecture. Quite an engineering art developed in how to write programs that would run equally correctly when compiled with these differing compilers targeted at different
hardware. The “portable” numerical programs that resulted were often much more complicated than corresponding programs targeted at just one system.[ref. IEEE Standard for Floating-Point Arithmetic revision due in 2019]
As we continued into 21st century yearning for seamless interconnectivity and quasi-operational machines new designs were needed. One such designed engineering utility was invented by Dr. Thomas Catalano, the Quantum Computer Full-Spatial median-free liquid photonic bit transfer computational processor/computer so to the guidelines to coherently run arbitrary instruction sets.

Standards: With the new Full-Spatial computational processors/computers a conjoined effort to efficiently commence usage processing.
A core processing unit runs single and/or overlayed data stream(s) as RGB color spectrum number sequencing as one "channeled" stream like a thread in a microprocessor. The "channeled" stream is sequencing data numerically by referencing the RGB color spectrum.
In waiting on a timeline for us converging to materialize a working group I will continue development of possible arithmetic structures for architecture based on design and engineering but until we formally meet formation of such is to defer the miniscule energy away from my current stature.
I anticipate our cooperative efforts.