

CS & IT ENGINEERING

DIGITAL LOGIC
SEQUENTIAL CIRCUIT



Lecture No. 06



By- CHANDAN SIR

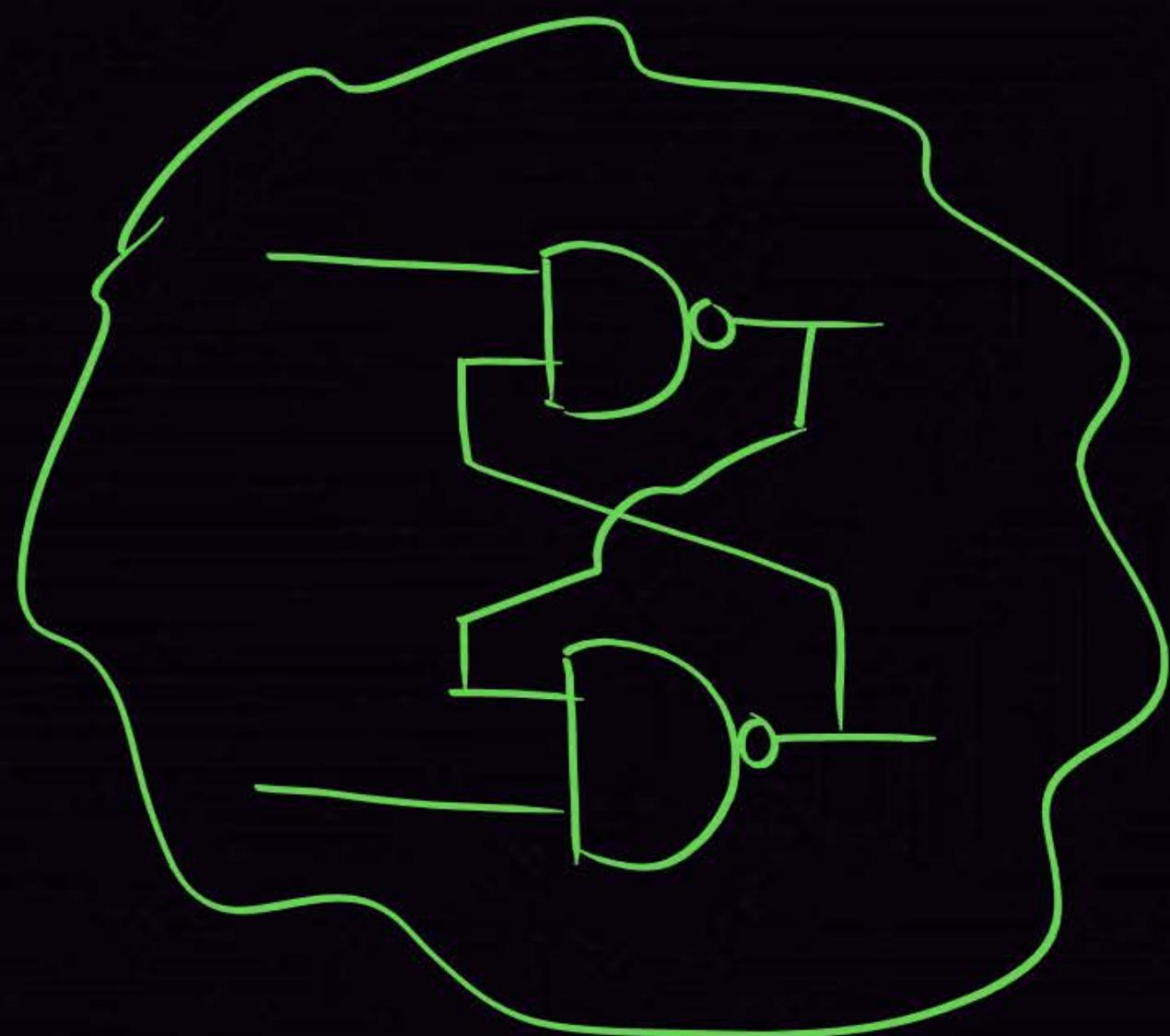
TOPICS TO BE COVERED

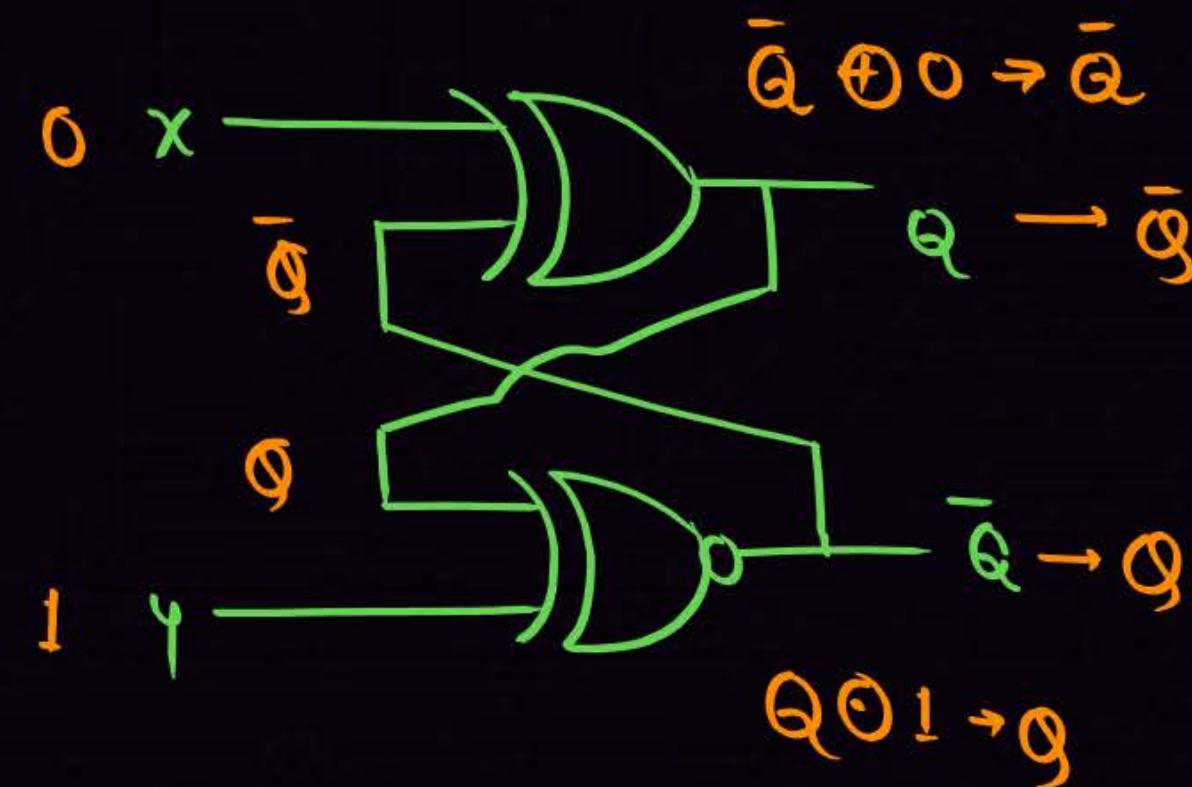
01 Counters

02 Practice

03 Discussion

Counter Basic
Asynchronous





X	Y	Q	\bar{Q}
0	0	\bar{Q}	\bar{Q}
0	1	\bar{Q}	Q
1	0	Q	\bar{Q}
1	1	Q	Q

→ inValid condition.

→ Toggle

→ HOLD / MEMOR / Previous state

→ Invalid
forbidden
don't care.

X-NOR

X-NOR

$$Q \oplus Q = 0$$

$$Q \odot Q = 1$$

$$Q \oplus 0 = Q$$

$$Q \odot 1 = Q$$

$$\bar{Q} \oplus 0 = \bar{Q}$$

$$\bar{Q} \odot 1 = \bar{Q}$$

$$Q \oplus \bar{Q} = 1$$

$$Q \odot \bar{Q} = 0$$

$$Q \oplus 1 = \bar{Q}$$

$$Q \odot 0 = \bar{Q}$$

$$Q \oplus 1 = 0$$

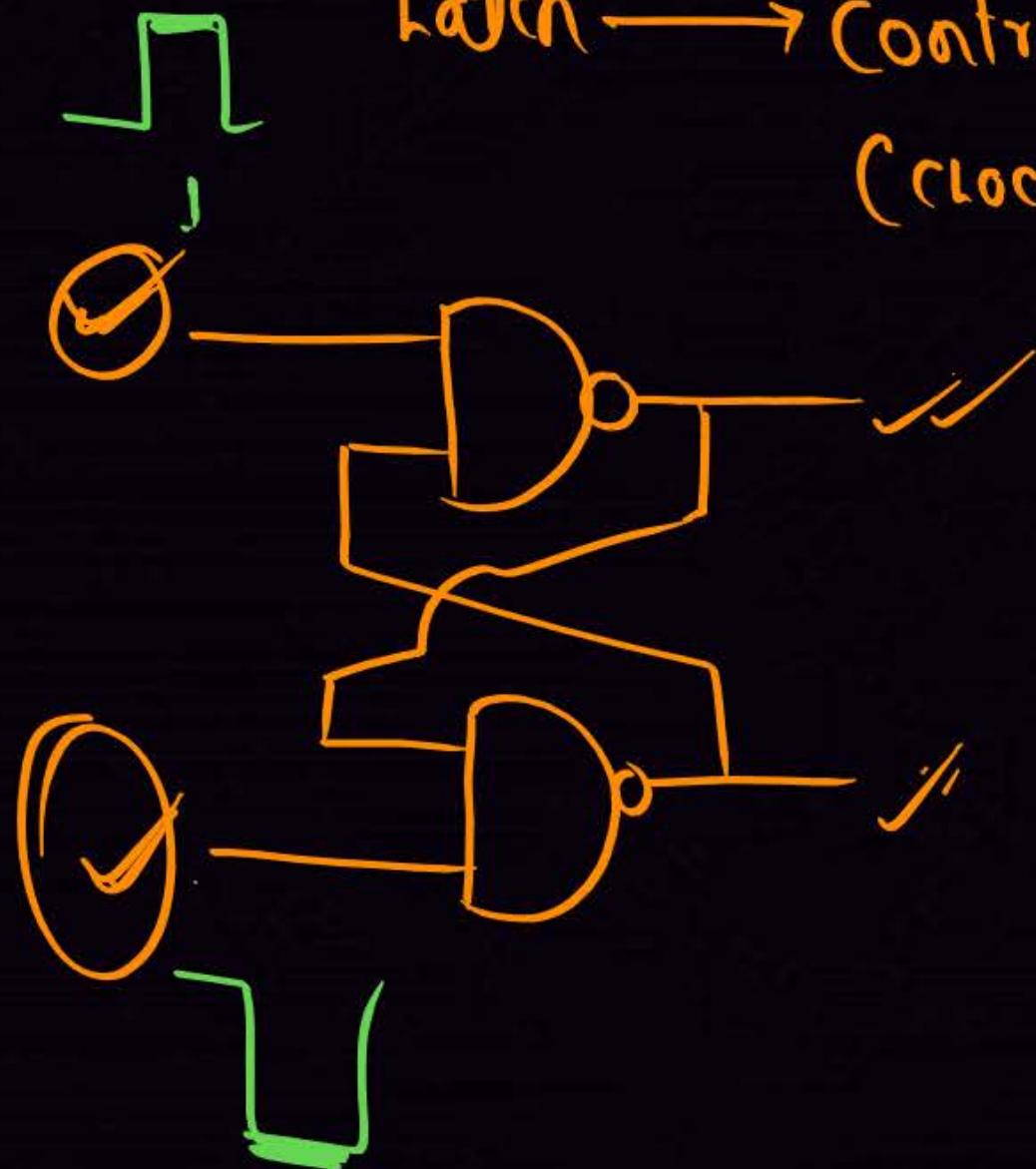
$$\bar{Q} \oplus 0 = Q$$

Level sensitive.

Edge sensitive.

Latch → Control
(clock)

Flip-Flop ✓



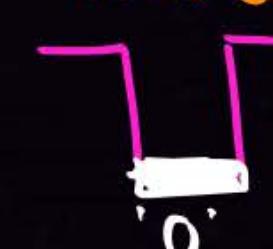
Triggering

Level triggered

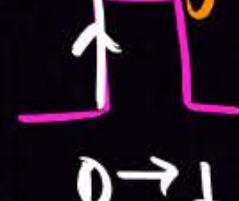
+ve Level



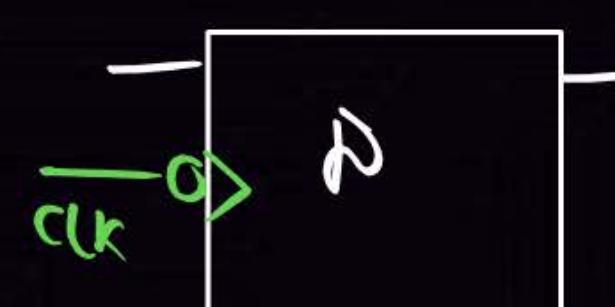
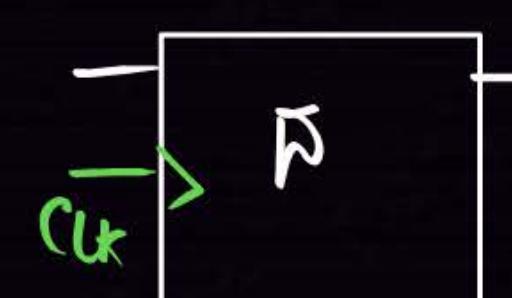
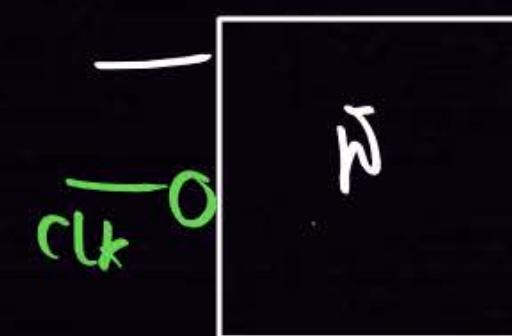
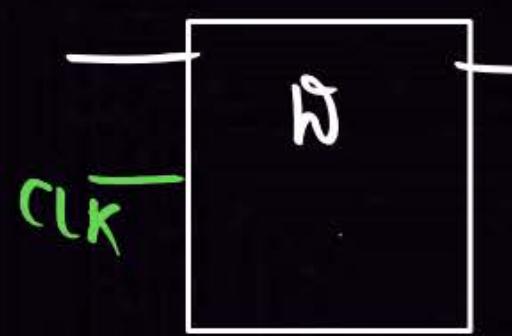
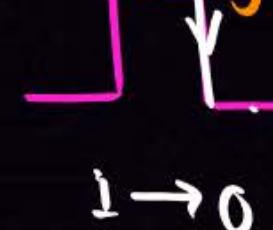
-ve Level



+ve edge



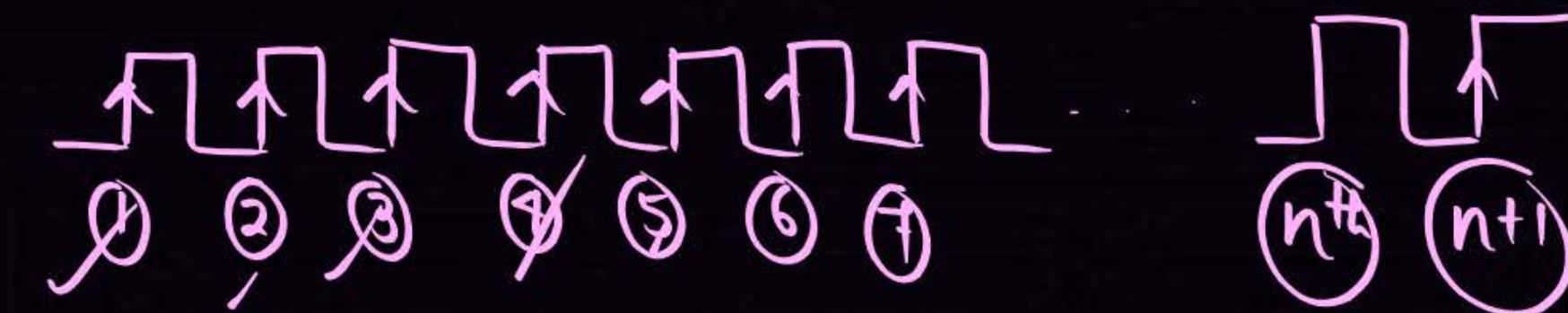
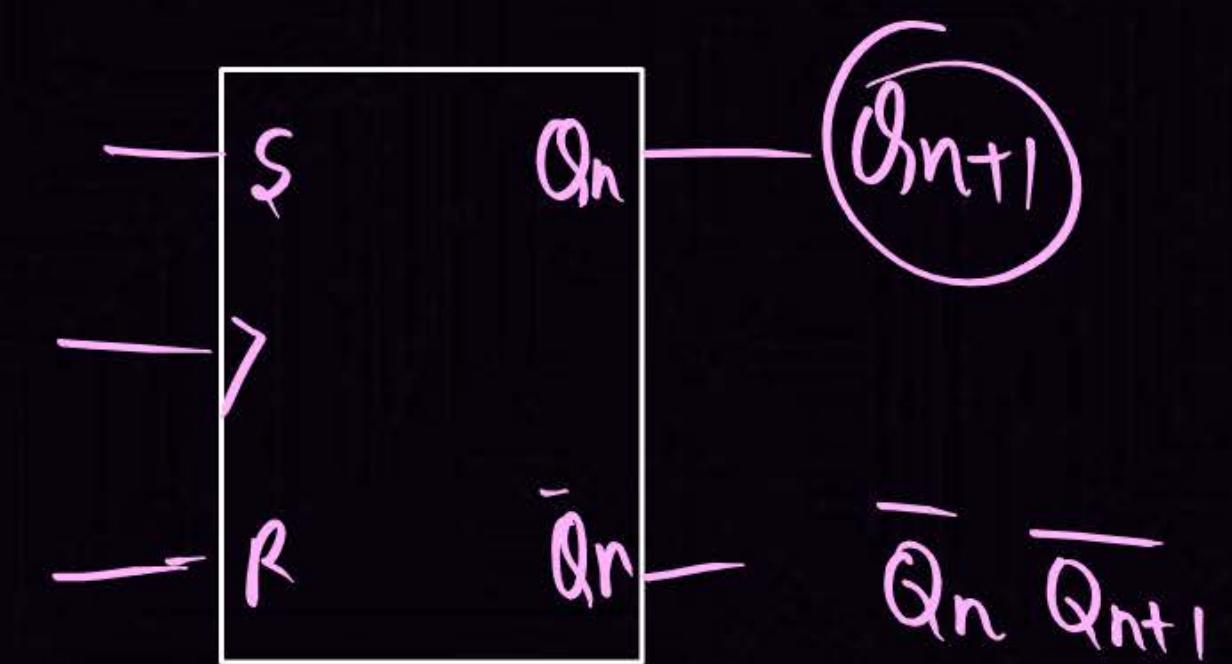
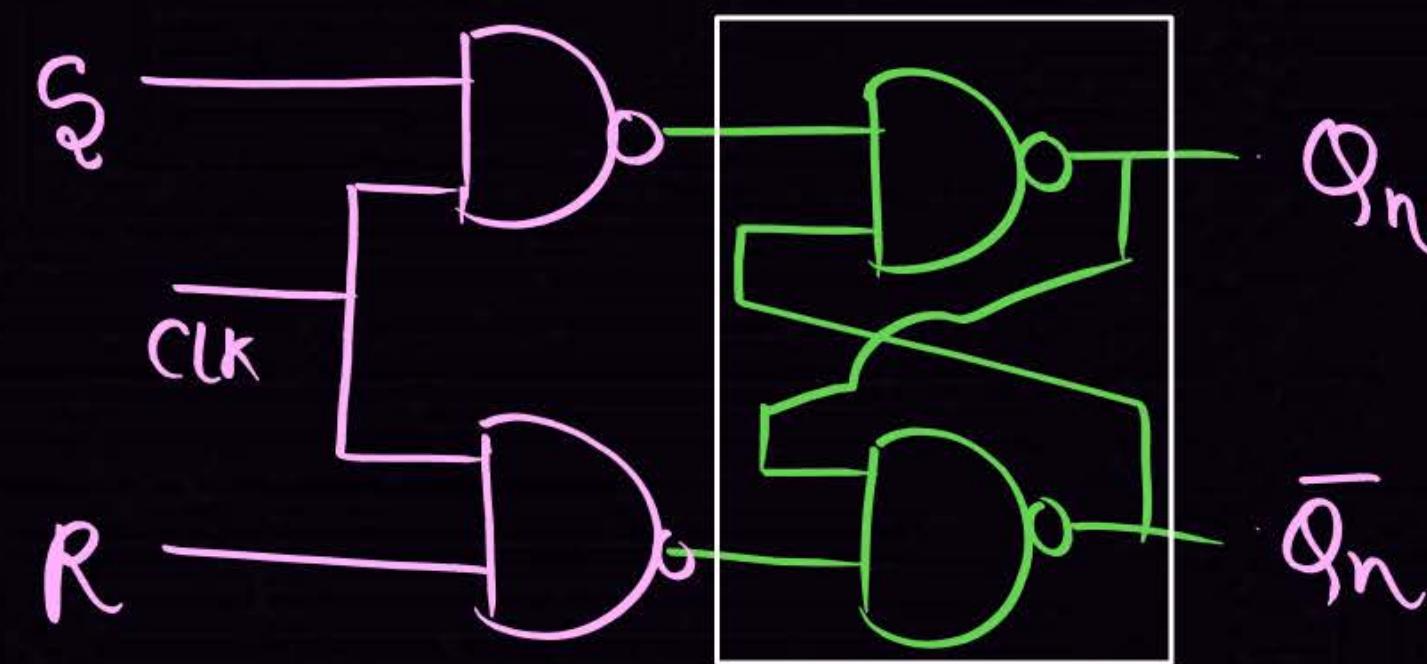
-ve edge

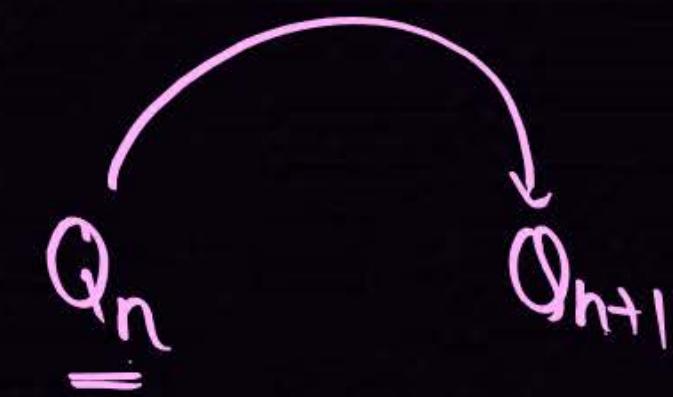


PW

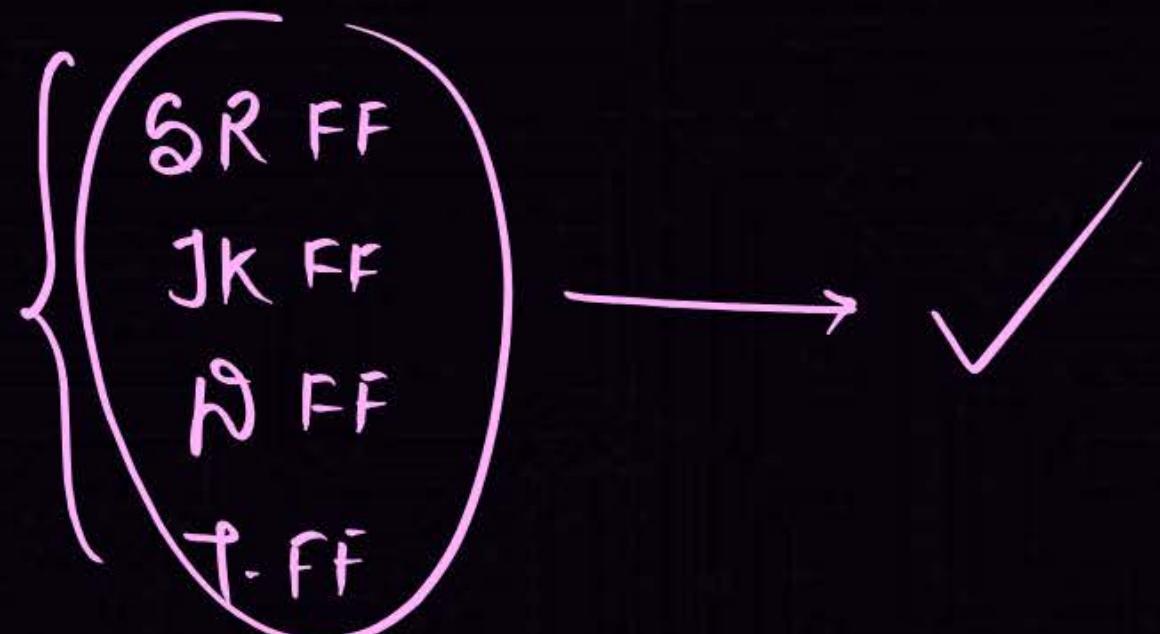
S R - Flip. Flop

$$Q_1 \ Q_2 \ Q_3 \ Q_4 \ \dots \ Q_n \ Q_{n+1}$$



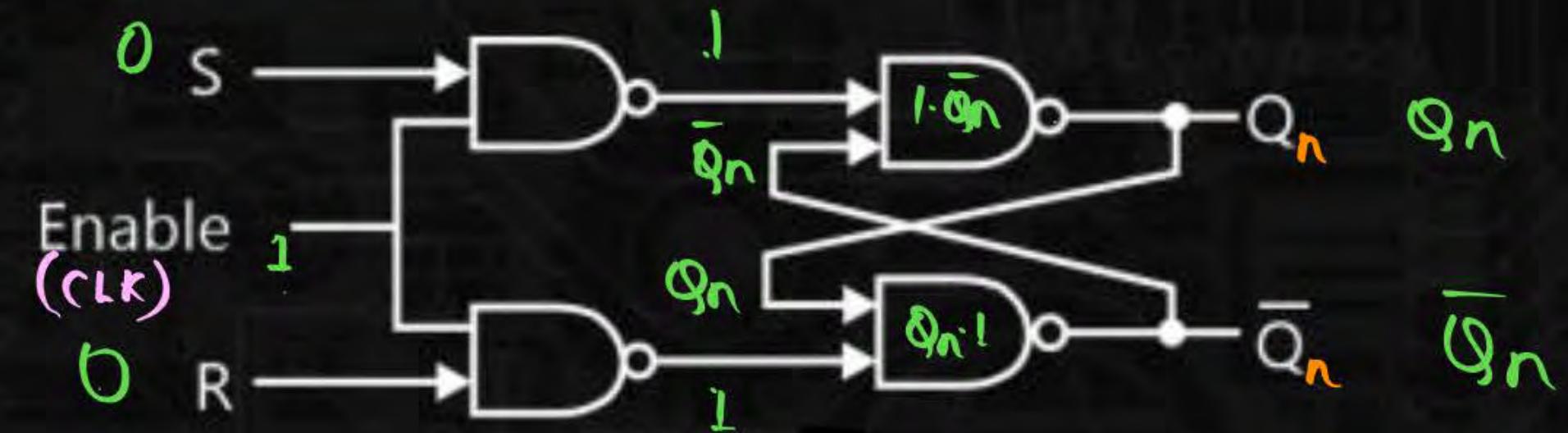
Q_n  Q_{n+1}

- ① Circuit Diagram / Symbol
- ② Truth Table.
- ③ Characteristic Table.
- ④ Characteristic Equation
- ⑤ Excitation Table.
- ⑥ State Diagram



(1) SR FLIP-FLOP [SET RESET FF]

(i) Circuit Diagram :



(ii) Truth Table :

S	R	Q_{n+1}	\bar{Q}_{n+1}	
0	0	Q_n	\bar{Q}_n	→ HOLD
0	1	0	1	RESET.
1	0	1	0	SET.
1	1	X	X	Invalid

SR FLIP-FLOP [SET RESET FF]

$$Q_{n+1}(S, R, Q_n) = \sum m(1, 4, 5) + \sum d(6, 7)$$

(iii) Characteristic Table:

	S	R	Q_n	Q_{n+1}
0→	0	0	0	0
1→	0	0	1	1
2→	0	1	0	0
3→	0	1	1	0
4→	1	0	0	1
5→	1	0	1	1
6→	1	1	0	X
7→	1	1	1	X

S	R	Q_{n+1}	Q_n
0	0	0	0
1	0	1	1
1	1	X	X

$$\left. \begin{array}{l} S=0 \\ R=0 \end{array} \right\} Q_{n+1} = Q_n$$

$$\left. \begin{array}{l} S=0 \\ R=1 \end{array} \right\} Q_{n+1} = 0$$

$$\left. \begin{array}{l} S=1 \\ R=0 \end{array} \right\} Q_{n+1} = 1$$

SR FLIP-FLOP [SET RESET FF]

(iv) Characteristic equations



$$Q_{n+1} = S + \bar{R}Q_n$$

\bar{S}	$\bar{R}Q_n$	$\bar{R}\bar{Q}_n$	$\bar{R}Q_n$	RQ_n	$R\bar{Q}_n$
0	00	11	01	11	10
1	11	11	X	X	X

SR FLIP-FLOP [SET RESET FF]

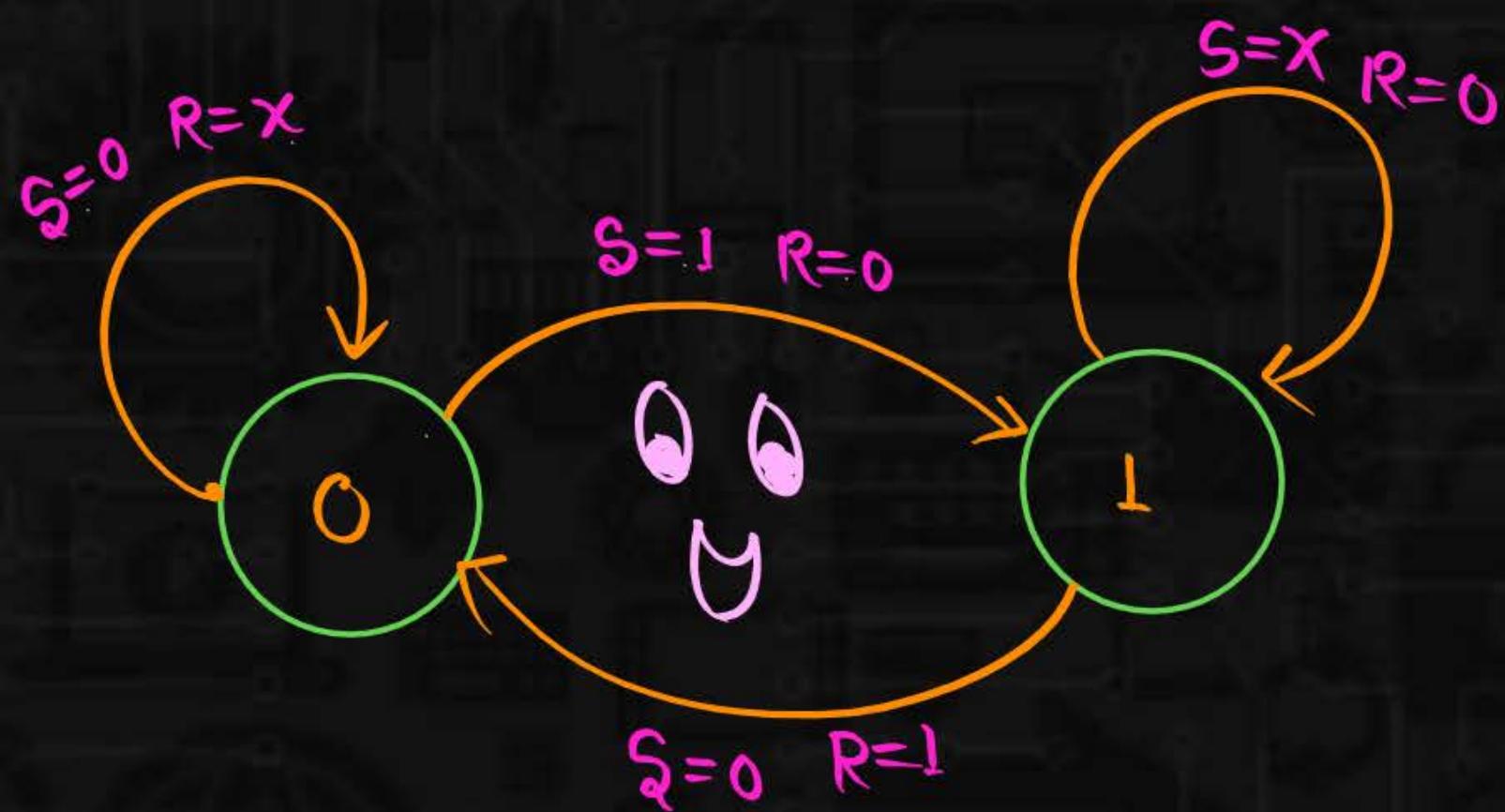
(v) Excitation Table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

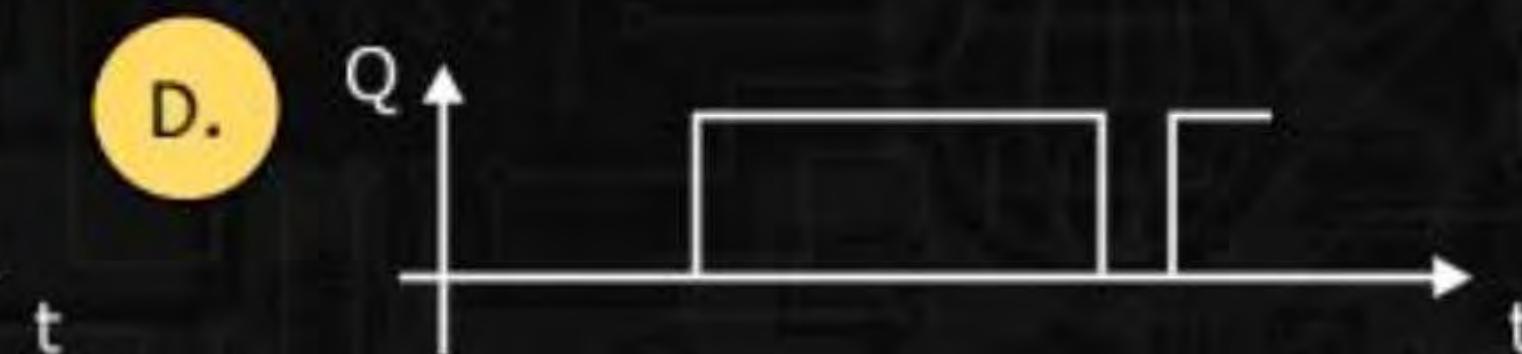
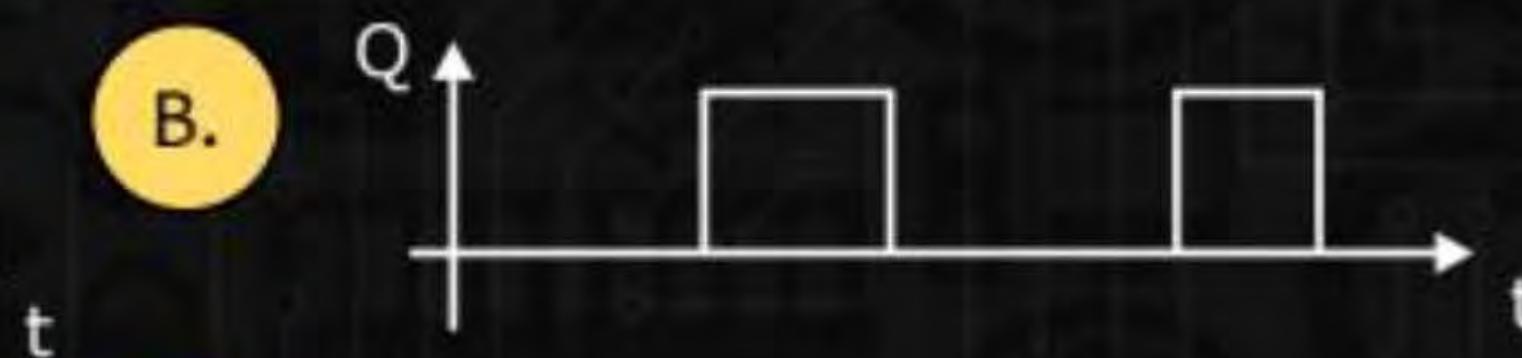
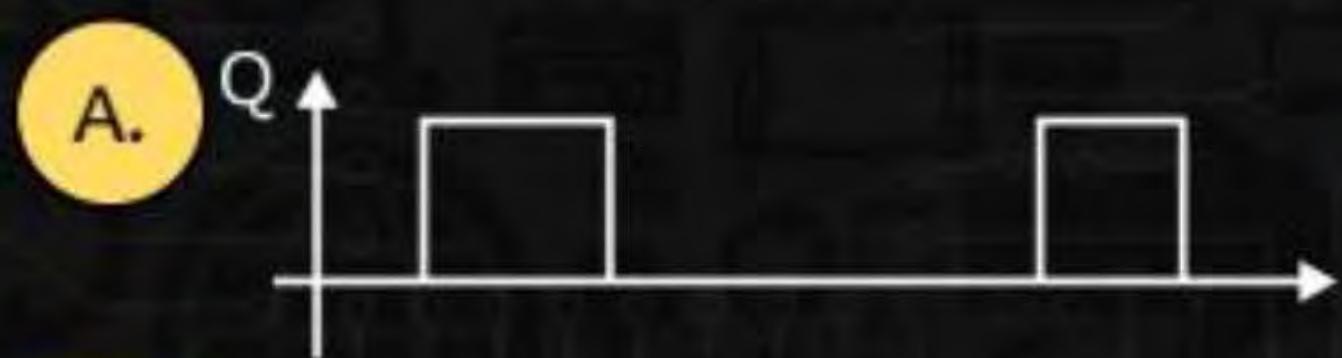
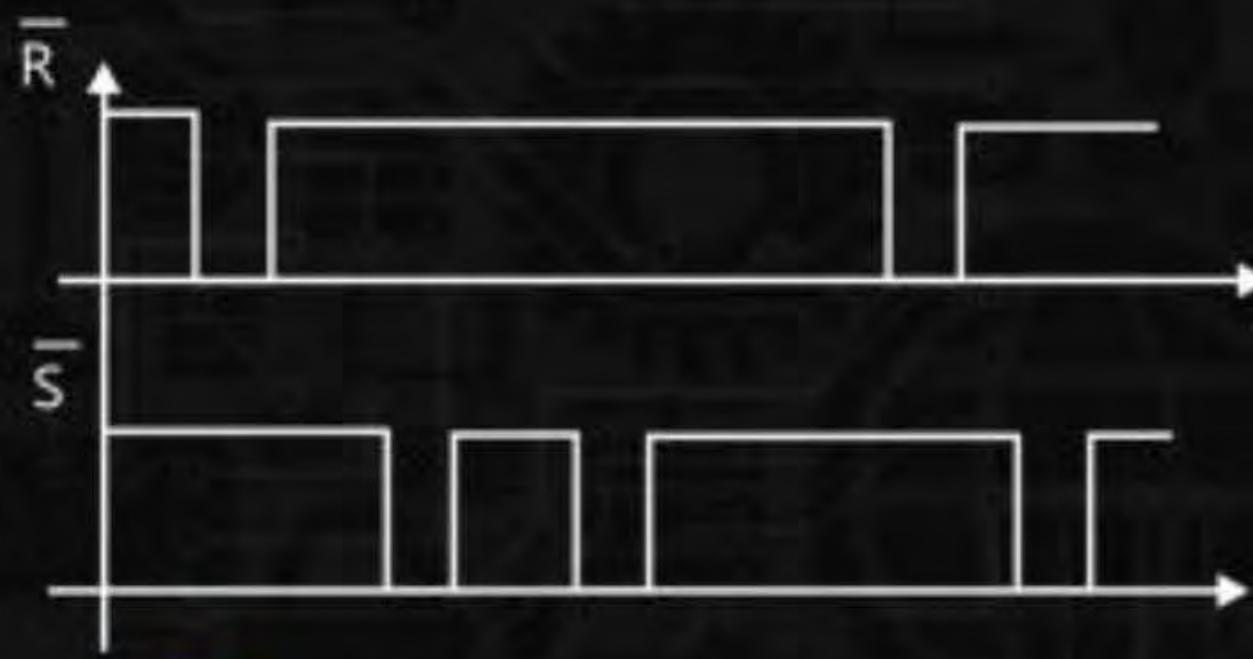
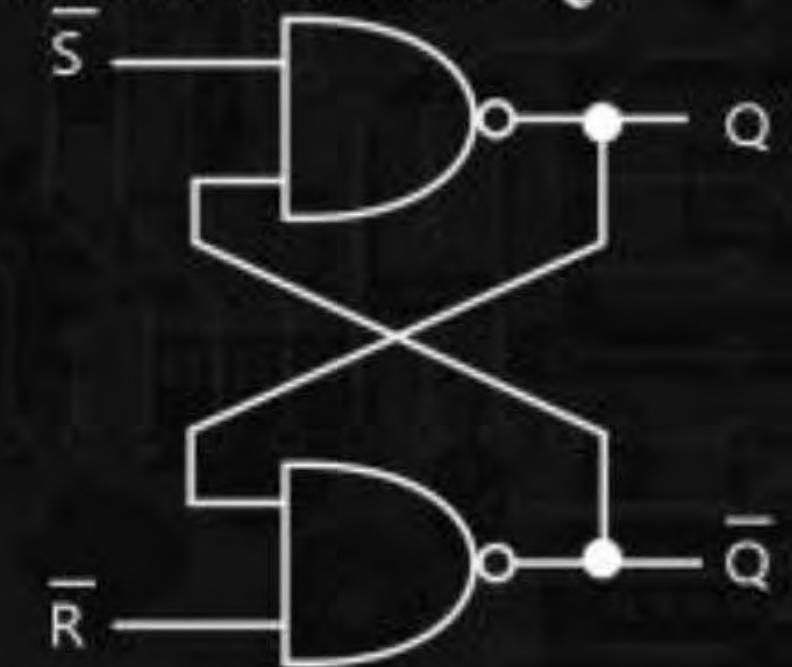
SR FLIP-FLOP [SET RESET FF]

(vi) State Diagram :



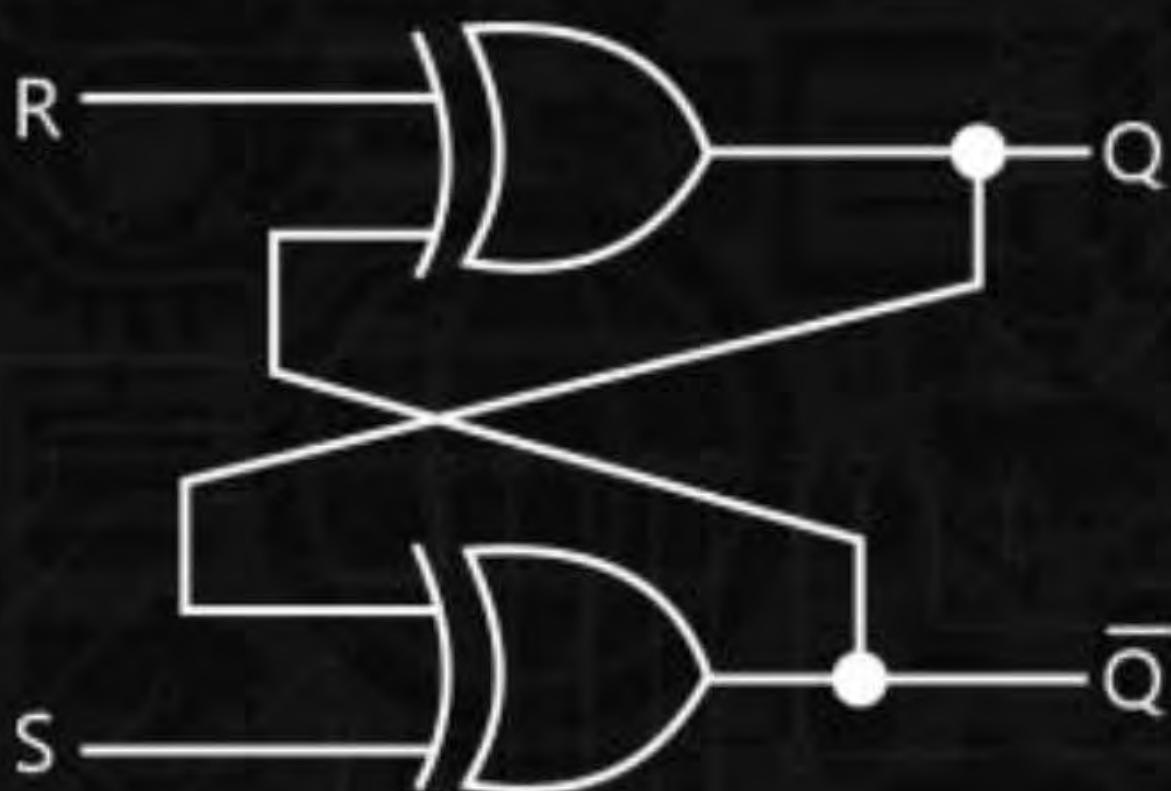
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Q. The \bar{S} and \bar{R} inputs shown in the figure are applied to a NAND latch. Assuming the Q is 0 initially, which plot gives correct waveform for Q ?



Q. Which of the following will be correct for the given sequential circuit?

- A. The circuit would hold the previous state for $S=0, R=0$
- B. The circuit would hold the previous state for $S=0, R=1$
- C. The circuit would hold the previous state for $S=1, R=1$
- D. The circuit would never be able to hold the previous state under any condition



JK FLIP FLOP

(1) Symbol



Figure 8: JK Flip-Flop

(2) Truth Table

J	K	Q _{n+1}
0	0	Q _n
0	1	0
1	0	1
1	1	Q̄ _n → Toggle

JK FLIP FLOP

(3) Characteristic Table

J	K	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

	J	K	Q_n	Q_{n+1}
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

JK FLIP FLOP

(4) Characteristic Equation

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

$\bar{J}\bar{K}Q_n$	$\bar{J}\bar{K}\bar{Q}_n$	00	$\bar{K}Q_n$	01	KQ_n	11	$K\bar{Q}_n$	10
0	0	0	1	1	0	0	0	0
1	1	1	1	0	1	0	1	0

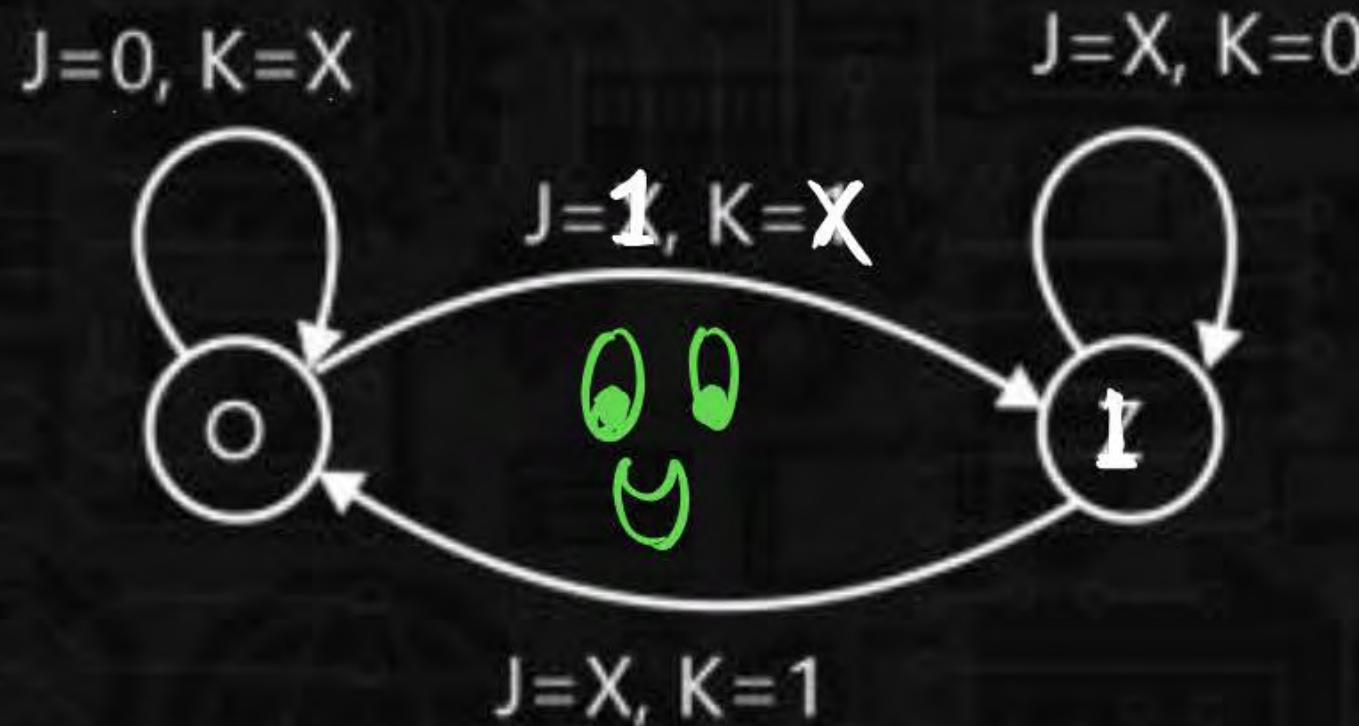
JK FLIP FLOP

(5) Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	\times
0	1	1	\times
1	0	\times	1
1	1	\times	0

JK FLIP FLOP

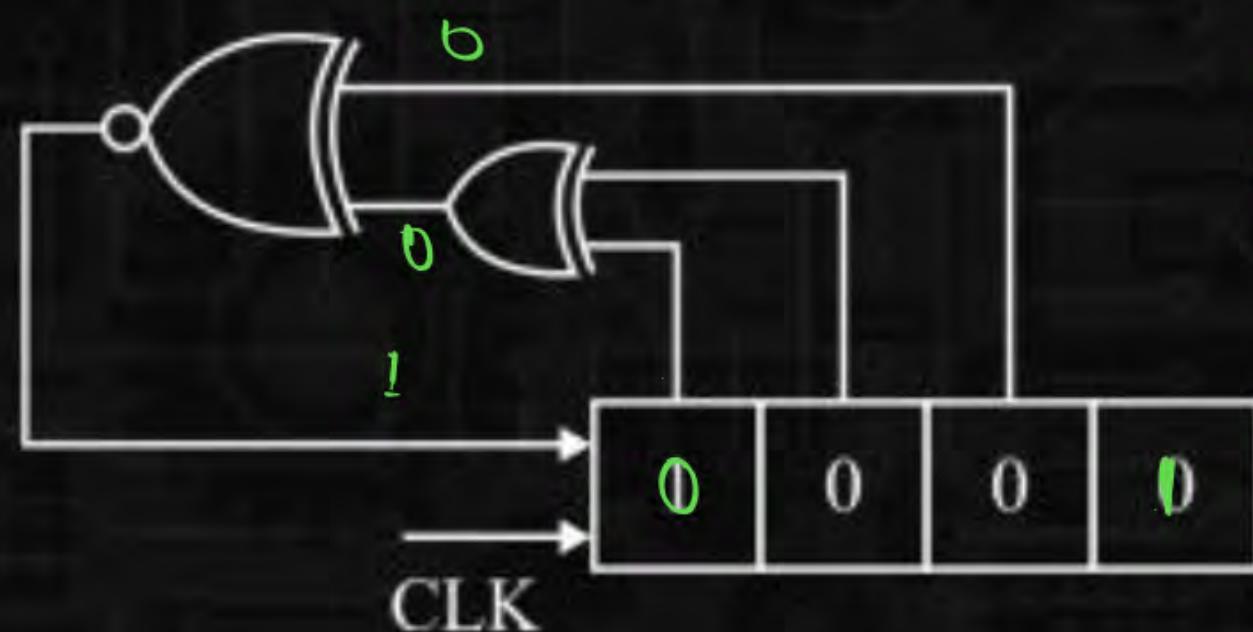
(6) State Diagram



Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Q.

After 97th clock the output
will be?



$$\frac{97}{4} \Rightarrow R=1$$

0 | 60

Clock	Q_3	Q_2	Q_1	Q_0
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				

TOGGLE MODE OF FLIP FLIPS

P
W

$$Q_{n+1} = T \oplus Q_n \Rightarrow I \oplus Q_n = \bar{Q}_n$$

$Q_{n+1} = \bar{Q}_n$

1. Toggle mode of T Flip Flop.

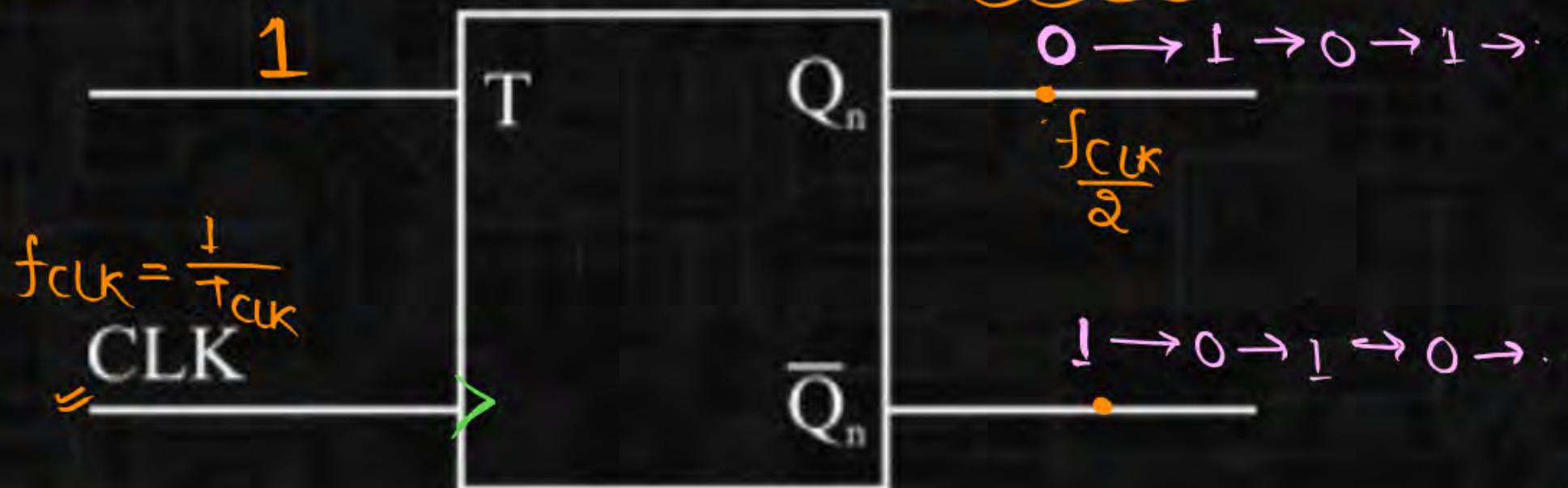
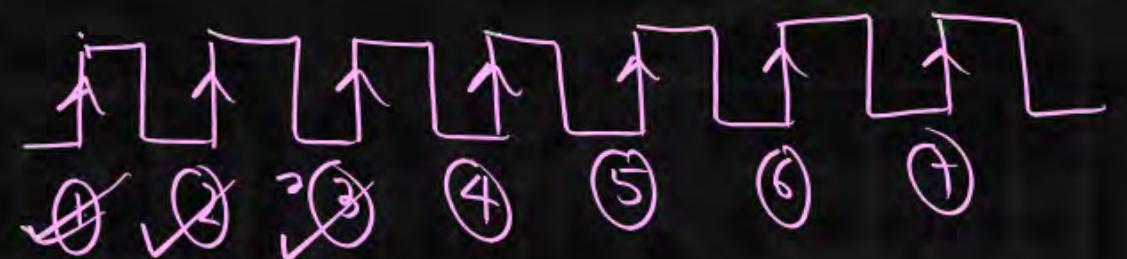


Figure 6: Toggling Mode of T Flip Flop

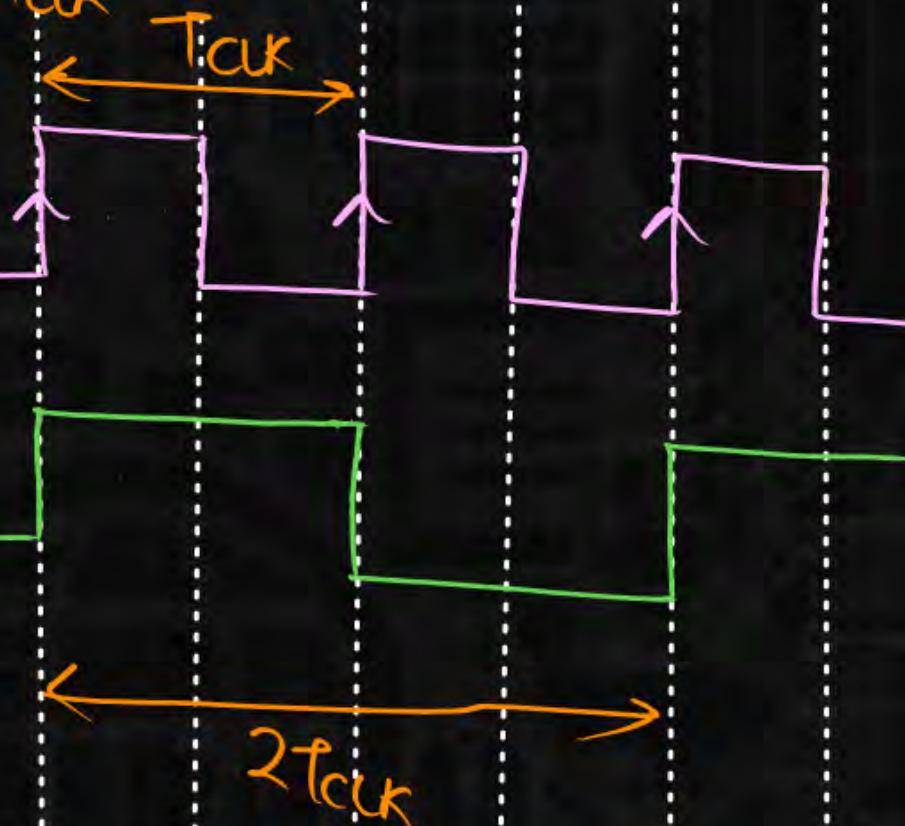


$$f_{CLK} = \frac{1}{T_{CLK}}$$

CLK

Q_n

$$Q_{n+1} = \bar{Q}_n$$



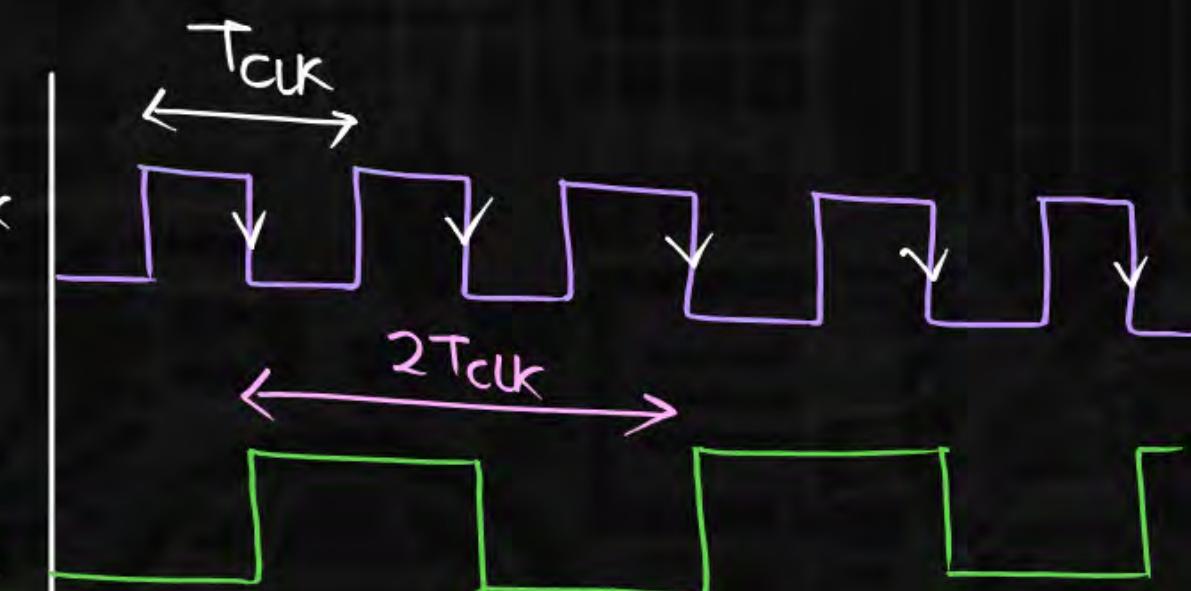
$$f_Q = \frac{1}{2T_{CLK}}$$

$$f_Q = \frac{f_{CLK}}{2}$$

TOGGLE MODE OF FLIP FLIPS

2. Toggle mode of J K Flip Flop.

(i)



$$f_Q = \frac{1}{2T_{clk}} = \frac{\left(\frac{1}{T_{clk}}\right)}{2} = \frac{f_{clk}}{2}$$

$$f_Q = \frac{f_{clk}}{2}$$

Figure 7: Toggling Mode of JK Flip Flop

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

$$= 1 \cdot \bar{Q}_n + 0 \cdot Q_n$$

$$Q_{n+1} = \bar{Q}_n$$

TOGGLE MODE OF FLIP FLIPS

2. Toggle mode of J K Flip Flop.

(ii)

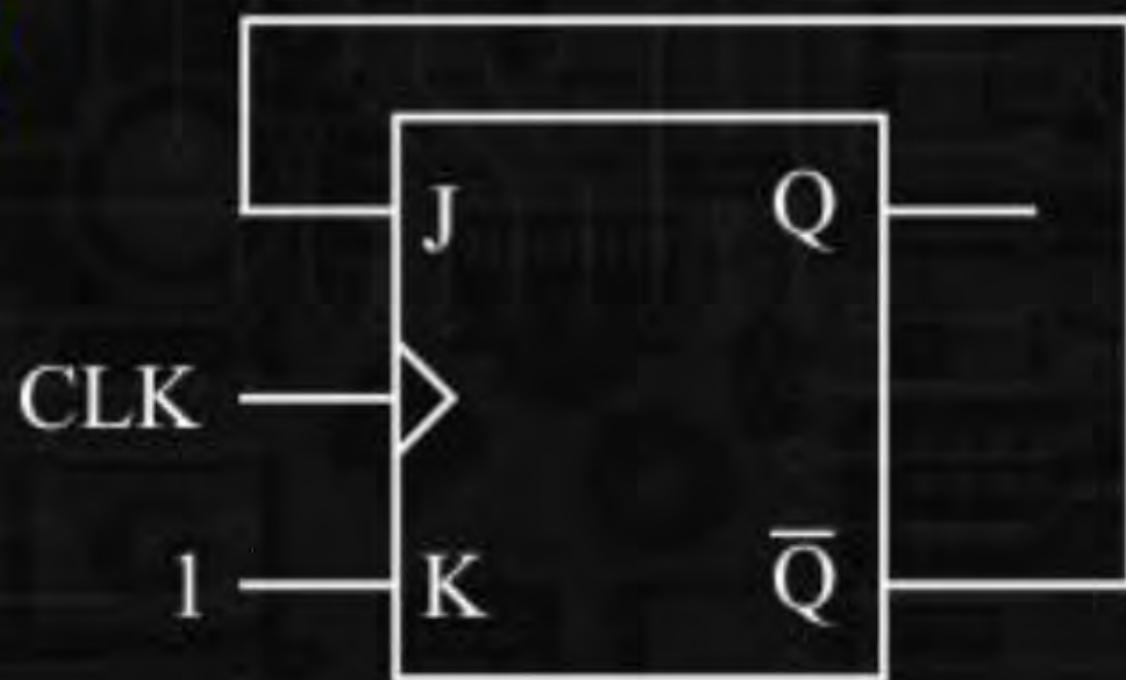


Figure 8: Toggling Mode of modified JK Flip Flop

$$\begin{aligned}Q_{n+1} &= J\bar{Q}_n + \bar{K}Q_n \\&= \bar{Q}_n\bar{Q}_n + 0 \cdot Q_n\end{aligned}$$

$$Q_{n+1} = \bar{Q}_n$$

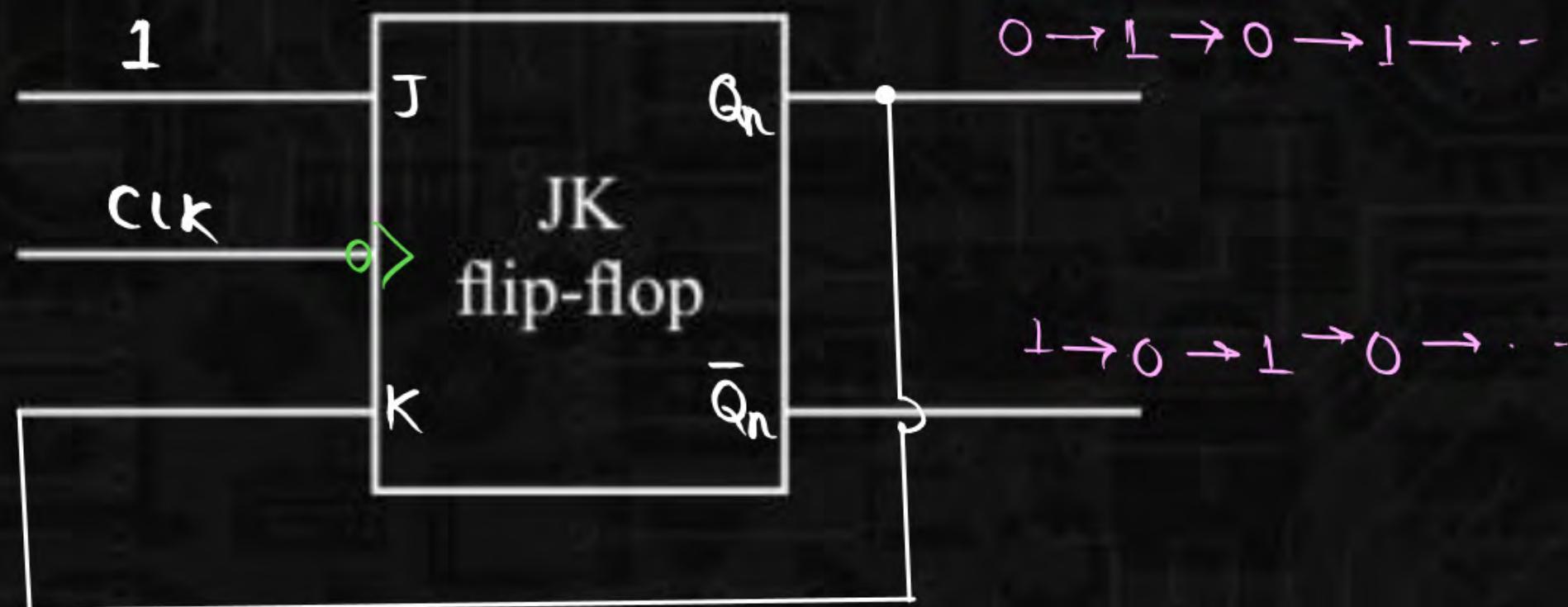
$$Q = 0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow \dots$$

$$\bar{Q} = 1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow \dots$$

TOGGLE MODE OF FLIP FLIPS

2. Toggle mode of J K Flip Flop.

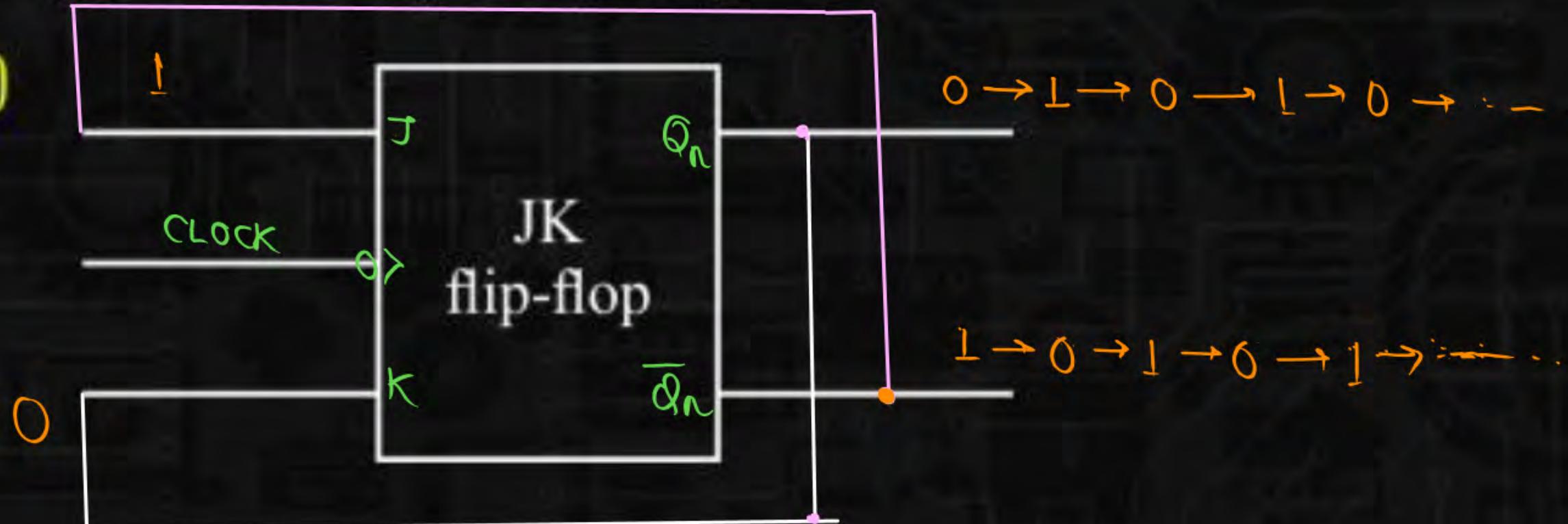
(iii)



TOGGLE MODE OF FLIP FLIPS

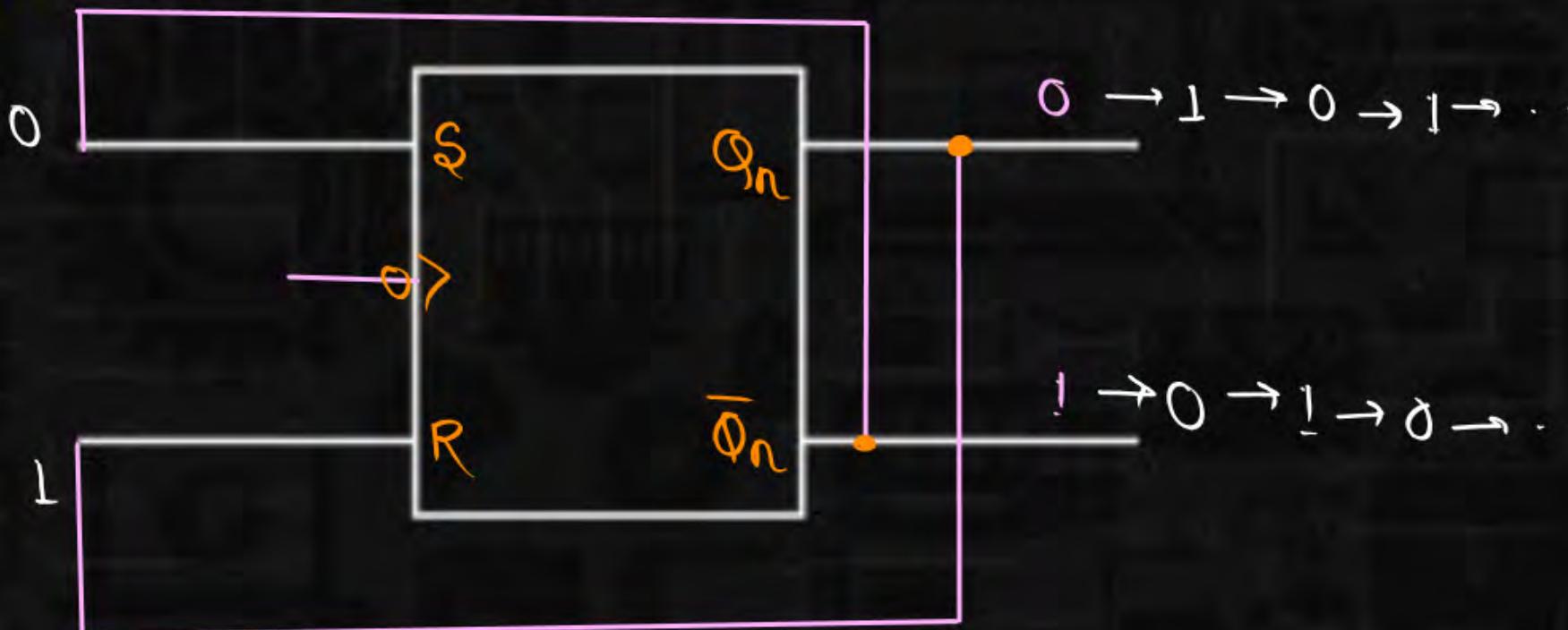
2. Toggle mode of J K Flip Flop.

(iv)



TOGGLE MODE OF FLIP FLIPS

3. Toggle mode of S R Flip Flop.

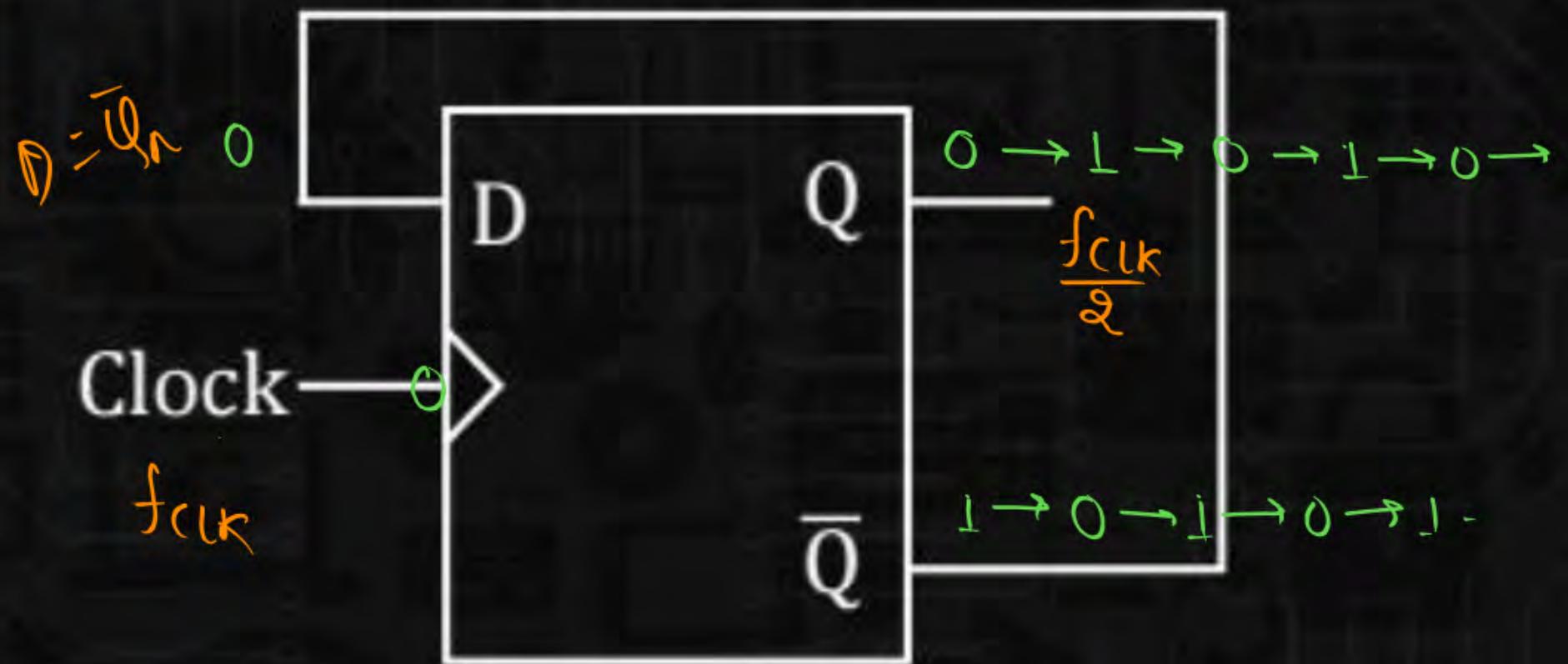


$$S = \bar{Q}_n$$
$$R = Q_n \rightarrow \bar{R} = \bar{Q}_n$$

$$\begin{aligned} Q_{n+1} &= S + \bar{R} Q_n \\ &= \bar{Q}_n + \bar{Q}_n \cdot Q_n \\ \text{Cloud: } Q_{n+1} &= \bar{Q}_n \end{aligned}$$

TOGGLE MODE OF FLIP FLOPS

4. Toggle mode of D Flip Flop.



$$Q_{n+1} = D$$

$$Q_{n+1} = \bar{Q}_n$$

COUNTER

1. Counters are used to count Number of clock^s. ✓
2. Counter are used as Frequency Divider Circuit.
3. Counter are also used in ADC.
4. Counters are also known as pulse stretcher circuit.
5. Counters also used in RADAR for detection of Range.

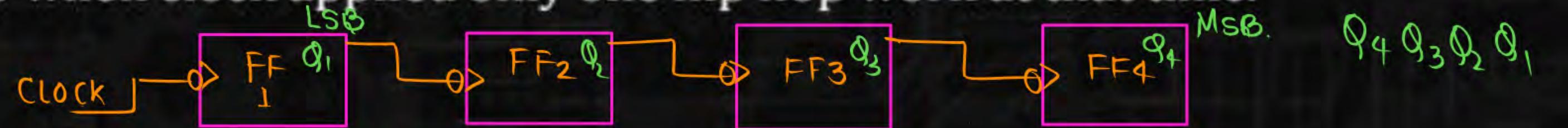
TYPES OF COUNTER

- ✓ 1. Asynchronous Counter
- ✓ 2. Synchronous Counter

TYPES OF COUNTER

1. Asynchronous Counter: Only one flip flop having external clock and output of that flip flop will become clock for the next flip flop.

So when clock applied only one flip flop work at that time.



2. Synchronous Counter: All Flip Flops are connected with the same clock. Hence when clock is applied all the flip flops work simultaneously.



COUNTER

Synchronous counter

- ① All the FF's are synchronized with same clock.
- ② Faster
- ③ All type of counting are possible.
- ④ No Transition error
- ⑤ Ex. Ring counter
Johnson counter

Asynchronous counter

- ① Only one FF having external clock and o/p of that FF will be clock for the next FF.
- ② slower
- ③ Only increasing or decreasing counting are possible.
- ④ Transition error occurs
- ⑤ Ex. Ripple counter.

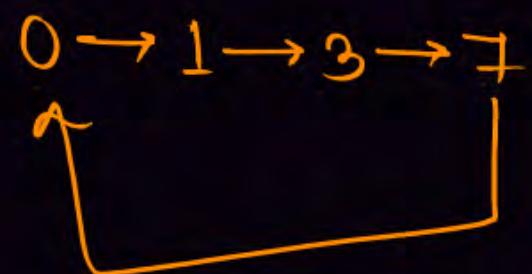
COUNTER MAXIMUM STATE

Maximum number of States = 2^n

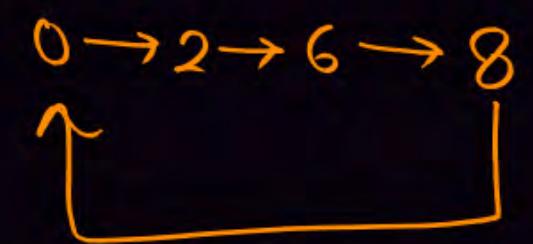
$n \rightarrow$ no. of FF's



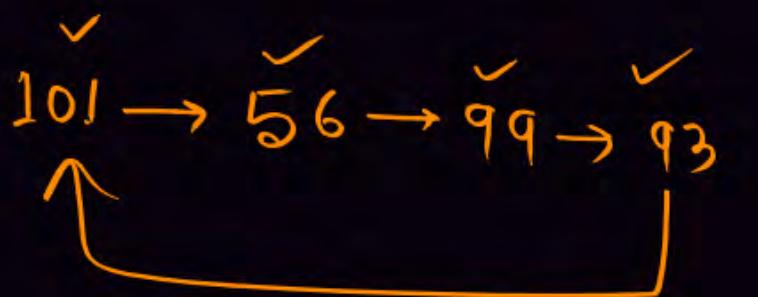
0 0)
0 1)
1 0)
1 1 } 4



(MOD) MODULUS = 4



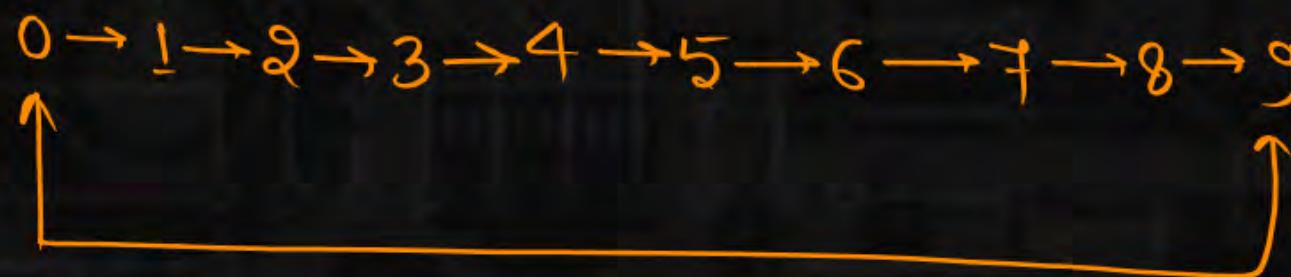
MOD=4



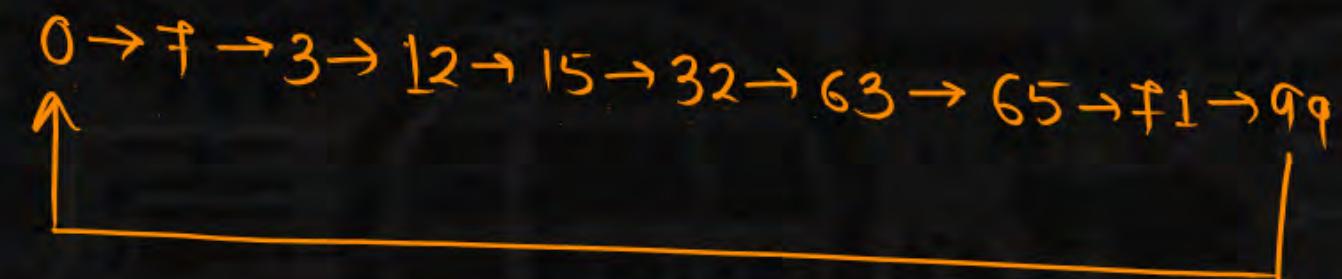
MOD=4

MODULUS OF THE COUNTER

Number of states that can be used by the counters are called Modulus(MOD) of the Counter.



$$\text{MOD} = 10$$



$$\text{MOD} = 10$$

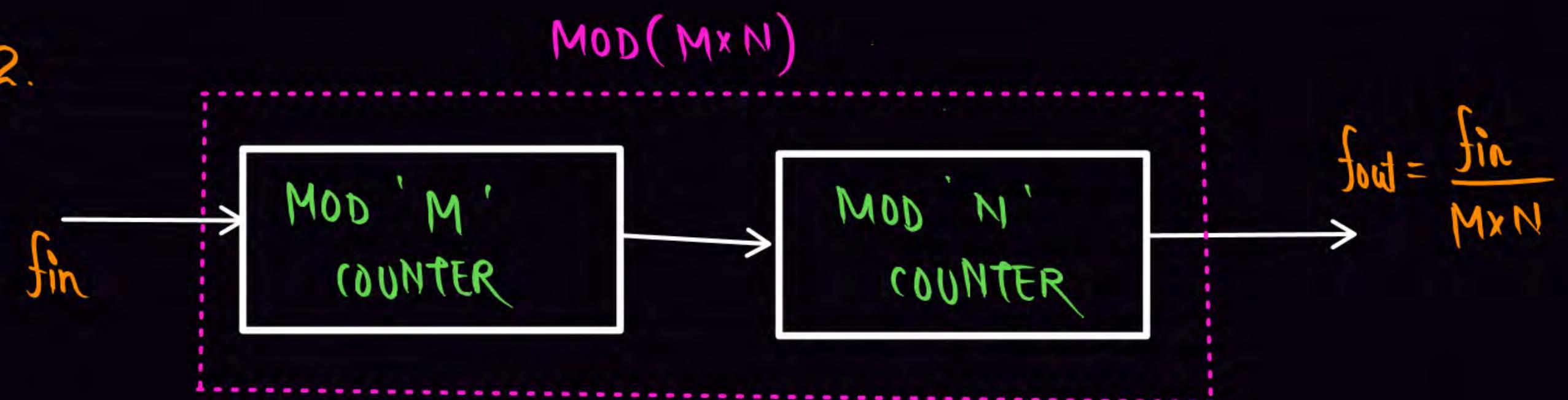
$$\text{MOD}(M) \leq 2^n$$

$$n \geq \log_2 M$$

NOTE 1.



2.

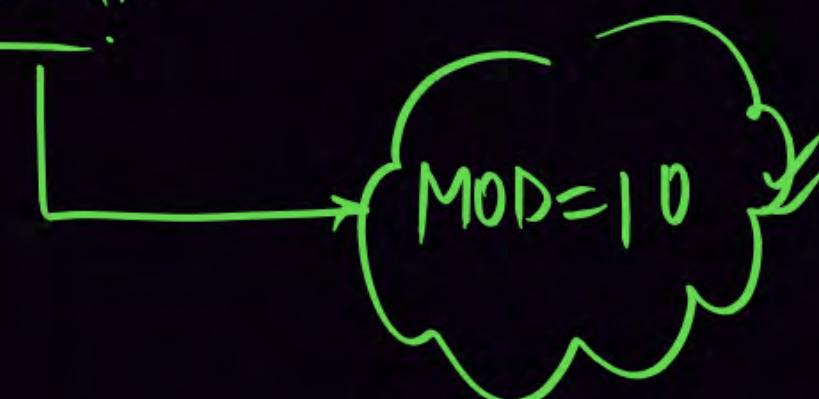


0000
0001
0010
0011
0100
0101
0110
0111
1000
1001

$\{$

$\text{BCD} =$

BCD counter



MOD-10 Counter



BCD X

not necessarily

Q.

If mode-5 counter is cascaded with mod-2 counter, then it will become?

- A. Mod 10 counter ✓
- B. BCD Counter ✗
- C. Both A and B ✗
- D. None ✗

$$5 \times 2 = \text{MOD-10}$$

Asynchronous counter \Rightarrow

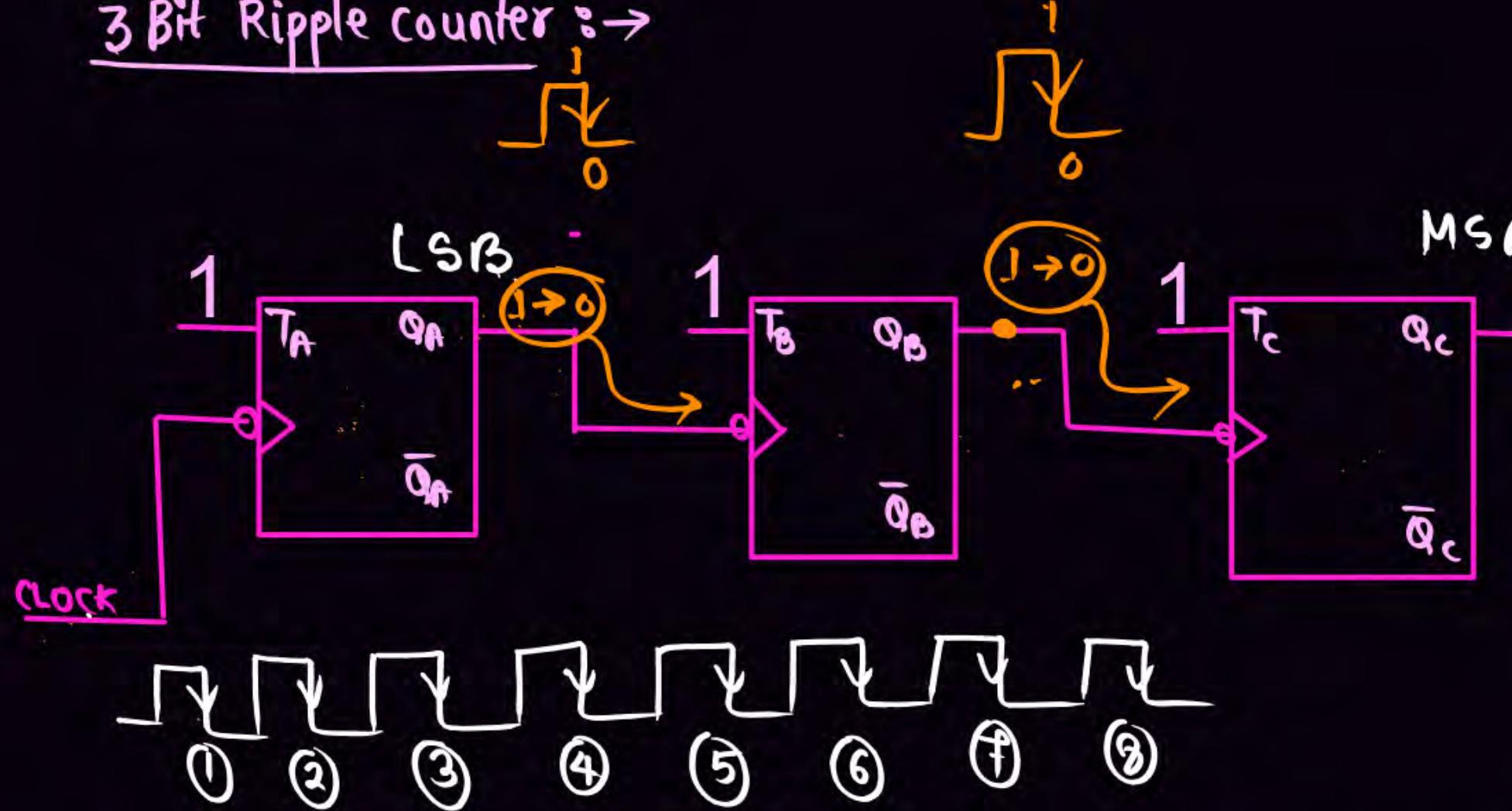
RIPPLE COUNTER



All the FF's are used in toggle mode.

3 Bit Ripple counter :-

P
W



① Q_A will toggle for every -ve edge of external clock.

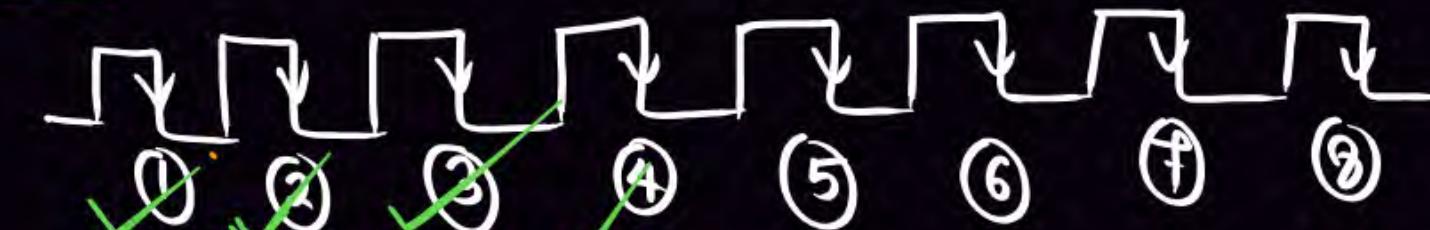
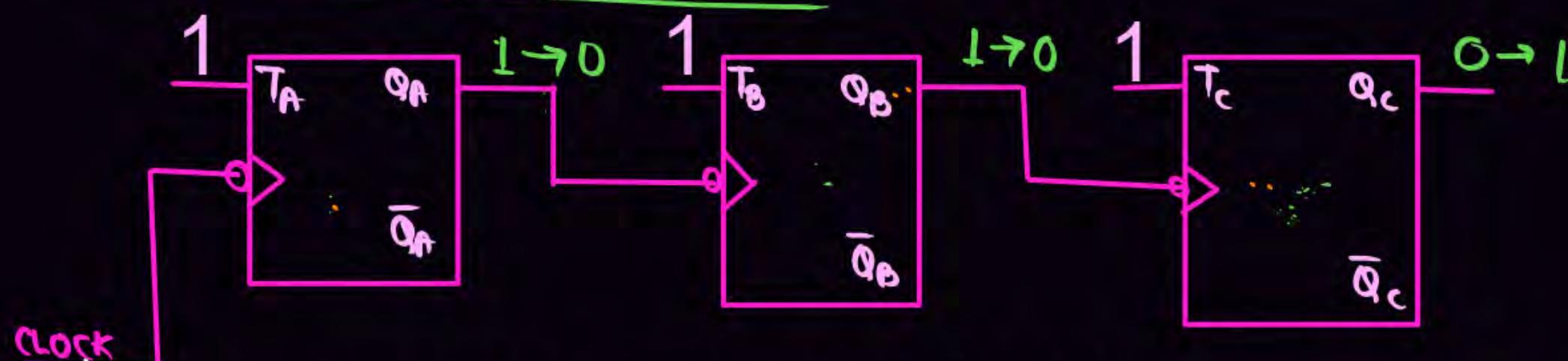
② Q_B will toggle when Q_A goes from 1 to 0.

③ Q_C will toggle when Q_B goes from 1 to 0.

3 Bit Ripple counter :-

J → 0

MOD: 8' UP Ripple counter.



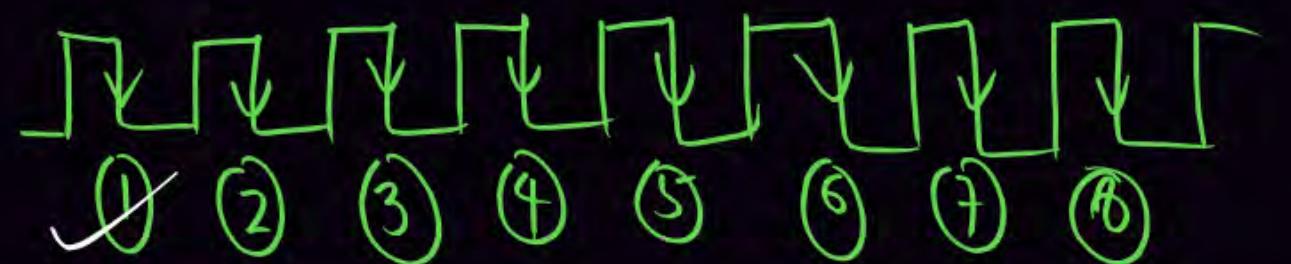
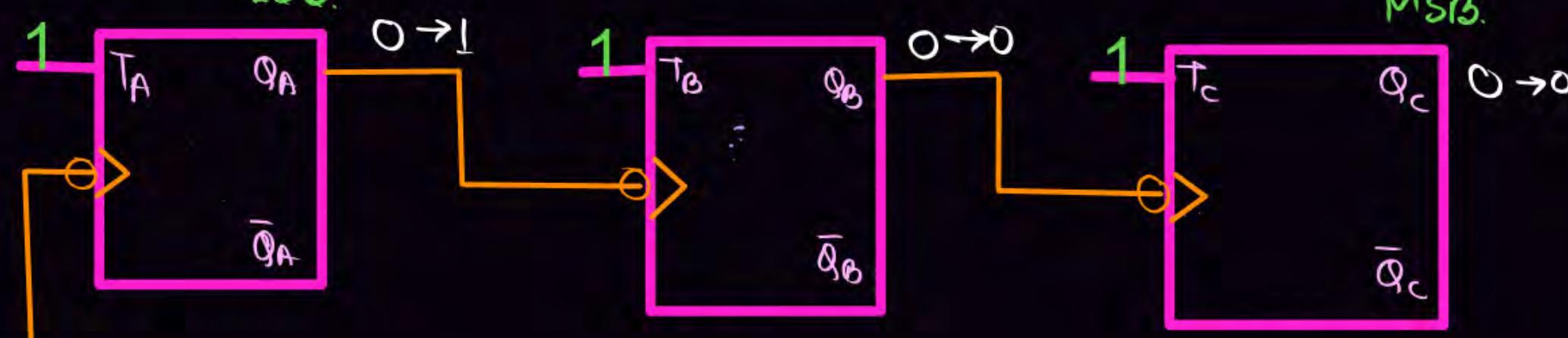
CLOCK	Q_A	Q_B	Q_C
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0
9	0	0	1
10	0	1	0

3 Bit Ripple Counter :-

MOD-8 UP

Ripple counter.

LSB.



$000 \rightarrow 001 \rightarrow 010 \rightarrow 011 \rightarrow 100 \rightarrow 101 \rightarrow 110 \rightarrow 111$

$1 \rightarrow 0$

$1 \rightarrow 0$

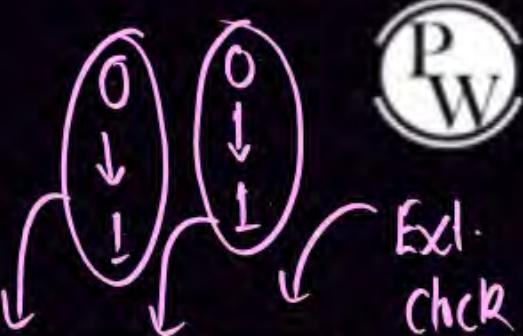
CLOCK	Q_c	Q_b	Q_a
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0
9	0	0	1

PW
Extende^d clock

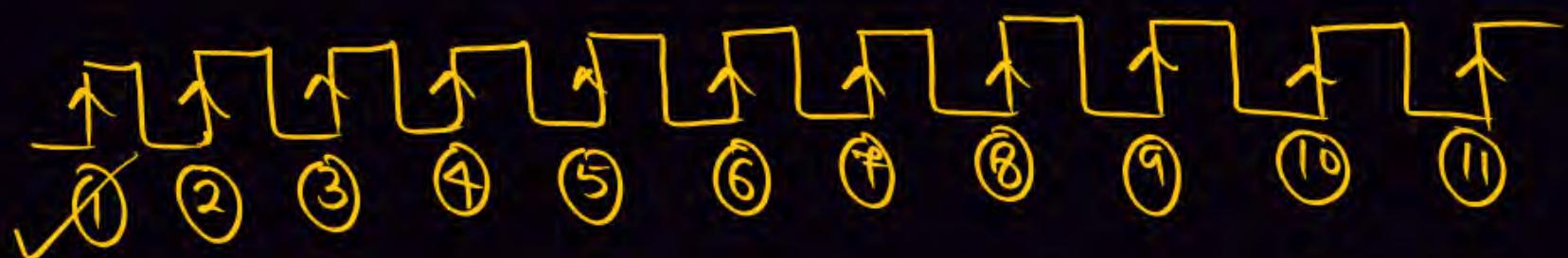
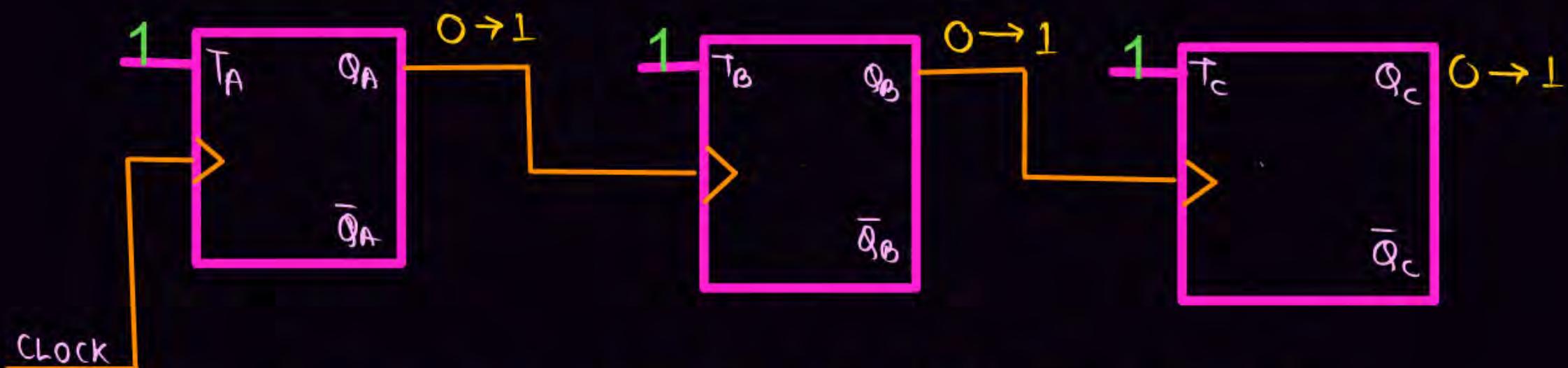
3 Bit Ripple Counter :-

$0 \rightarrow 1$

$0 \rightarrow 1$



MOD-8 DOWN RIPPLE COUNTER :-



$000 \rightarrow 111 \rightarrow 110 \rightarrow 101 \rightarrow 100 \rightarrow 011 \rightarrow 010 \rightarrow 001$



CLOCK	Q _C	Q _B	Q _A
0	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0
9	1	1	1

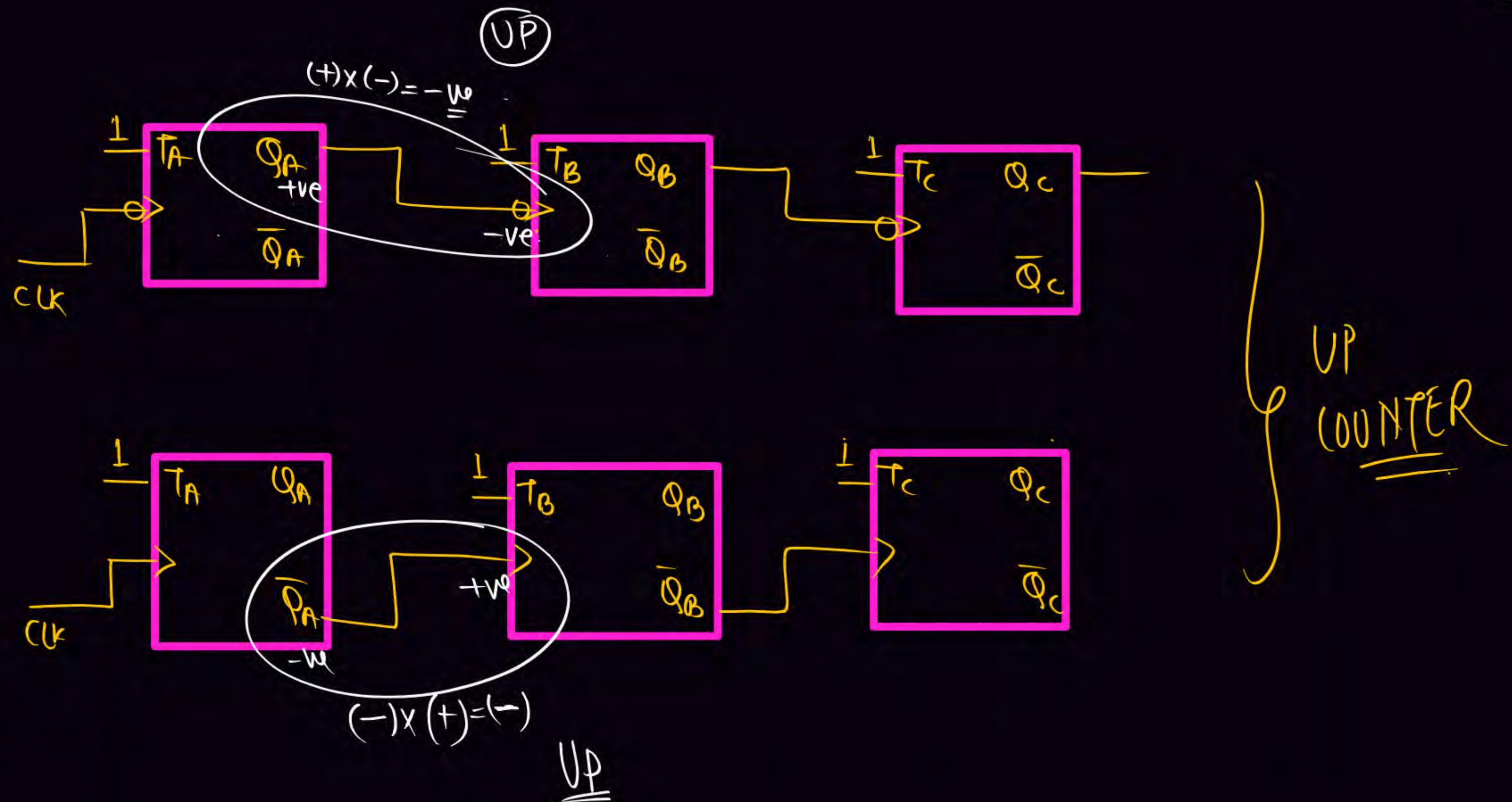
$\bar{g} \rightarrow -ve$

$o \rightarrow -ve$

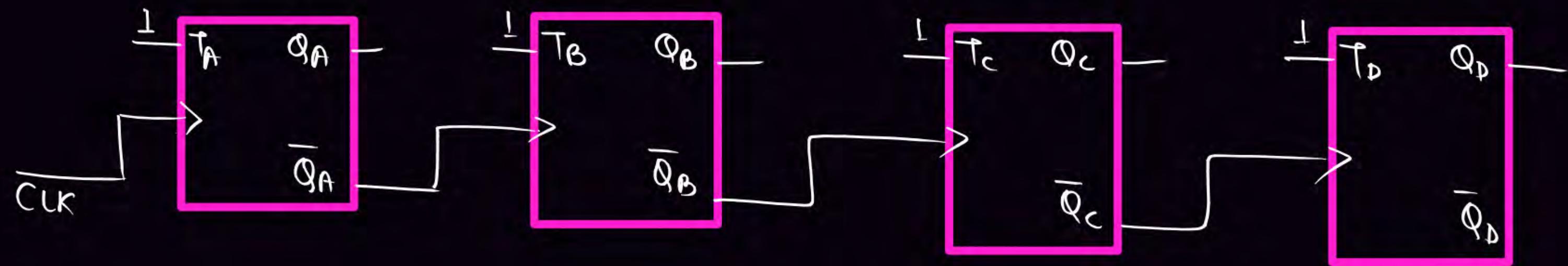
$-ve \rightarrow UP$

$+ve \rightarrow DOWN$

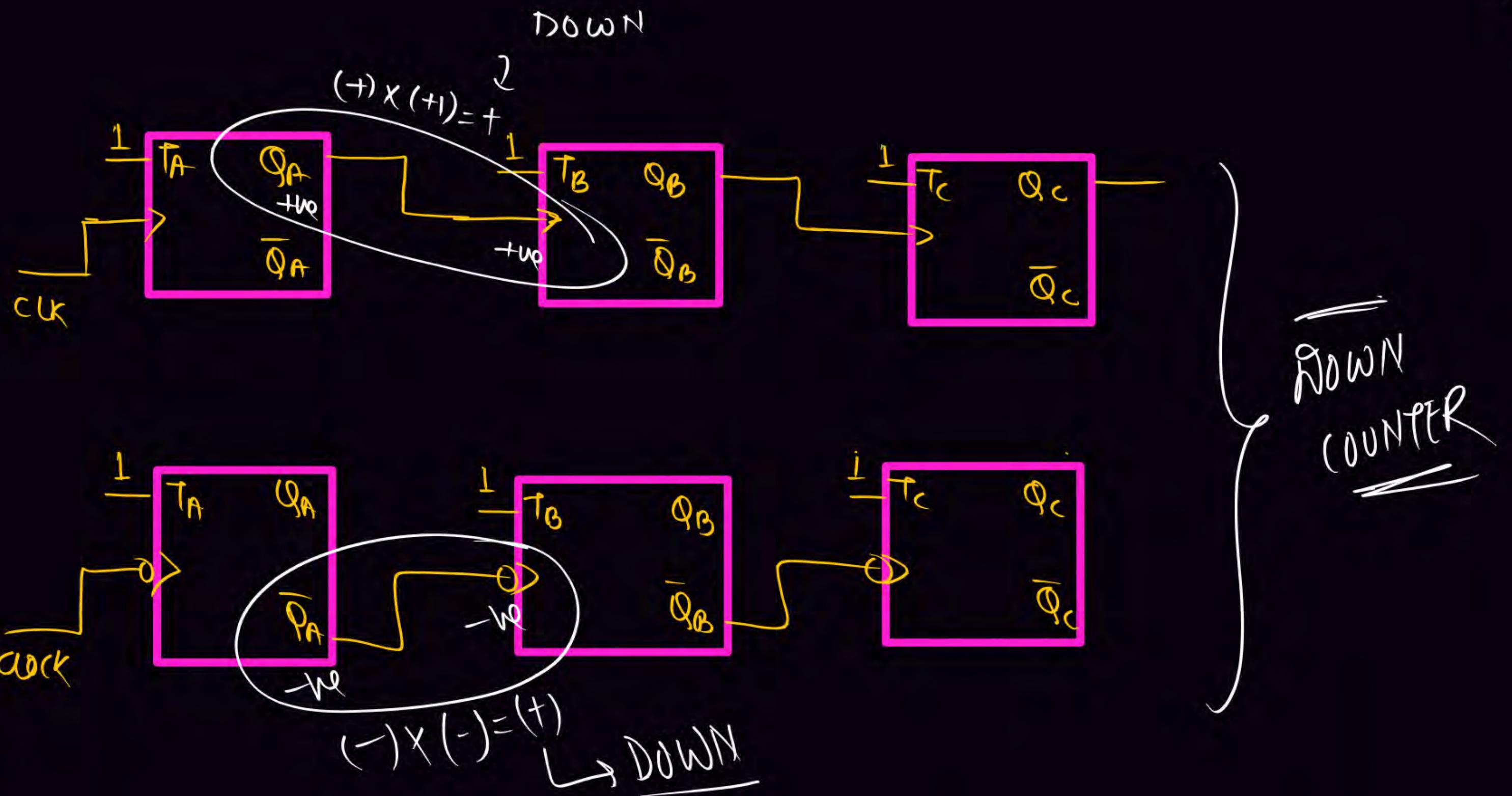
P
W



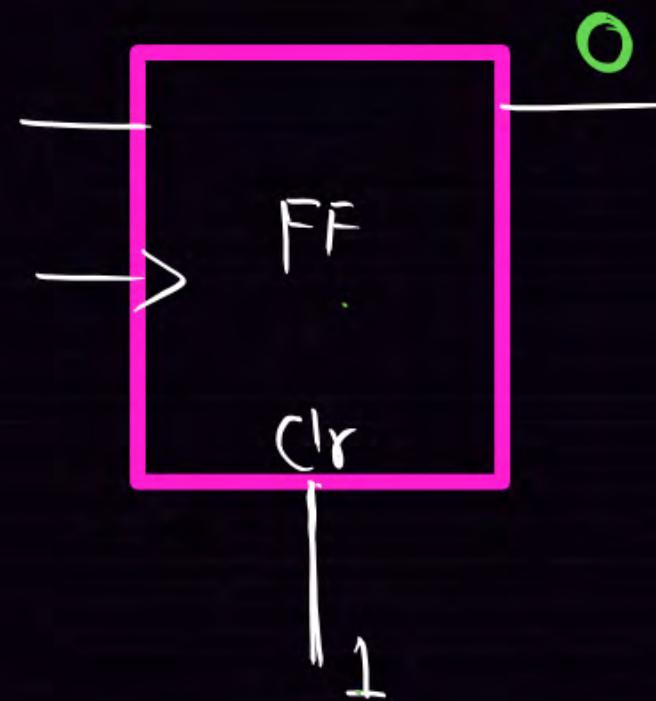
Q Design a MOD 16 UP Ripple counter in which \bar{Q} will be taken as clock?



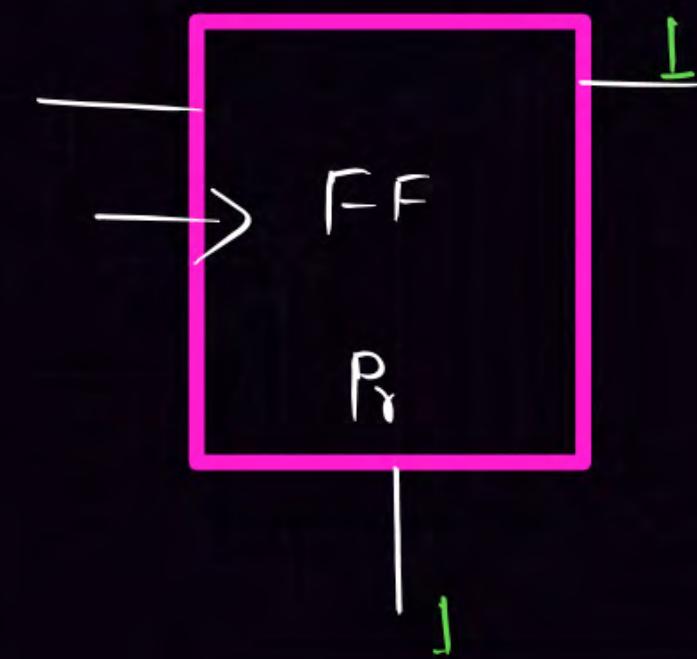
MOD-16 UP Ripple
Counter.



Reset. (clear)

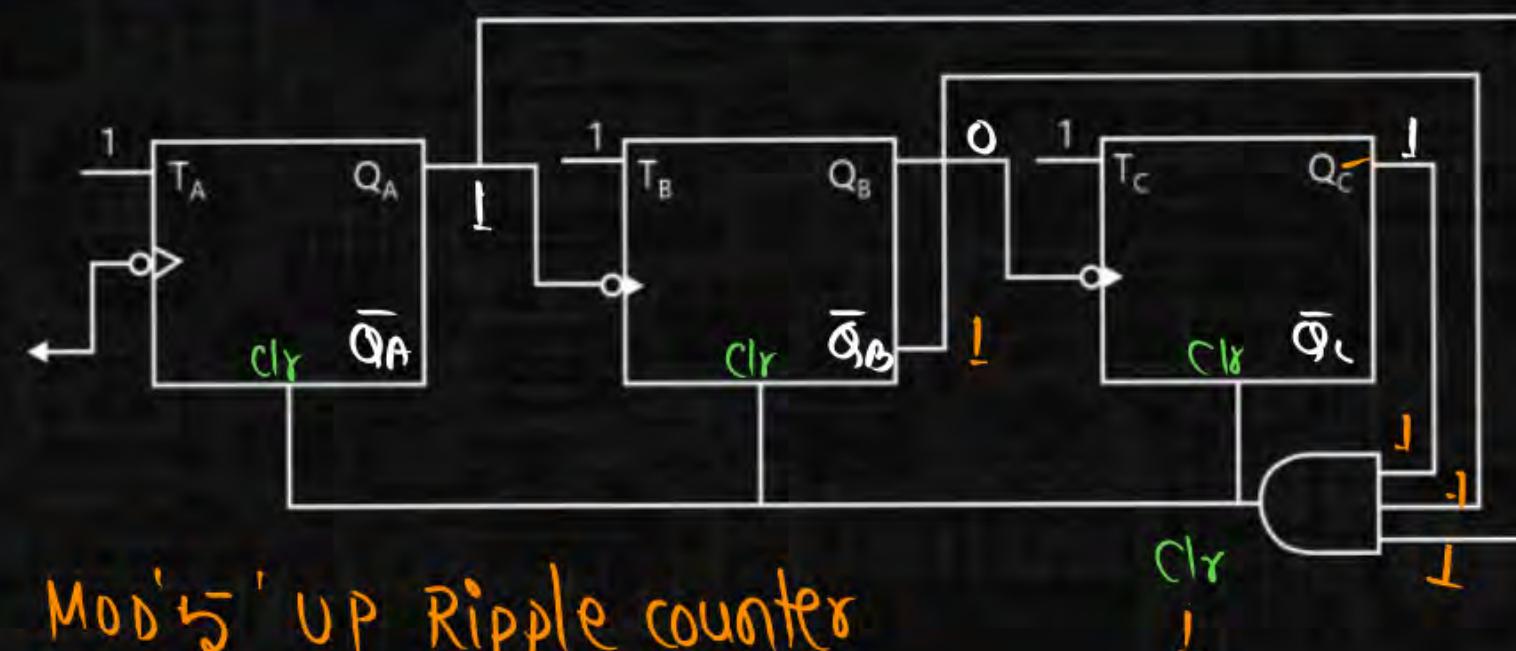


Preset.



Feedback reduces the number of states.

FEEDBACK REDUCES THE NUMBER OF STATES



Mod's UP Ripple counter

$$\text{Clr} = Q_C \bar{Q}_B Q_A$$

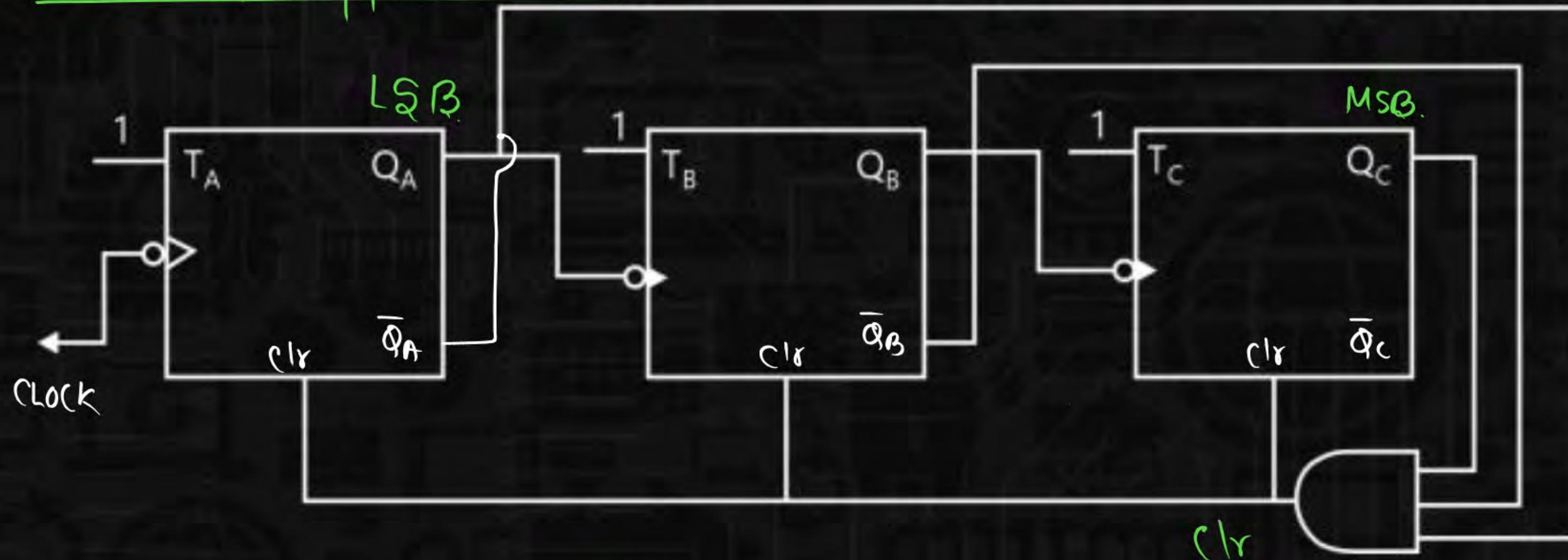
$$1 \ 0 \ 1 = 5$$

000 → 001 → 010 → 011 → 100

CLOCK	Q _C	Q _B	Q _A	Clr = Q _C Q _B Q _A
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	0	1
6	0	0	1	0
7	0	1	0	0
8	0	1	1	0
9	1	0	0	0

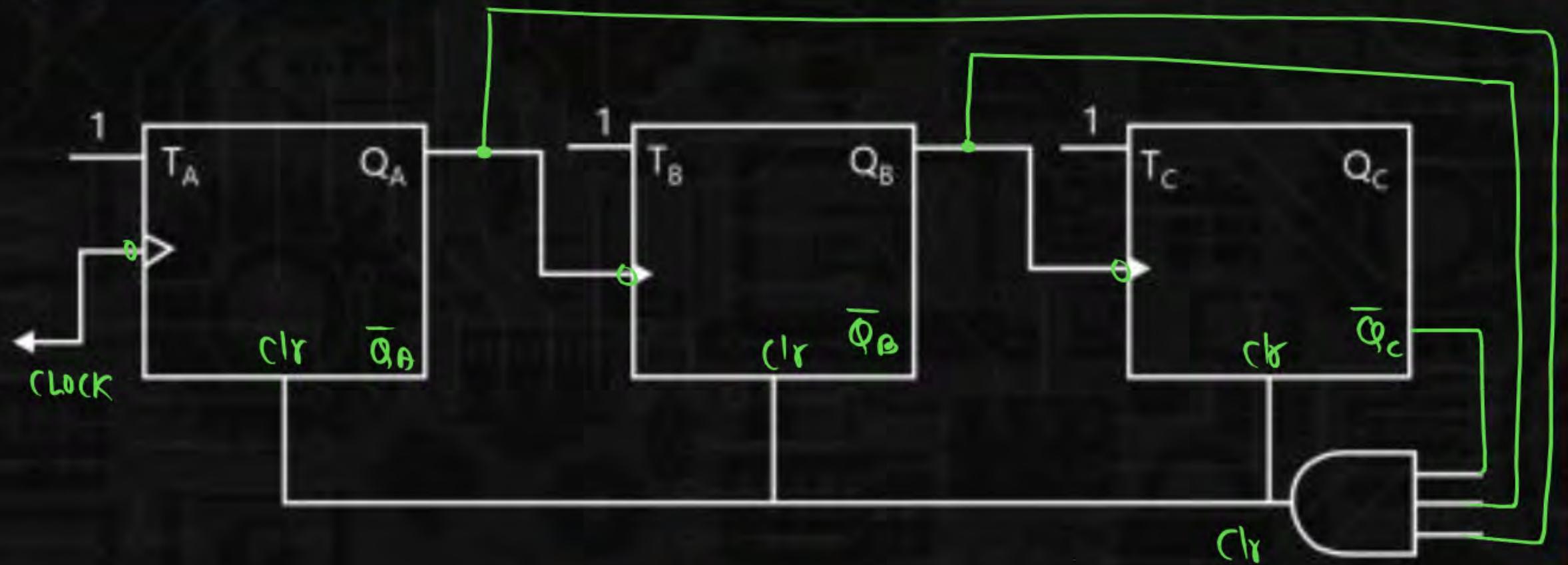
FEEDBACK REDUCES THE NUMBER OF STATES

MOD-4 UP Ripple counter :-



$$\text{clr} = \bar{Q}_C \bar{Q}_B \bar{Q}_A$$
$$1 \ 0 \ 0 = 4$$

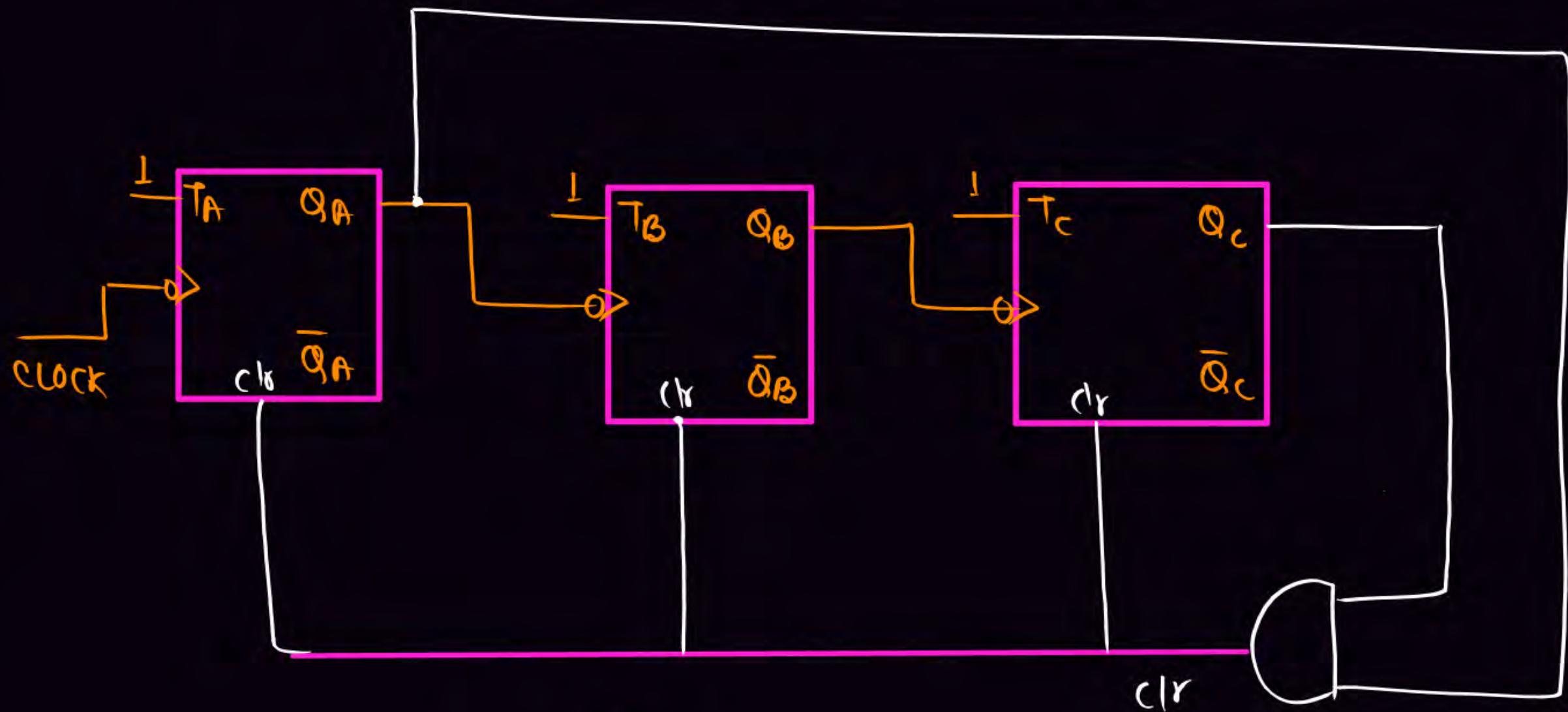
ASYNCHRONOUS COUNTER



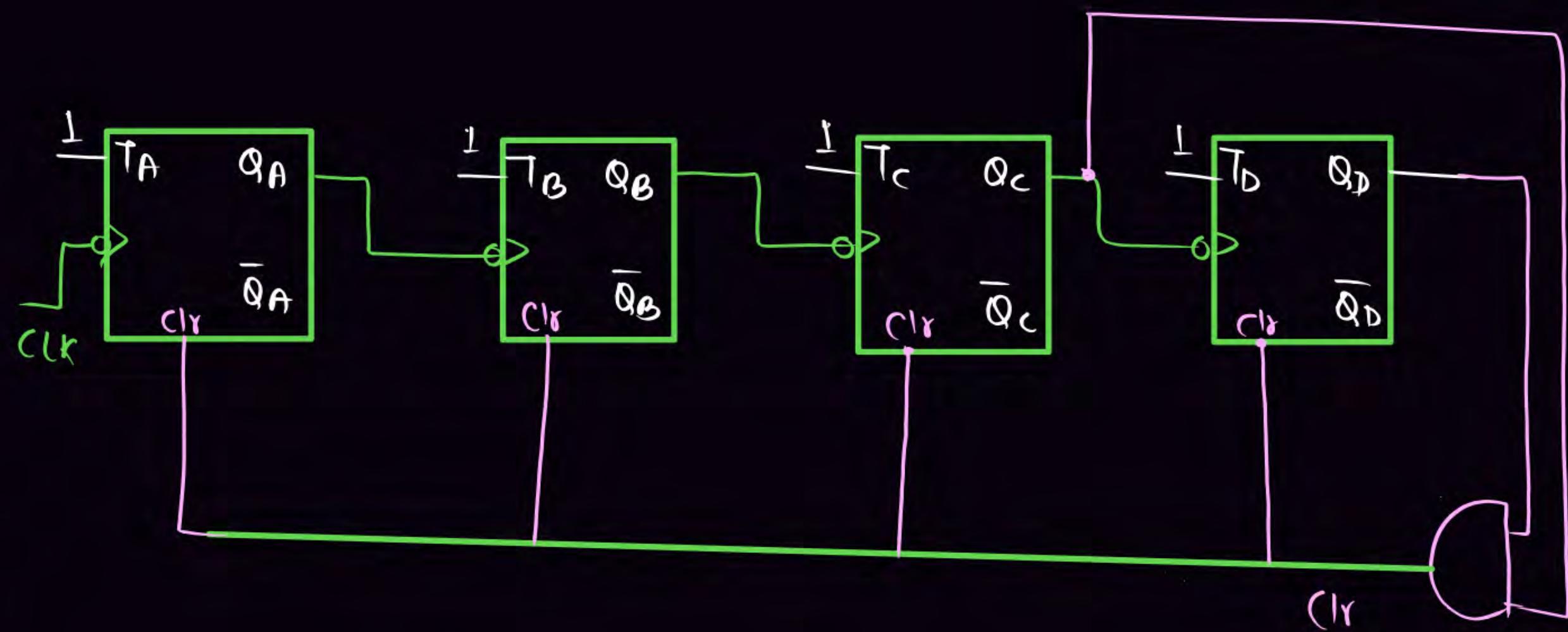
$$\text{Clr} = \overline{Q}_C \overline{Q}_B \overline{Q}_A$$

0 L J \Rightarrow MOD(3) UP Ripple
counter

CLK	0	1	2	3	4	5	6	7	8
Q _A	0	1	0	1	0	1	0	1	0
Q _B	0	0	1	0	1	0	1	0	1
Q _C	0	0	0	1	0	1	0	1	0

MOD-5 UP Ripple counter :-

$$\begin{aligned} C_{lr} &= \overline{Q}_C \overline{Q}_B \overline{Q}_A \\ &= 1 \ 0 \ 1 = 5 \end{aligned}$$


$$\text{Clr} = Q_D \bar{Q}_C \bar{Q}_B \bar{Q}_A$$

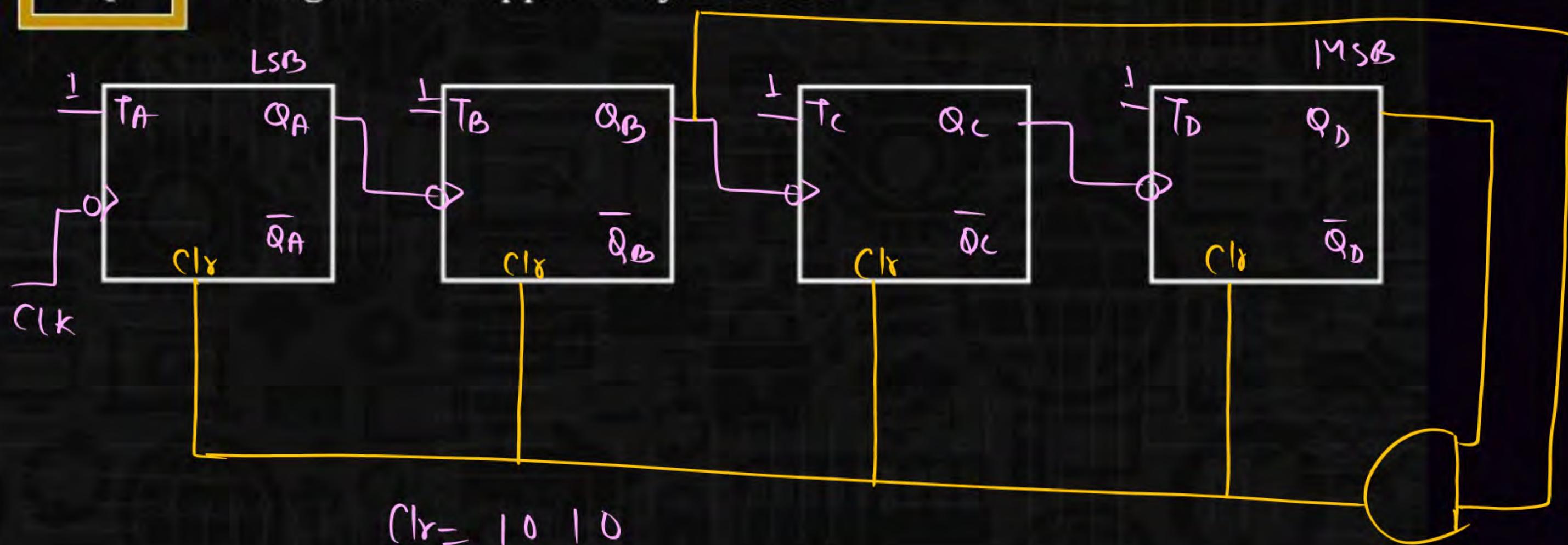
1 1 0 0 → 12 MOD-12 UP Ripple counter.

Q.

Design a BCD Ripple Carry counter?

P
W

P
W



$$Clk = 1010$$

$$Q_D \bar{Q}_C Q_B \bar{Q}_A$$

- HFO
- { Q. Design a MOD-13 UP Ripple counter?
Q. Design a MOD-23 UP Ripple counter?

