CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Basics of COA

Lecture No.- 04

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Recap of Previous Lecture

- Topic: CPU Registers
- Topic: Memory Addressing
- Topic: Memory Access

Topics to be Covered

Topic Architecture Type (Based on Size of Input)

Topic Micro Operation

Topic Memory Access

[NAT]

#Q. Consider a memory with size 64Kbytes. The address size to access memory, if memory is word addressable(1 word = 2 bytes), is 15 bits?

$$\text{no. of cells} = \frac{64\text{kB}}{2\text{B}} = 32\text{k} = 2^5 \cdot 2^{10} = 2^{15}$$

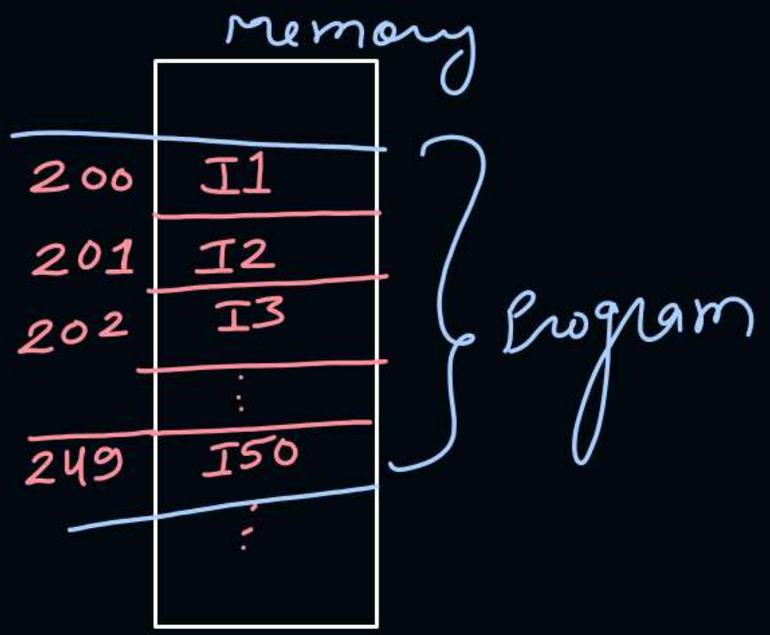
add. = 15 bits

How instructions stored in memory :-

Ex ① :-

Mem ⇒ byte addressable

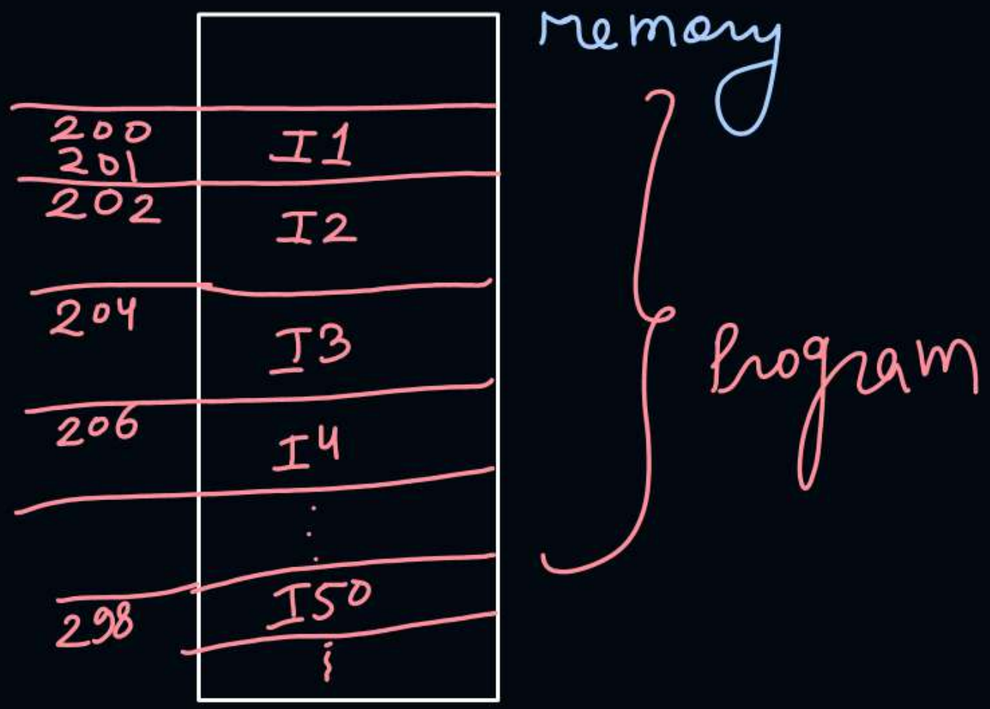
inst^{n}. size ⇒ 1 Byte



Ex :- ② :-

Mem ⇒ byte addressable

instruction size = 2 bytes

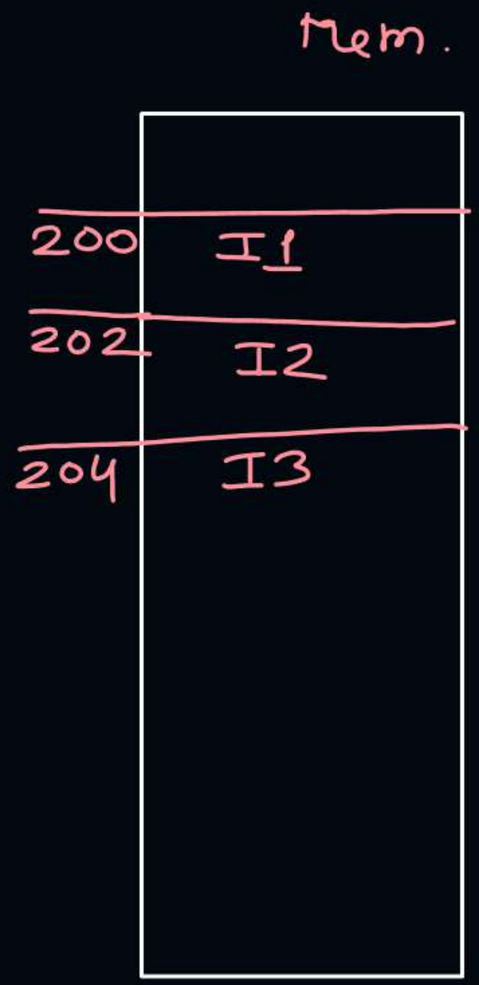


ex (3) :-

Inst^{n} size = 4 bytes

mem. ⇒ word addressable

word = 2 bytes



[NAT]

default mem. ⇒ byte addressable

#Q. A CPU has 4 bytes instructions. A program (Instructions I_1 to I_{200}) starts at address 200 (in decimal). Find the address of following instructions:

1. I_1 ⇒ 200
2. I_5 ⇒ 216
3. I_{120} ⇒ 676

$200 + ((120-1) * 4)$

$= 200 + 476$

$= 676$

[NAT]

Ans = 524

#Q. A CPU has 4 bytes instructions. A program (Instructions I_1 to I_{200}) starts at address 500 (in decimal). What should be the PC value when instruction I_6 will be executing in CPU?

while I_6 is in execution then I_7's address will be in PC.

add. of inst^n I_7 = (7 − 1) * 4 + 500

= 524 Ans.

[NAT]

#Q. A CPU has 4 bytes instructions. A program (Instructions I_1 to I_{200}) starts at address 500 (in decimal). What should be the PC value when instruction i will be executing in CPU?

when instⁿ i is in execution
PC stores add. of $(i+1)$

add. of $(I+1) = (I+1-1) * 4 + 500$

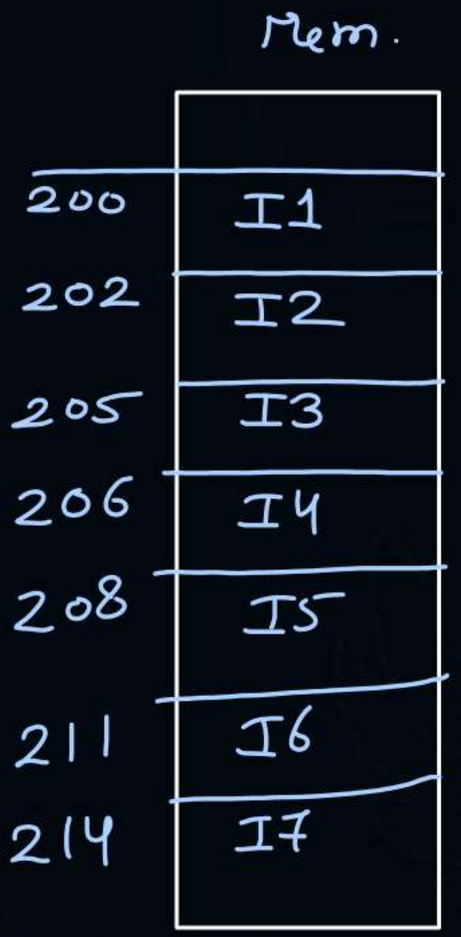
$= 500 + 4i$

Topic : Address of Variable Size Instructions

ex:-

Memory ⇒ byte addressable

Instⁿ	size
I1	2 bytes
I2	3 bytes
I3	1 byte
I4	2 bytes
I5	3 bytes
I6	3 bytes



Topic : Micro Operation

→ smallest operat^{n} CPU can perform at a time.

- The operations executed on values stored in registers
- Symbolic Notation to describe the micro-ops: Register Transfer Language (RTL)

Topic : Micro Operation

$R1 \leftarrow 5$
$R2 \leftarrow 85$

- Register Transfer: $R2 \leftarrow R1$
- Comma: $R2 \leftarrow R1$, $PC \leftarrow PC + 1$ (both can be done in parallel)
- Memory Transfer:

Memory Read :-

Register ← memory

DR ← M[address]

DR ← M[500]

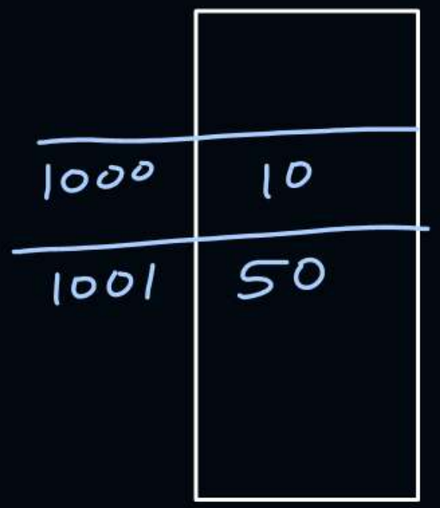
DR ← M[AR]

Memory write :-

M[address] ← DR

---

ex :-



R1 ← M[1000] R1 = 10

AR = 1001

R3 ← M[AR]

R3 = 50

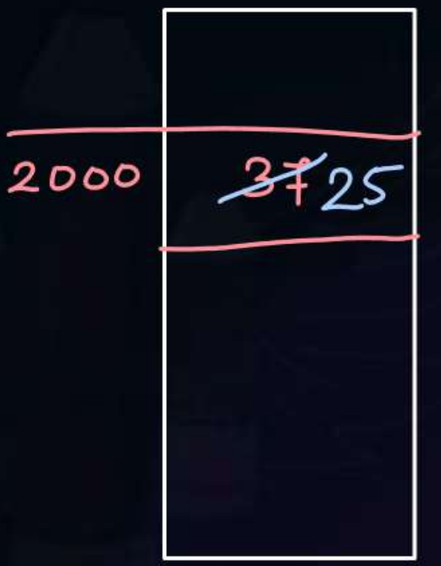
[NAT]

Ans = 25

#Q. Consider the following program segment. Here R1 and R2 are the general purpose register. Assume that the content of memory location 2000 is 37. All numbers are in decimal. After the execution of this program the value of memory location 2000 is?

R1 = 12
R2 = ~~37~~ 25

Instructions	Operations
MOV R1, #12	R1 ← #12
MOV R2, (2000)	R2 ← M[2000]
SUB R2, R1	R2 ← R2 – R1
MOV (2000), R2	M[2000] ← R2
HALT	Stop



[NAT]

Ans = 27

#Q. Consider the following program segment. Here R1 and R2 are the general purpose register. Assume that the content of memory location 3000 is 13. All numbers are in decimal. After the execution of this program the value of memory location 3000 is?

Instructions	Operations
MOV R1, #7	R1 ← #7
MOV R2, (3000)	R2 ← M[3000]
ADD R2, R1	R2 ← R2 + R1
ADD R1, R2	R1 ← R1 + R2
MOV (3000), R1	M[3000] ← R1
HALT	Stop

R1 = ~~7~~ 27

R2 = ~~13~~ 20

Note :-

conditions are checked on just prev. inst$^{n's}$ result.

[NAT]

Ans = 23

#Q. Consider the following program segment. Here R1 and R2 are the general-purpose register. Assume that the content of memory location 1000 is 5. All the numbers are in decimal.

	Instructions	Operations
	MOV R1, (1000)	R1 ← M[1000]
	MOV R2, #8	R2 ← #8
LOOP:	ADD R2, R1	R2 ← R2 + R1
	DEC R1	R1 ← R1 – 1
	BNZ LOOP	Branch on not zero
	HALT	Stop

R1 = 5 4 3 2 1 0

R2 = 8 13 17 20 22 23

The value of R2 at the end of program execution is?

[MCQ] GATE- PYQ 2007

#Q. Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1, (3000)	R1 ← M[3000]	2
LOOP:	MOV R2, (R3)	R2 ← M[R3]	1
	ADD R2,R1	R2 ← R1 + R2	1
	MOV (R3),R2	M [R3] ← R2	1
	INC R3	R3 ← R3 + 1	1
	DEC R1	R1 ← R1 – 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. The number of memory reference for accessing the data in executing the program completely is

A 10

B 11

C 20

D 21

R1 = ~~105~~ 7

R2 = ~~100 110~~ ~~100 100~~ ~~100 109~~ ~~108~~ 107

R3 = ~~2000~~ ~~2001~~ ~~2002~~ 2003

Loop runs 10 times.

No. of mem. references

= 1 + (2 * 10)

= 21

[MCQ]

#Q. Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1, (3000	R1 ← M[3000]	2
LOOP:	MOV R2, (R3)	R2 ← M[R3]	1
	ADD R2,R1	R2 ← R1 + R2	1
	MOV (R3),R2	M [R3] ← R2	1
	INC R3	R3 ← R3 + 1	1
	DEC R1	R1 ← R1 – 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is:

A 100

B 101

C 102

D 110

[MCQ]

#Q. Consider the following program segment. Here R1, R2 and R3 are the general-purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1, (3000)	R1 ← M[3000]	2
LOOP:	MOV R2, (R3)	R2 ← M[R3]	1
	ADD R2,R1	R2 ← R1 + R2	1
	MOV (R3),R2	M [R3] ← R2	1
	INC R3	R3 ← R3 + 1	1
	DEC R1	R1 ← R1 – 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Home work.

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction "INC R3", what return address will be pushed on the stack?

A 1005

B 1020

C 1024

D 1040

If an interrupt occurs during execution of an inst^{n}.
then CPU completes current inst^{n},
CPU stores add. of next inst^{n} on to stack,
CPU goes for interrupt service.

[NAT]

GATE- PYQ 2001

#Q. Consider the following instruction sequence where registers R1, R2 and R3 are general purpose and MEMORY [X] denotes the content at the memory location X.

	Instruction	Semantics	Instruction Size (bytes)
1000	MOV R1, (5000)	R1 ← MEMORY[5000]	4
1004	MOV R2, (R3)	R2 ← MEMORY[R3]	4
1008	ADD R2, R1	R2 ← R1 + R2	2
1010	MOV (R3), R2	MEMORY[R3] ← R2	4
1014	INC R3	R3 ← R3 + 1	2
1016	DEC R1	R1 ← R1 – 1	2
1018	BNZ 1004	Branch if not zero to the given absolute address	2
1020	HALT	Stop	1

Assume that the content of the memory location 5000 is 10, and the content of the register R3 is 3000. The content of each of the memory locations from 3000 to 3010 is 50. The instruction sequence starts from the memory location 1000. All the numbers are in decimal format. Assume that the memory is byte addressable.

After the execution of the program, the content of memory location 3010 is 50.

2 mins Summary

Topic Micro Operation

Topic Memory Access

Happy Learning

THANK - YOU