CS & IT ENGINEERING

DIGITAL LOGIC

Sequential Circuit

Lecture No. 08

By- CHANDAN SIR

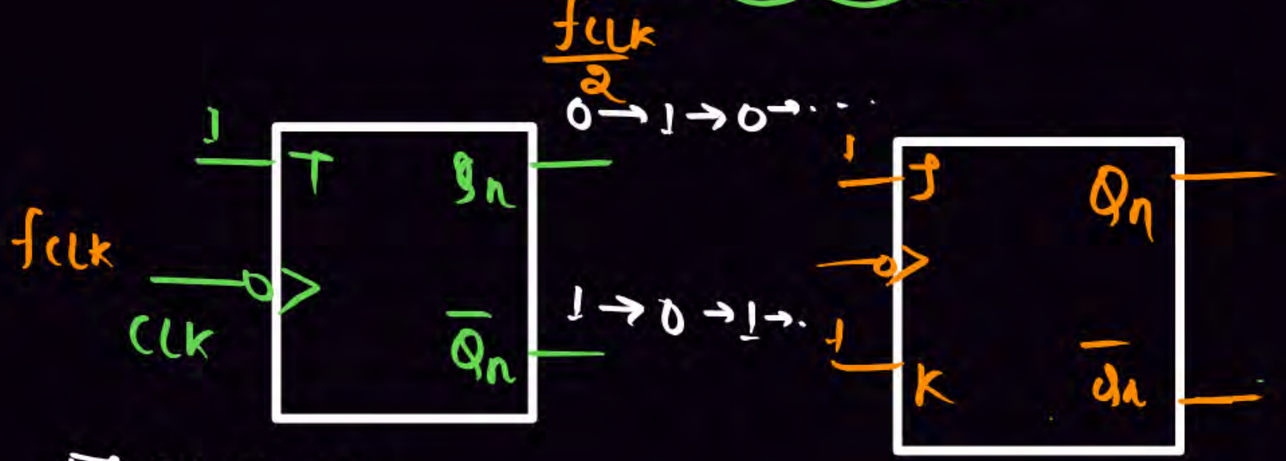
01 Counters

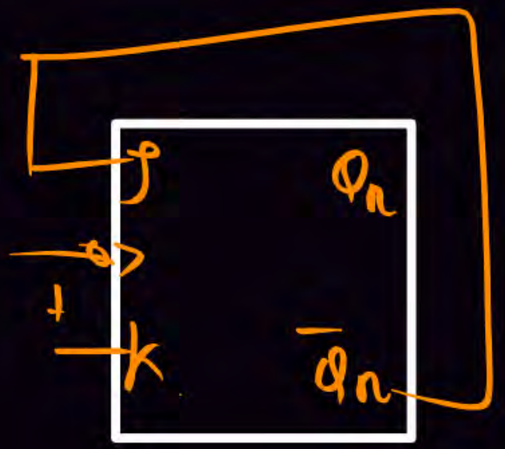
02 PRACTICE

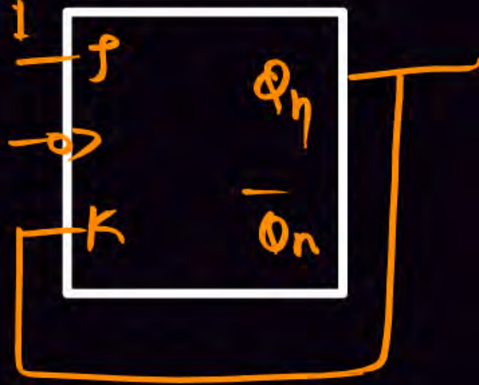
03 DISCUSSION

→ Toggle Mode of the FF

$Q_{n+1} = \bar{Q}_n$







$Q_{n+1} = T \oplus Q_n$

$Q_{n+1} = 1 \oplus Q_n$ $T=1$

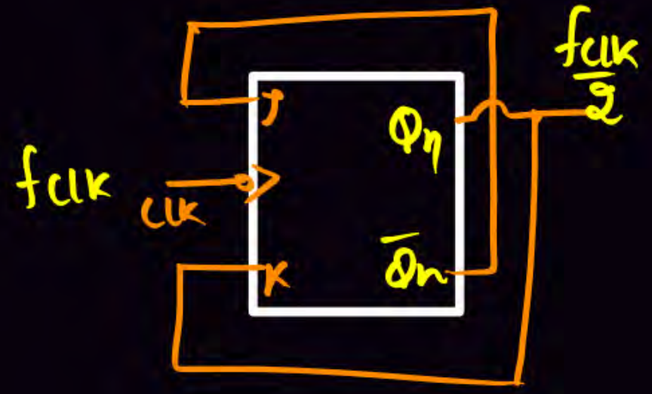
$\boxed{Q_{n+1} = \bar{Q}_n}$

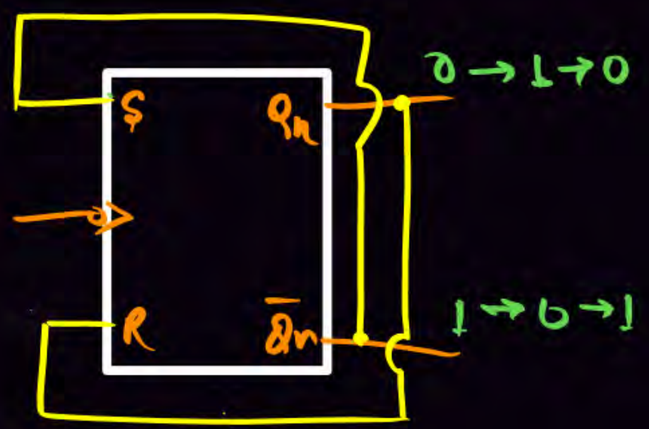
$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$

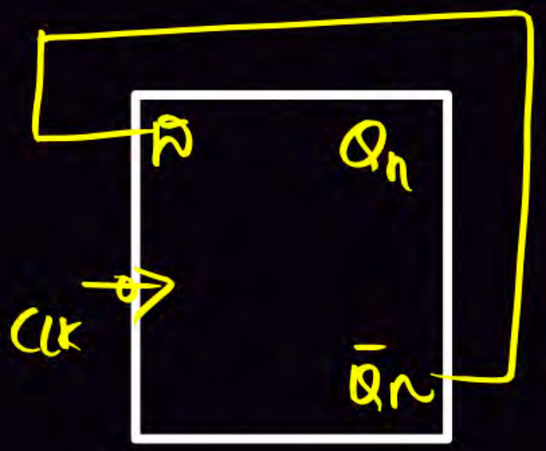
$J=1 \quad K=1$

$Q_{n+1} = 1 \cdot \bar{Q}_n + 0 \cdot Q_n$

$\boxed{Q_{n+1} = \bar{Q}_n}$







$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

$$J = \bar{Q}_n \quad K = Q_n$$

$$Q_{n+1} = \bar{Q}_n \cdot \bar{Q}_n + \bar{Q}_n Q_n$$

$$Q_{n+1} = \bar{Q}_n$$

$$Q_{n+1} = S + \bar{R}Q_n$$

$$S = \bar{Q}_n \quad R = Q_n$$

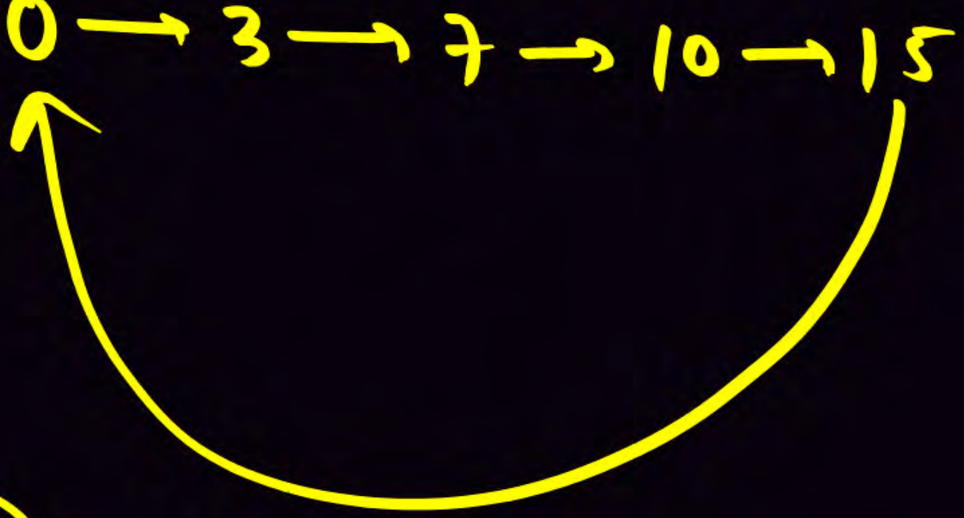
$$Q_{n+1} = \bar{Q}_n + \bar{Q}_n Q_n$$

$$Q_{n+1} = \bar{Q}_n$$

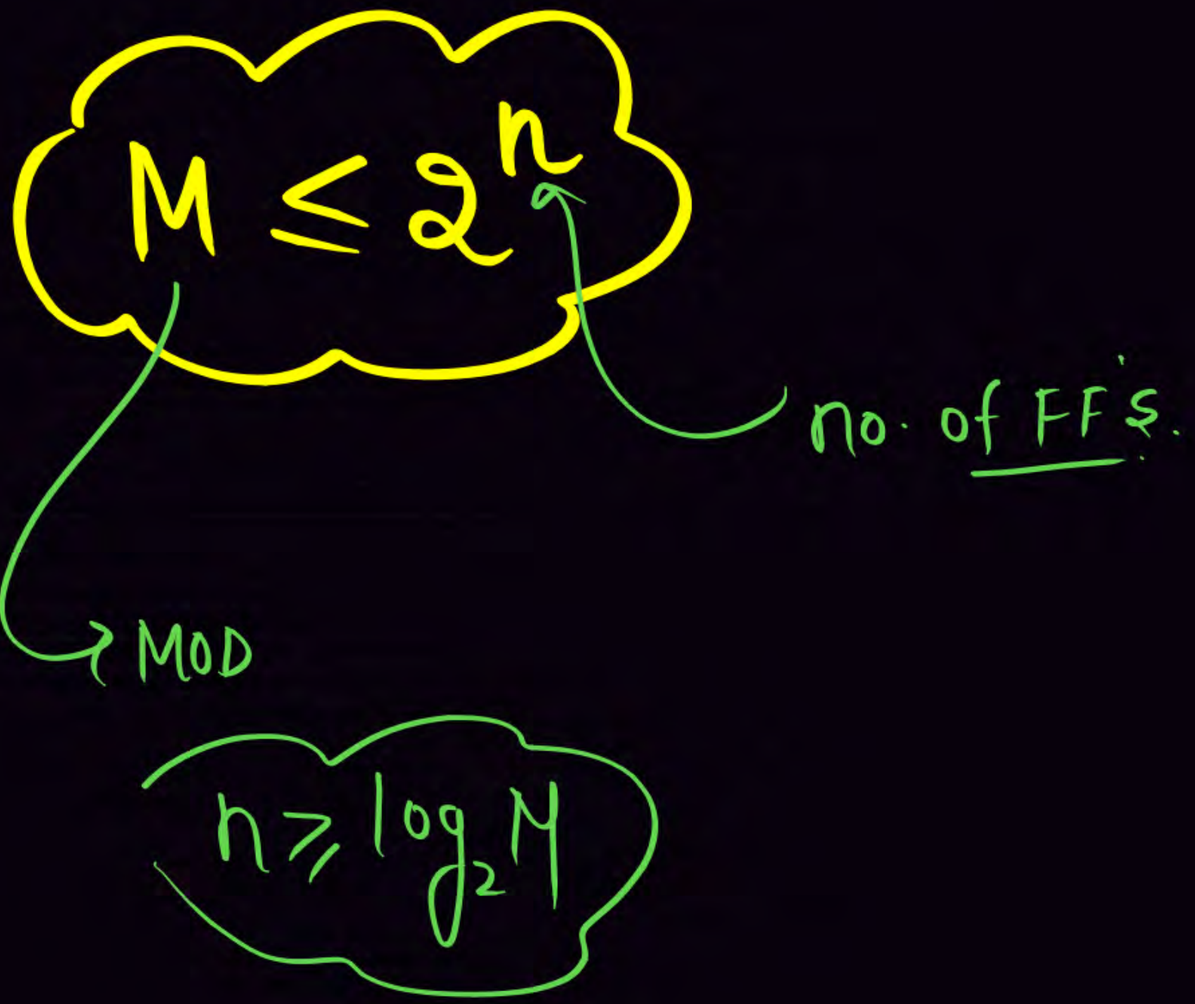
'n' ⟶ no. of FF

Maximum no. of states = 2^n

MOD



MOD = 5


$M \leq 2^n$
no. of FF's.
MOD
$n \geq \log_2 M$

Register

→ use to store group of bits.

→ n FF's are required to store 'n' bits.

Shift Register

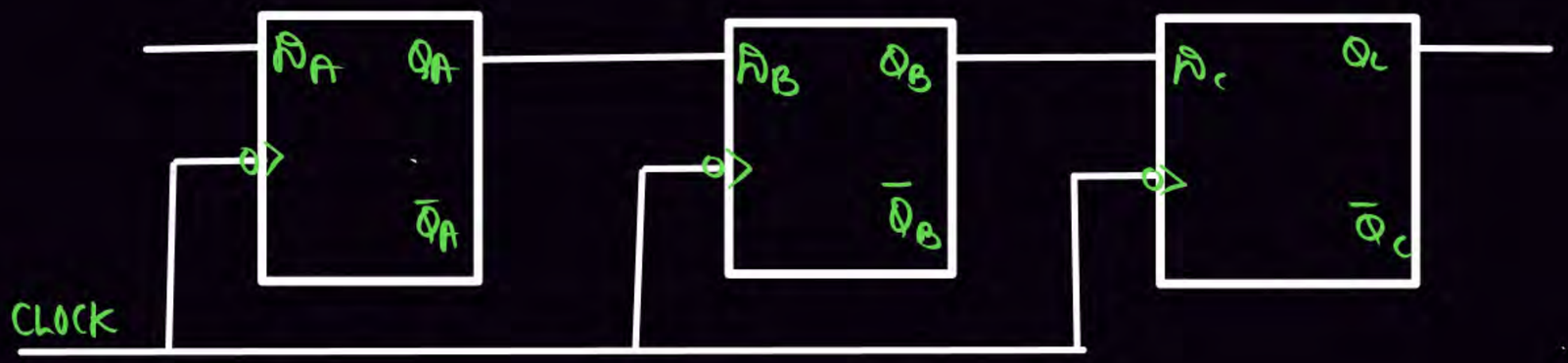
1. Serial input serial output Shif Register [SISO]
2. Serial input parallel output shift Register [SIPO]
3. Parallel input serial output shift Register [PISO]
4. Parallel input Parallel output shift Register [PIPO]

① SISO SHIFT REGISTER

3bit

1 0 1

INPUT →



→ OUTPUT

Clock	1 0 1	Q_A	Q_B	Q_C
0		0	0	0
1		1	0	0
2.		0	1	0
3.		1	0	1

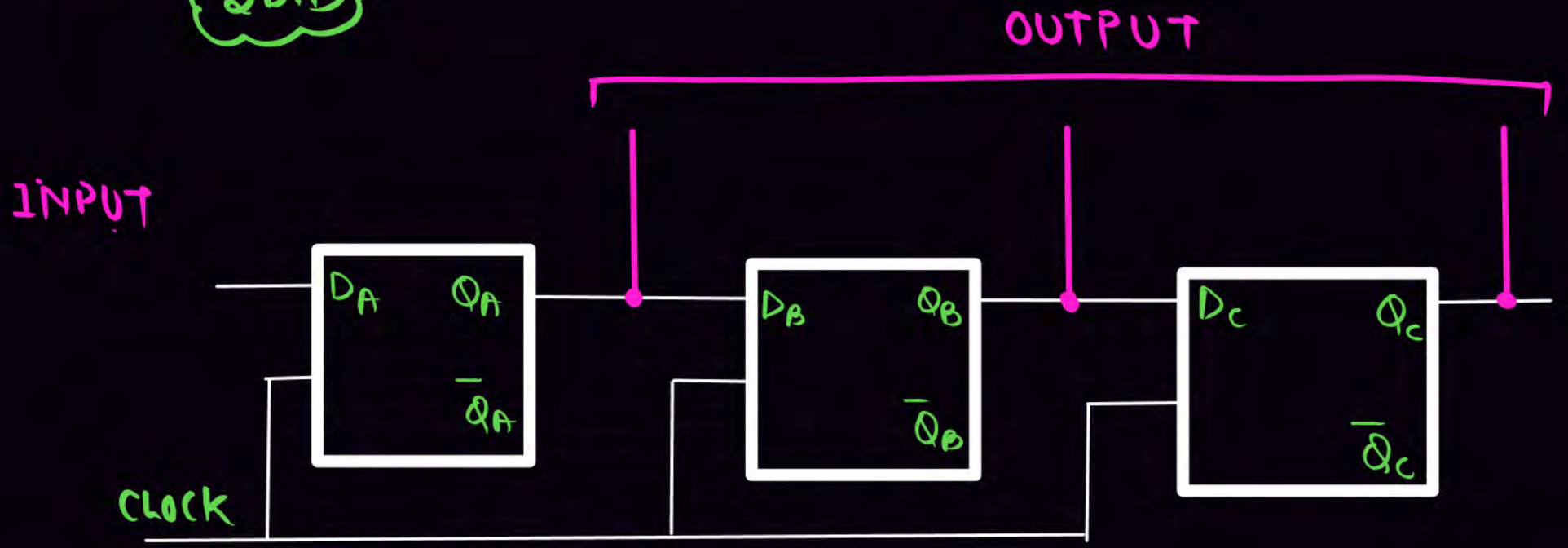
① To store 'n' bits in n bit SISO minimum n clocks are required.

② To Retrive n bits from 'n' bit SISO minimum (n-1) Clocks are required.

③ It is the slowest shift Register.

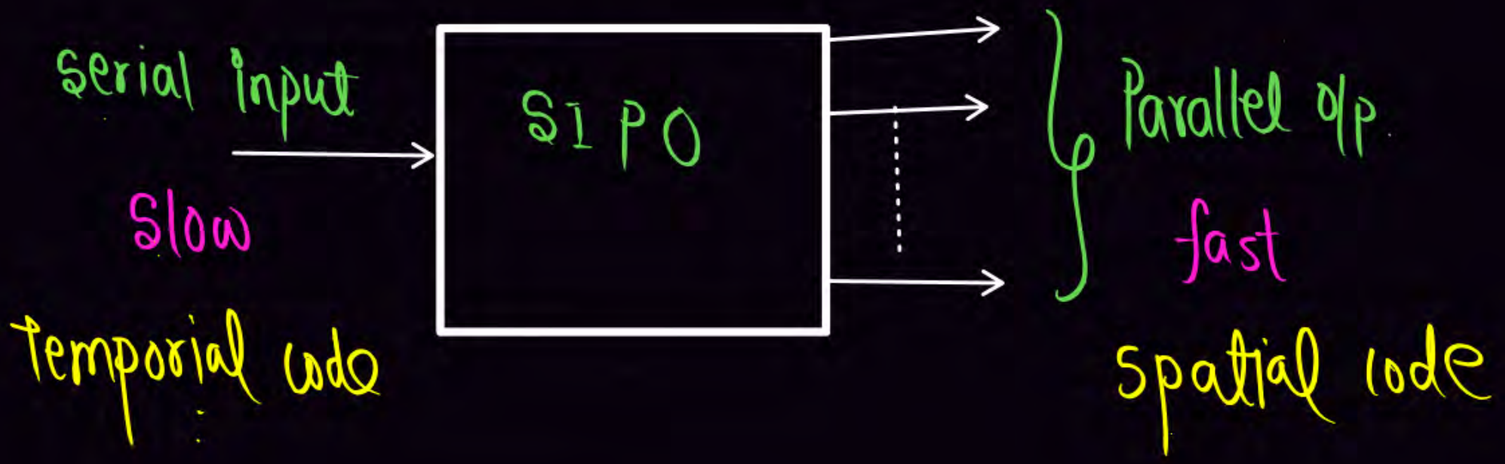
② SIPO SHIFT REGISTER

3bits



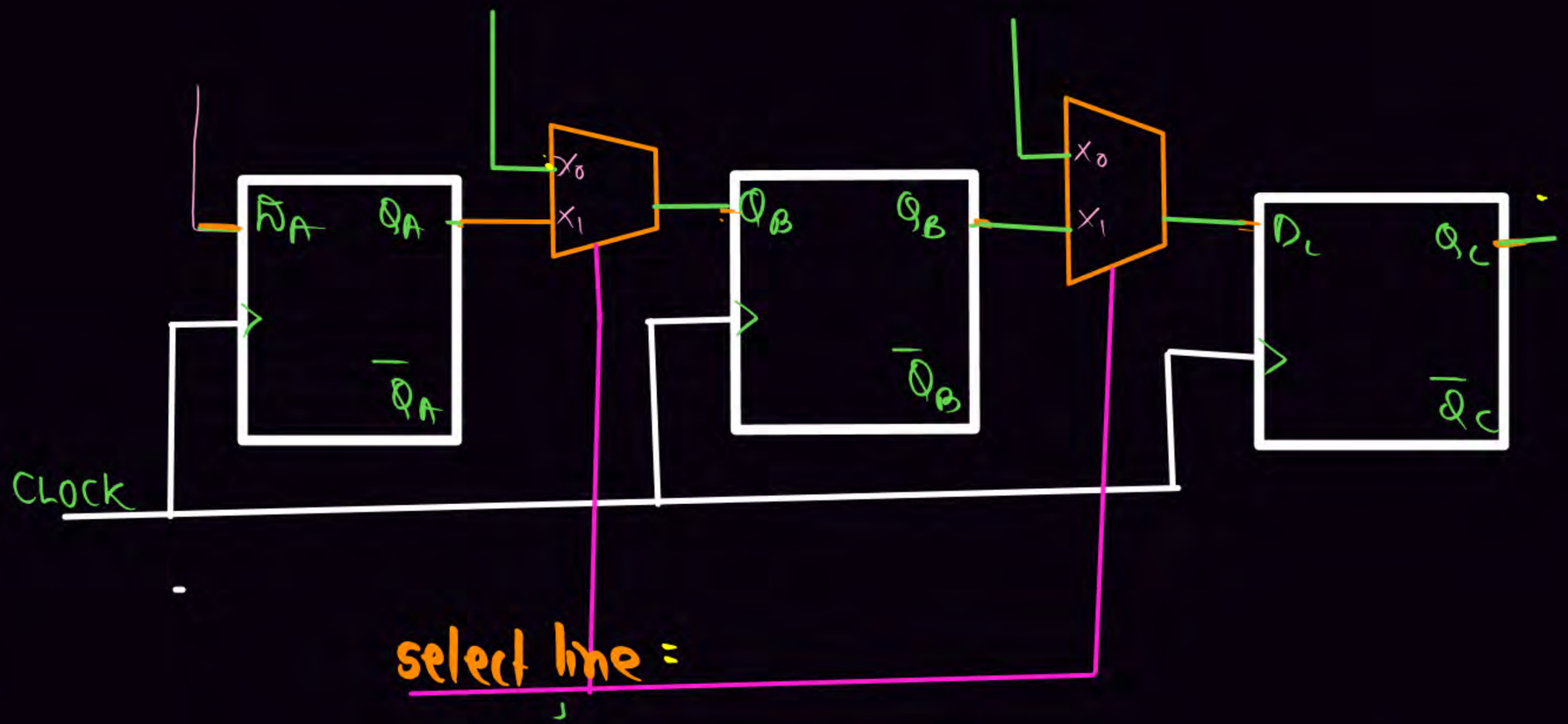
① To store 'n' bit in n bit SIPO minimum 'n' clocks are required.

② To Retrive n bits from n bit SIPO there is no clock requirment.



③ PISO SHIFT REGISTER

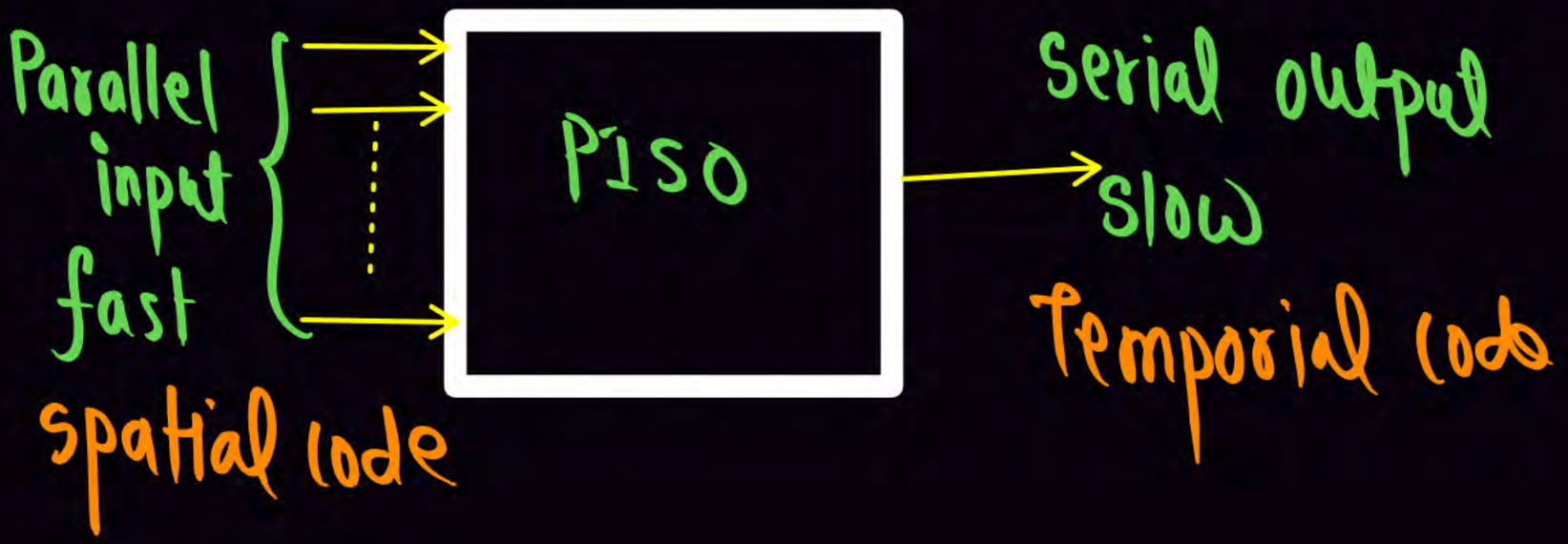
3 bits



① To store 'n' bits in 'n' bit PISO minimum one clock is required.

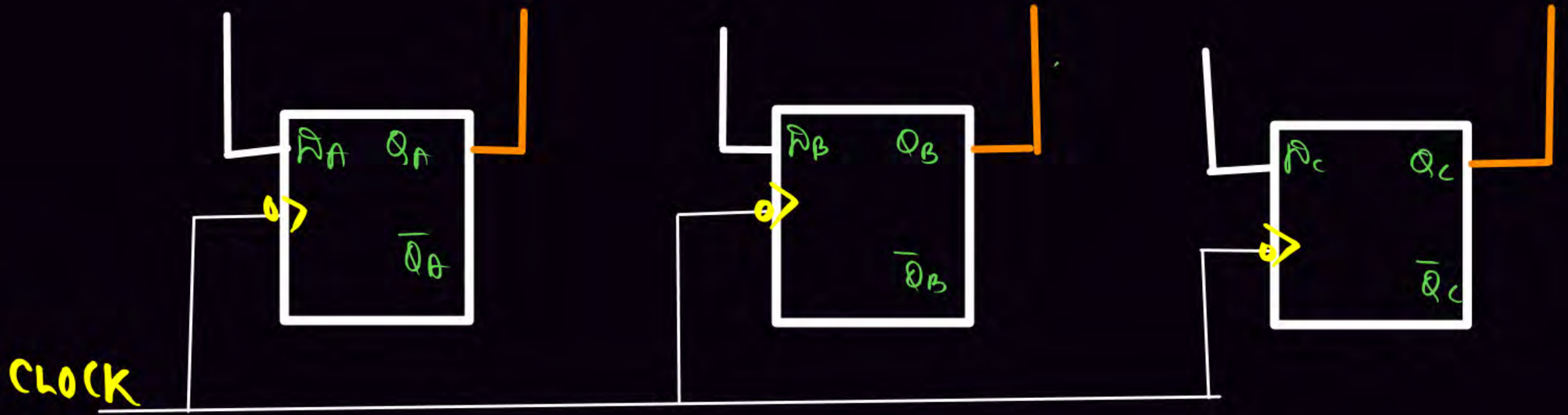
② To Retrive 'n' bits from n bit PISO, minimum (n-1) clocks are required.

③



④ PIPO SHIFT REGISTER

3bit



① To store n bits in n bit PIPO there is one clock required.

② To Retrive 'n' bit from n bit PIPO, there is no clock requirement.

③ PIPO is the fastest shift Register.

	Store	Retrive	Total	
SISO	n	n-1	2n-1	→ Slowest
SIPO	n	0	n	
PISO	1	n-1	n	
PIPO	1	0	1	→ Fastest

Thank you

GW

Soldiers !