



CS & IT ENGINEERING

Digital Logic

Logic Gate



Lecture No. 1



By- CHANDAN SIR

TOPICS TO BE COVERED

- 01 Syllabus
- 02 Weightage
- 03 Reference Books
- 04 NOT GATE

CS & IT ENGINEERING

Digital Logic

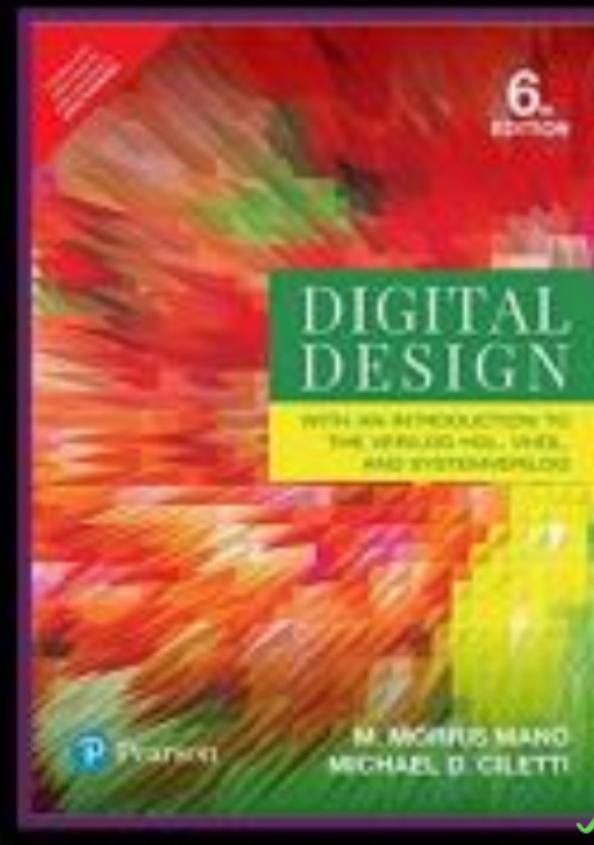
Boolean algebra. Combination and sequential circuits. Minimization.
Number representations and computer arithmetic (fixed and floating point).

2023 → 6

DIGITAL LOGIC

Number of Questions	2 to 4
Marks	4 to 6
Frequently Asked Topics	Boolean algebra. Combinational and sequential circuits. Minimization. Number representation.

Reference Books



Unsolved

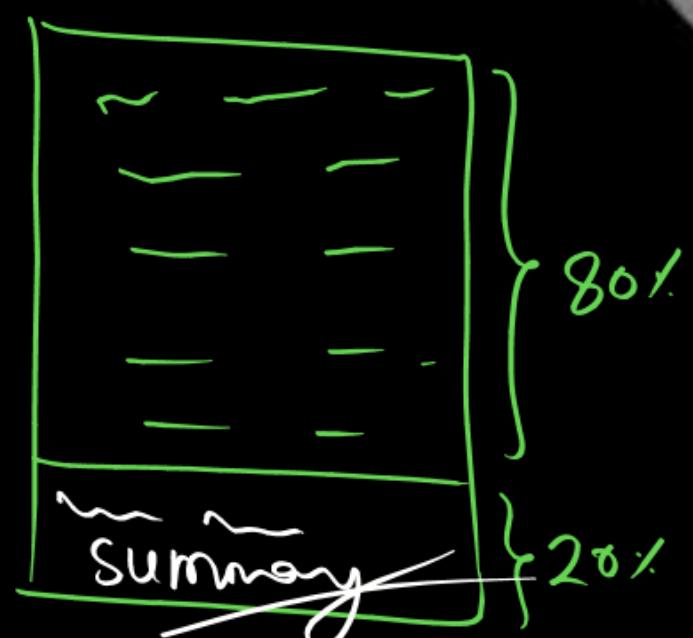


Book Name: Digital Design
Author: M. Morris Mano &
Michael D. Ciletti
Publisher: Pearson Publisher

Book Name: Digital,
fundamental
Author: Thomas L. Floyd
Publisher: Pearson Publisher

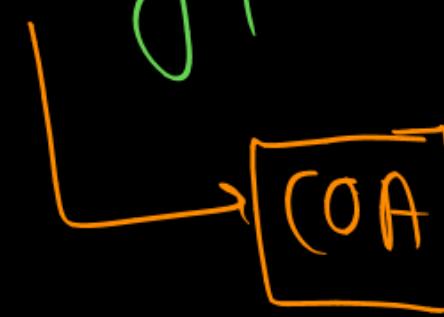
Guidelines to Attend Live Class

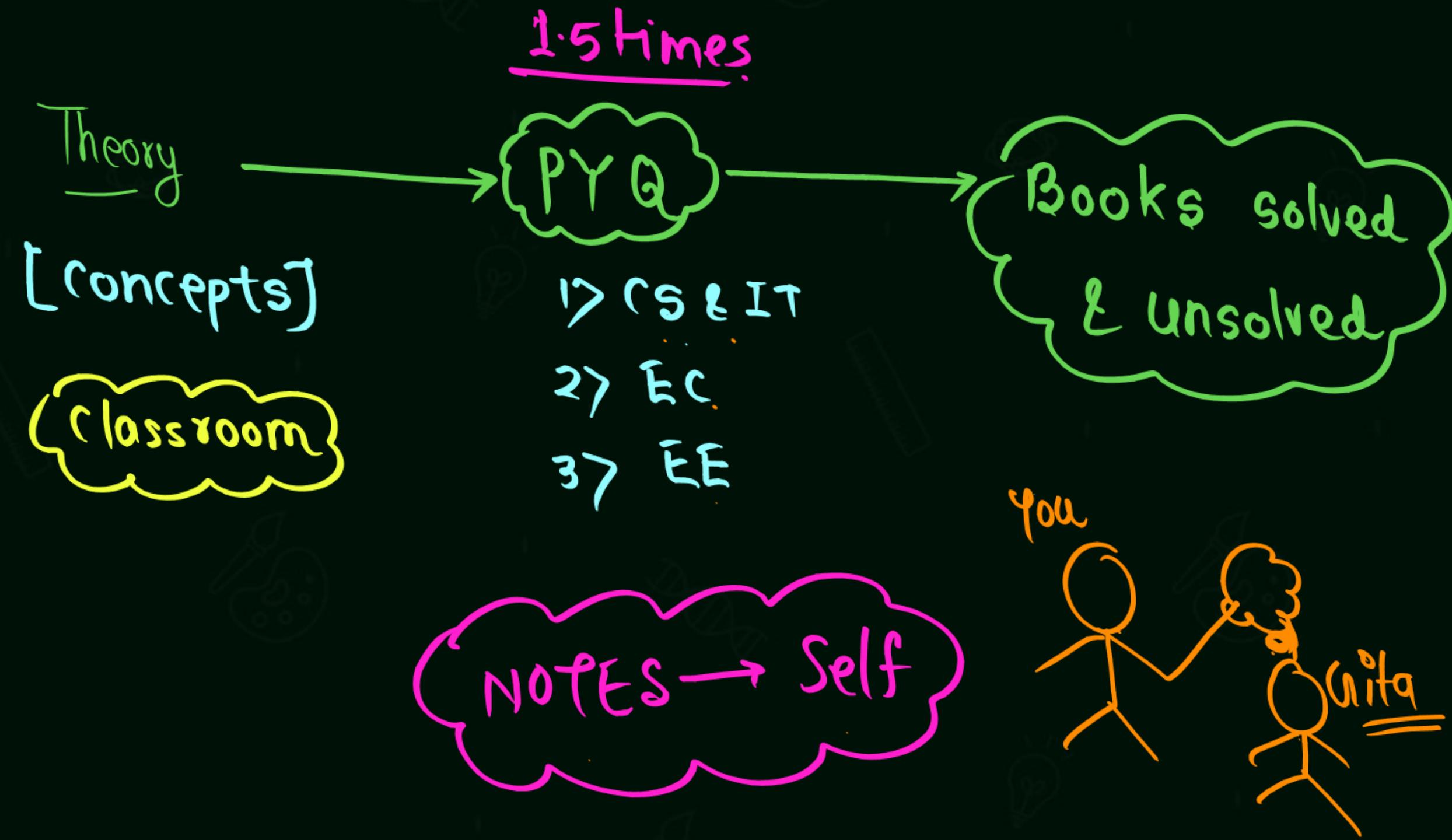
- Attend the class with positive attitude. ✓
- Punctuality is necessary. ✓
- Follow the day-wise study plan. ✓
- Attempt DPP daily as per the schedule.
- Hold chat while attending the class. We will allow you to ask and put your questions in the comment box. ✓



S.N.	Chapter	Topic
1	Logic Gate	NOT, AND, OR, <u>NAND, NOR, X-OR, X-NOR</u>
2	Minimization	Boolean algebra, <u>K-MAP</u>
3	Combination Circuit	comparator, <u>MUX, DE-MUX, Encoder, Decoder, HA, FA</u> H.S, F.S., Serial adder, <u>parallel adder, Multiplier,</u>
4	Sequential Circuit	Latches, <u>Flip-Flops, Registers, Counters</u>
5	Number System	<u>Base conversion, Magnitude Representation</u> <u>fixed & floating point Representation.</u>

✓ fixed & floating point Representation.



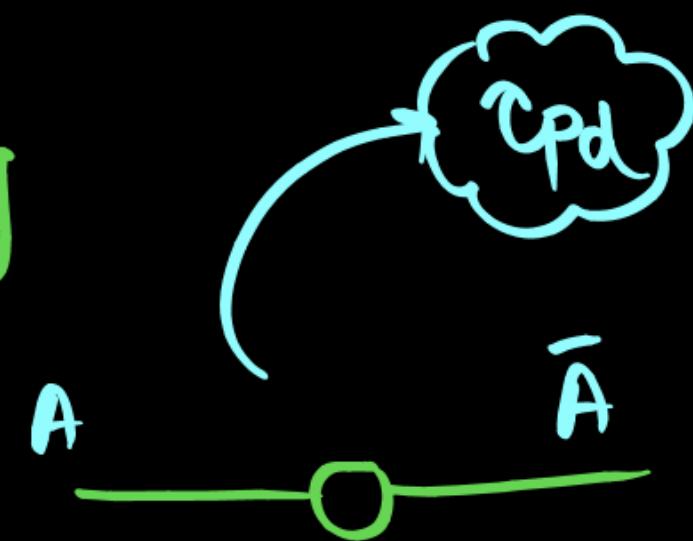
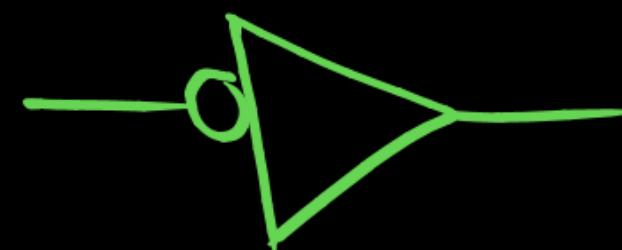
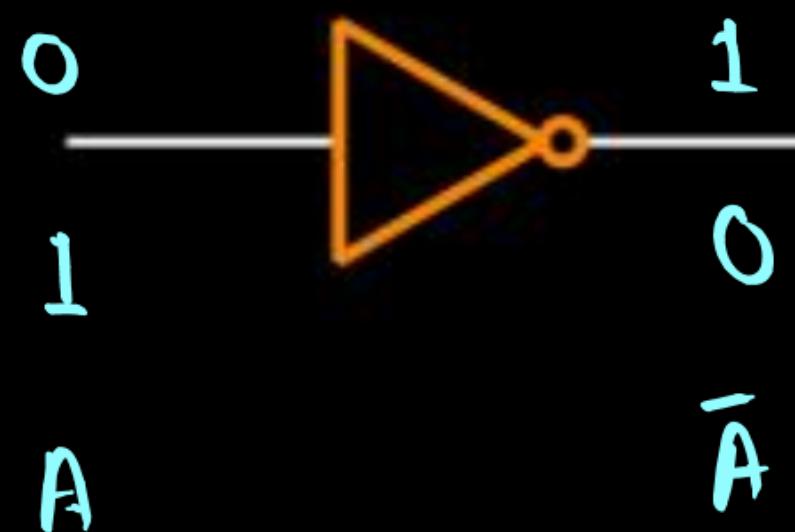


INVERTER

- Logic Gate

1. NOT GATE

[INVERTER, NEGATION]

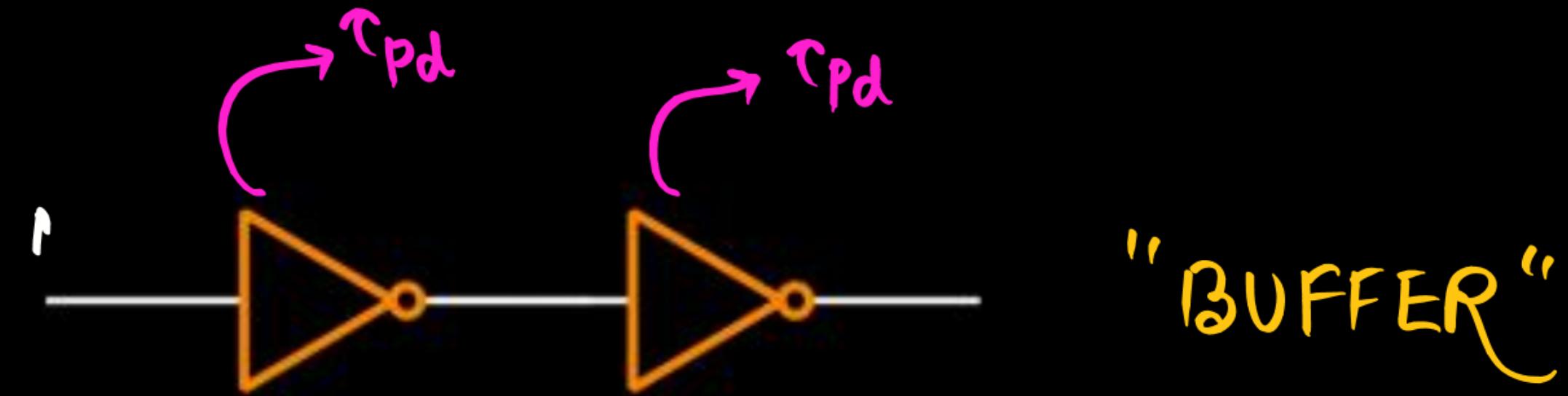


Propagation Delay (τ_{pd})

INVERTER & AND GATE

- Logic Gate

- NOT GATE

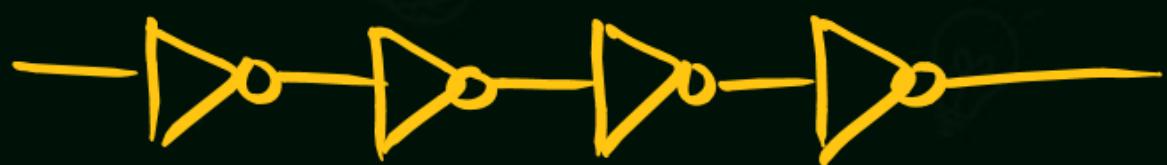


BUFFER :-

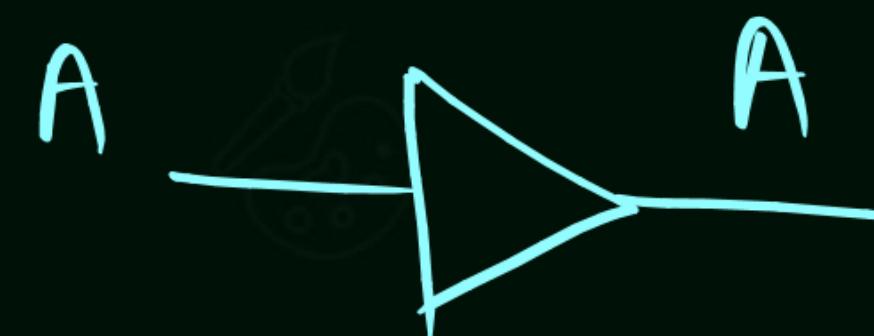


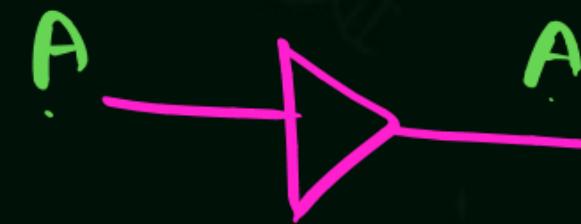
$2\tau_{pd}$

$4\tau_{pd}$



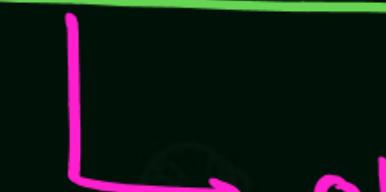
whatever input is applied same we will get in the op.



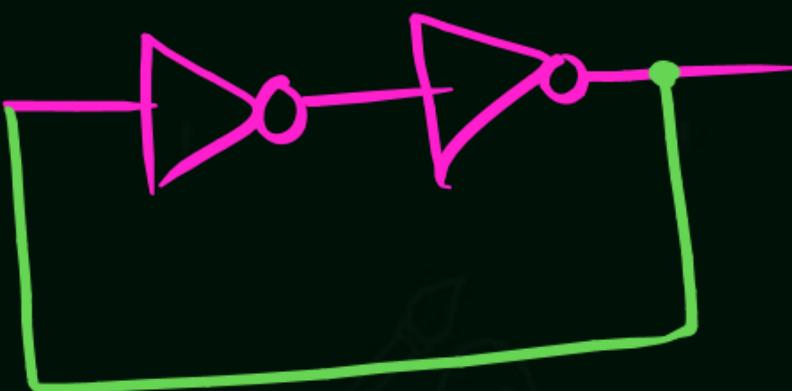
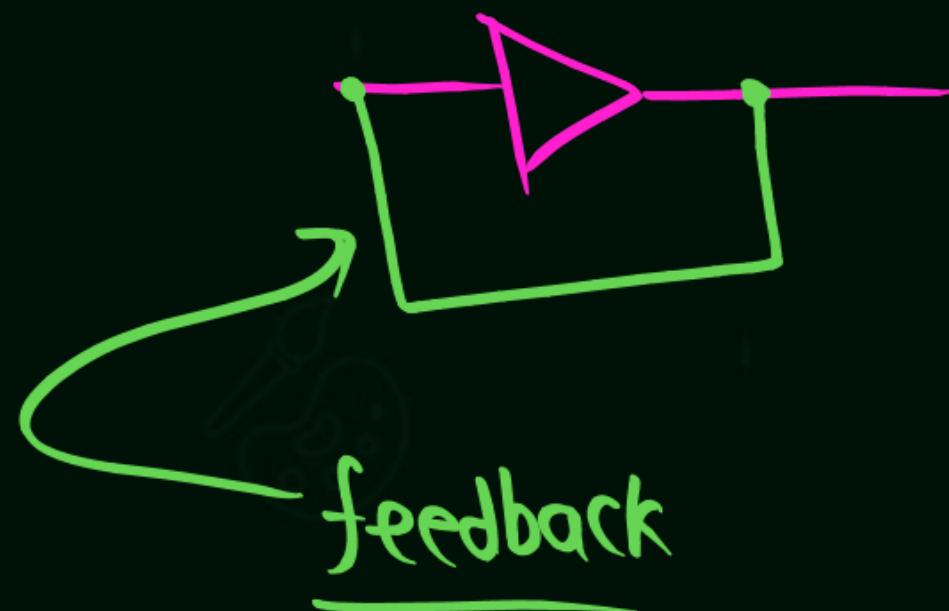


BUFFER → use of Buffer
↓
→ To "Provide Relay"

FEEDBACK :-



Op connected with input

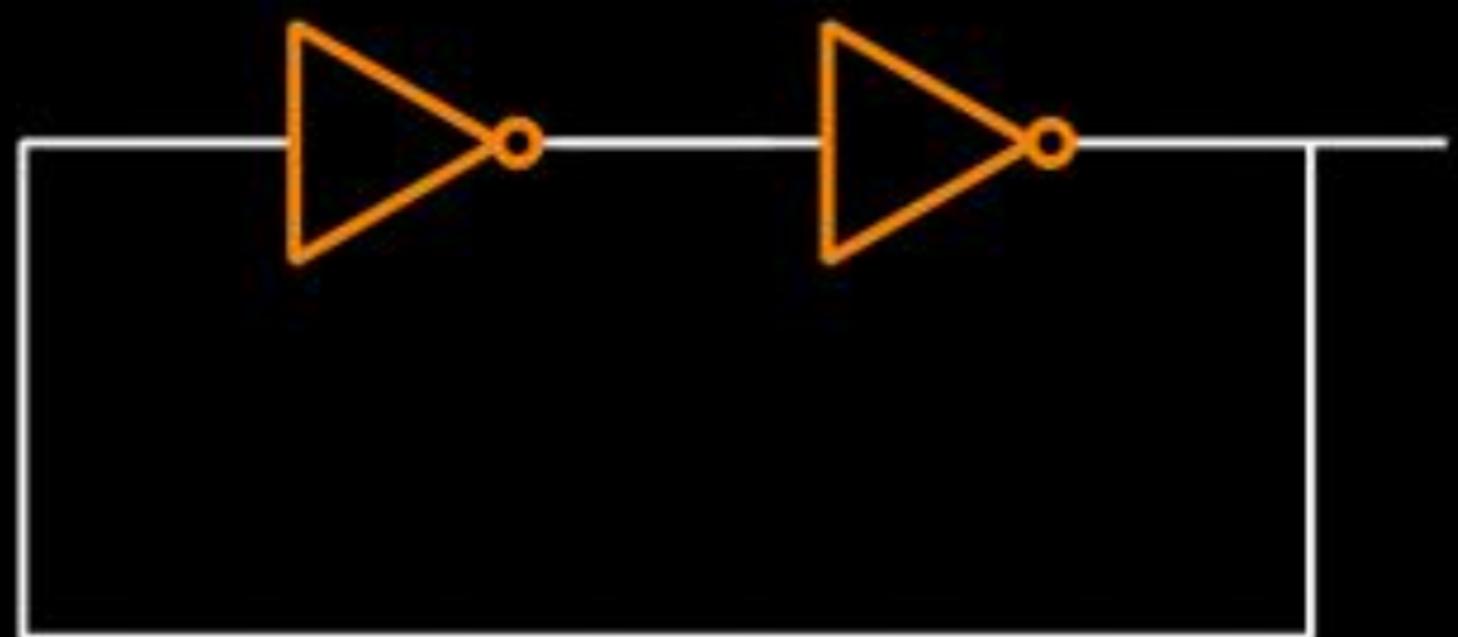


INVERTER & AND GATE

- Logic Gate

1. NOT GATE

If Even number of NOT GATE connected in Loop:

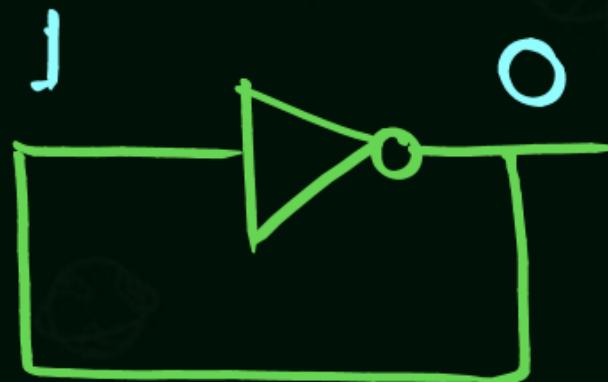


- ① Basic memory element
- ② Bistable Multivibrator
- ③ $f = \Omega R_2$



Basic memory element

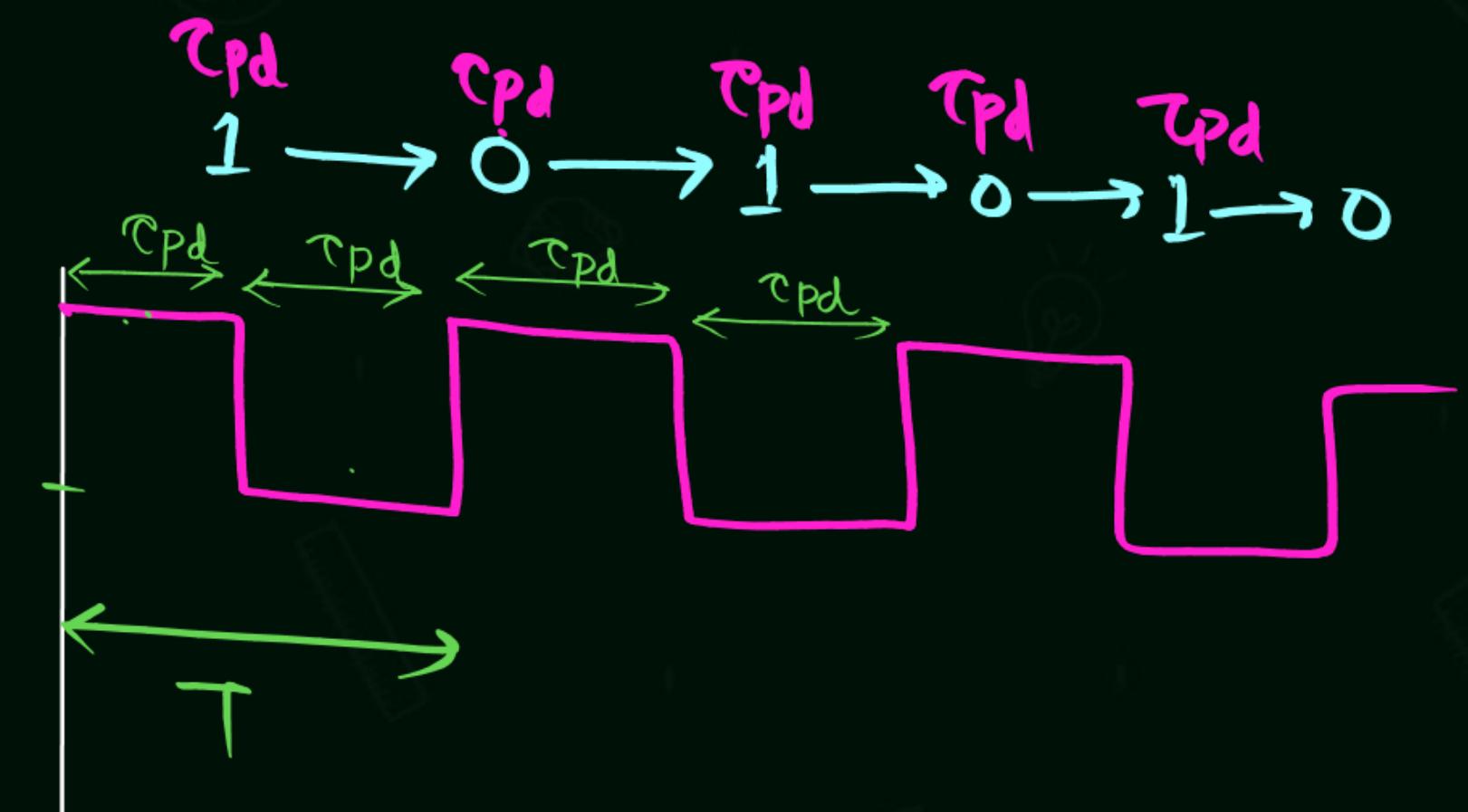
Odd
no. of
NOT
GATE



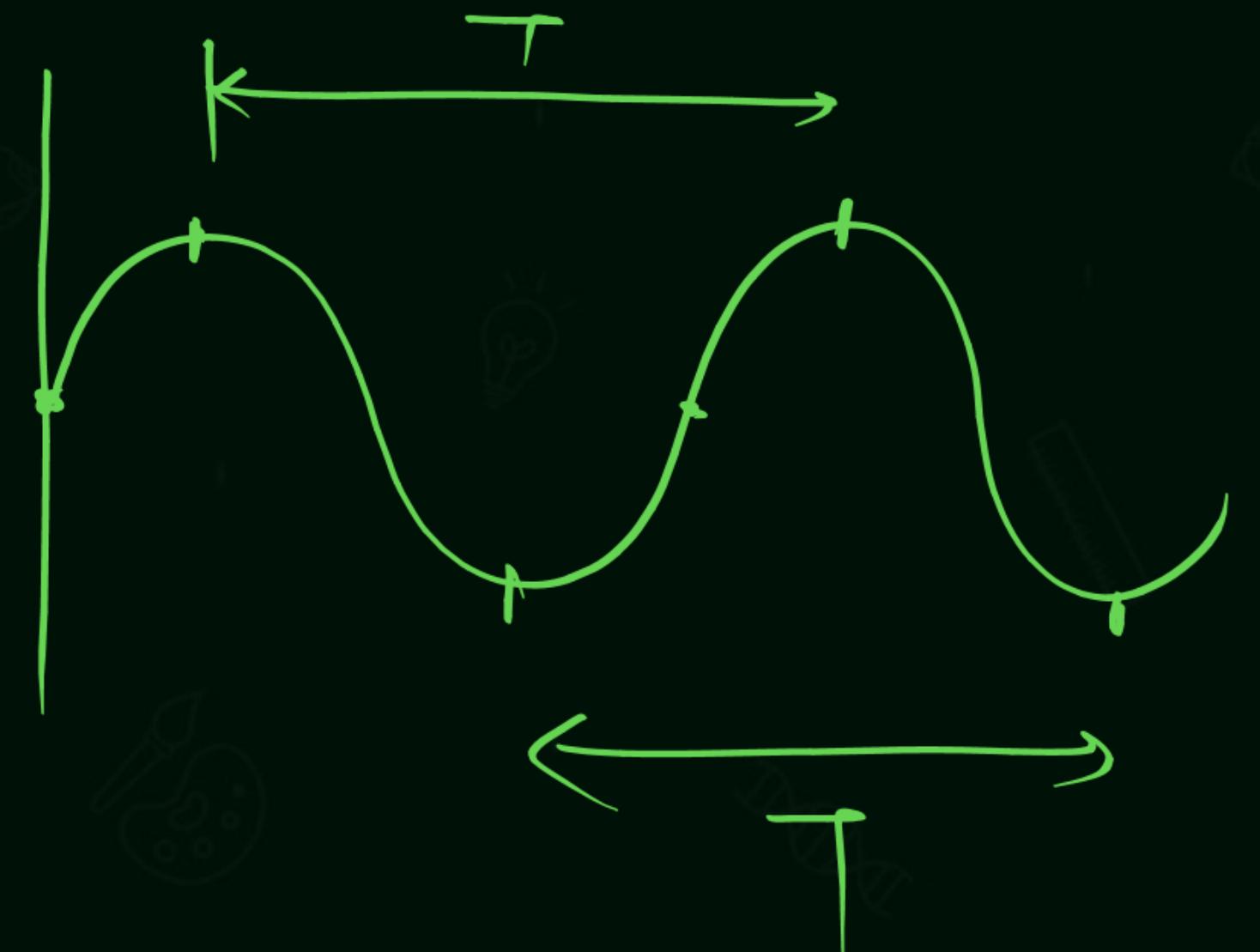
in
loop

HIGH

LOW



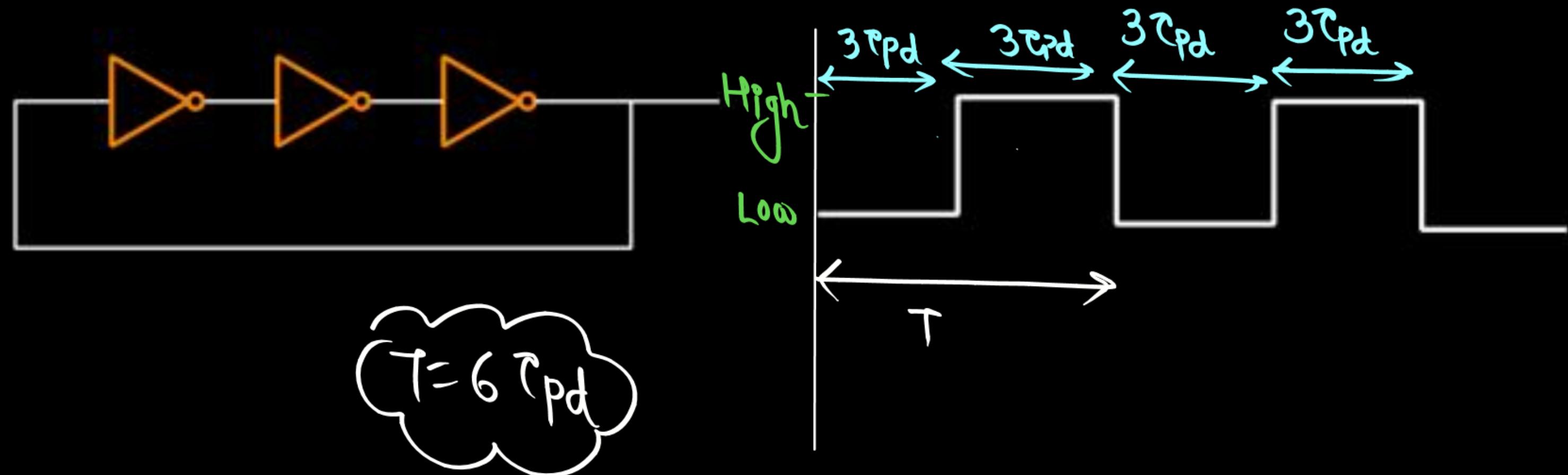
$$T = 2\tau_{pd}$$



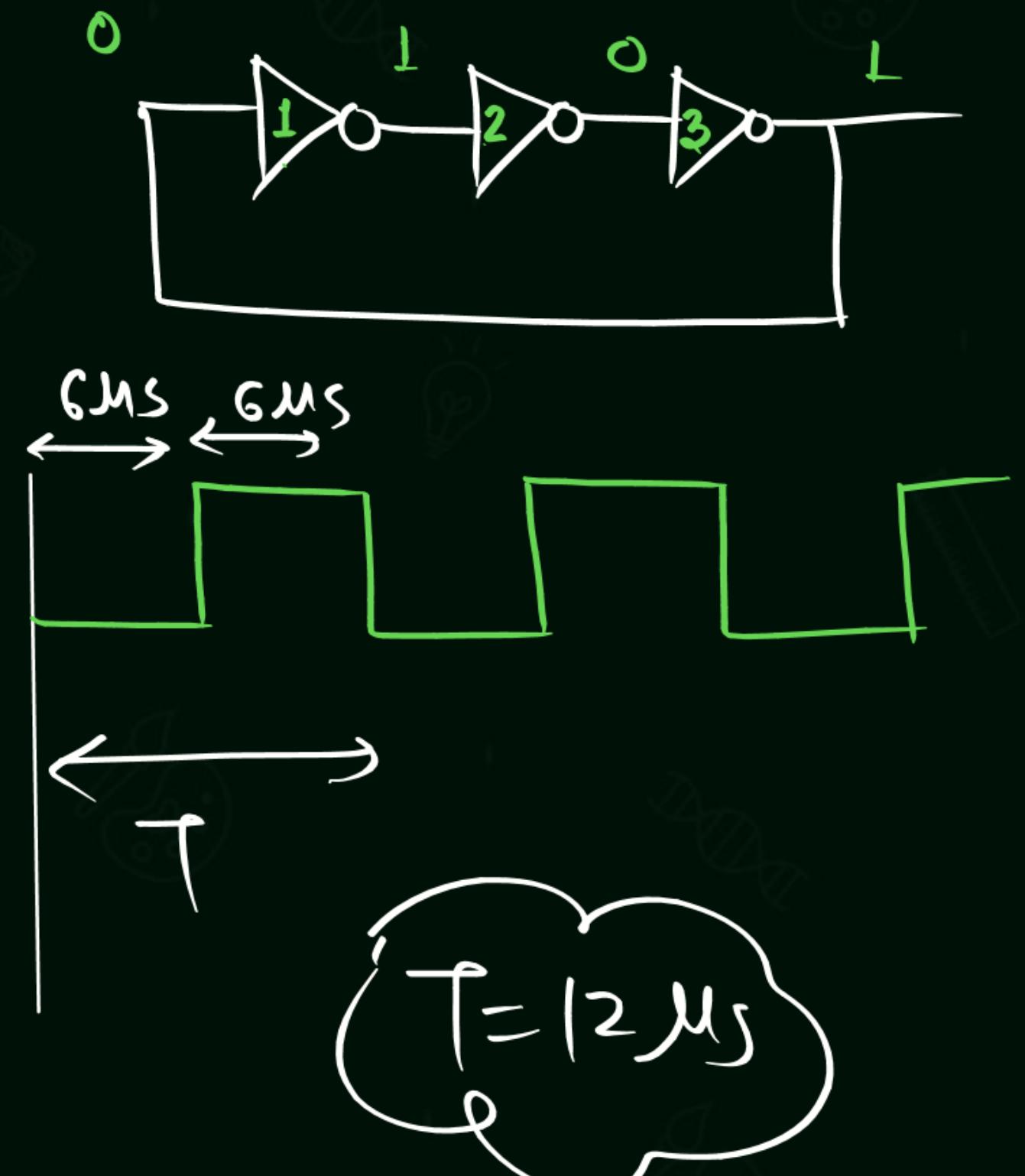
INVERTER & AND GATE

- Logic Gate

- NOT GATE



Question



$$T_{NOT_1} = 1 \mu s$$

$$T_{NOT_2} = 2 \mu s$$

$$T_{NOT_3} = 3 \mu s.$$

What is the time period
of O/P.



DD number of NOT GATE in Loop:-

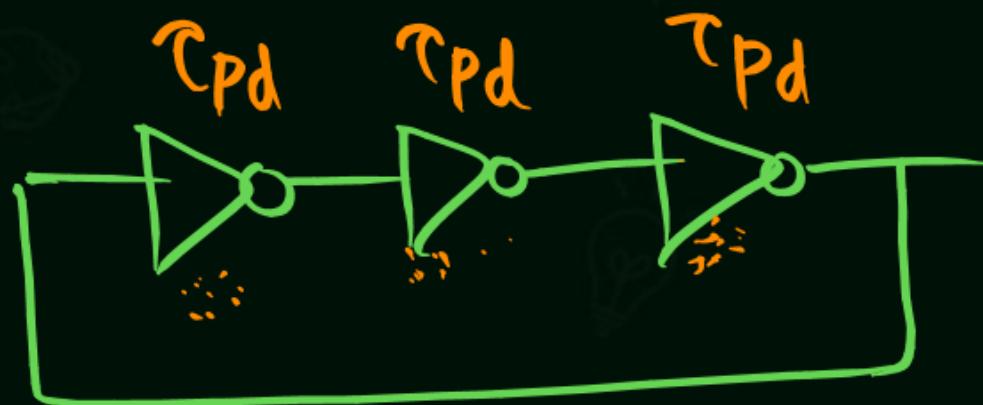


$$T = 2 \times [\text{sum of delay of all the NOT GATE in Loop}]$$

$$f = \frac{1}{T}$$

When all NOT GATES are identical :→

for odd^{no} NOT
GATE in Loop.



$$f = \frac{1}{T}$$

$$T = 6 \tau_{pd}$$

$$T = 2 \times 3 \times \tau_{pd}$$

$$T = 2 \times N \times \tau_{pd}$$

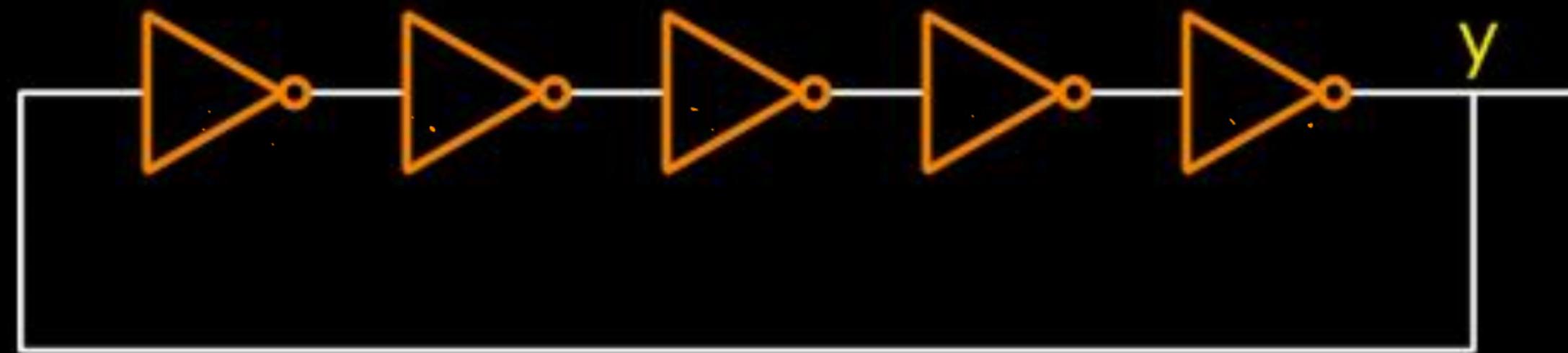
$$f = \frac{1}{2 \times N \times \tau_{pd}}$$

Q.1

Pico second

10^{-12}

For the circuit given below, all NOT Gates are identical to each other and having propagation delay 10 ps . Find the frequency of generated wave form?

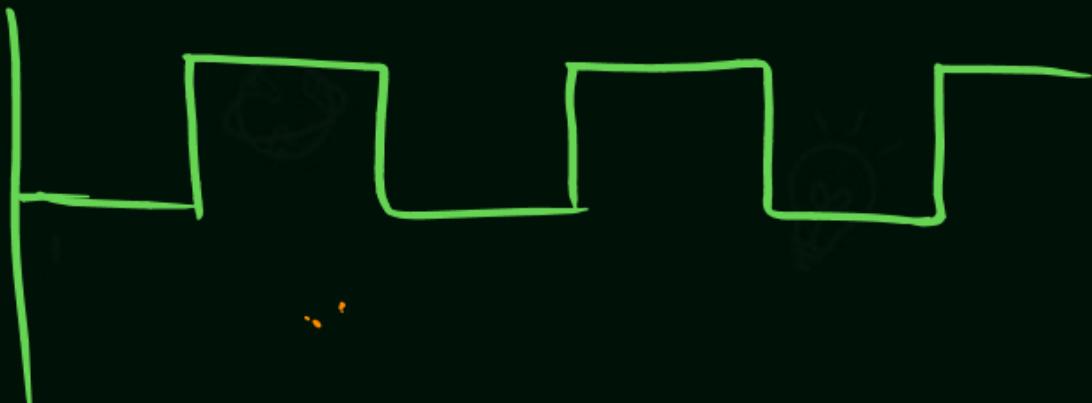
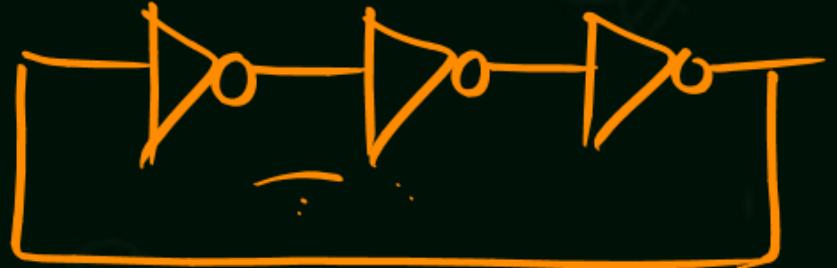


"frequency"

$$f = \frac{1}{2 \times N \times C_{pd}} = \frac{1}{2 \times 5 \times 10 \times 10^{-12} \text{ second}}$$
$$= \frac{10^{-12}}{10 \times 10} = \frac{1000 \times 10^9}{10 \times 10} H_z = 10 \times 10^9 H_z = 10 G H_z$$

$10^9 = G$

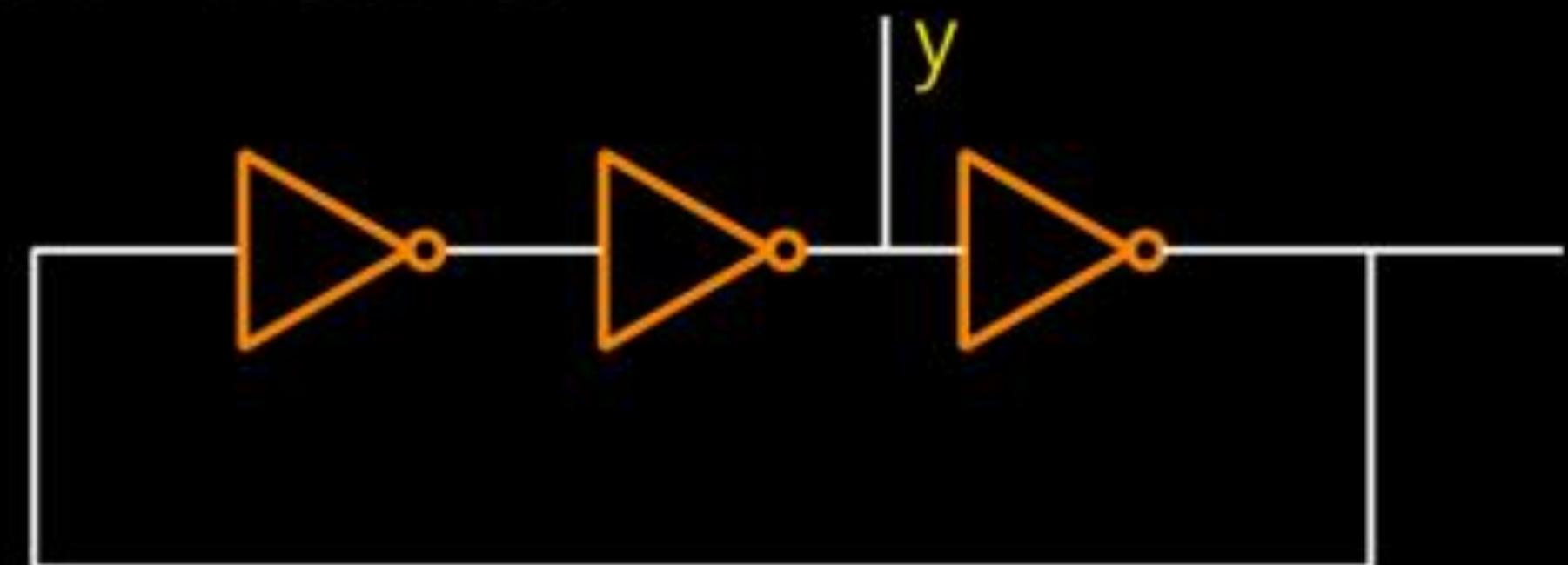
When  odd no. of NOT gates are in Loop:-



- ① Astable Multivibrator
- ② Square wave generator
- ③ Clock generator
- ④ Free Running circuit
- ⑤ Ring oscillator

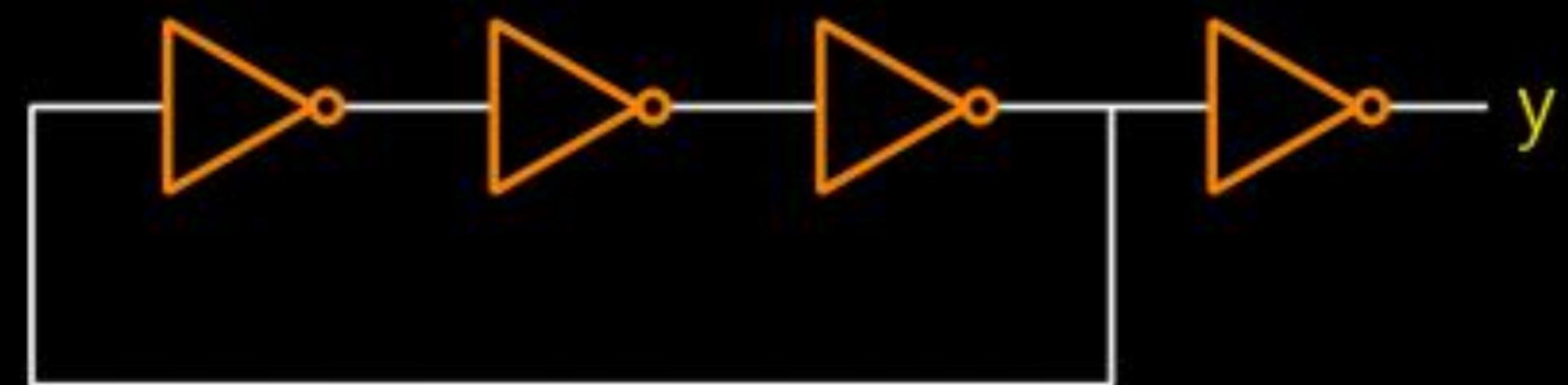
Q.2

Circuit given below are called.



Q.3

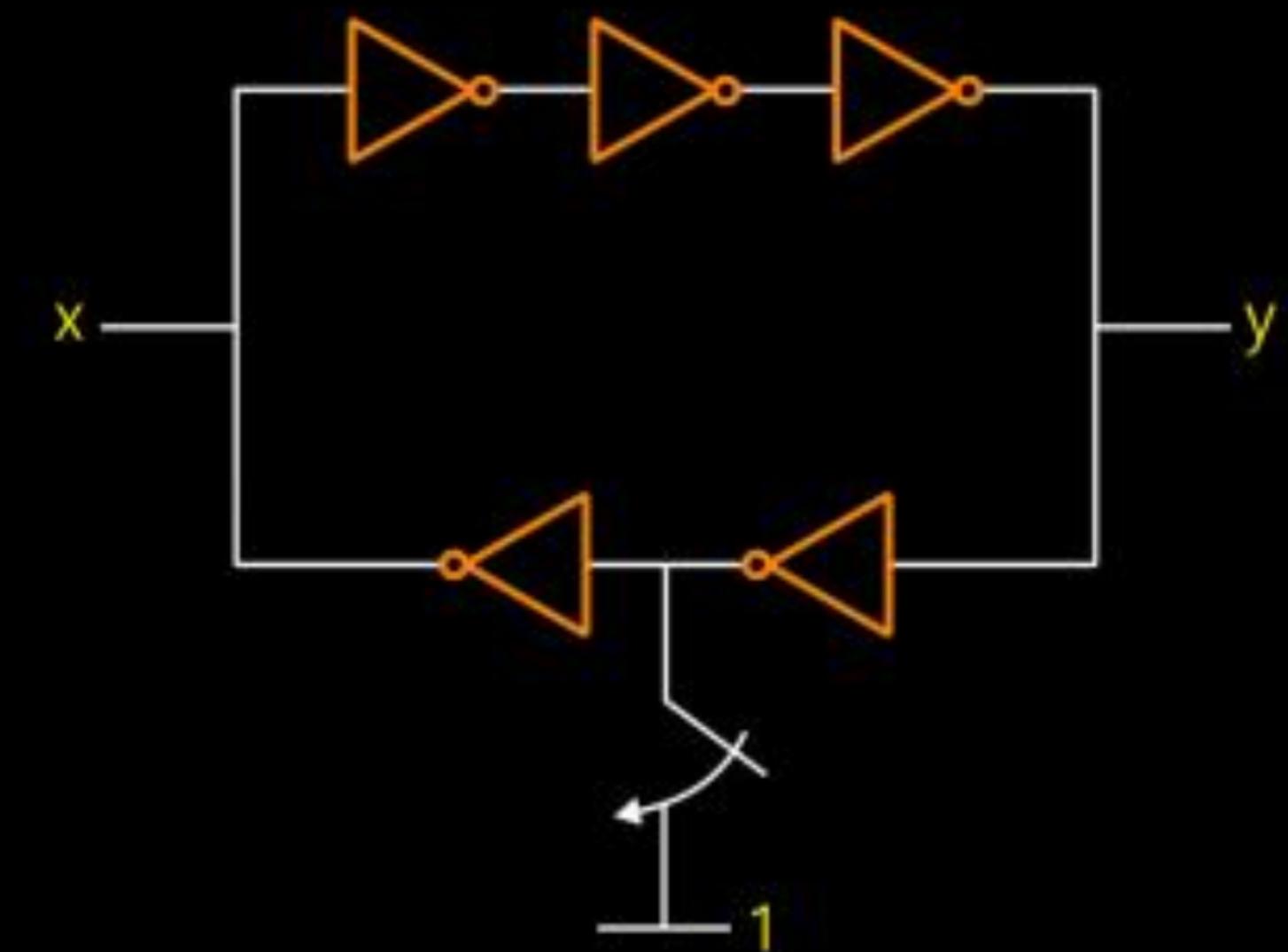
Sketch the waveform of y ?



Q.3

For the circuit given below x & y condition will be-

- A** x stable y toggle
- B** x toggle y stable
- C** x & y both toggle
- D** x & y both stable



Thank you
GW
Soldiers!

