CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Instruction & Addressing Modes

Lecture No.- 02

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Recap of Previous Lecture

Topic Instruction

Topic ISA

Topic Types of Instruction

Topics to be Covered

Topic Instruction

Topic Multiple Instruction Support

ceil $\lceil \rceil$ $\lceil 2.6 \rceil = 3$

$\lceil 2.02 \rceil = 3$

floor $\lfloor \rfloor$ $\lfloor 2.6 \rfloor = 2$

$\lfloor 2.9 \rfloor = 2$

Topic : Instruction

A group of bits which instructs computer to perform some operation

Topic : Types of Instruction

- 3-Address Instruction:
- 2-Address Instruction:
- 1-Address Instruction:
- 0-Address Instruction:

[NAT]

#Q. Consider a digital computer which supports 64 2-address instructions. If address length is 9-bits then the length of the instruction is 24 bits?

inst^n length = 6 + 9 + 9 = 24 bits

= 3 bytes

no. of inst^{ns} = 64 $\Rightarrow$ opcode = $\log_2 64$ = 6 bits

[NAT]

#Q. Consider a digital computer which supports 64 2-address instructions. If address length is 9-bits then the length of the instruction is _____ bits?

In above question: Each instruction must be stored in memory in a byte-aligned fashion. If a program has 200 instructions, then amount of memory required to store the program text is 600 bytes?

in byte addressable memory

for 1 inst^n = 3 bytes

200 inst^{ns} = 200 * 3 = 600 bytes

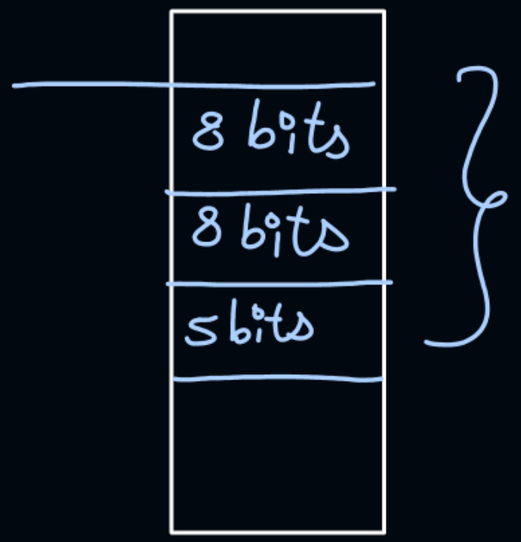
[NAT]

#Q. Consider a digital computer which supports 32 2-address instructions. Consider the address length is 8-bits. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 300 instructions, then amount of memory required to store the program text is 900 bytes?

no. of $inst^{ns}$ = 32 ⇒ opcode = $\log_2 32$ = 5 bits

opcode	a.1	a.2
5	8	8

⇒ 21 bits



3 bytes for 1 inst^{n}

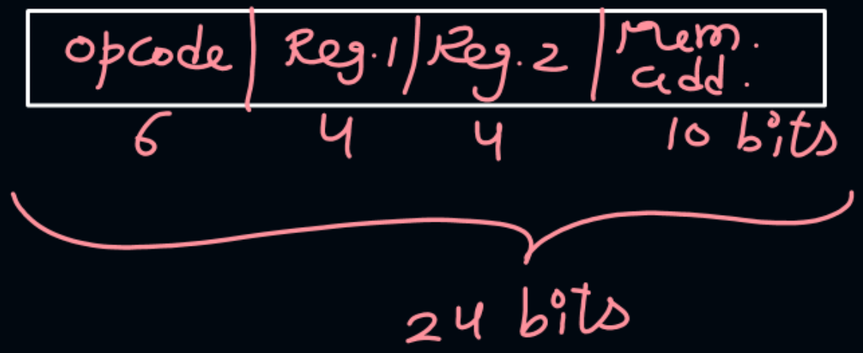
for 300 inst^{ns} $\Rightarrow$ 300 * 3 = 900 bytes

[NAT]

#Q. A processor has 50 distinct instructions and 16 general purpose registers. Each instruction in system has one opcode field, 2 register operand field and a 10 bits memory address field. The length of the instruction is 24 bits?

no. of $inst^{ns}$ = 50 $\Rightarrow$ opcode = $\lceil \log_2 50 \rceil$ = 6 bits

no. of GPR^S = 16 (R0 $\Rightarrow$ 0000
R1 $\Rightarrow$ 0001
R2 $\Rightarrow$ 0010
;
;
R15 $\Rightarrow$ 1111) $\rightarrow$ Reg. number = 4 bits

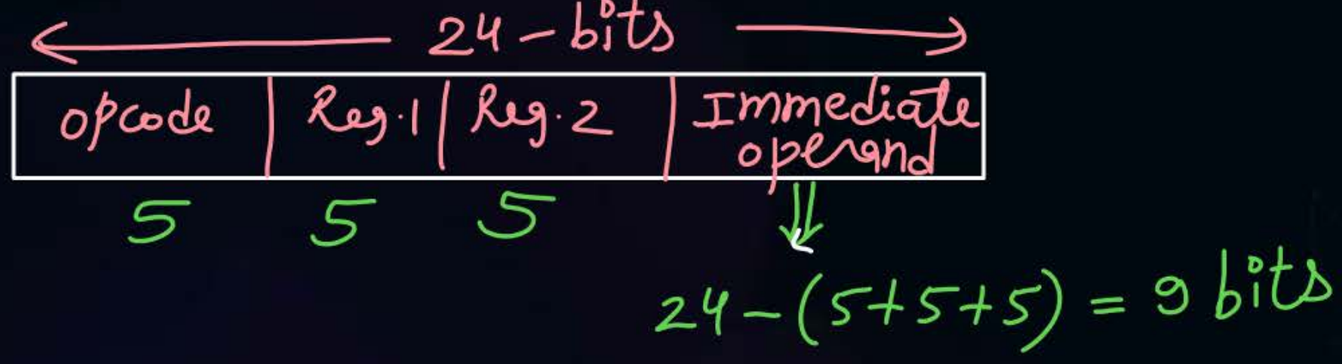

opcode
Reg. 1
Reg. 2
Mem. add.
6
4
4
10 bits
24 bits

[NAT]

opcode = 5 bits

Reg. = 5 bits

#Q. A processor has 20 distinct instructions and 32 general purpose registers. A 24- bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ___?



[NAT]

#Q. A processor has 20 distinct instructions and 32 general purpose registers. A 24- bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ___?

In above question: Assume that immediate operand field is an unsigned number, What is its maximum and minimum value possible?

Ans ⇒ min ⇒ 0

max ⇒ 511

for n no. of bits

format	min	max
Unsigned	0	$(2^n - 1)$
sign-magnitude	$-(2^{n-1} - 1)$	$+(2^{n-1} - 1)$
1^s complement	$-(2^{n-1} - 1)$	$+(2^{n-1} - 1)$
2^s complement	$-(2^{n-1})$	$+(2^{n-1} - 1)$

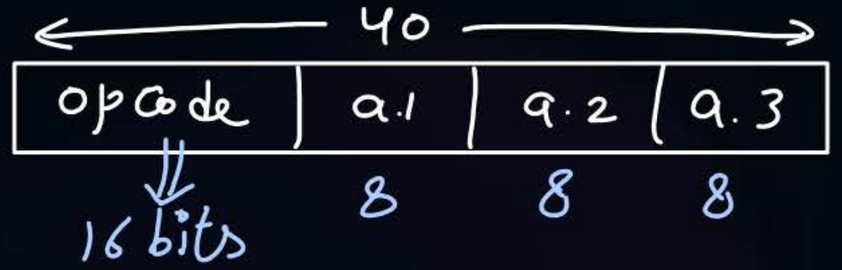
for $n = 9$

0 $2^9 - 1 = 511$

[NAT]

default ⇒ byte addressable mem.

#Q. Consider a system which support only 3 address instructions only, and supports 256B memory. If the instruction size is 40-bits then maximum & minimum number of instruction supported by the system are?



$$\text{no. of cells} = \frac{256\,B}{1B} = 256 = 2^8$$

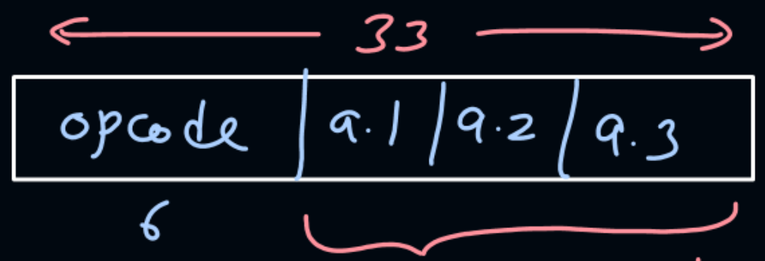
$$\text{add.} = 8 \text{ bits}$$

$$\text{min} = 1$$

$$\text{max} = 2^{16} = 65536$$

Ques) consider a system which supports 64 3-address inst^ns. If inst^n length is 33 bits then address length is ___ bits?

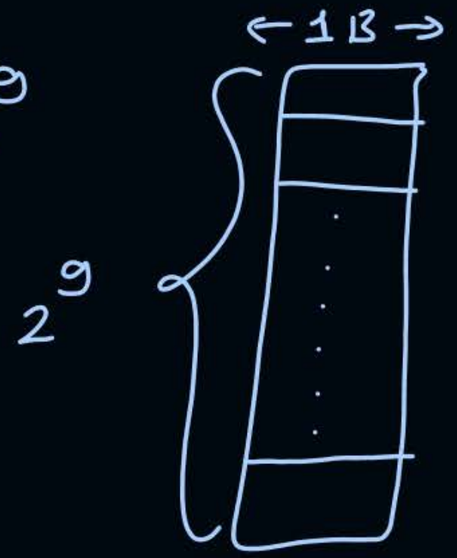
Soln



27 bits ⇒ hence each add. = 9 bits

Ques) In prev. Quest^{n} size of memory supported by system 512 bytes ? [byte addressable memory as default]

Soln



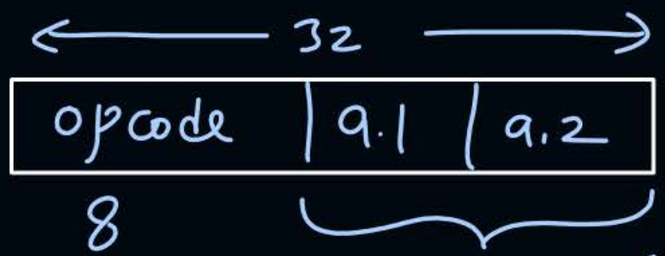
no. of cells = 2^9

mem. size = $2^9 * 1\,B$

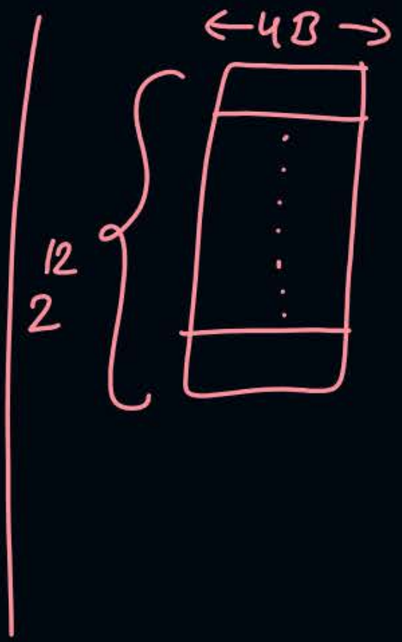
= 512 B

Ques) Consider a system which supports 250 2-address instructions. Each inst^{n} length is 32 bits. The system supports word addressable mem. with word size 4 bytes. The max. size memory system supports = 16 k bytes?

Soln



32 − 8 = 24 bits ⇒ add. = 12 bits



Mem. size

$= 2^{12} * 4B$

$= 2^{12} * 2^{2} B$

$= 2^{14} B = 2^{4} \cdot 2^{10} B$

$= 16 KB$

2 mins Summary

Topic Instruction

Topic Multiple Instruction Support

Happy Learning

THANK - YOU