CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Basics of COA

Lecture No.- 03

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Recap of Previous Lecture

- Topic: CPU Registers
- Topic: Types of Architecture
- Topic: Program Counter
- Topic: Instruction Register
- Topic: Stack Pointer

Topics to be Covered

- Topic: CPU Registers
- Topic: Memory Addressing
- Topic: Memory Access
- Topic: Architecture Type (Based on Size of Input)

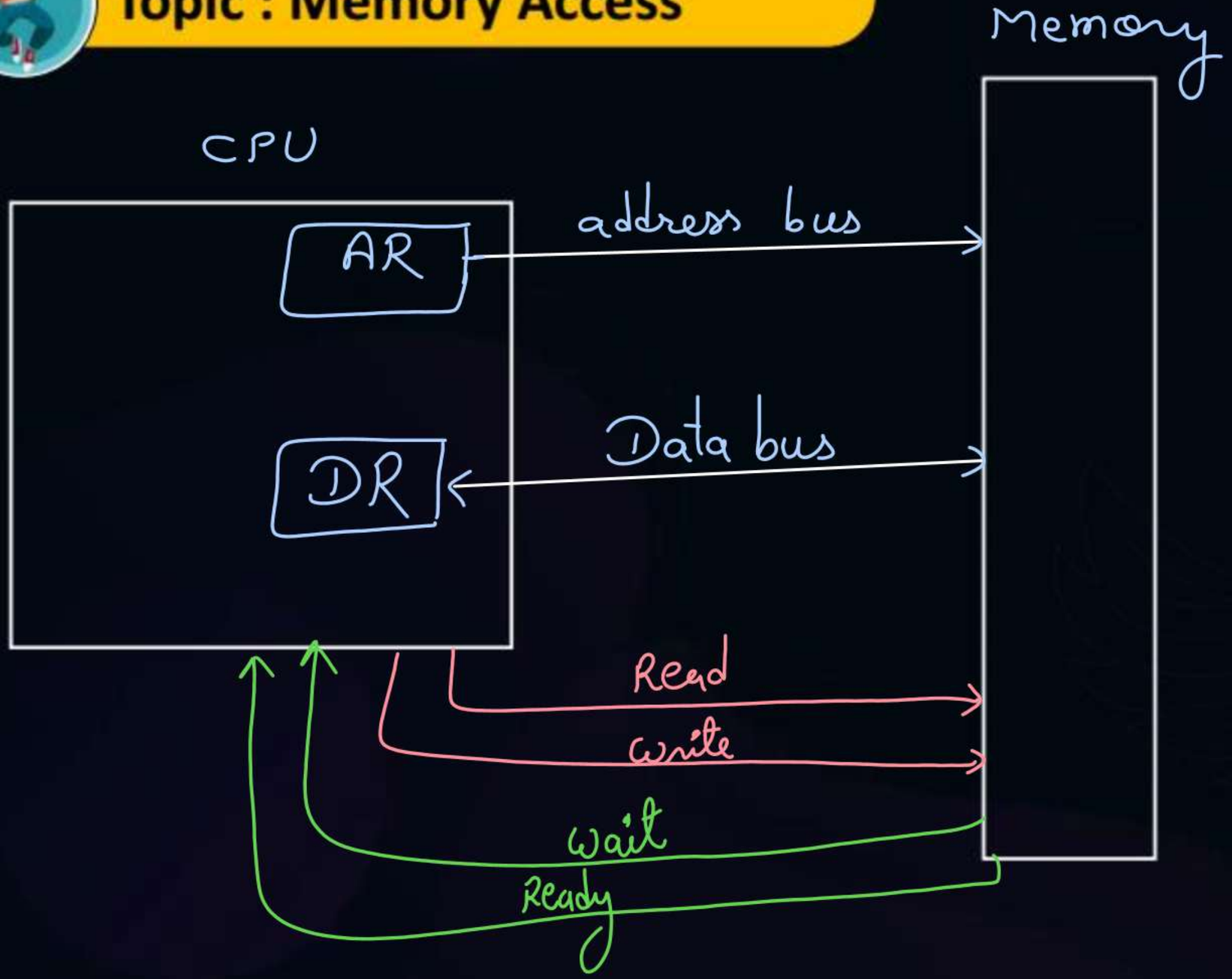
Topic : Address Register or MAR

- Used to send address to memory

Topic : Data Register or MDR

- Used to send data to memory
- And to receive data from memory

Topic : Memory Access



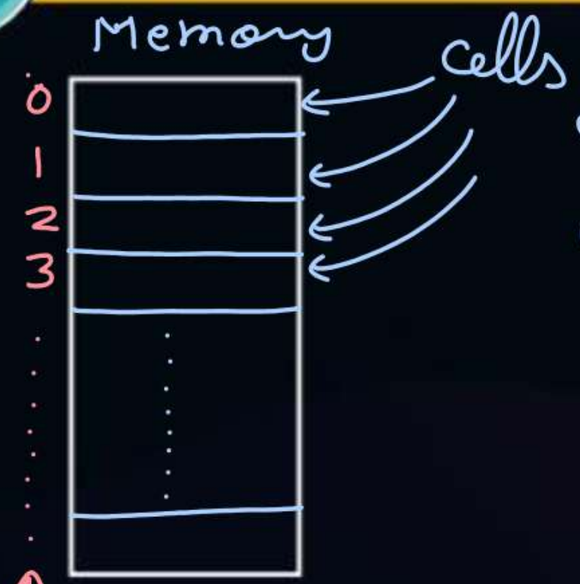
Memory Read :-

1. CPU sends address to memory through address bus
2. CPU sends enabled Read control signal to memory
3. Memory reads on given address and the content is sent to CPU through Data bus.

Memory write :-

1. CPU sends add. to memory through add. bus
2. — 11 — data ——— 11 ——— data —11—
3. CPU sends enabled write control signal.
   memory performs write of given data on given address.

Topic : Memory Addressing



4 cells

add. size = 2 bits

8 cells

add. size = 3 bits

Topic : Memory Addressing

No. of cells	4	8	16	32	2^x	n
address size in bits	2 bits	3 bits	4 bits	5 bits	x bits	$\log_2 n$ bits

$$\log_2 2^x \Rightarrow x$$

Ques) no. of cells in a mem. = 256

add. size = 8 bits ?

Soln

$256 = 2^8$

add. = $\log_2 2^8$ = 8 bits

Ques) no. of cells = 64 M

add. size = 26 bits ?

Soln

cells = $2^6 \cdot 2^{20} = 2^{26}$

add. = 26 bits

Ques) no. of cells = 16 k

add. size = 14 bits ?

Soln

$2^4 \cdot 2^{10} = 2^{14}$

add. = 14 bits

Ques) A memory with add. = 12 bits

no. of cells = 4 k ?

Soln

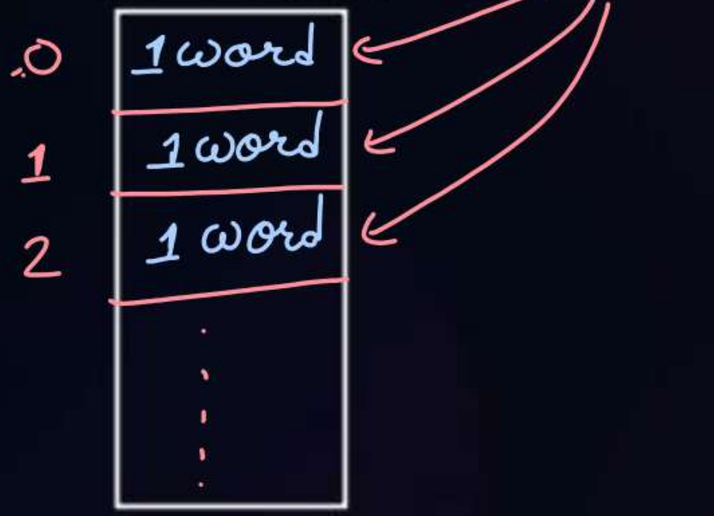
$= 2^{12} = 2^2 \cdot 2^{10} = 4k$

Topic : Memory Types

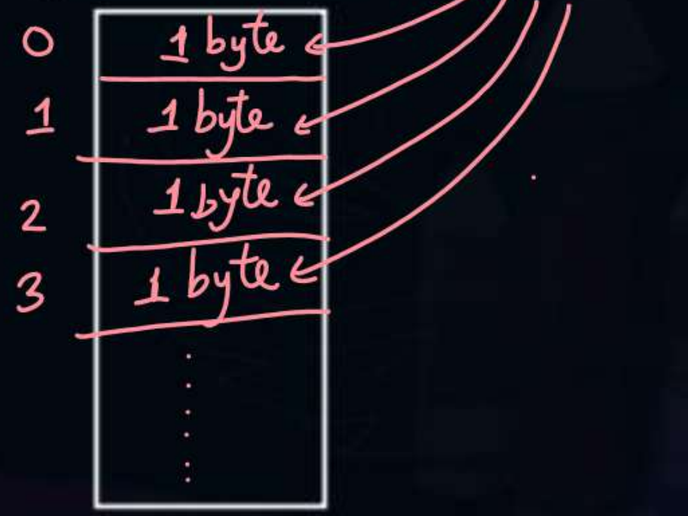
1. Byte Addressable → on each cell of memory 1 byte is stored
2. Word Addressable → —"— —"— 1 word —"—

word size = 2 bytes or 4 bytes or 8 bytes . . . . .

Word Addressable



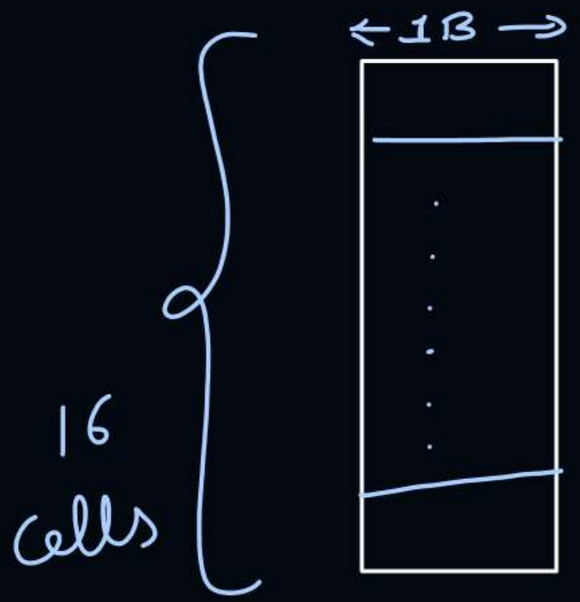
Byte Addressable



ex:-

Byte addressable memory:-

no. of cells = 16



Total mem. capacity = 16 * 1B

= 16 Bytes

add. size = $\log_2 16 = \log_2 2^4 = 4$ bits

ques) If a byte addressable memory has 32k bytes capacity. No. of cells in memory = 32k ? add. size for mem. = 15 bits

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Soln

32k bytes = no. of cells * 1B

no. of cells = 32k

$= 2^5 \cdot 2^{10}$

$= 2^{15}$ ⇒ add. = 15 bits

Ques) Consider a byte addressable mem. of size 4GB. Add. size of memory 32 bits?

Soln

$$\text{no. of cells} = \frac{4GB}{1B} = 4G = 2^2 \cdot 2^{30} = 2^{32}$$

$$\text{add.} = \log 2^{32} = 32 \text{ bits}$$

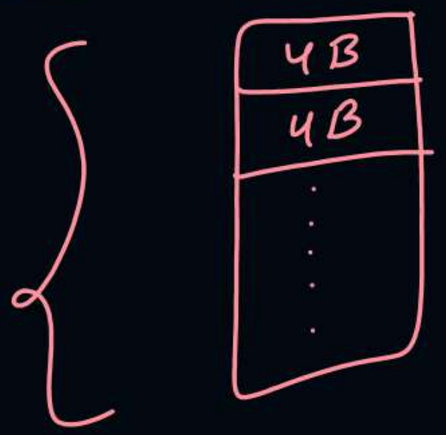
Ques) Memory size = 256 bytes

word addressable memory.

1 word = 4 bytes

No. of cells in memory = 64

add. size = 6 bits



$$\text{no. of cells} = \frac{256\,B}{4\,B} = 64 = 2^6$$

$$\text{add.} = \log_2 2^6 = 6 \text{ bits}$$

Ques) word addressable memory of size 2GB.

word size = 8 bytes

address = 28 bits

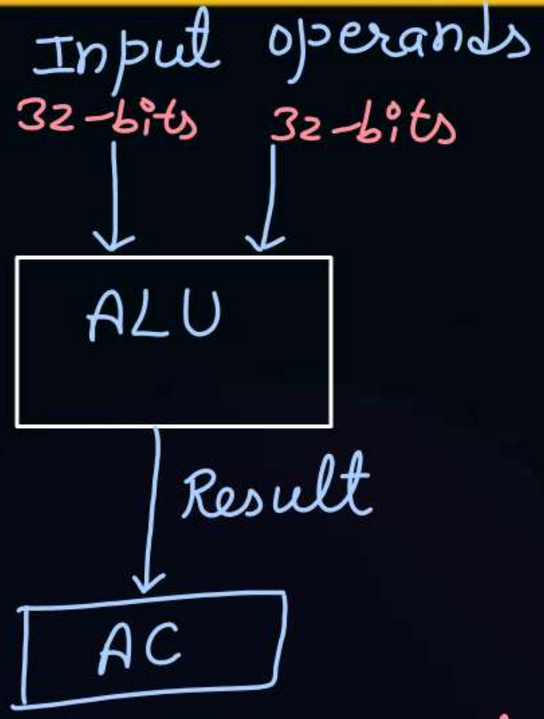
Soln

$$\text{no. of cells} = \frac{2GB}{8B} = \frac{2^1 \cdot 2^{30}}{2^3} = 2^{28}$$

$$\text{add.} = \log_2 2^{28} = 28 \text{ bits}$$

Topic : Architecture Type (Based on Size of Input) of ALU

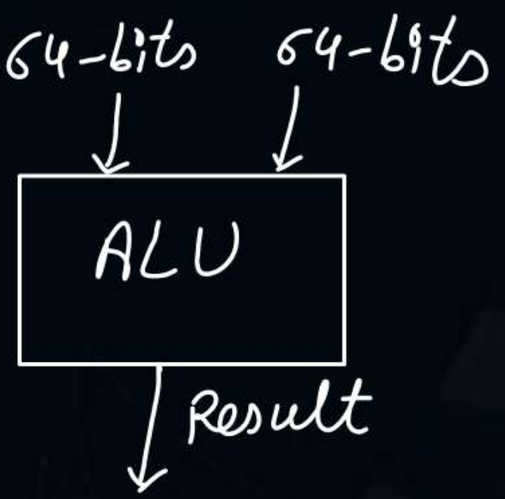
ex:-



32-bit architecture

CPU word = 32-bits
= 4 bytes

64-bits architecture



CPU word = 64 bits
= 8 bytes

2 mins Summary

- Topic: CPU Registers
- Topic: Memory Addressing
- Topic: Memory Access
- Topic: Architecture Type (Based on Size of Input)

Happy Learning

THANK - YOU