CS & IT ENGINEERING

DIGITAL LOGIC

Sequential Circuit

Lecture No. 3

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01 JK Flip Flop

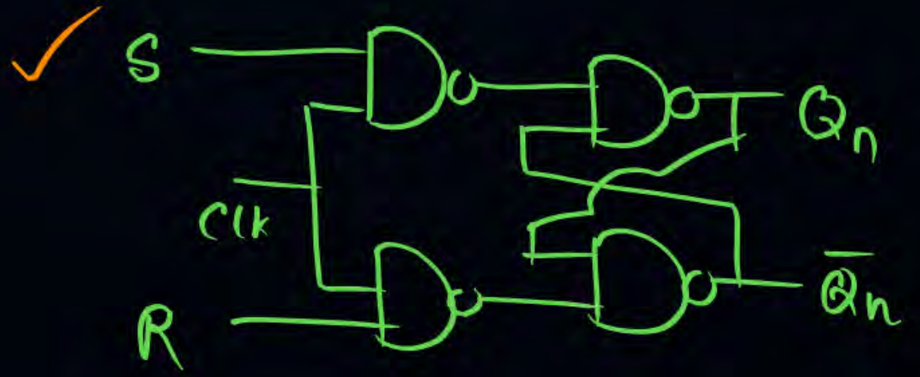
02 PRACTICE

03 DISCUSSION

Flip-Flop

1> Circuit Diagram
2> Truth table
3> Char. Table
4> Char. Equation
5> Excitation table
6> ⋮ om

SR FF

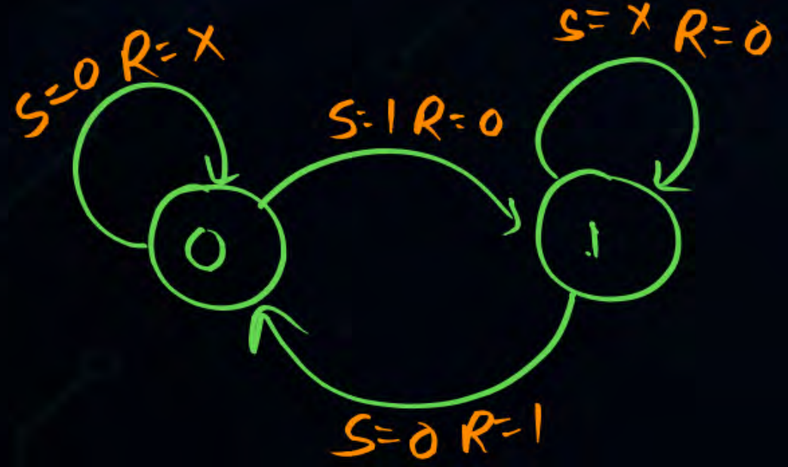


S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

$$Q_{n+1} = X + \bar{Y} Q_n$$

$$Q_{n+1} = S + \bar{R} Q_n$$

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0


S=0 R=X
S=X R=0
S=1 R=0
0
1
S=0 R=1

JK FLIP FLOP

1. Symbol

2. Truth Table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

JK FLIP FLOP

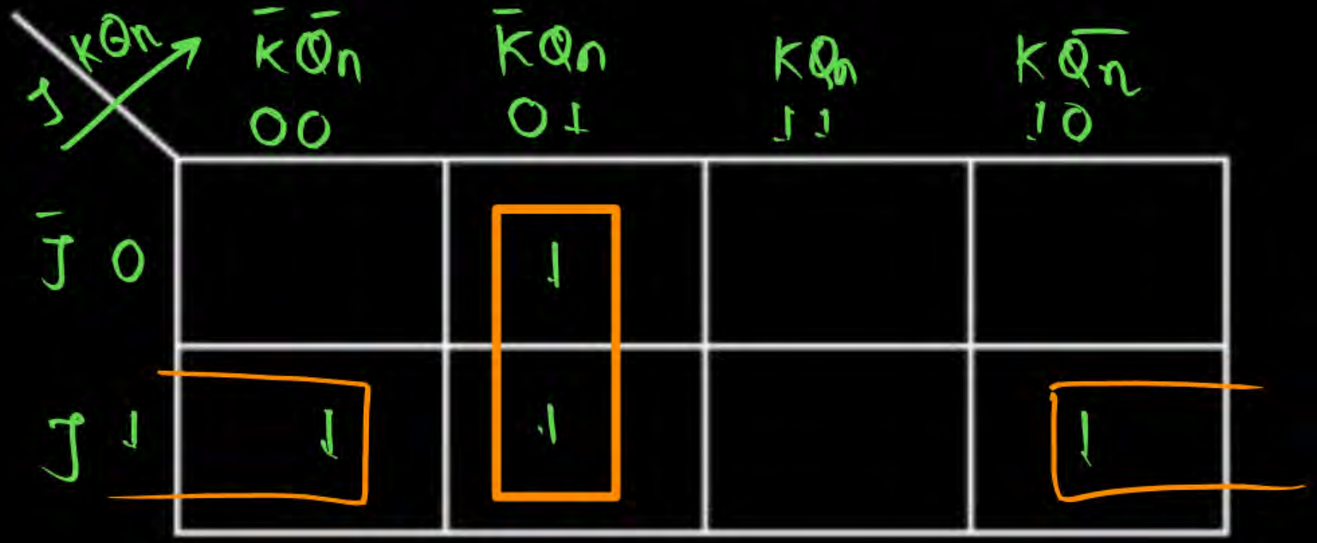
3. Characteristics Table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$Q_{n+1}(J, K, Q_n) = \Sigma m(1, 4, 5, 6)$

JK FLIP FLOP

4. Characteristics Equation



$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

JK FLIP FLOP

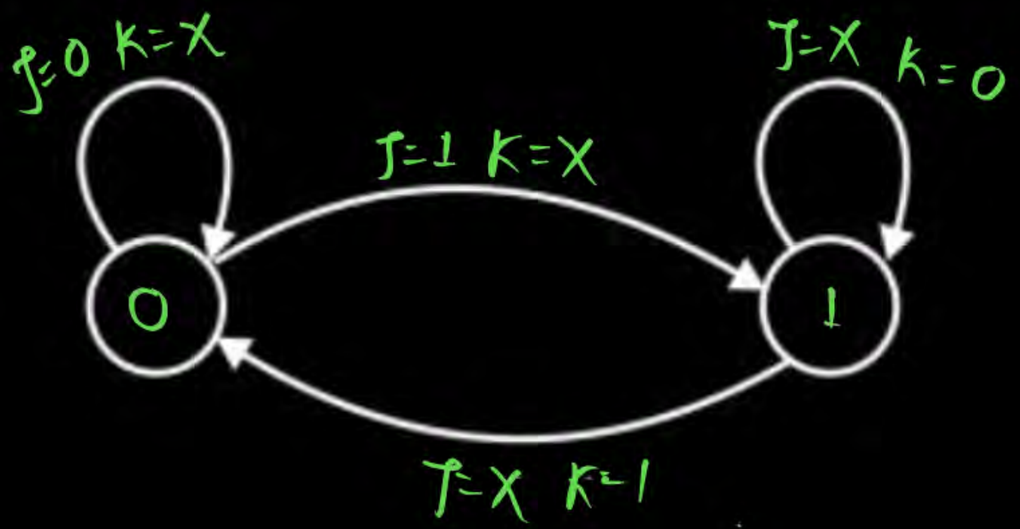
5. Excitation Table :→

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

JK FLIP FLOP

6. State Diagram

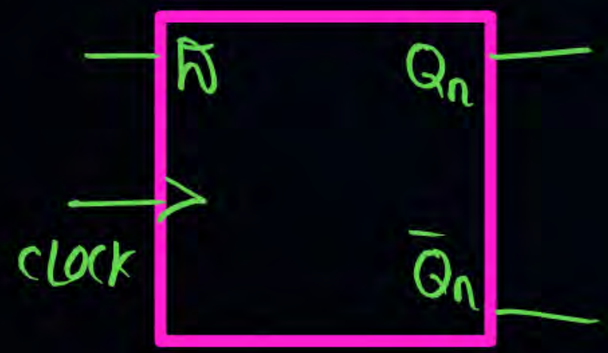


Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D-FF (Data FF, Delay FF, Transparent FF)

↳ "D" FF is a Flip-Flop in which whatever the input is applied will come in the output along with the clock.

① Symbol



② Truth Table

CLK	D	Q_{n+1}
↓	0	0
↓	1	1

③ Characteristic Table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

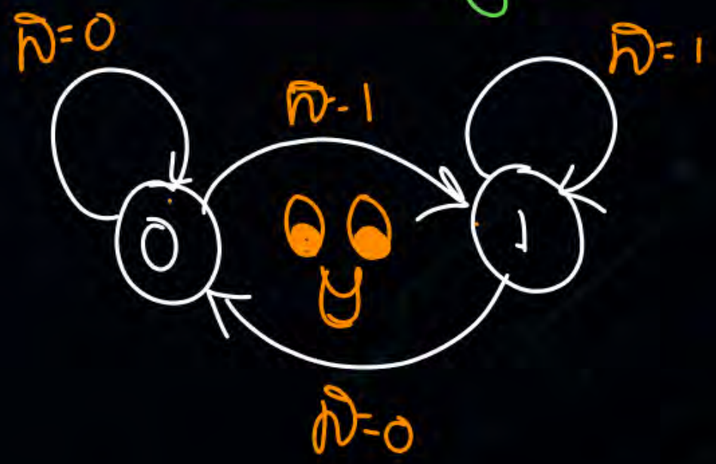
④ Characteristic Equation :→

$$Q_{n+1} = D$$

⑤ Excitation Table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

⑥ State Diagram



1 The T-FF [Toggle FF]

C.T.

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Truth table

T	Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

Q.

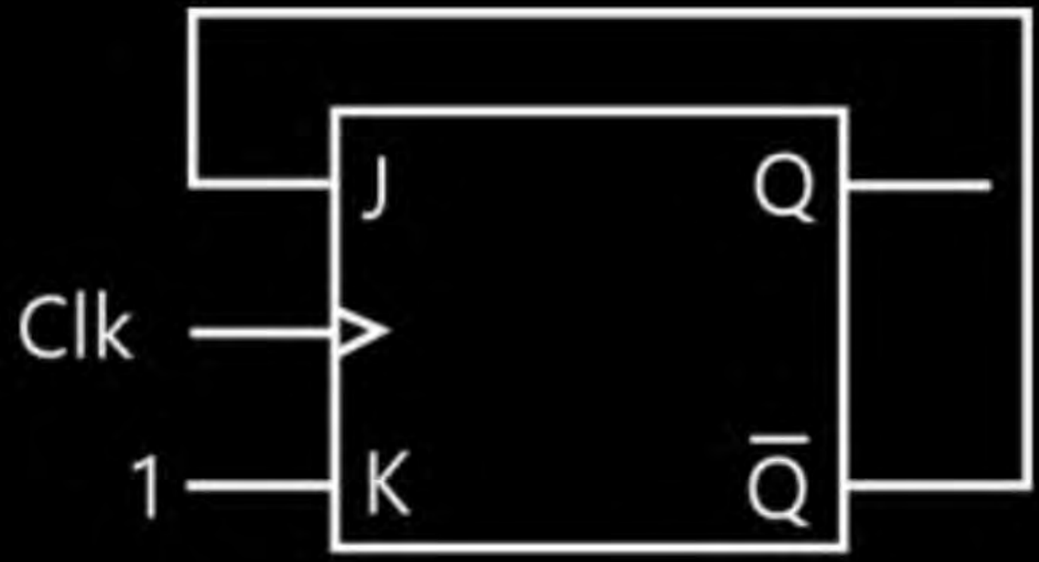
The J-K FF shown below is initially cleared and then clocked for 5 pulses, the sequence at the Q output will be

A 010000

B 011001

C 010010

D 010101



Thank you

GW

Soldiers !