CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Memory Organization

Lecture No.-01

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Recap of Previous Lecture

- **Topic** Direct Memory Access (DMA)
- **Topic** Cycle Stealing
- **Topic** Burst Mode

Topics to be Covered

Topic Memory Hierarchy

Topic Memory Presentation

Interleaving mode:-

CPU gives the control of the buses to DMAC only when it does not need buses. Ex:- instⁿ decode, ALU operatⁿ etc.

⇒ Percentage of time CPU is blocked due to DMA is almost zero in this mode.

DMA :-

DMA Initialization

Data transfer b/w mem & I/O

DMA transfer completion

[MCQ] GATE-PYQ

#Q. A hard disk with a transfer rate of 10 Mbytes/second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation ?

A 5.0%

B 1.0%

C 0.5%

D ✓ 0.1%

Processor used = 300 + 900 = 1200 cycles = $\frac{1200 * 1}{600MHz}$ = 2 μsec

for 10MB data, time = 1 sec

for 20kB —11—, time = $\frac{1\,sec}{10MB} * 20kB$

= 2000 μsec

% of time CPU Consumed = $\frac{2\ \mu sec}{2+2000} * 100\%$

= 0.1 %

GATE-PYQ

#Q. On a non-pipelined sequential processor, a program segment, which is the part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.

```
        Initialize the address register      1
        Initialize the count to 500          1
LOOP:   Load a byte from device              2
        Store in memory at address given by address register   2
        Increment the address register       1
        Decrement the count                  1
        If count !=0 go to LOOP              1
```

7 * 500 ⇒ 3500

Total = 2 + 3500 = 3502 cycles

Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute.

The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory.

What is the approximate speed up when the DMA controller based design is used in a place of the interrupt driven program based input-output?

Interrupt I/O time = $2 + 7 * 500 = 3502$ cycles

DMA Technique = $20 + 2 * 500 = 1020$ cycles

$$\text{speed up} = \frac{\text{Interrupt mode time}}{\text{DMA technique time}} = \frac{3502}{1020} \simeq 3.4$$ Ans.

[NAT]

#Q. The DMA controller has data count register of size 8-bits. The memory is byte addressable. The maximum number of bytes the DMA can transfer to memory at a time without giving the control of the buses back to CPU?

↓ when data count becomes zero.

max value with which data count can be initialized $= (11111111)_2$

$= (255)_{10}$ bytes

$= (2^8 - 1)_{10}$ bytes

[NAT]

#Q. The DMA controller has data count register of size 8-bits. The memory is byte addressable.

1. Minimum how many times DMA needs to take control from CPU to transfer a file of 500 bytes? $\left\lceil \frac{500\,B}{255\,B} \right\rceil = 2$
2. Minimum how many times DMA needs to take control from CPU to transfer a file of 15K bytes?

$$\left\lceil \frac{15 * 2^{10}\ B}{255\ B} \right\rceil = 61$$

[NAT]

GATE- PYQ

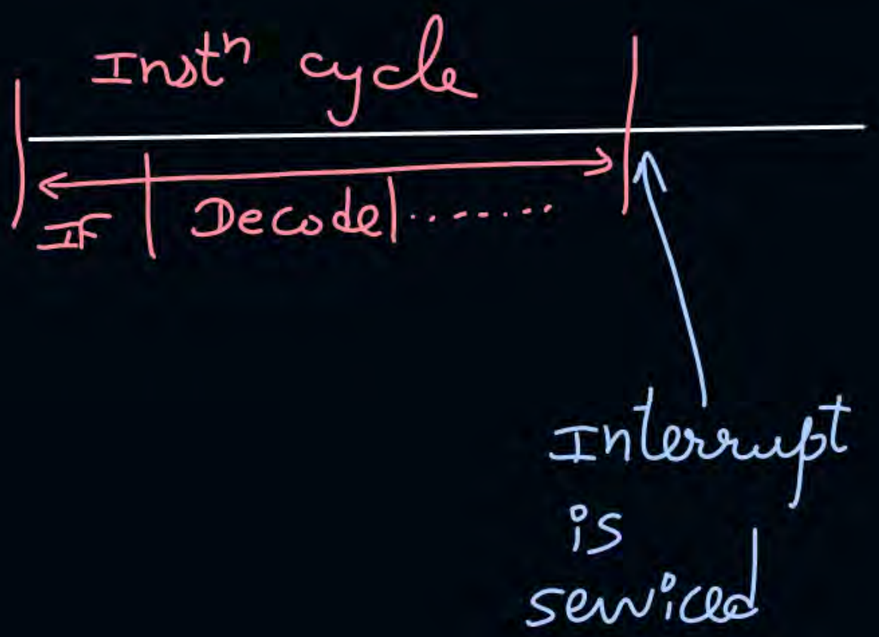
#Q. The size of the data count register of a DMA controller is 16bits.

The processor needs to transfer a file of 29, 154 kilobytes from disk to main memory.

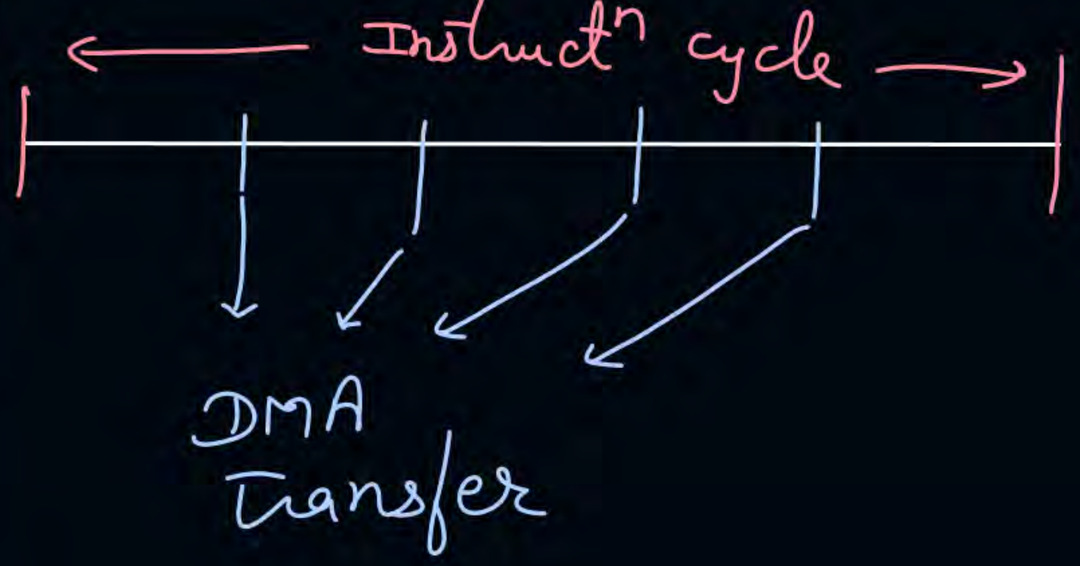
The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is _____ .

$$\left\lceil \frac{29154 * 2^{10}}{2^{16} - 1} \right\rceil = 456 \text{ Ans.}$$

Interrupt (External)



DMA:-



Memory Organization

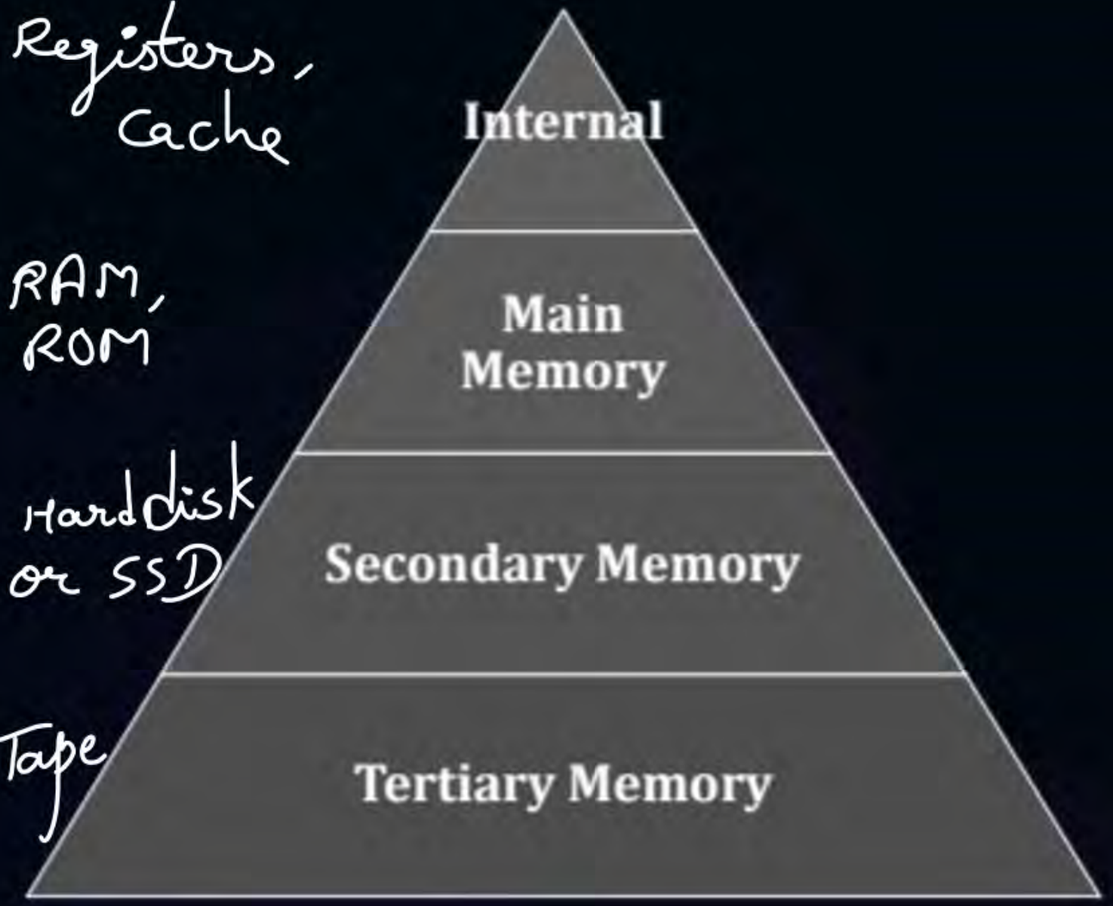
Topic : Memory Hierarchy

Memory hierarchy used when discussing performance issues.

Goal of Memory Hierarchy:

1. To maximize the Access Speed
2. To minimize the Per Bit Storage Cost

Topic : Memory Hierarchy



Registers, Cache

RAM, ROM

Hard disk or SSD

Tape

Memory cycle time :-

Time needed to read/write on one address of memory.

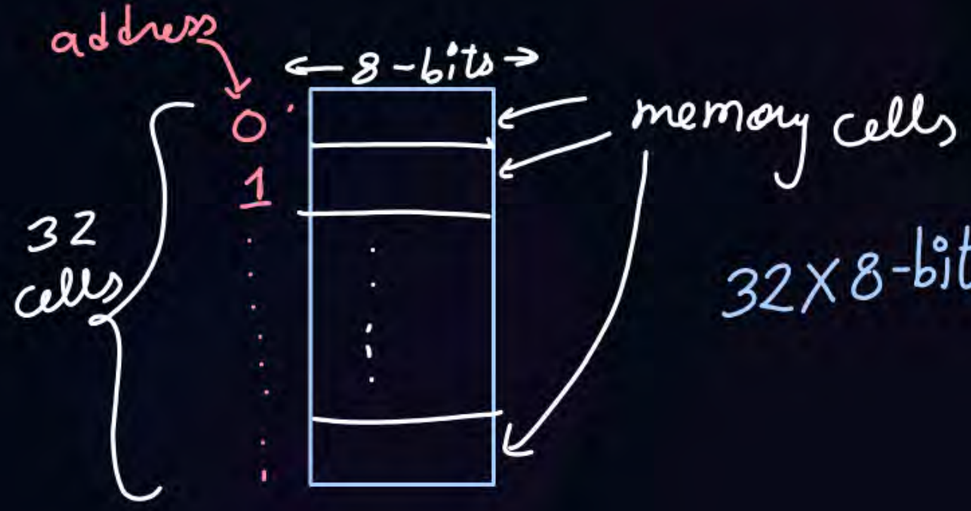
Topic : Memory Presentation

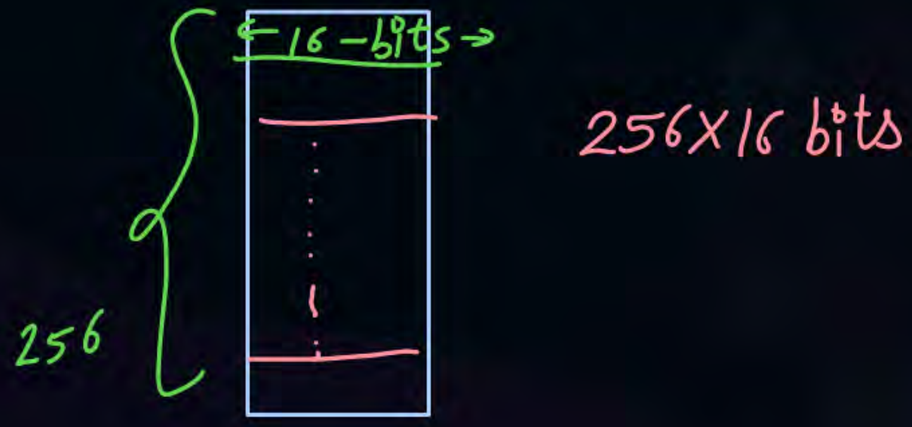
Addressable memory

Memory is represented as:

= No. of cells × 1 cell storage capacity

= No. of memory locations × bits per memory location





Topic : Memory Presentation

No. of cells	4	8	2^x	n
Address size	2 bits	3 bits	x bits	$\lceil \log_2 n \rceil$ bits

Topic : Memory Presentation

Assume a mem.

128k x 8 bits

128k x 1 byte ⟹ no. of cells = 128k = 2^{17}

per address ⟹ 1 byte stored ⟹ byte addressable memory

= 128k bytes ⟹ add. size = 17 bits

[MCQ]

#Q. Memory is represented as?

A. A×B where A = No. of memory locations, B = No. of bits in each location

B. $2^a \times B$ where a = No. of address bits, B = No. of bits in each location

C. B×A where, B = No. of bits in each location, A = No. of memory locations

D. (A) & (B) both ✓

[MCQ]

#Q. A memory has 14-bits address bus. Then how many memory locations are there?

$= 2^{14} = 16k = 16384$

A. 16K

B. 16384

C. 2^{14}

D. ✓ All

[MCQ]

#Q. The memory cycle time of a memory is 200nsec. The maximum rate with which the memory can be accessed?

Note: Consider memory as byte addressable.

A. 500 Bytes / Sec

B. 2000 Bytes / Sec

C. ✓ 5 Mbytes / Sec

D. 5 GBytes / Sec

In 200 ns, data accessed = 1 byte

In 1 ns, —11— = $\frac{1 \text{ byte}}{200 \text{ nsec}}$

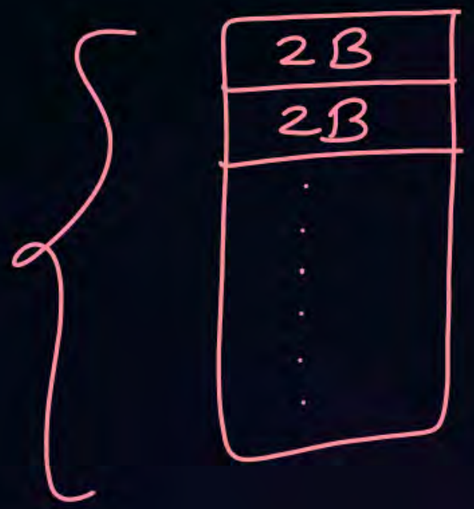
In 1 sec, —11— = $\frac{1 \text{ byte}}{200 * 10^{-9} \text{ sec}}$

$= \frac{10^9 \text{ bytes}}{200 \text{ sec}} = 5 \text{ MB/sec}$

[NAT]

GATE- PYQ

#Q. A processor can support a maximum memory of 4 GB, where the memory is word addressable (a word consists of two bytes). The size of the address bus of the processor is at least 31 bits?



no. of cells (addresses) $= \frac{4GB}{2B} = 2G = 2^{31}$

$\Downarrow$

add. = 31 bits

2 mins Summary

Topic Memory Hierarchy

Topic Memory Presentation

Happy Learning

THANK - YOU