

# CS & IT ENGINEERING

## COMPUTER ORGANIZATION AND ARCHITECTURE

### IO Organization

Lecture No.- 03

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# Recap of Previous Lecture



**Topic**

Modes of Transfer

**Topic**

Programmed IO

**Topic**

Interrupt IO



# Topics to be Covered



**Topic**

Direct Memory Access (DMA)

**Topic**

Cycle Stealing

**Topic**

Burst Mode



#Q. A device with data transfer rate 20 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 10 microsecond.

- (550  $\mu$ s)
1. Total time required in programmed IO for 10 bytes data transfer?
  2. Total time required in interrupt IO for 10 bytes data transfer?
  3. What is the minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode?

$$\begin{aligned}
 \text{1. Time needed in programmed I/O} &= \text{time to check status} + \text{Data transfer time} \\
 &= 1 \text{ Byte status Reg.} + 10 \text{ Bytes transfer time} \\
 &= 50 \mu\text{sec} + (10 * 50) = 550 \mu\text{sec}
 \end{aligned}$$

for 20kB, device takes = 1sec

$$\text{for 1 Byte} \quad \text{---||---} = \frac{1\text{sec}}{20\text{kB}} * \cancel{1\text{B}}$$

$$= \frac{1}{20} \text{ msec}$$

$$= \frac{1000}{20} \text{ } \mu\text{sec}$$

$$= 50 \text{ } \mu\text{sec}$$



2. Total time in interrupt I/O = Interrupt overhead + Service time

$$= 10 \mu\text{sec} + (10 * 50) \mu\text{s}$$
$$= 510 \mu\text{sec}$$

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3. performance gain  
or  
speed up  
of faster technique

$$= \frac{\text{older technique time}}{\text{faster technique time}} = \frac{550 \mu\text{sec}}{510 \mu\text{sec}}$$
$$= 1.078$$



[NAT]

Ans = 25

GATE-PYQ 2005



#Q. A device with data transfer rate 10KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 4 microsec. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program-controlled mode?

$$\begin{aligned} \text{for } 10 \text{ KB, time} &= 1 \text{ sec} \\ \text{for } 1 \text{ B, time} &= \frac{1 \text{ sec}}{10 \text{ KB}} * \cancel{1 \text{ B}} \\ &= \frac{1}{10} \text{ msec} \\ &= 100 \text{ } \mu\text{sec} \end{aligned}$$

$$\begin{aligned} \text{Programmed I/O time} &= 100 + 0 = 100 \text{ } \mu\text{s} \\ \text{Interrupt I/O time} &= 4 + 0 = 4 \text{ } \mu\text{s} \end{aligned}$$

$$\text{performance gain} = \frac{100 \text{ } \mu\text{s}}{4 \text{ } \mu\text{s}} = 25$$



## Topic : DMA

(Direct Memory Access)



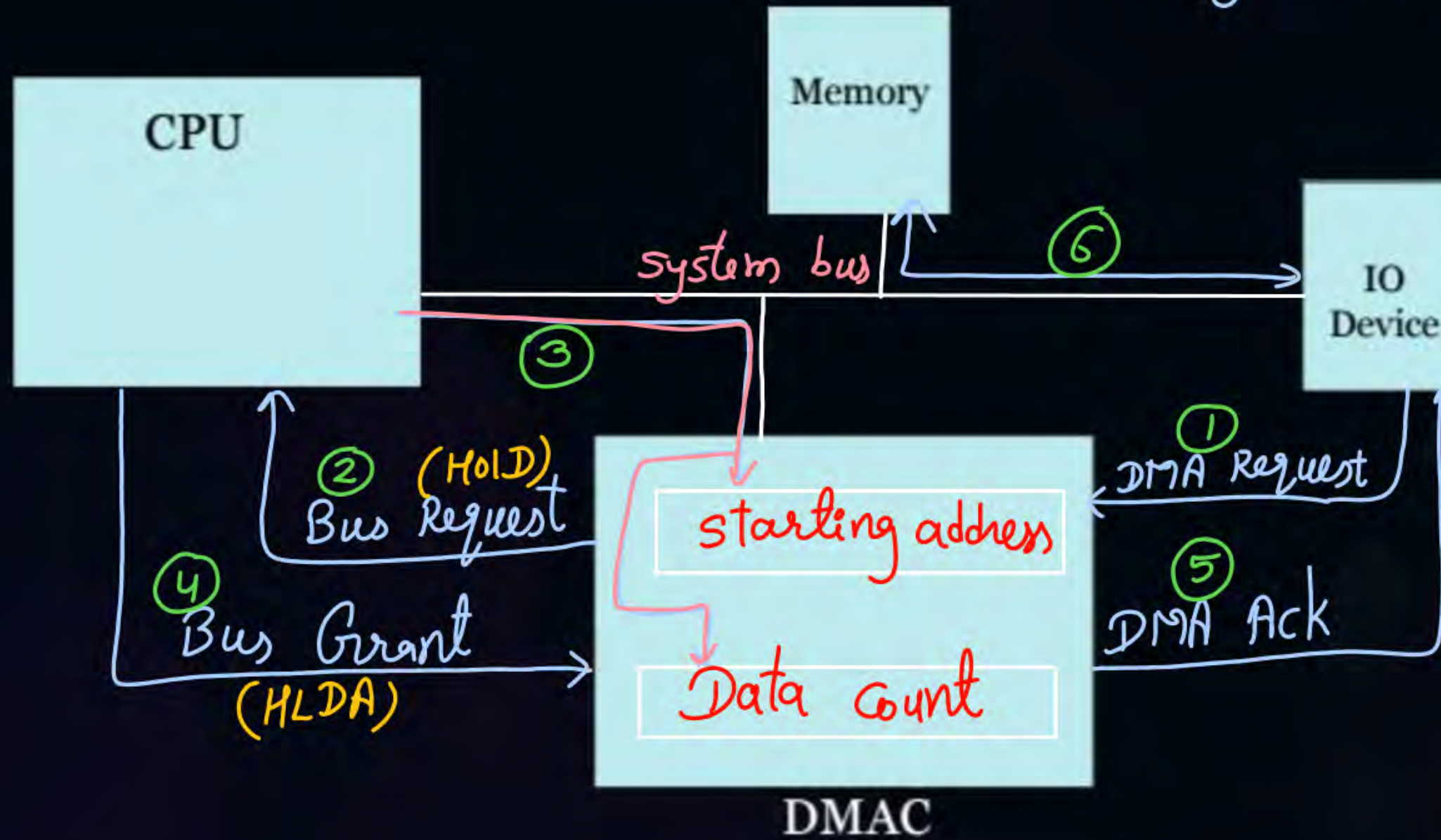
- Enables data transfer between I/O and memory without CPU intervention
- Need a hardware: DMAC (DMA Controller)





## Topic : DMA

$$t_x = 100 \text{ ms}$$
$$t_y = 5 \text{ ms}$$







## Topic : DMA

1. Starting Address :- add. of mem. starting from where data transfer starts in memory
2. Data Count :- No. of bytes/words to be transferred.

<u>example</u>	Initially	After 1B transferred	After 1B		
starting add.	200	201	202	...	Transfer stops when data count becomes zero.
Data count	50	49	48	...	



During DMA transfer CPU can not use system buses.

So CPU can perform only those operations which do not require system bus; which means CPU remains idle or blocked during that time.



## Topic : Modes of DMA Transfer

After how much time (when) CPU takes back control of the bus from DMAC.





## Topic : Modes of DMA Transfer

1. Burst Mode
2. Cycle Stealing
3. Interleaving DMA



## Topic : Modes of DMA Transfer



### **Burst Mode :**

when control of the buses is given to DMAC, then a burst (block) of data is transferred before CPU takes back the bus control.





## Topic : Modes of DMA Transfer



### Cycle Stealing :

slow I/O device takes time to prepare data internally. During that time CPU keeps the control of the buses. When the data (1 byte or 1 word) is prepared, DMAC steals buses for 1 cycle from CPU and transfers the prepared data to memory; and again bus control is returned to CPU after that.

Data preparation time in I/O  $\Rightarrow$  Calculated based on speed of I/O

Data transfer time to memory  $\Rightarrow$  ——— | | ——— " ——— of memory

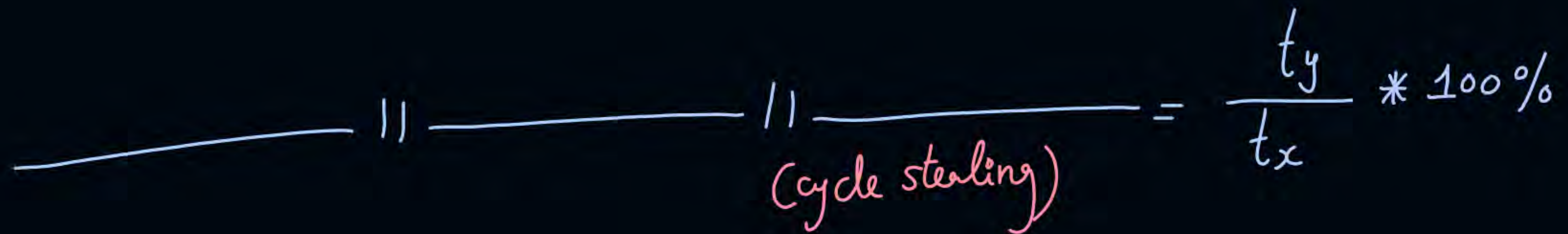
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Assume,  
Data preparation time in I/O =  $t_x$   
Data transfer time to memory =  $t_y$

$$\text{Percentage of time CPU is blocked due to DMA} = \frac{t_y}{t_x + t_y} * 100\%$$

(Burst Mode)



The diagram illustrates the cycle stealing technique. It consists of a horizontal line representing a timeline. Two vertical double lines (||) intersect this horizontal line, dividing it into three segments. The middle segment is labeled "(cycle stealing)" in red. The entire diagram is followed by an equals sign and the formula  $\frac{t_y}{t_x} * 100\%$ .

$$\text{---} || \text{---} || \text{---} = \frac{t_y}{t_x} * 100\%$$

(cycle stealing)

$$\text{Ans} = 12.5\%$$

#Q. Consider a device operating on 1MBPS speed and transferring the data to memory using cycle stealing mode of DMA. If it takes 2 microseconds to transfer 16 bytes data to memory when it is ready/prepared. Then percentage of time CPU is blocked due to DMA is?

$$t_y = 2 \mu\text{sec}$$
$$t_x = 16 \mu\text{sec}$$

$$\text{for 1MB preparat}^n, \text{time} = 1\text{sec}$$

$$\text{for 16B} \text{ --- }, \text{time} = \frac{1\text{sec}}{1\text{MB}} * 16\text{B}$$

$$t_x = 16 \mu\text{sec}$$

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$$\begin{aligned} \% \text{ of time CPU blocked due to DMA} &= \frac{2 \mu\text{s}}{16 \mu\text{s}} * 100\% \\ &= 12.5\% \end{aligned}$$





## 2 mins Summary



**Topic**

Modes of Transfer

**Topic**

Programmed IO

**Topic**

Interrupt IO



**Happy Learning**

**THANK - YOU**