CS & IT ENGINEERING

DIGITAL LOGIC

Sequential Circuit

Lecture No. 09

By- CHANDAN SIR

01 Counters

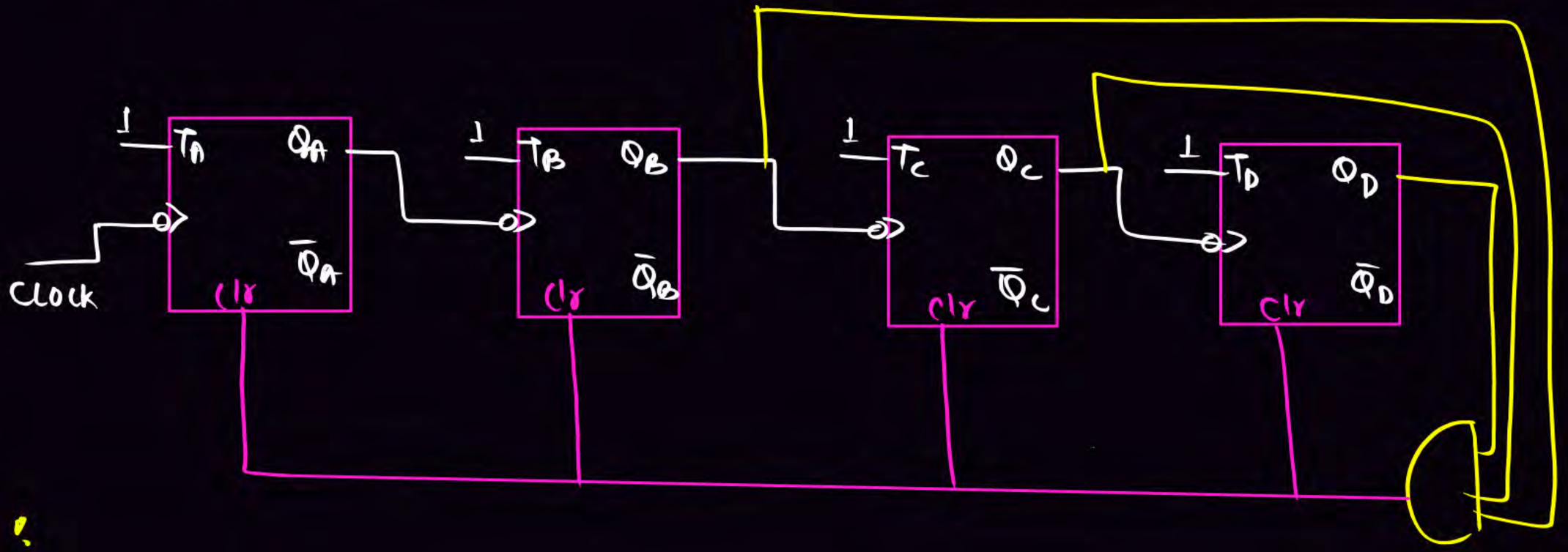
02 PRACTICE

03 DISCUSSION

COUNTER

1. Asynchronous counter [Ripple counter]
2. Synchronous counter
   - Ring counter
   - Johnson counter

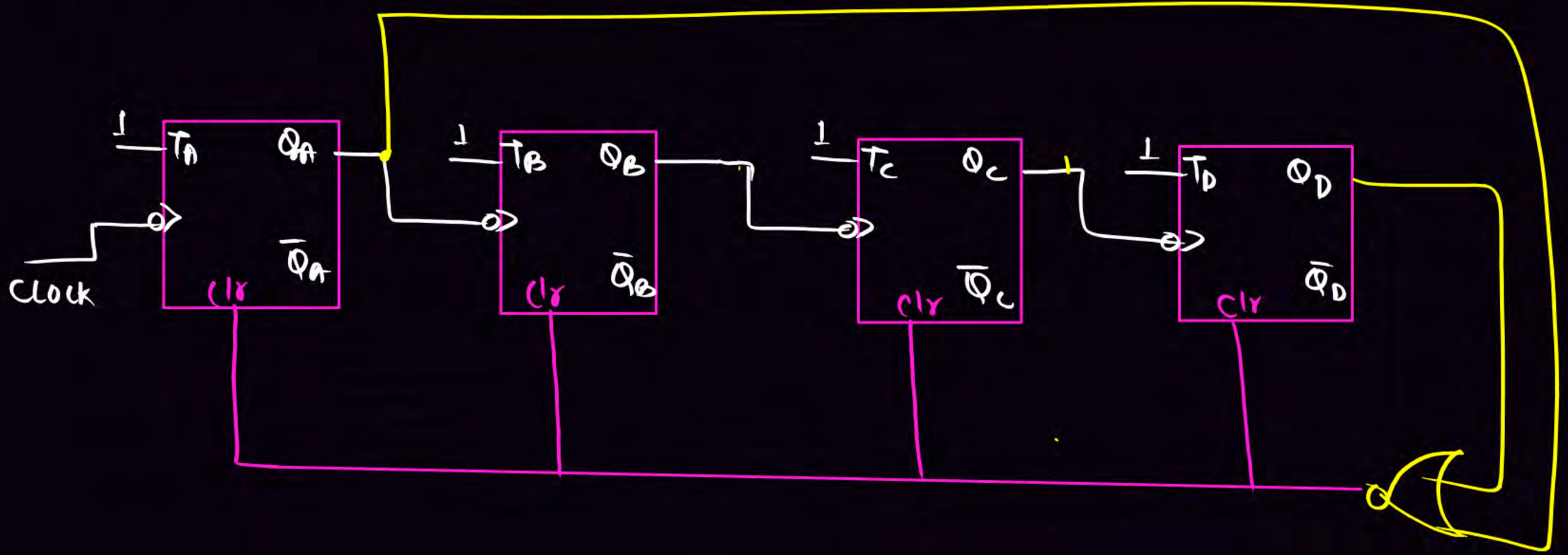
Asynchronous counter



$Clr = Q_D Q_C Q_B \bar{Q}_A$

$1110 = (14)$

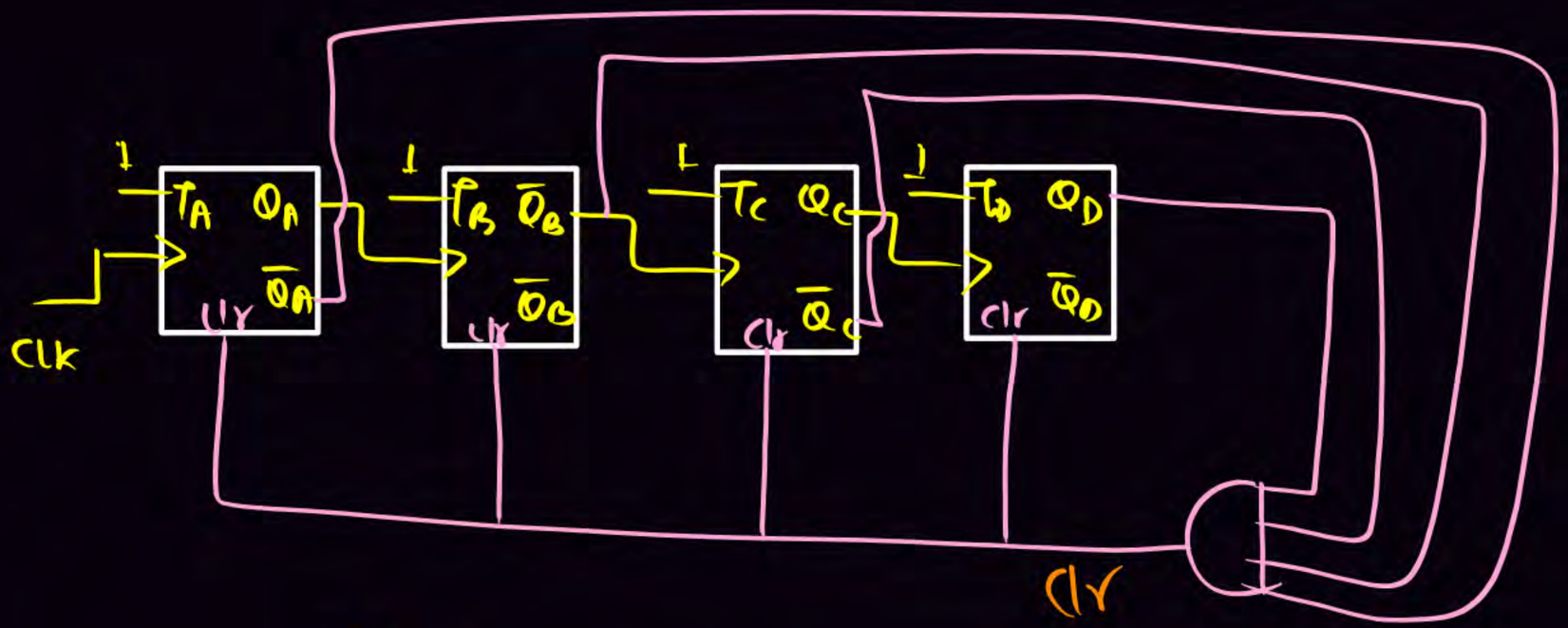
Asynchronous counter



CLOCK	$Q_D Q_C Q_B Q_A$	$CLR = \overline{Q_D + Q_A}$
0	0 0 0 0	1
1	0 0 0 1	0
2	0 0 1 0	1 → 0
3	0 0 0 1	0
4		
5		
6		
7		
8		

MOD = 2

5



4bit down counter

$Clr = Q_D \bar{Q}_C Q_B \bar{Q}_A$

1 0 1 0 = 10

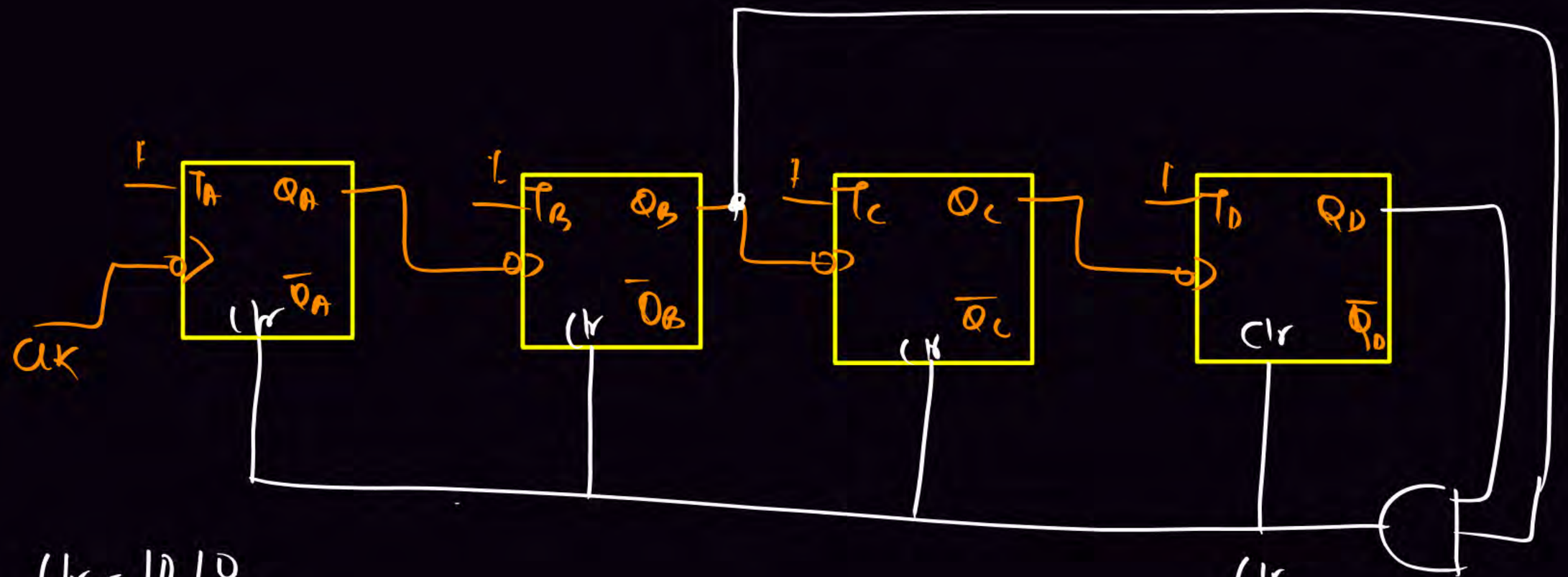
16 − 10 = 6

MOD 6 down

Ripple counter

BCD counter

0000
0001
0010
0011
0100
0101
0110
0111
1000
1001

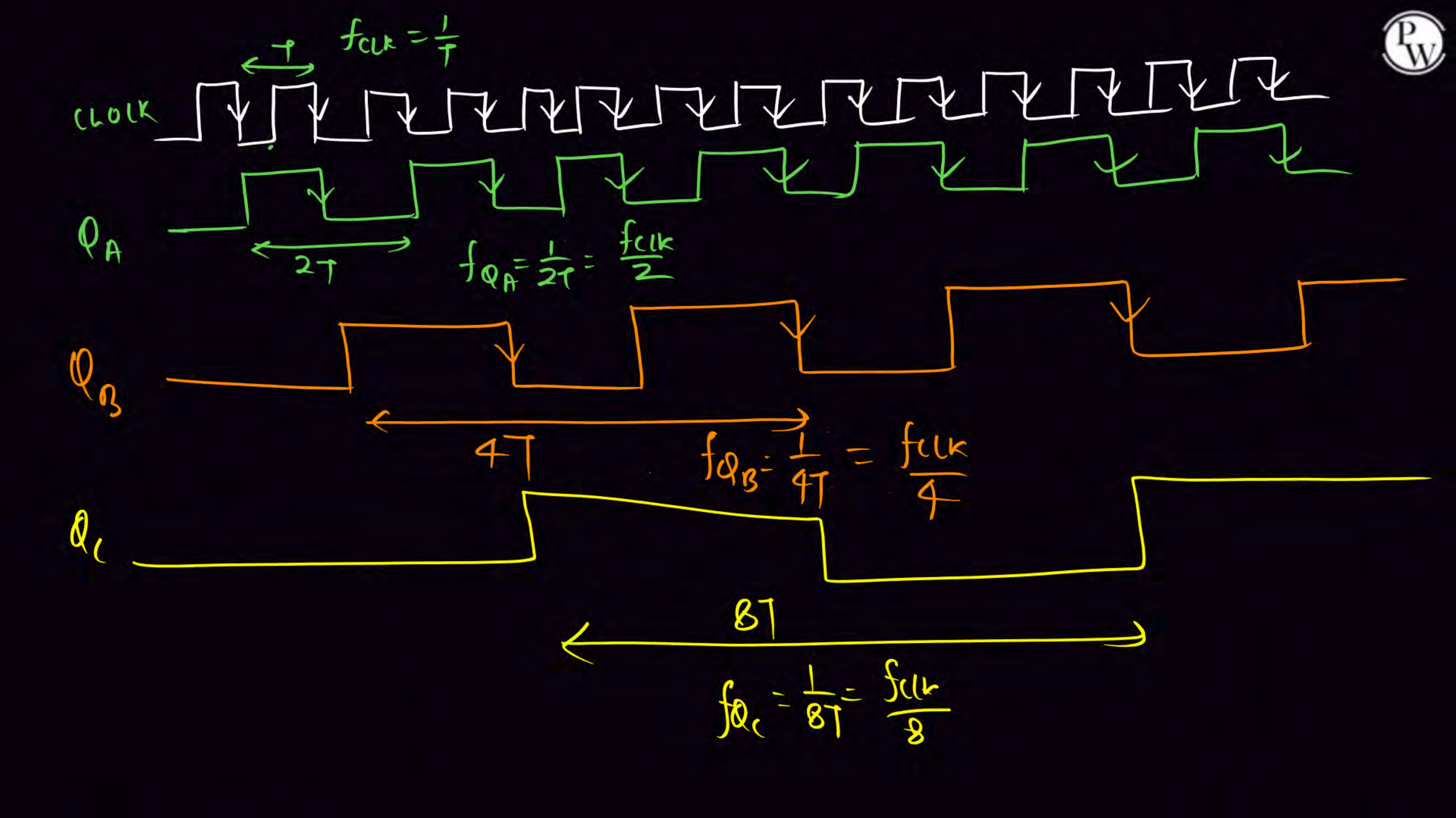


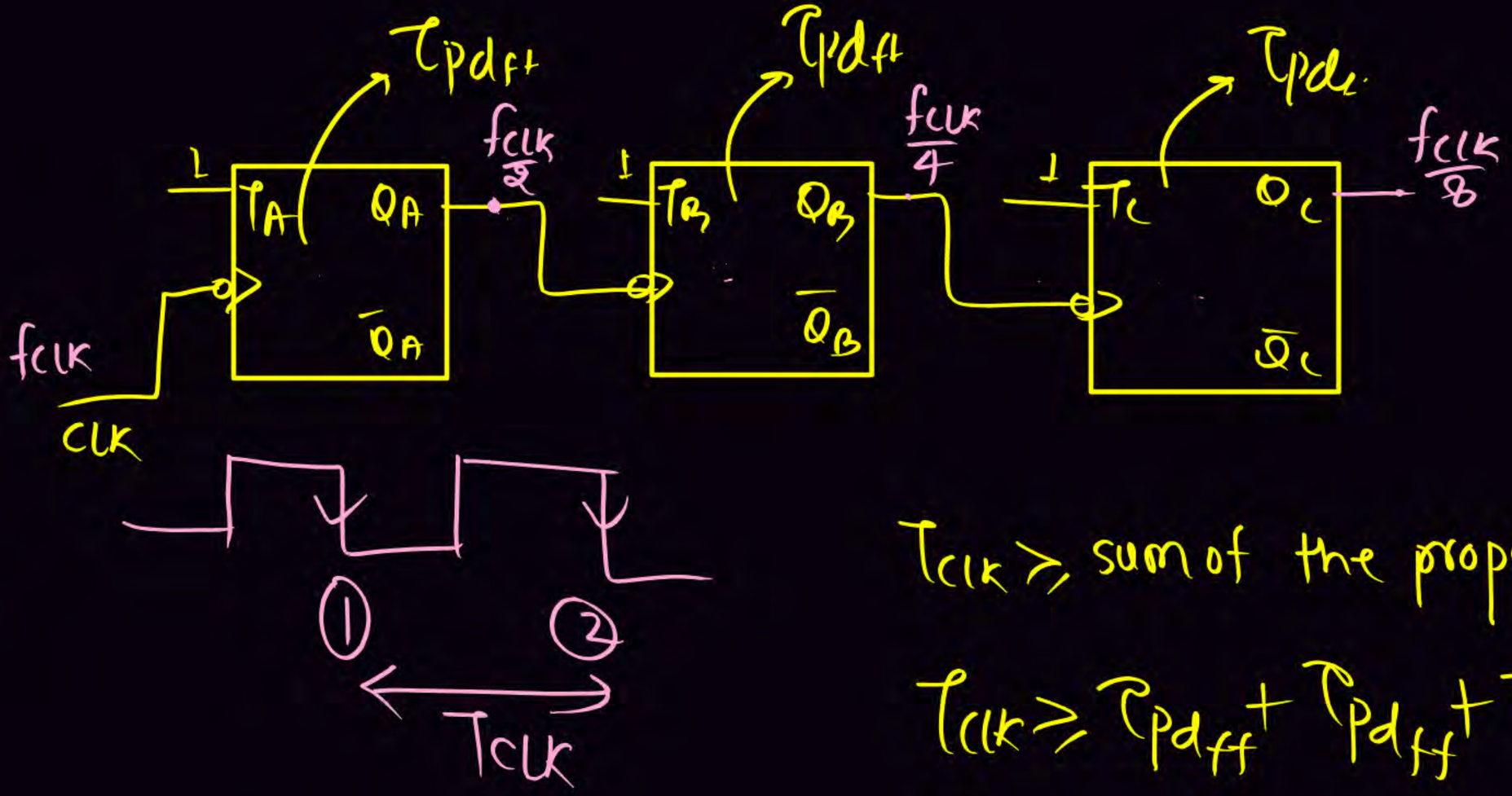
$Clr = 1010$

$= Q_D \bar{Q}_C Q_B \bar{Q}_A$

$Clr = Q_D \bar{Q}_C Q_B \bar{Q}_A$

$1010 = (10)$


T
$f_{CLK} = \frac{1}{T}$
CLOCK
Q_A
2T
$f_{Q_A} = \frac{1}{2T} = \frac{f_{CLK}}{2}$
Q_B
4T
$f_{Q_B} = \frac{1}{4T} = \frac{f_{CLK}}{4}$
Q_C
8T
$f_{Q_C} = \frac{1}{8T} = \frac{f_{CLK}}{8}$



$T_{CLK} \geq$ sum of the propagation delay of all the FF.

$T_{CLK} \geq \tau_{pd_{FF}} + \tau_{pd_{FF}} + \tau_{pd_{FF}}$

$T_{CLK} \geq 3\tau_{pd_{FF}}$

n bit Ripple counter

$$T_{clk} \geq n \cdot \tau_{pdff}$$

$$f_{clk} \leq \frac{1}{n \cdot \tau_{pdff}}$$

$$(f_{clk})_{max} = \frac{1}{n \cdot \tau_{pdff}}$$

Q In 4 bit Ripple counter all the FF's are identical and having propagation delay 10 μs. Then for smooth operation maximum clock frequency will be?

$$(f_{clk})_{max} = \frac{1}{n \cdot t_{pd_{FF}}} = \frac{1}{4 \times 10 \times 10^{-6}} = \frac{10^6}{4 \times 10} = \frac{1000 \times 10^3}{4 \times 10} = 25\ kHz$$

Thank you

GW

Soldiers !