CS & IT



ENGINEERING



Combinational Circuit

Lecture No. 2



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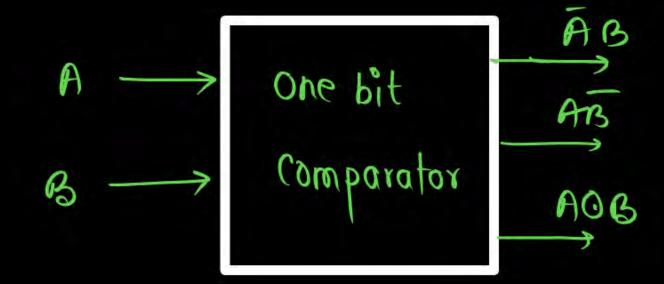
TOPICS TO
BE
COVERED

01 MULTIPLEXER

02 QUESTION PRACTICE

03 DISCUSSION

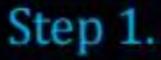
$$\sqrt{X(A>B)} = A\overline{B}$$







Q. Design a two-Bit comparator?





Step 2. Truth table

A ₁	Ao	B ₁	B ₀	x	у	
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			



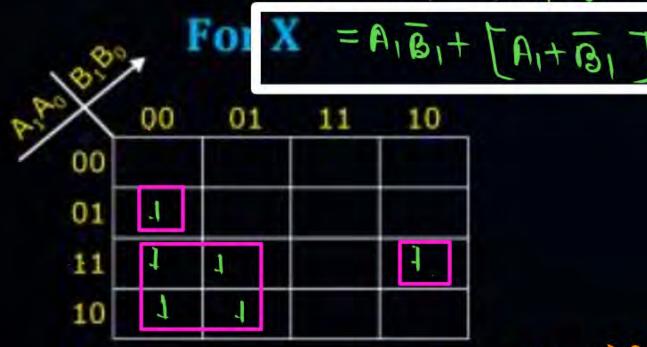
Pw

COMPARATOR

$$\Upsilon(A < B) = \overline{A_1}B_1 + \overline{A_1}\overline{A_0}B_0 + \overline{A_0}B_1B_0$$

Thin mixed

$$X(A>B)=A_1\overline{B}_1+A_0\overline{B}_1\overline{B}_0+A_1A_0\overline{B}_1$$

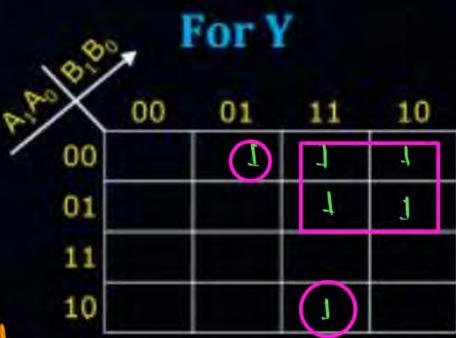


 $\chi = A_1 \overline{B}_1 + (A_1 O B_1) \cdot A_0 \overline{B}_0$

$$\chi(A>B) = A_1B_1 + \overline{A_1A_0B_1B_0} + A_1A_0B_1B_0 \qquad \text{Expression.}$$

$$= A_1B_1 + \overline{A_1B_1} + \overline{A_1B_1} + \overline{A_1B_1} + \overline{A_0B_0}$$

$$= A_1B_1 + \overline{A_1B_1} + \overline{A_1B_1} + \overline{A_0B_0}$$



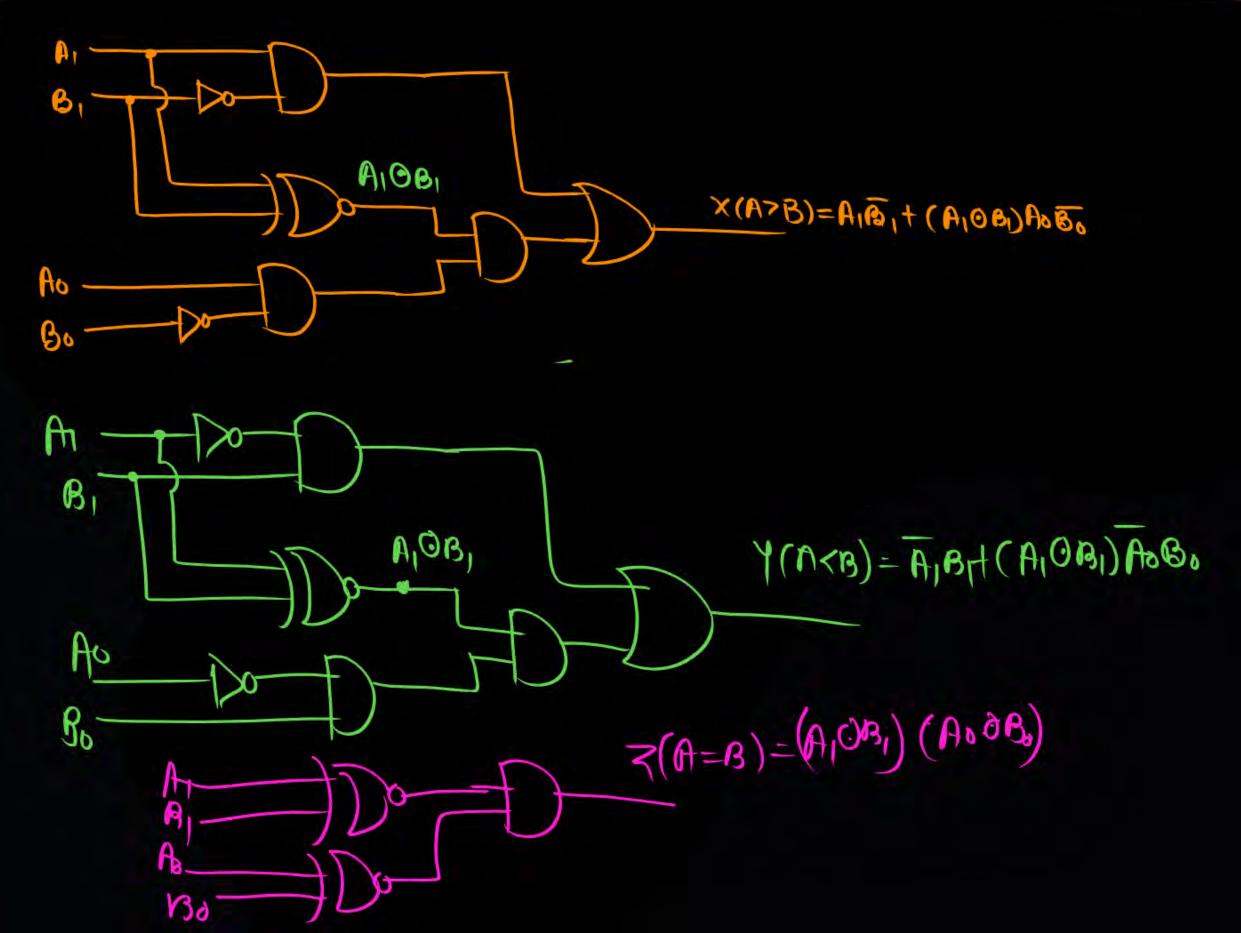


Step 4. Minimization

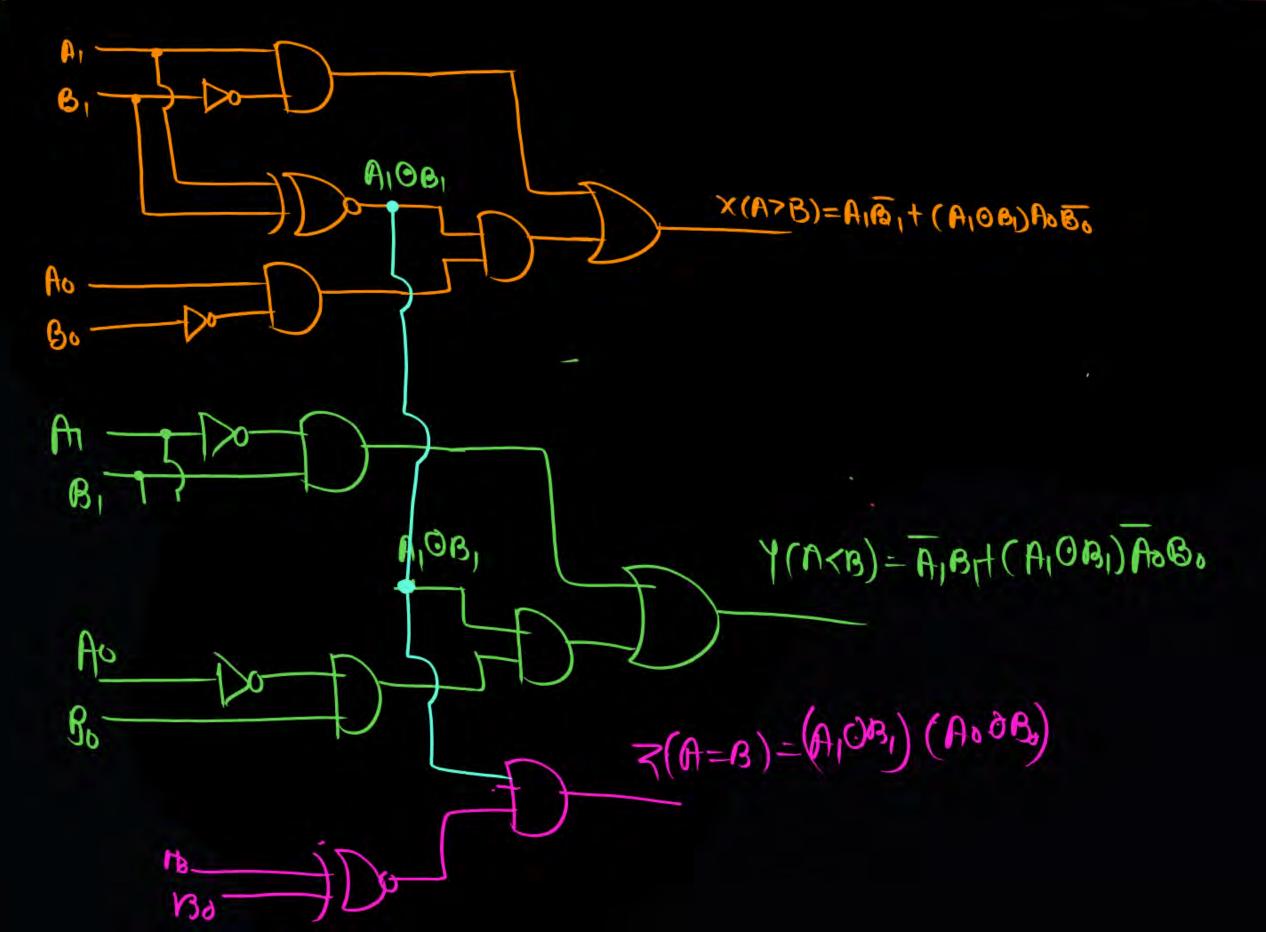
For
$$Z = (A_1 \odot B_1) \cdot (A_0 \odot B_0)$$

100	×			
B'SON	00	01	11	10
00	1			
01		1		
11			1	
10				1











FOR ONE BIT COMPARATOR

Total condition = 4

Equal condition = 2

Unequal condition = 2

Greater = Less condition = 1



FOR TWO BIT COMPARATOR

Total condition = 16

Equal condition = 4

Unequal condition = 12

Greater = Less condition = 6

6



FOR THREE BIT COMPARATOR

Total condition = 64

Equal condition = 8

Unequal condition = 56

Greater = Less condition = 28



'N' BIT COMPARATOR

Total condition = 2^{2n}

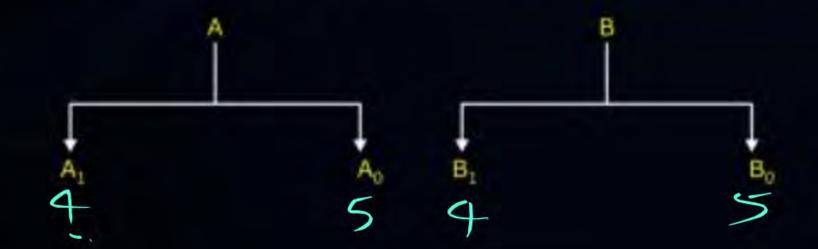
Equal condition = 2ⁿ

Unequal condition = $2^{2n} - 2^n$

Greater = Less condition = $(2^{2n} - 2^n)/2$

SHORT TRICK TO USE SEMI MINIMIZED EXPRESSION





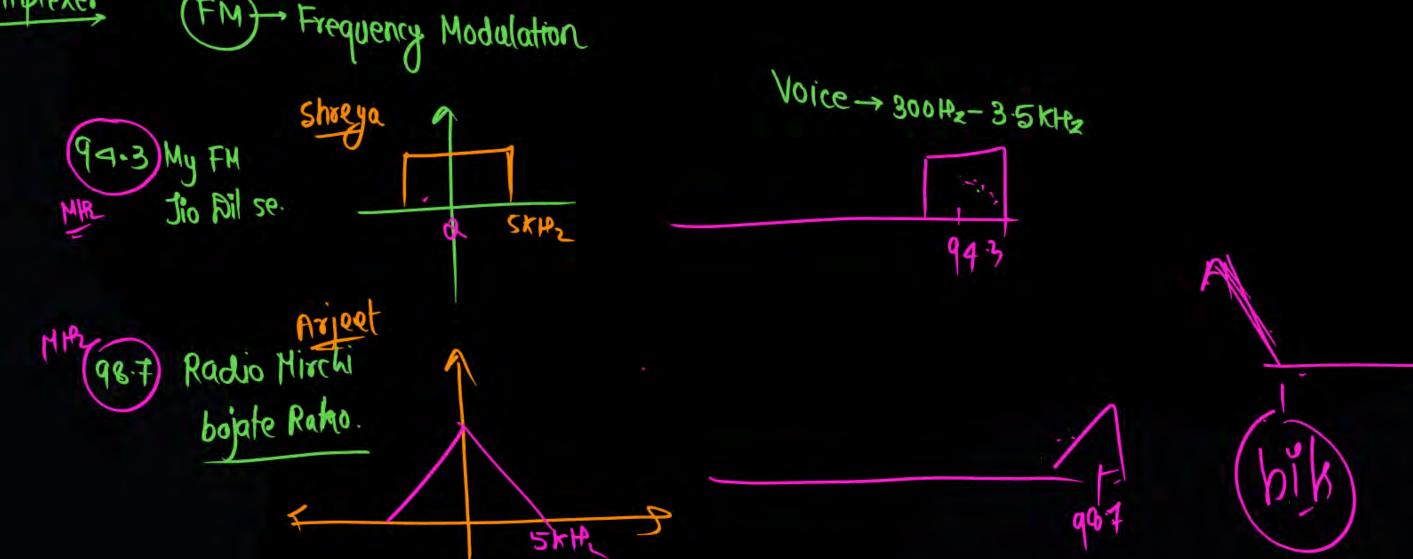
$$X(A>B) = A_1B_1 + (A_1OB_1)A_0B_0$$

$$\chi(A > B) = A_2 B_2 + (A_2 O B_2) A_1 B_1 + (A_2 O B_2) \cdot (A_1 O B_1) A_0 B_0$$

$$\chi(A < B) = \overline{A_2} B_2 + (A_2 O B_2) \overline{A_1} B_1 + (A_2 O B_2) \cdot (A_1 O B_1) \overline{A_0} B_0$$

$$\chi(A = B) = (A_2 O B_2) \cdot (A_1 O B_1) \cdot (A_0 O B_0)$$



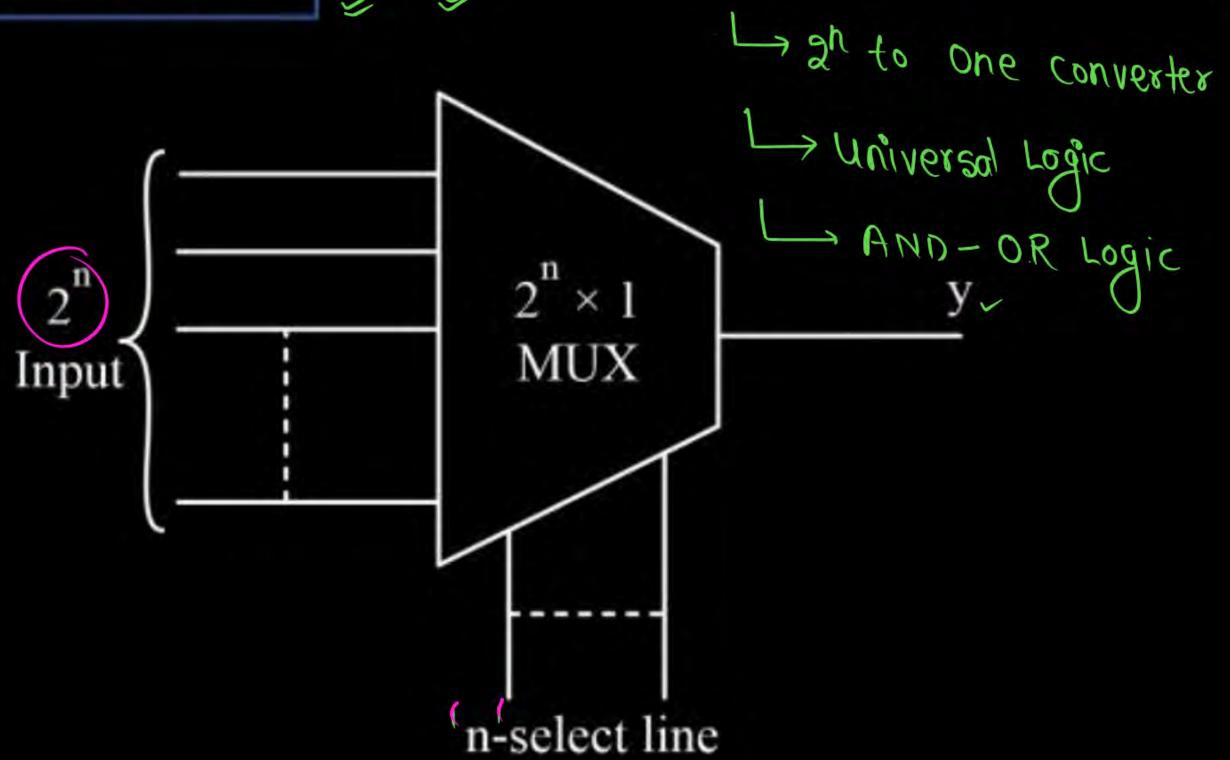




MULTIPLEXER







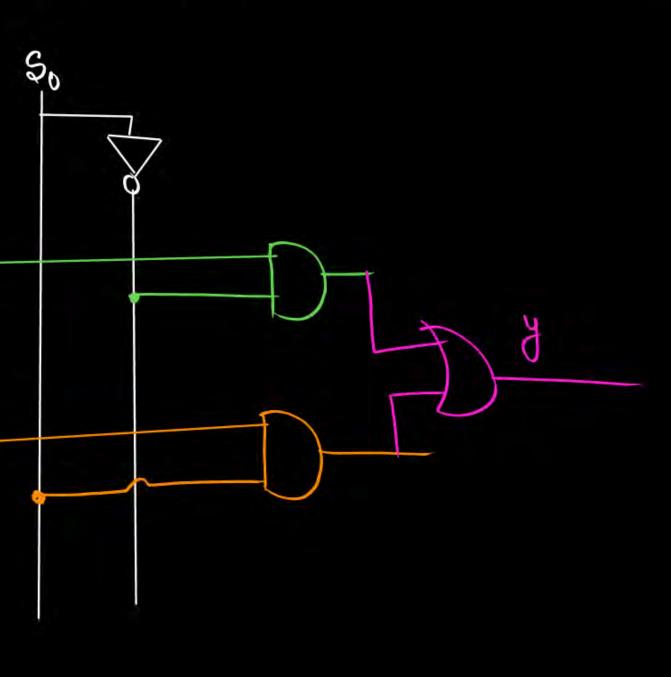
Multiplexer

Pw

Design a 2 × 1 MUX

Step 1:>	70	So
	<u>I</u>	₹S _o
		So

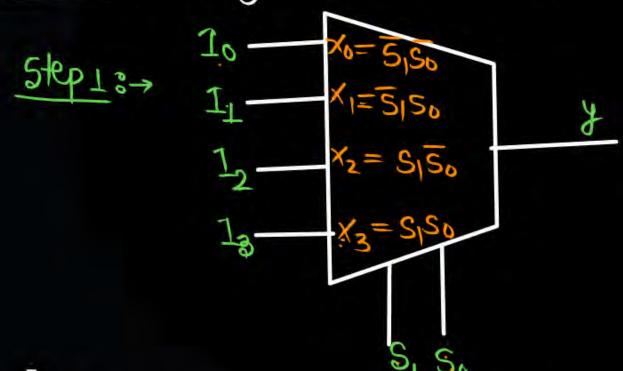
	a1004 ?-
= 50 To+	Sol
	Steps:



5	P	D.	8
	1		<u> </u>

\$0	7
0	Io
, 1	I_1

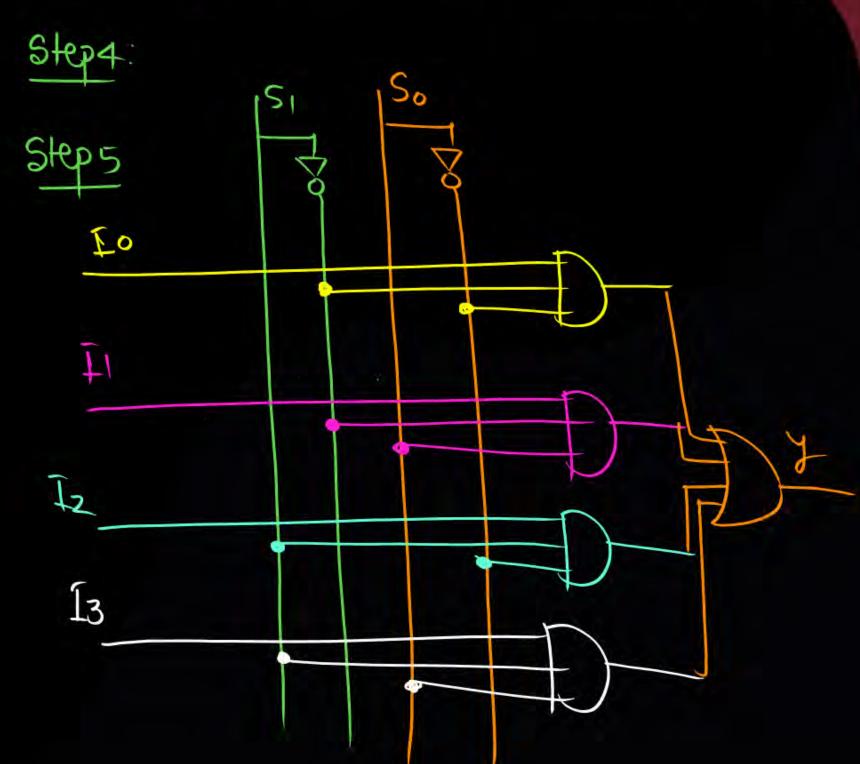
Question - Resign a 4x1 Mux?



Ste	P.Q.

0		
S	So	y
0		To
0	1	I,
1	0	T2
1	1	13





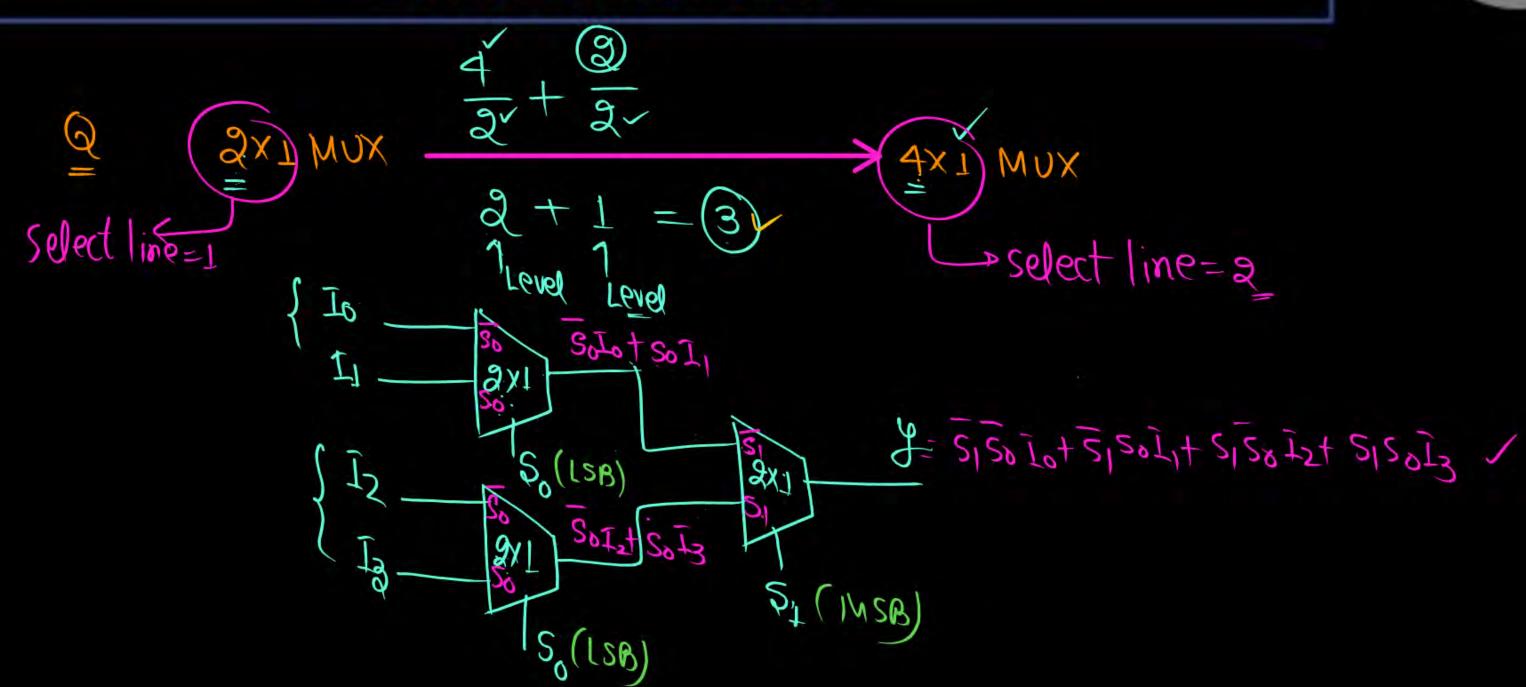
Q. Design a 8x1 Mux

Je Besign a 16x1 MUX.



Type 1. Designing of Higher order Mux By using Lower Order Mux







$$\frac{8}{2} + \frac{4}{2} + \frac{2}{2}$$

$$4 + 2 + 1 = 4$$
Aus

$$Q = 2 \times 1 \text{ MUX} = \frac{64}{2} + \frac{39}{3} + \frac{16}{3} + \frac{8}{2} + \frac{4}{2} + \frac{2}{2}$$

$$= 32 + 16 + 8 + 4 + 2 + 1 = 63$$

$$g = 2x1 MUX \qquad (a'-1) \qquad \Rightarrow a'' x1 MUX$$

$$\frac{16}{4} + \frac{4}{4} \rightarrow 16 \times 1 \text{ MUX}$$

$$= 4 \times 1 \text{ MUX}$$

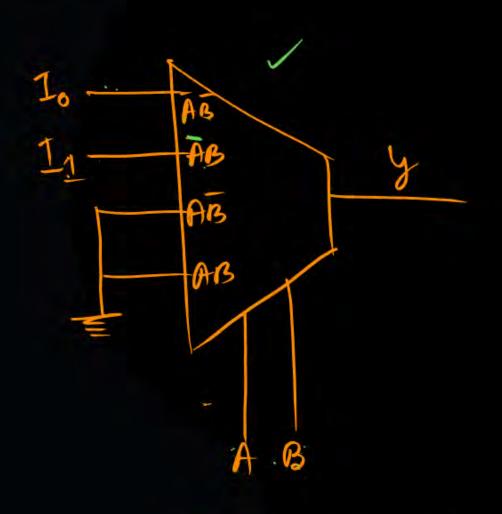
$$4 + 1 = \cancel{5} \text{ Arg}$$

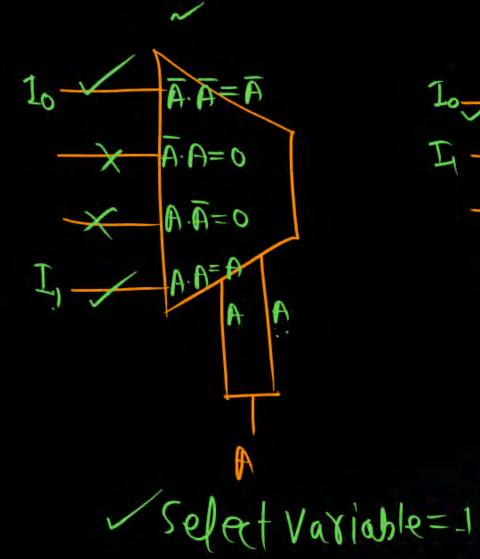
$$Q = 4 \times 1 \text{ MUX} \xrightarrow{64} + \frac{16}{4} + \frac{4}{4} \longrightarrow 64 \times 1 \text{ MUX}$$

$$16 + 4 + 1 = 21$$









$$\begin{array}{c|c}
\hline
I_0 & I_A = A \\
\hline
I_1 & A = A \\
\hline
X_1 & A = A \\
\hline
X_1 & A = A \\
\hline
X_2 & A = A \\
\hline
X_3 & A = A \\
\hline
X_4 & A = A \\
\hline
X_5 & A = A \\
\hline
X_6 & A = A \\
\hline
X_7 & A = A \\
\hline$$

Select Variable=1



8 + 4x1 Mux 9= 8x1 MUX. Select line=3 13

MULTIPLEXER



Design 64×1 MUX using 8×1 MUX.

$$8 \times 1 = \frac{64 + 8}{8 + 1 - (9)} \Rightarrow 64 \times 1 \text{ MOX}$$

$$4 \times 1 \text{ MUX} = \frac{32 + 8 + 2}{4 + 4} \Rightarrow 32 \times 1 \text{ MUX}$$

$$8 + 2 + 1 - (1) \Rightarrow 32 \times 1 \text{ MUX}$$



$$\frac{256 + 16}{16 + 16} \rightarrow 256 \times 1 \text{ MUX}$$

$$\frac{16 + 1 - 17}{40}$$



