CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

CPU & Control Unit

Lecture No.- 03

By- Vishvadeep Gothi sir

Recap of Previous Lecture

Topic Data Path

Topic Control Unit

Topic Hardwired Control Unit

Topics to be Covered

- Topic: Hardwired Control Unit
- Topic: Microprogrammed Control Unit
- Topic: RISC vs CISC
- Topic: Byte Ordering

Topic : Hardwired Control Unit

Control logic is implemented with Gates, flip-flops, decoders and other digital circuits.

Advantage: Can be optimized to produce a faster mode of operation.

Disadvantage: Rearranging the wires among various components is difficult.

→ can be implemented only for simple computers.

1. what type of inst^{ns}, CPU can support?

2. How to execute an inst^{n}?

↳ sequence of micro-operations to execute inst^{n}.

Inst^{n}	I1	I2	I3	I4 . . .
1.	micro-op 1	micro-op 1	:	:
2.	micro-op 2	micro-op 2	:	:
3.	micro-op 3	:	:	:
4.	4	:	:	:
5.	5	:	:	:
6.	:	:	:	:

for each micro-op^{n} what control word to be generated

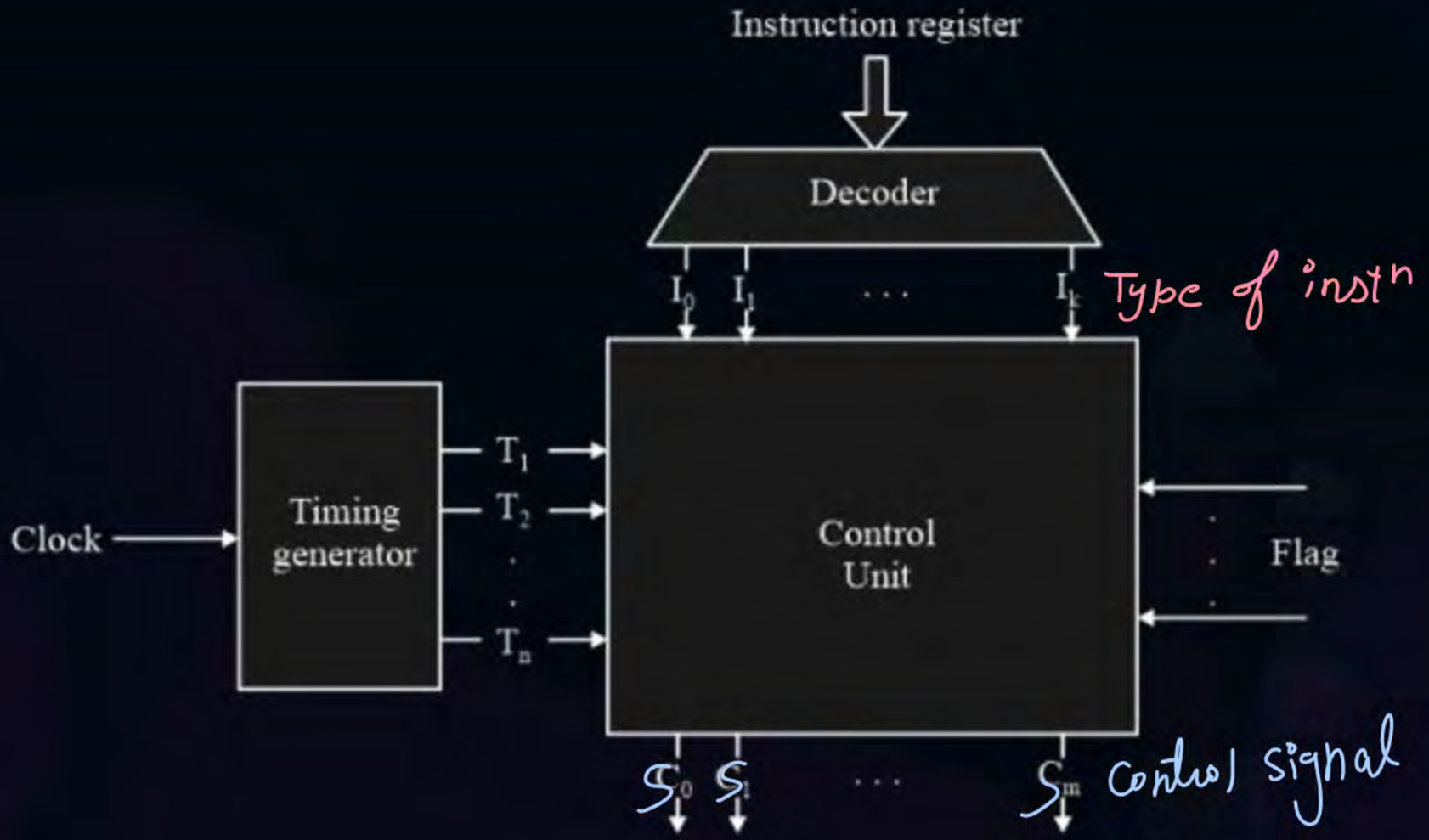
⇓

which signal to be active & which to be inactive

Table for Implementat^{n}

	I1	I2	IJ - - - -
T1	00110111000 (S3 S4 S6 S7 S8)		
T2			
T3			
T4			
T5			

Topic : Hardwired Control Unit



[MCQ]

GATE- 2005

#Q. A hardwired CPU uses 10 control signals S1 to S10, in various time steps T1 to T5, to implement 4 instructions I1 to I4 as shown below:

	T1	T2	T3	T4	T5
I1	S1, S3, S5	S2, S4, S6	S1, S7	S10	S3, S8
I2	S1, S3, S5	S8, S9, S10	S5, S6, S7	S6	S10
I3	S1, S3, S5	S7, S8, S10	S2, S6, S9	S10	S1, S3
I4	S1, S3, S5	S2, S6, S7	S5, S10	S6, S9	S10

Which of the following pairs of expressions represent the circuit for generating control signals S5 and S10 respectively?

A $S5 = T1+I2\cdot T3$ and
$S10 = (I1 + I3)\cdot T4 + (I2 + I4)\cdot T5$

B $S5 = T1+(I2+I4)\cdot T3$ and
$S10 = (I1 + I3)\cdot T4 + (I2 + I4)\cdot T5$

C $S5 = T1+(I2+I4)\cdot T3$ and
$S10 = (I1 + I3 + I4)\cdot T2 + (I2 + I3)\cdot T4+(I2+I4)\cdot T5$

D ✓ $S5 = T1+(I2+I4)\cdot T3$ and
$S10 = (I2 + I3)\cdot T2+I4\cdot T3+(I1 + I3)\cdot T4+(I2+I4)\cdot T5$

$S5 = T1 + I2\,T3 + I4\,T3$
$= T1 + (I2 + I4)\,T3$

Topic : Micro-Programmed Control Unit

Control logic is implemented with micro-programs.

Advantage: Updating the control logic is easy.

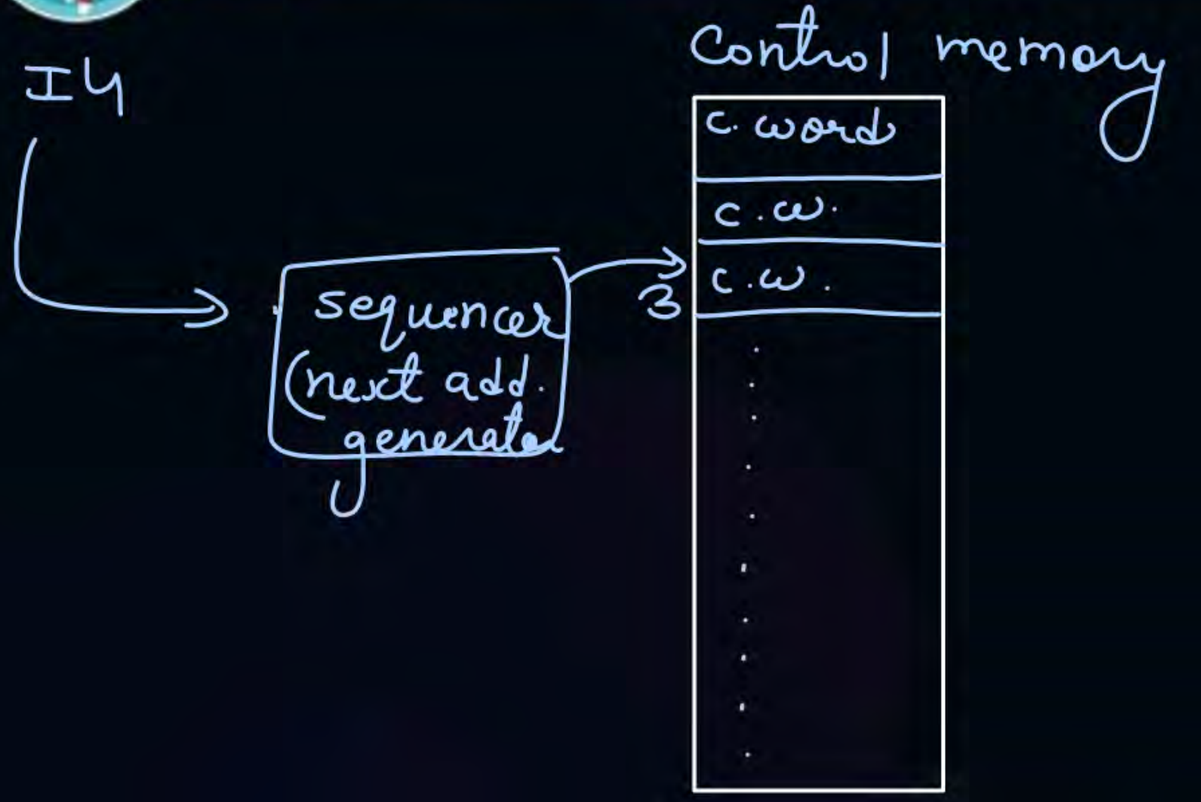
↳ can be implemented for complex computers also.

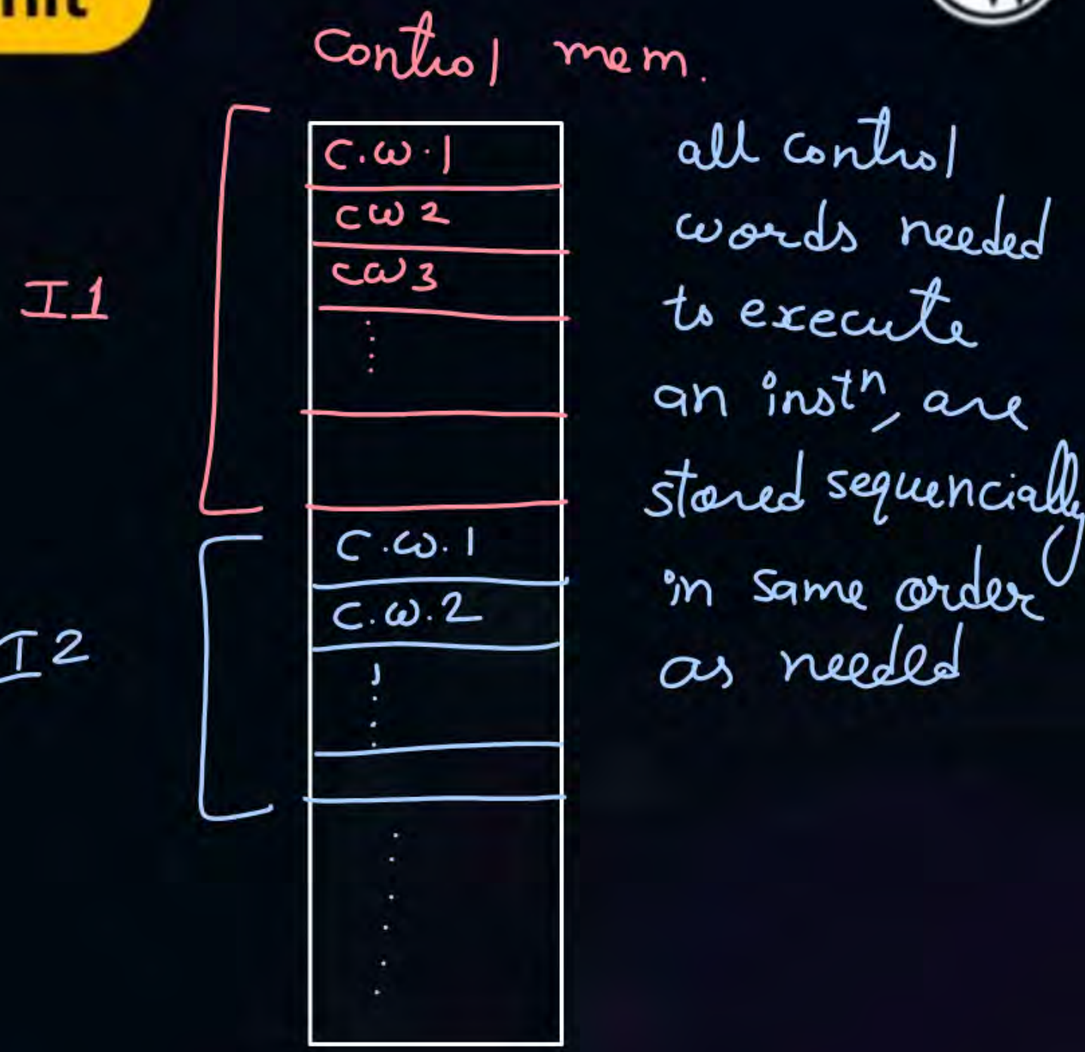
Disadvantage: Slower than hardwired control unit.

↳ All possible control words are stored in a memory inside control unit.

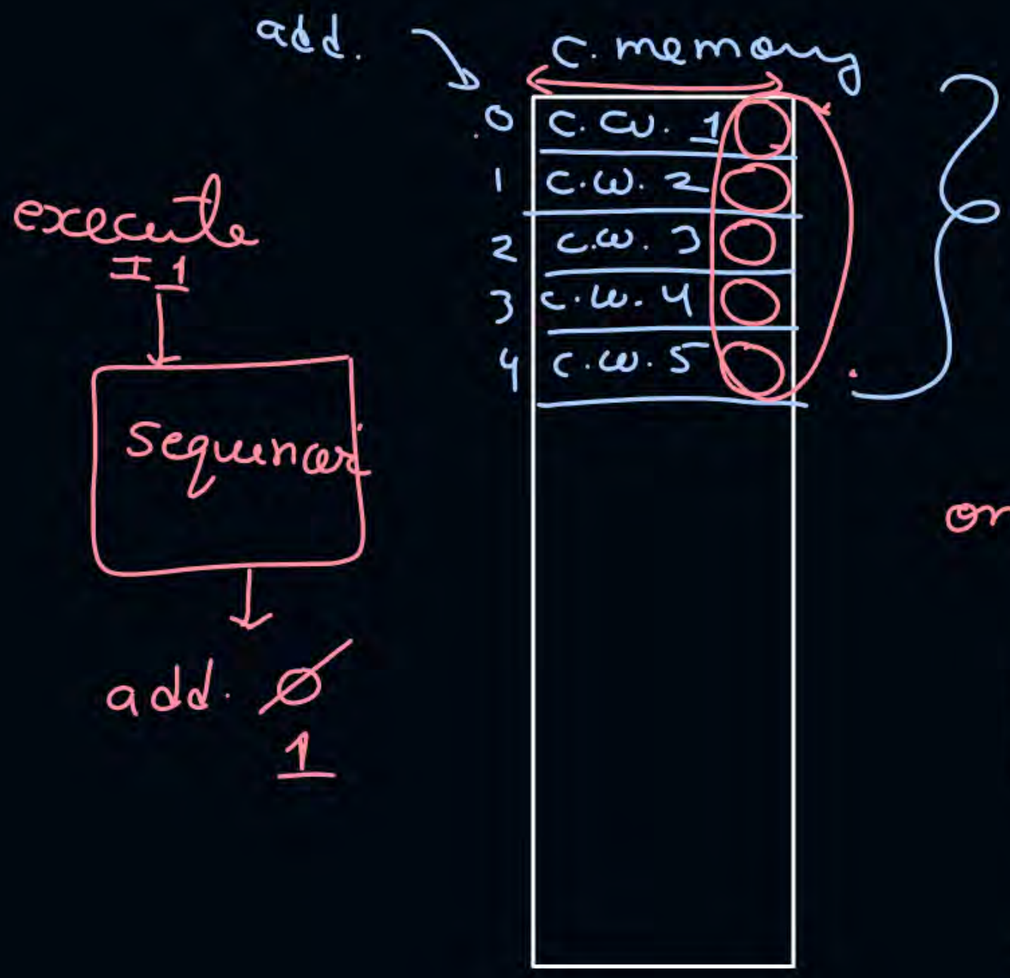
whenever needed, as per the requirement a control word is read from memory.

Topic : Micro-Programmed Control Unit

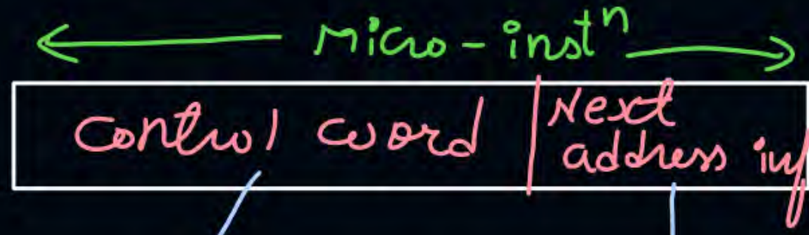




all control words needed to execute an instⁿ, are stored sequencially in same order as needed



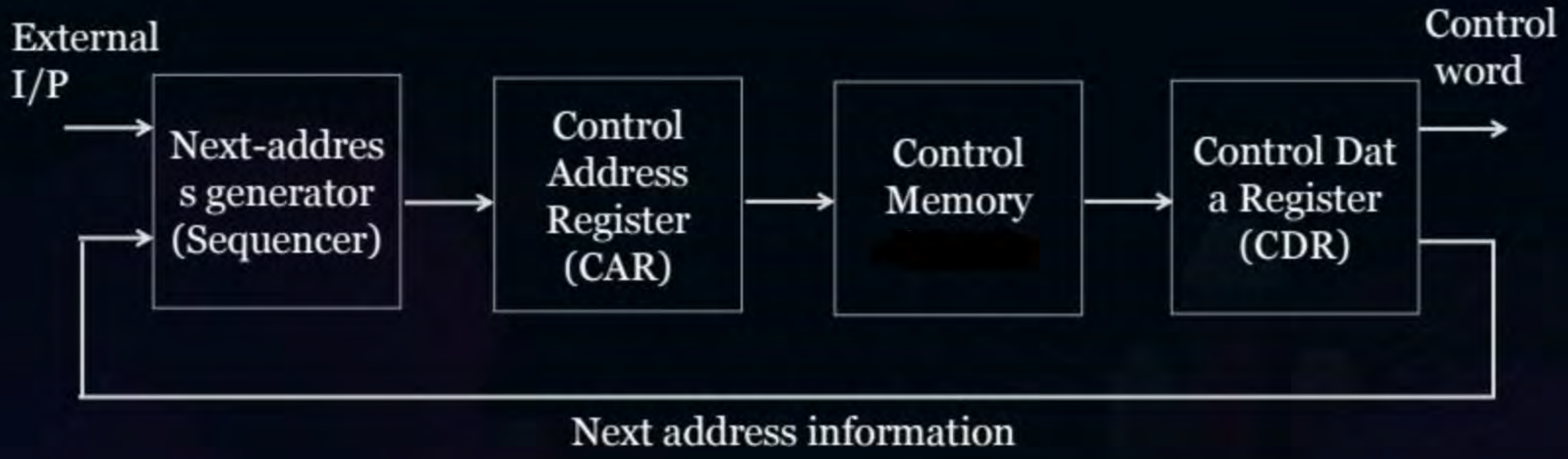
on Each add. in control memory



for micro-operatⁿ

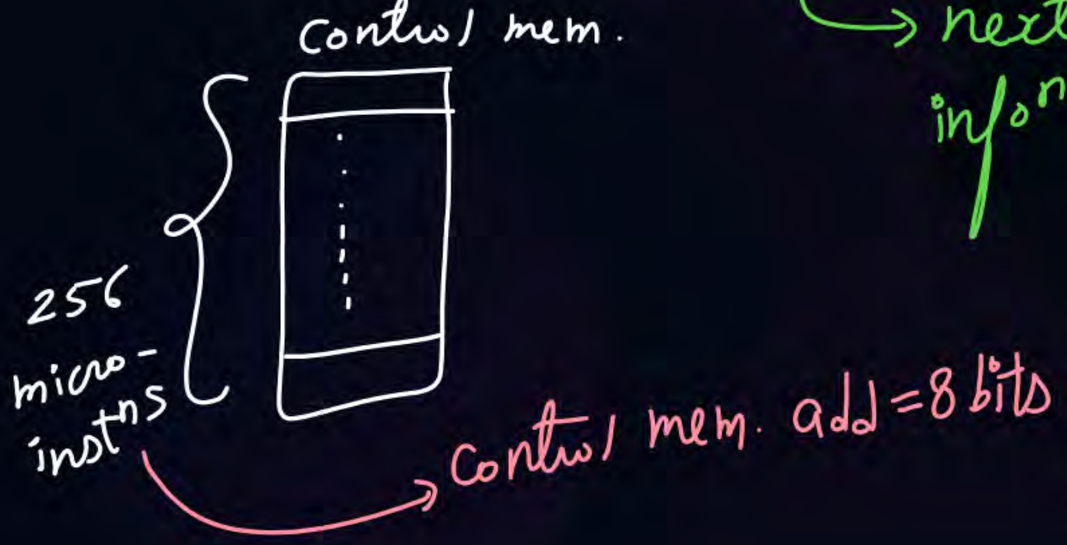
sent to sequencer to help it generating next add.

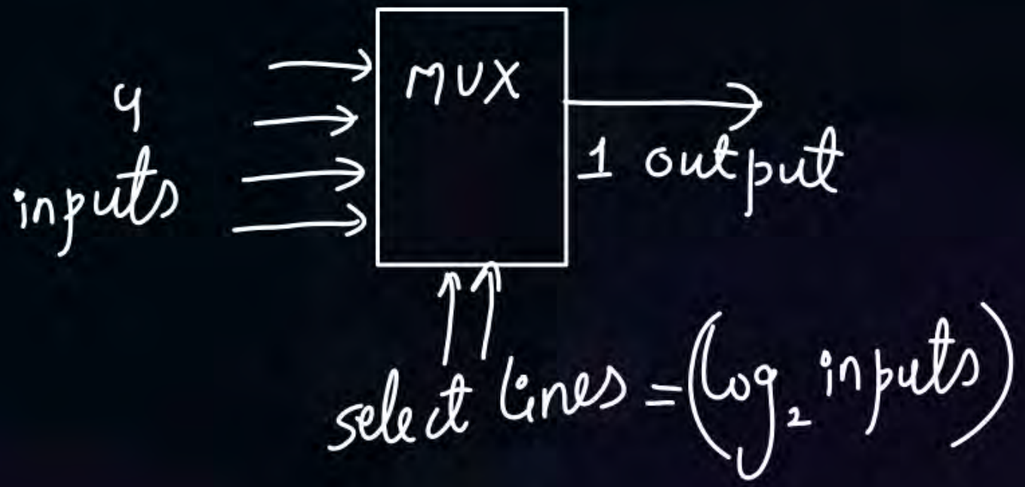
Topic : Control Word Sequencing



Topic : Control Word Sequencing

standard format of control unit micro-instⁿ



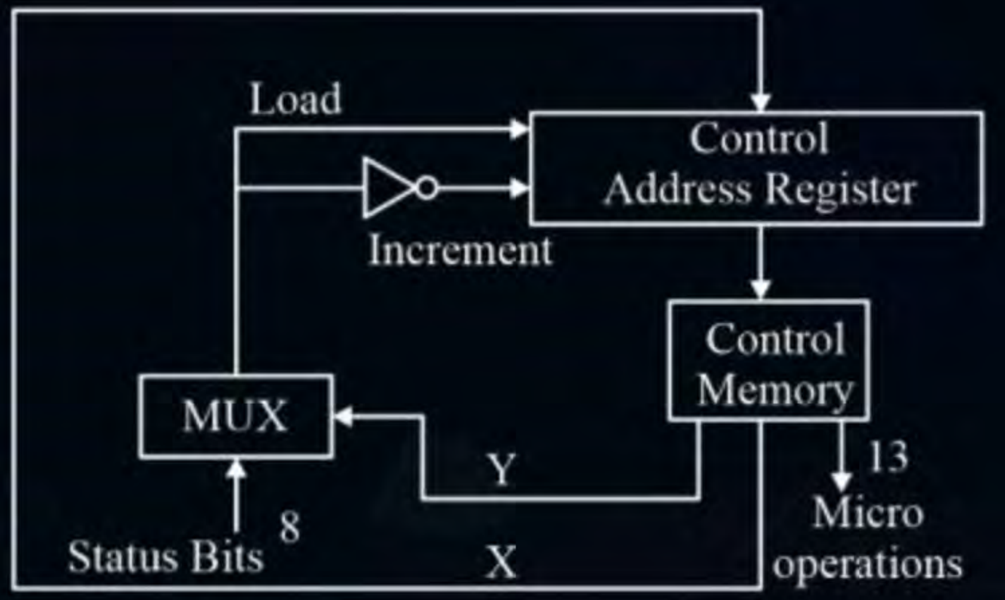


[MCQ]

#Q. The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the inputs of the MUX.

8 → mux select 3-bits

How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?



A ✓ 10, 3, 1024

B 8, 5, 256

C 5, 8, 2048

D 10, 3, 512

micro-instn

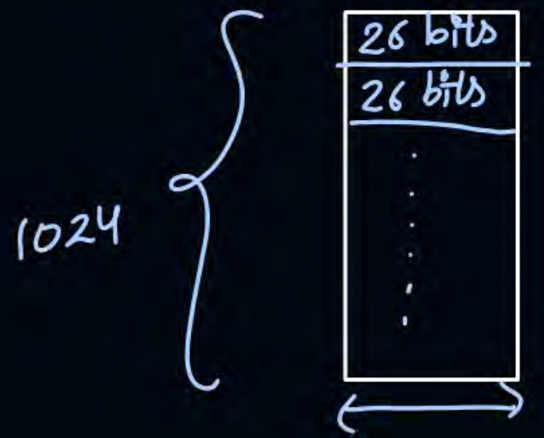
26-bits

Micro-opn (Signals)	Next add.	MUX select
13	x	y
	10	3

X ⇒ 10 bits ⇒ no. of words in mem. = 2^{10} = 1024

y ⇒ 3 bits

C. mem.



Size of control memory = 1024 * 26 bits

= 26 k bits

Topic : Types of Microprogrammed Control Unit

- Horizontal
- vertical

2 mins Summary

- **Topic** Hardwired Control Unit
- **Topic** Microprogrammed Control Unit
- **Topic** RISC vs CISC
- **Topic** Byte Ordering

Happy Learning

THANK - YOU