CS & IT ENGINEERING

DIGITAL LOGIC

Sequential Circuit

Lecture No. 07

By- CHANDAN SIR

01 ASYNCHRNOUS COUNTER

02 Synchronous Counter

03 Discussion

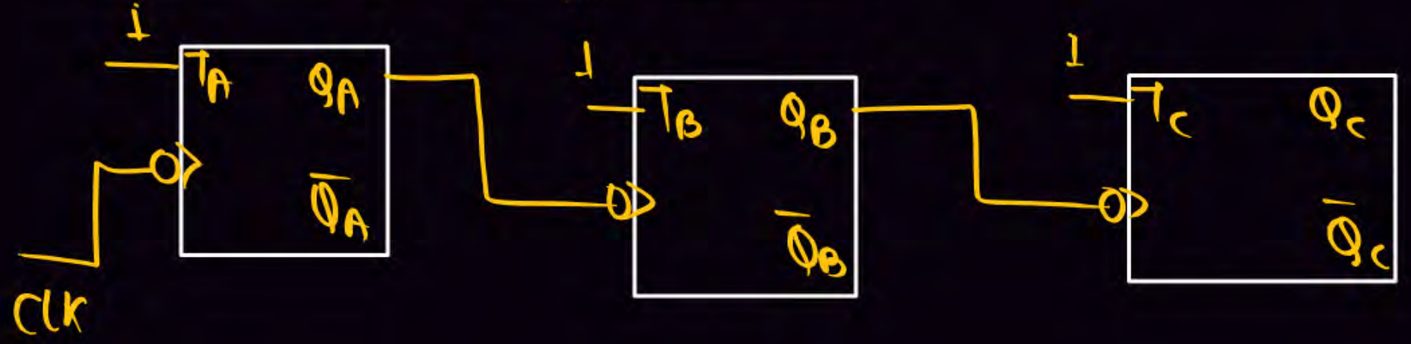
Sequential circuit

- Latches
  - Flip-Flop
    - SR, JK, D, T,
  - Designing
- Registers
  - SISO
  - SIPO
  - PISO
  - PIPO
- COUNTERS
  - Synchronous
  - Asynchronous

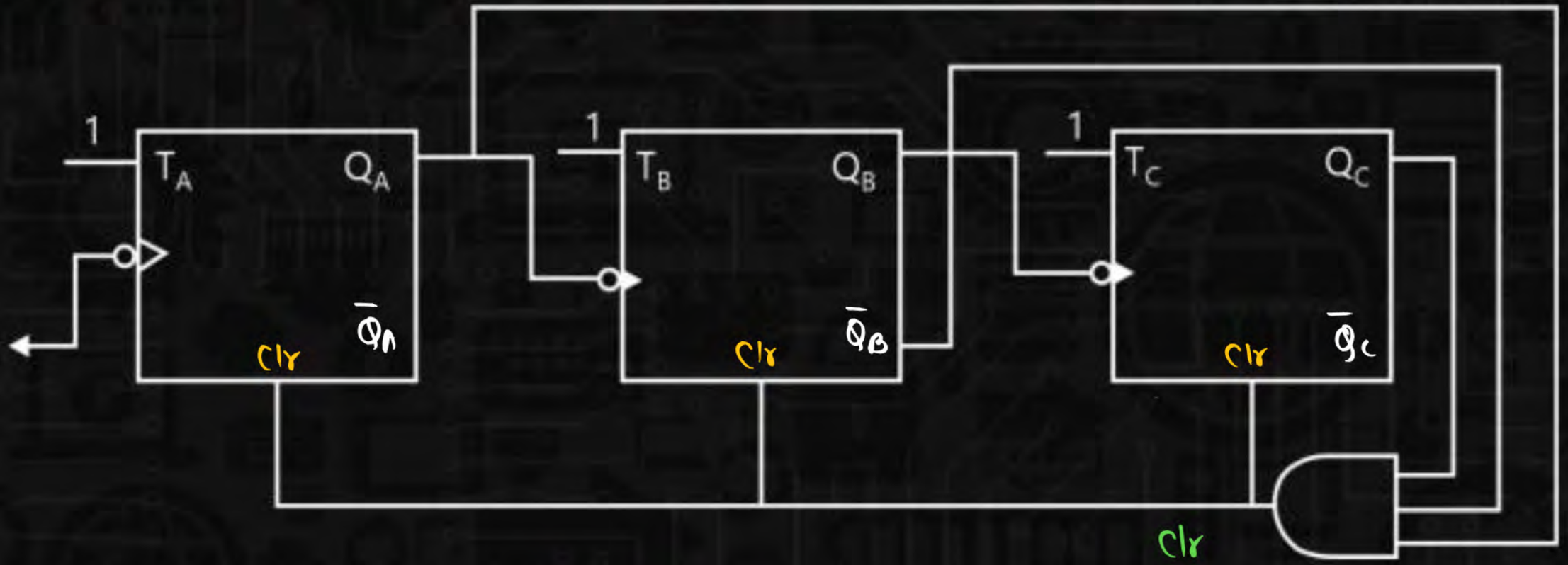
Asynchronous Counter

→ Ripple counter

MOD-8 UP Ripple counter

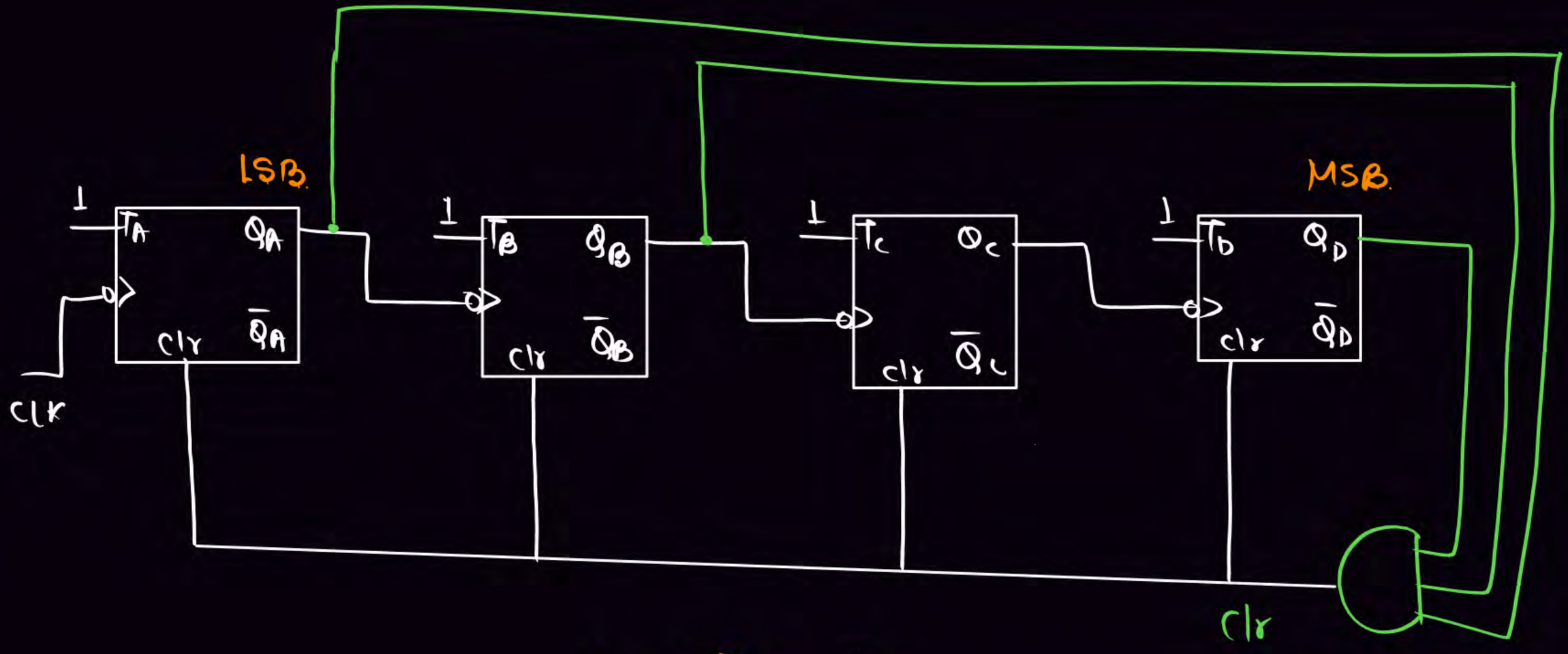


FEEDBACK REDUCES THE NUMBER OF STATES



$Clr = Q_C \cdot \bar{Q}_B \cdot Q_A$

$1\ 0\ 1 \Rightarrow (5)$

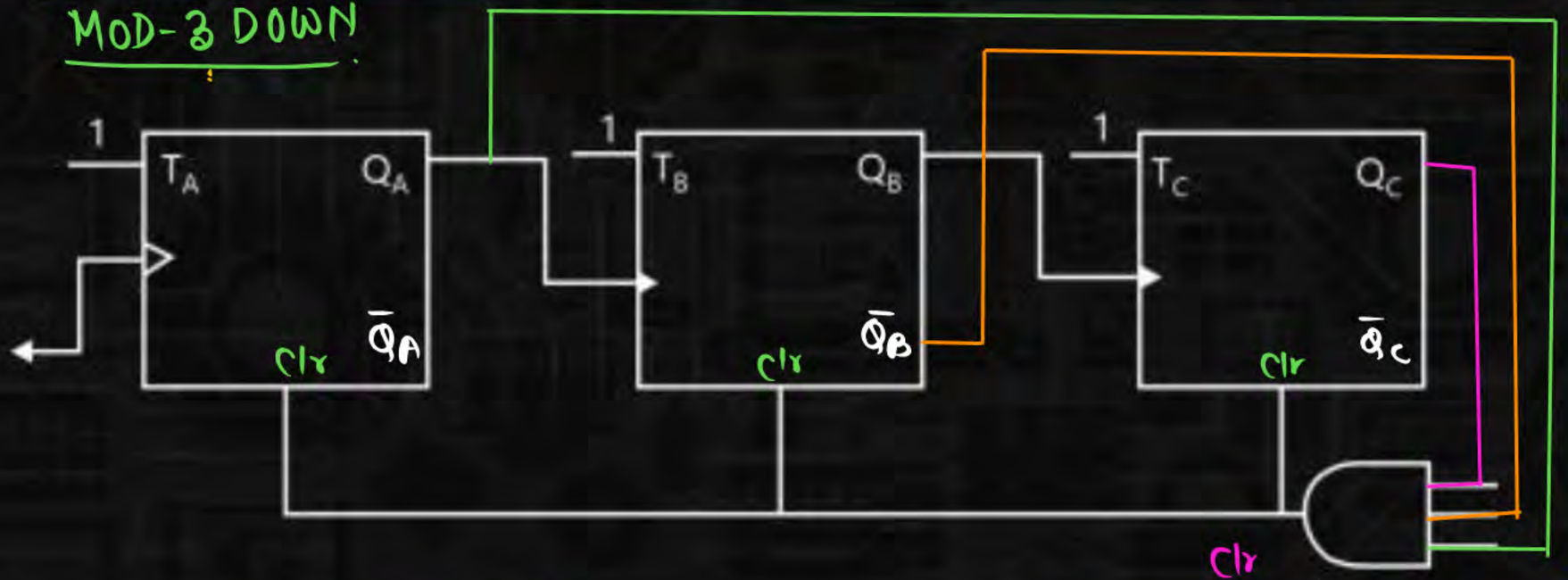


$Clr = Q_D \bar{Q}_C Q_B Q_A$

1 0 1 1 → MOD-11 UP Ripple counter

ASYNCHRONOUS COUNTER

MOD-3 DOWN



$Clr = Q_C \bar{Q}_B Q_A$

CLK	Q_C	Q_B	Q_A	Clr
0	0	0	0	0
1	1	1	1	0
2	1	1	0	0
3	~~1~~ 0	~~0~~ 0	~~1~~ 0	~~1~~ 0
4	1	1	1	0
5				
6				
7				
8				

000 → 111 → 110

8 − 5 = 3 ↓

Full-Up = DOWN

$Clr = Q_C \bar{Q}_B Q_A$

101

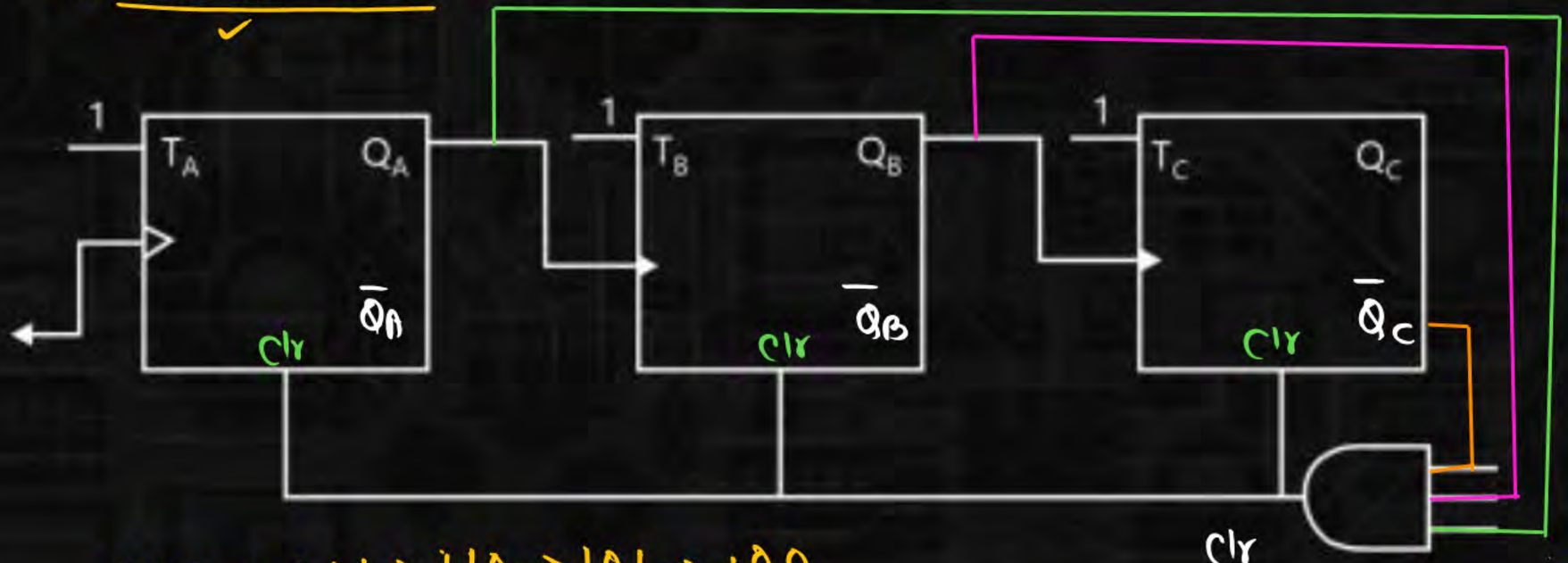
(5)

ASYNCHRONOUS COUNTER

FULL-UP = DOWN

8 − 3 = (5)

← MOD 5 DOWN →



$Clr = \bar{Q}_C Q_B Q_A$

CLK	Q_C	Q_B	Q_A	Clr
0	0	0	0	0
1	1	1	1	0
2	1	1	0	0
3	1	0	1	0
4	1	0	0	0
5	~~0~~ 0	~~1~~ 0	~~1~~	~~1~~ 0
6	1	1	1	0
7	1	1	0	0
8				

000 → 111 → 110 → 101 → 100

$Clr = \bar{Q}_C Q_B Q_A$

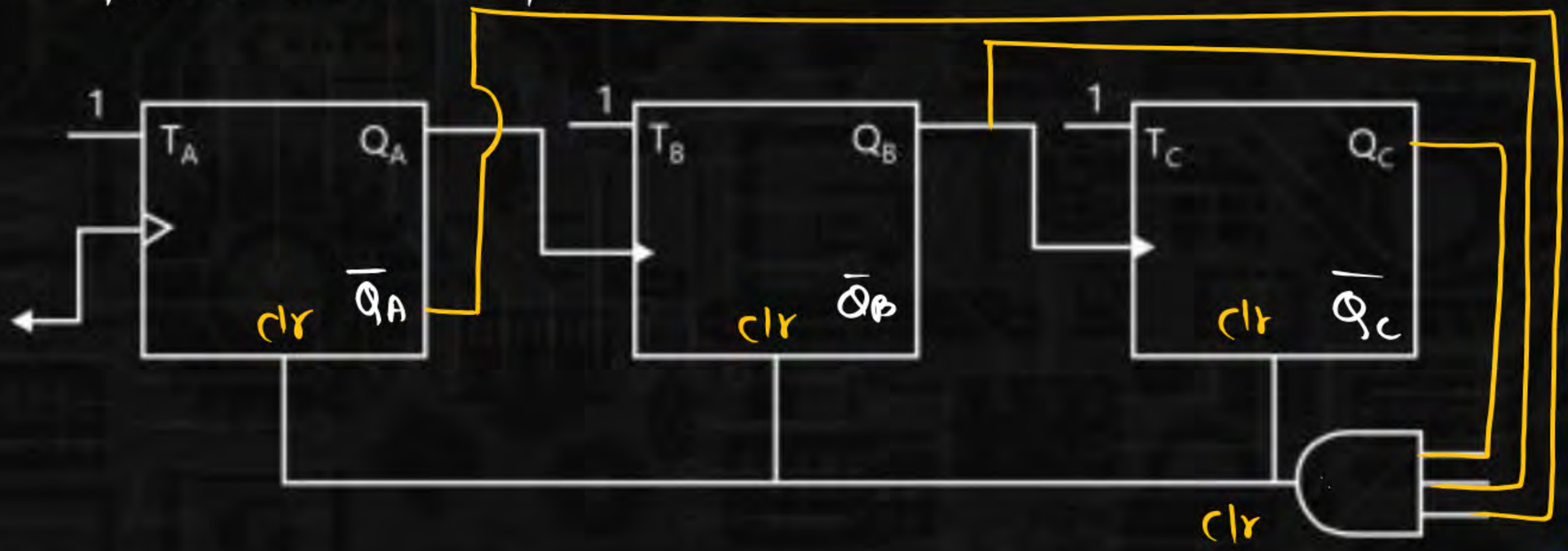
0 1 1

$Q_C Q_B Q_A$

0 1 1

ASYNCHRONOUS COUNTER

MOD-'2' DOWN Ripple counter.



CLK				
0				
1				
2				
3				
4				
5				
6				
7				
8				

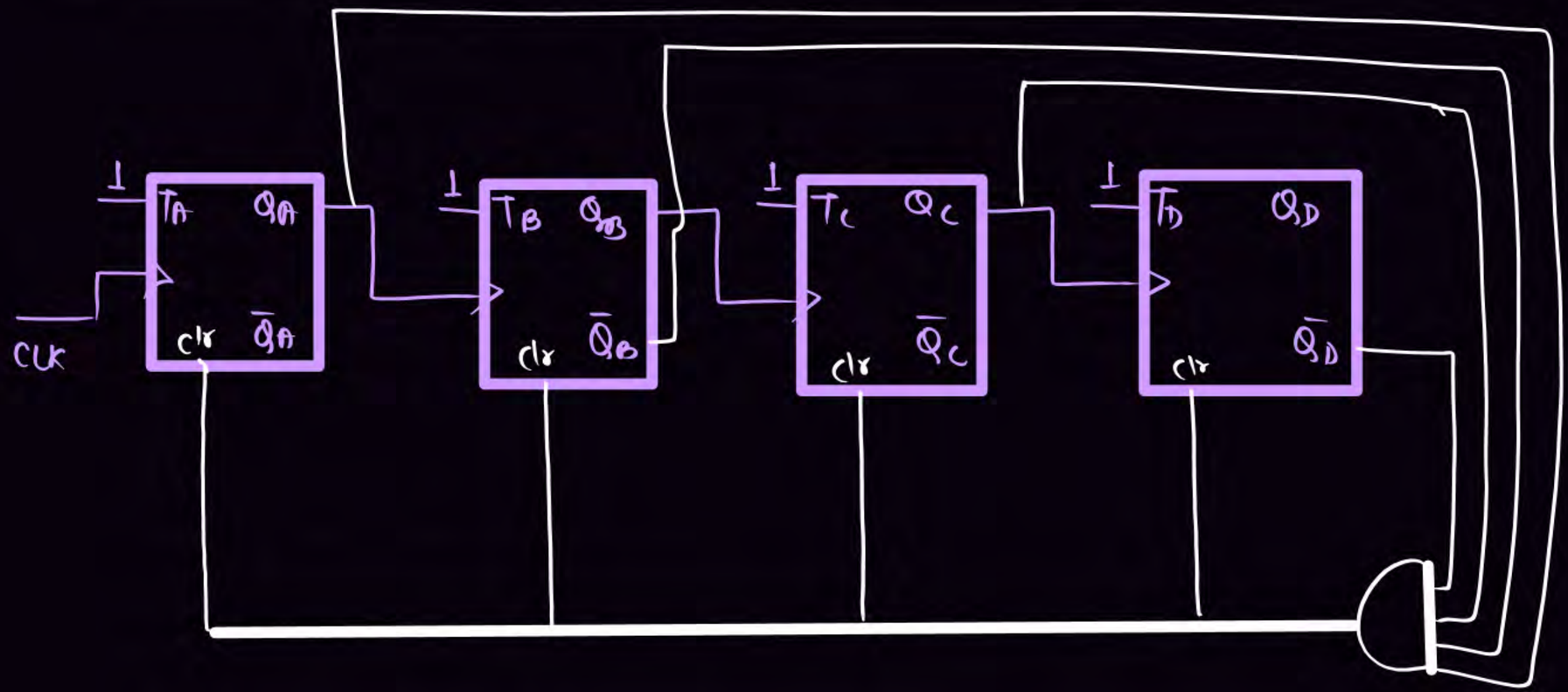
FULL − UP = DOWN

8 − 6 = (2)1

$clr = Q_C Q_B \bar{Q}_A$

1 1 0 = 6

MOD "11" DOWN RIPPLE COUNTER :→



FULL – UP = DOWN

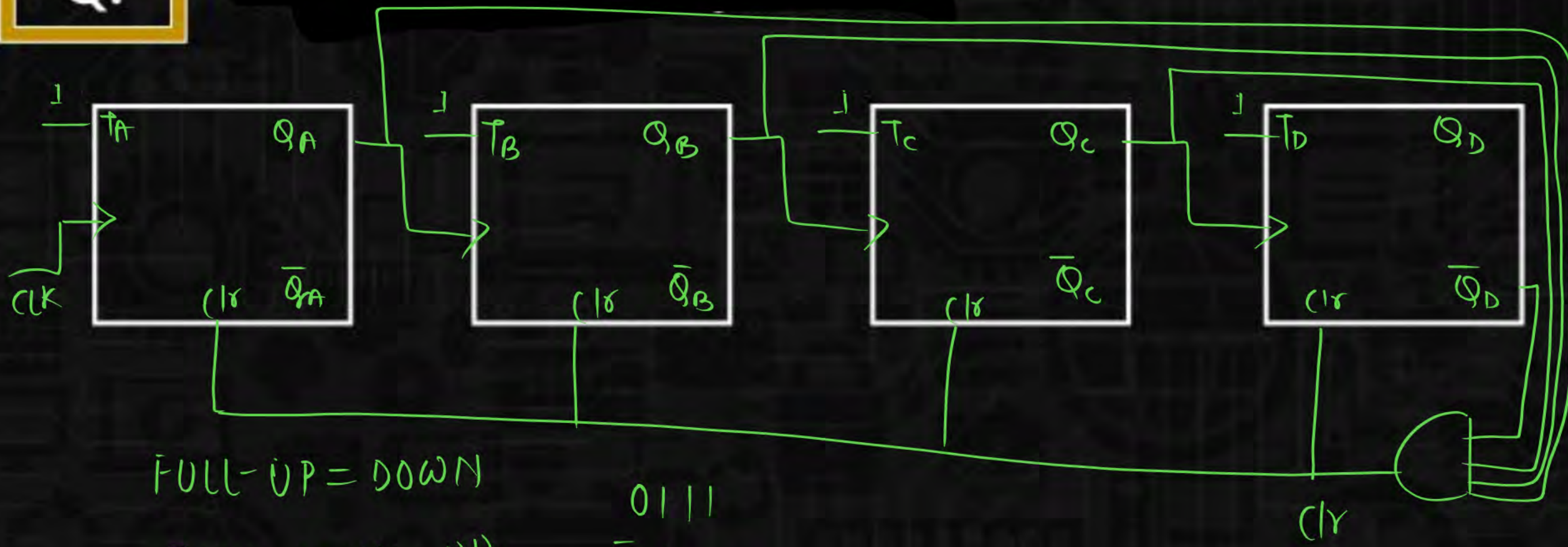
$16 - 5 = (11)$

$\bar{Q}_D Q_C \bar{Q}_B Q_A$

$0\ 1\ 0\ 1 = 5$

Q.

Design a MOD-9 DOWN Ripple counter?



FULL-UP = DOWN

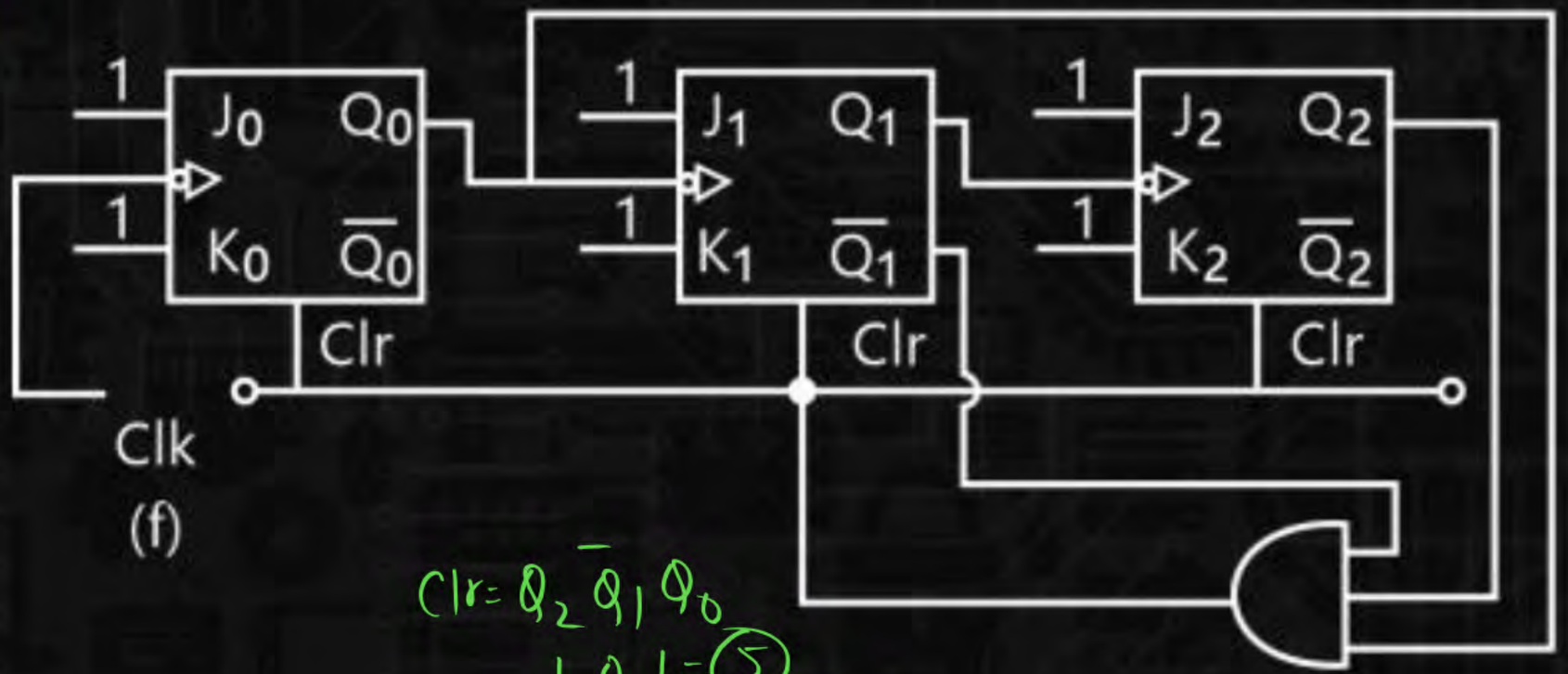
FULL-DOWN = UP

16 − 9 = 7

0111

$\bar{Q}_D Q_C Q_B Q_A$

Q. Which type of counter is shown below?



$Clr = Q_2 \overline{Q}_1 Q_0$

$1\ 0\ 1 = (5)$

A. mod 5 down counter

B. mod 5 up counter

C. mod 6 up counter

D. mod 6 down counter

Q.

Consider the following counter

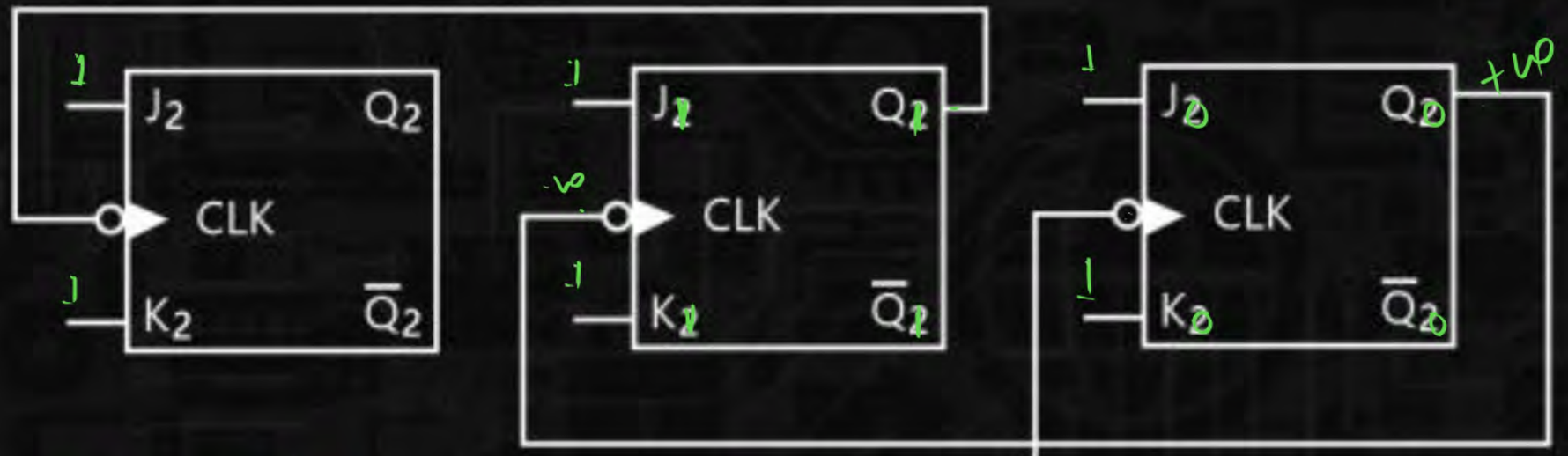
If counter starts at 000, what will be the count after 13 clock pulses?

A. 100

B. 101

C. 110

D. 111



UP → MOD '8'

8 + 5 = 13

101

8th 0 → 000
9th 1 → 001
10th 2 → 010
11th 3 → 011
12th 4 → 100
13th 5 → 101
14th 6 → 110
15th 7 → 111

Ans

8th 0 → 000
9th → 1 → 111
10th → 2 → 110
11th → 3 → 101
12th → 4 → 100
13th → 5 → 011
6 → 010
7 → 001

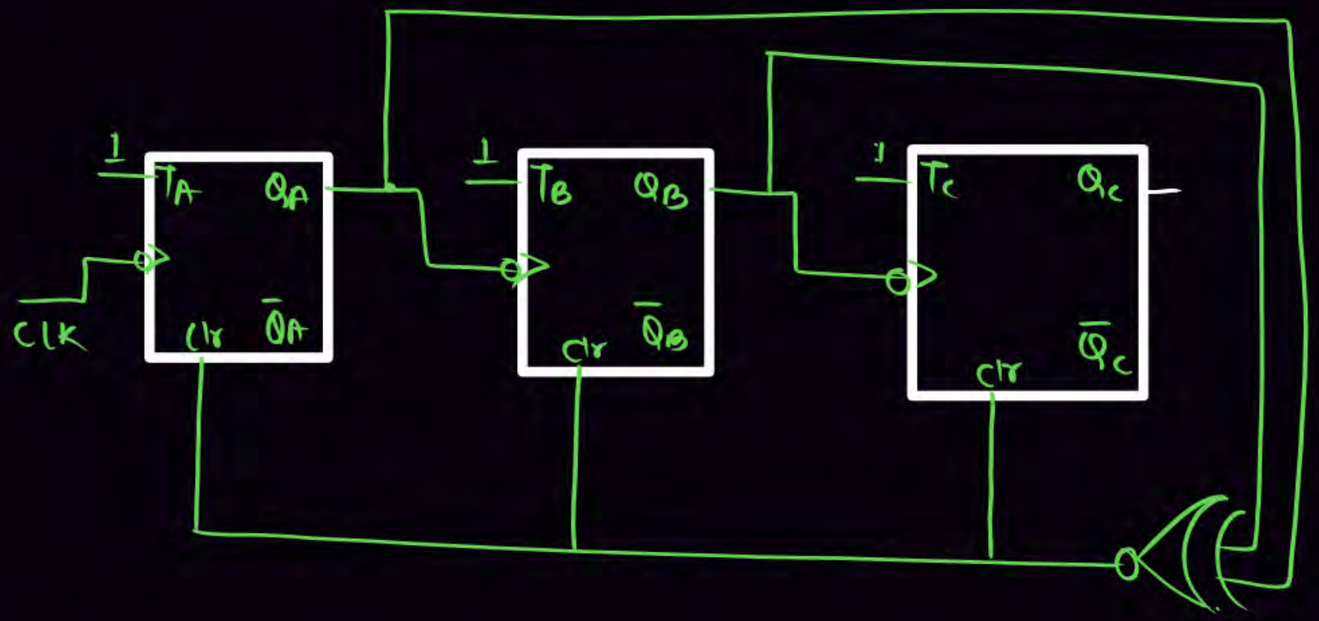
"n" bit Ripple counter

$$T_{clk} \geq n \cdot \tau_{pdff}$$

$$\frac{1}{T_{clk}} \leq \frac{1}{n \cdot \tau_{pdff}}$$

$$f_{clk} \leq \frac{1}{n \cdot \tau_{pdff}}$$

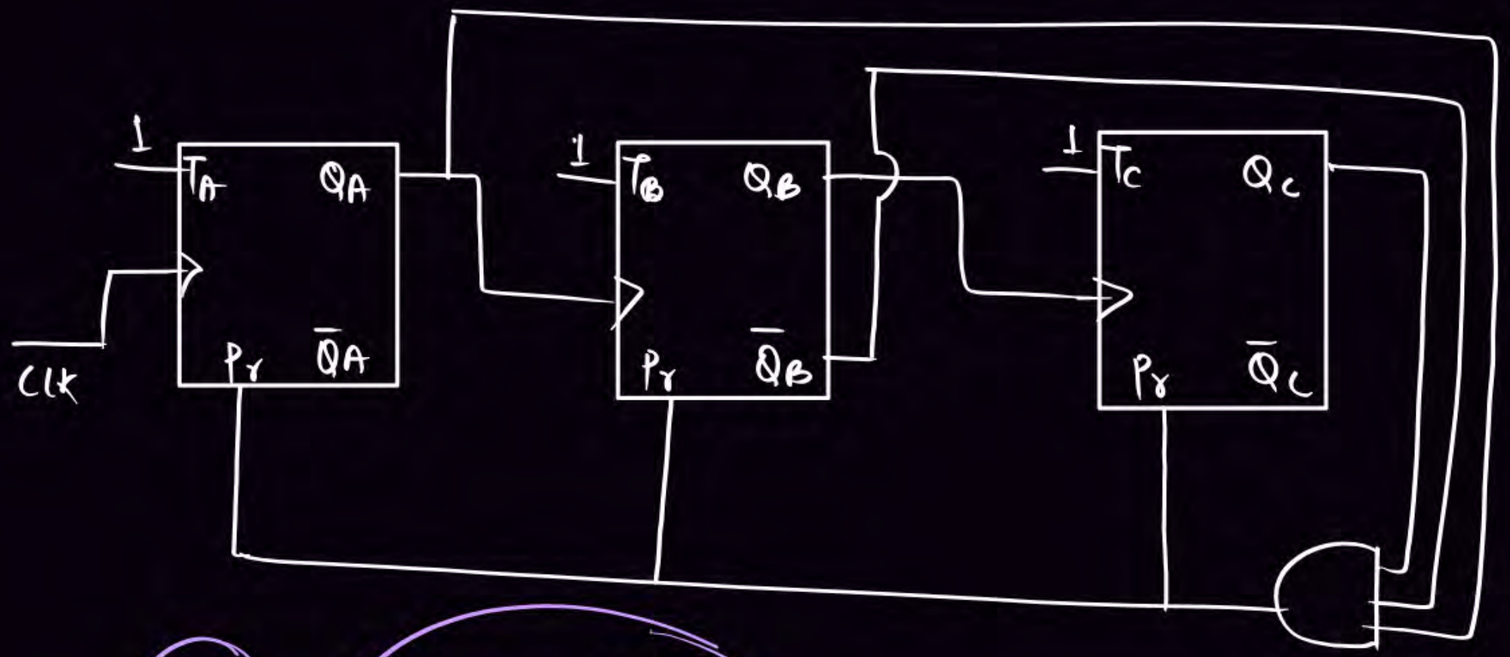
$$(f_{clk})_{max} = \frac{1}{n \cdot \tau_{pdff}}$$

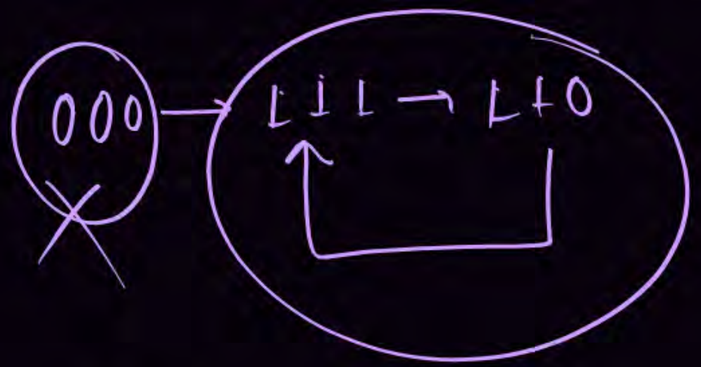


MOD - 3

$000 \rightarrow 001 \rightarrow 010$

CLK	Q_C	Q_B	Q_A	$Clr = Q_B \odot Q_A$
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	0	0	0	1
4				
5				





MOD-2

$P_r = Q_C \bar{Q}_B Q_A$

101

$P_r = Q_C \bar{Q}_B Q_A$

CLK	Q_C	Q_B	Q_A	P_r
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	1	1
6				

Synchronous counter :→

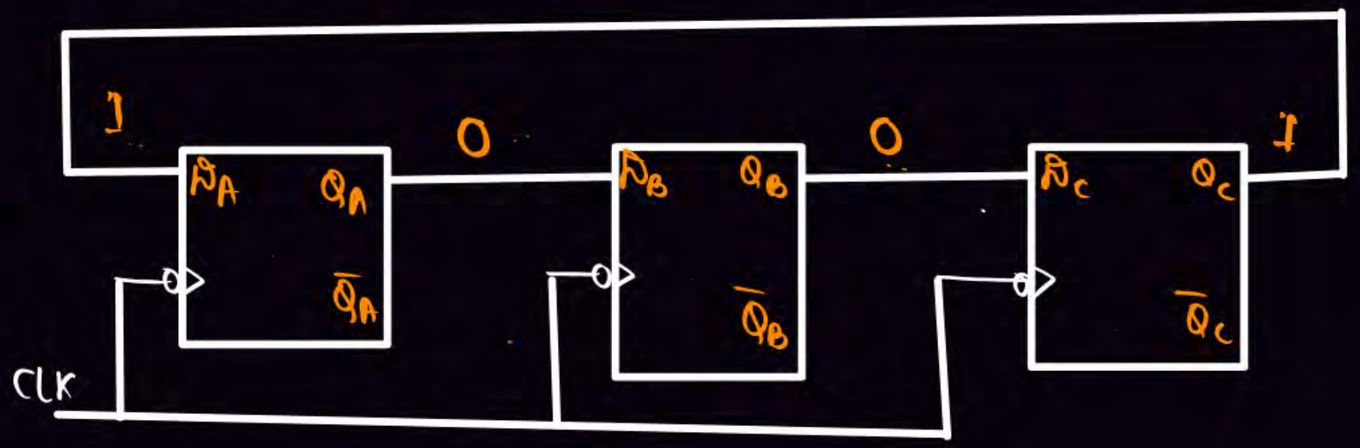
✓ 1) Ring counter

✓ 2) Johnson counter

① RING COUNTER :→

↳ It is a SISO shift Register in the form of Ring.

3 bit Ring counter



CLK	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	0	1	0
3	0	0	1
4	1	0	0
5	0	1	0
6	0	0	1

3 bit Ring counter

1 0 0
0 1 0
0 0 1

MOD-3

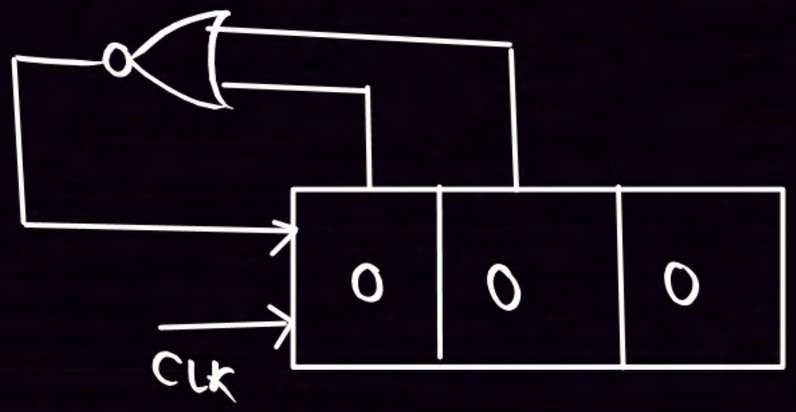
4 bit Ring counter

1 0 0 0
0 1 0 0
0 0 1 0
0 0 0 1

MOD-4

"N" bit Ring counter

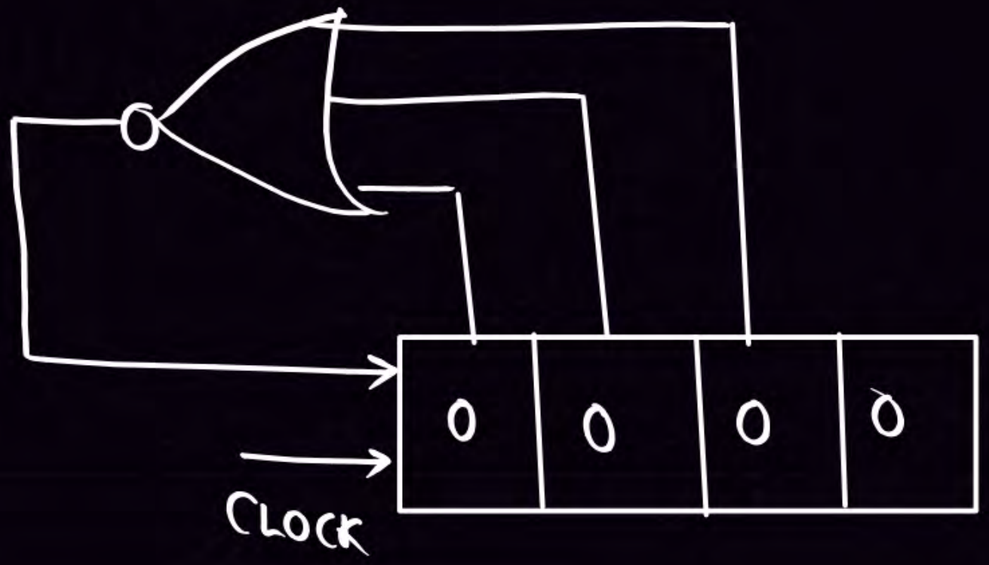
MOD = used states = N



1 0 0

0 1 0

0 0 1

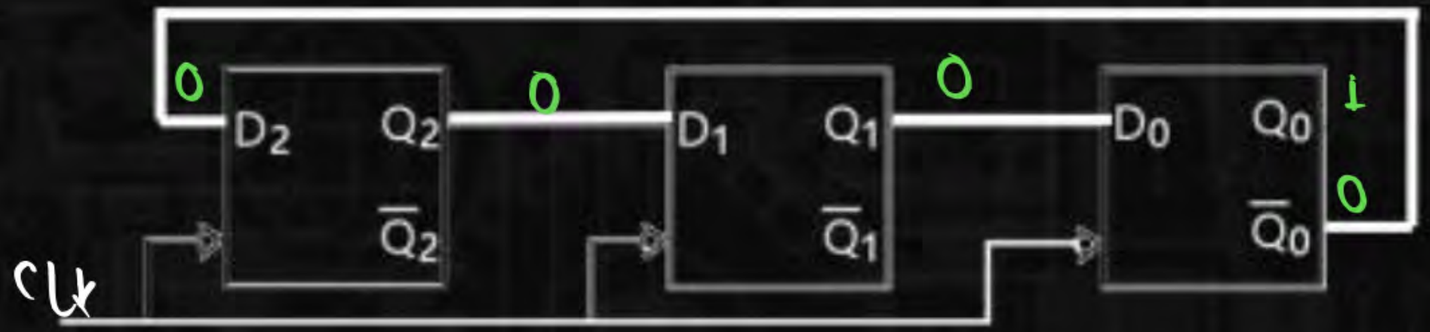


1 0 0 0
0 1 0 0
0 0 1 0
0 0 0 1

Self starting Ring counter

JOHNSON COUNTER

- Twisted Ring Counter
- Creeping Counter
- Mobies Counter
- Walking Counter



MOD - 6

Clock	Q_2	Q_1	Q_0
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1
6	0	0	0
7	1	0	0
8	1	1	0
9	1	1	1

3 bit Johnson counter

MOD-6

0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1

4 bit Johnson counter

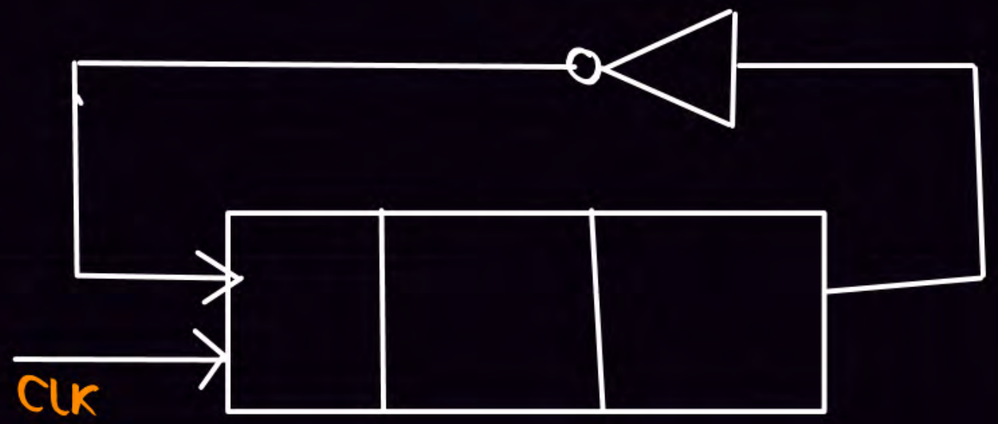
MOD-8

0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1

"N" bit Johnson counter

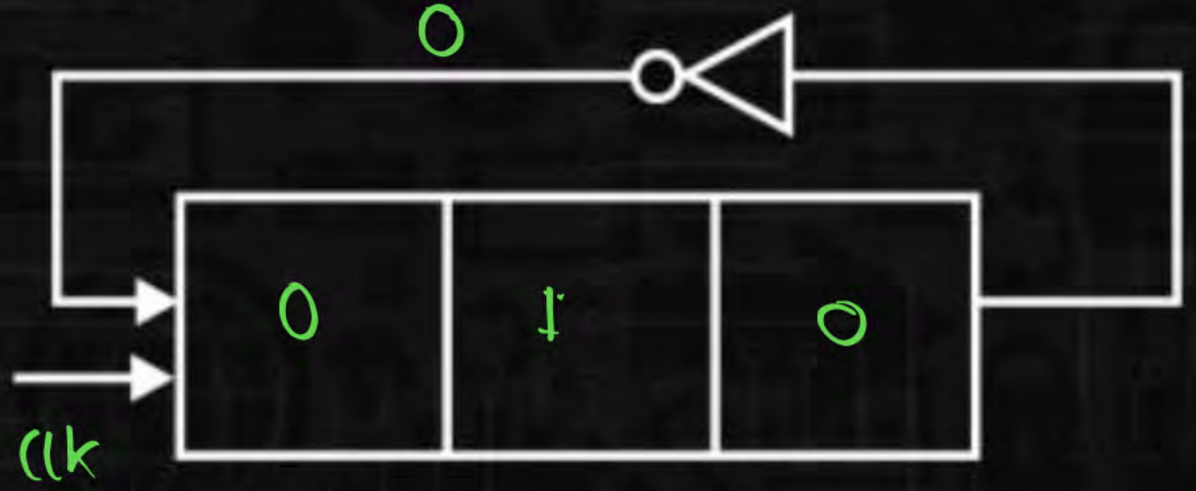
MOD = Used states = 2N

"Symbolic Representation."



LOCK OUT PROBLEM

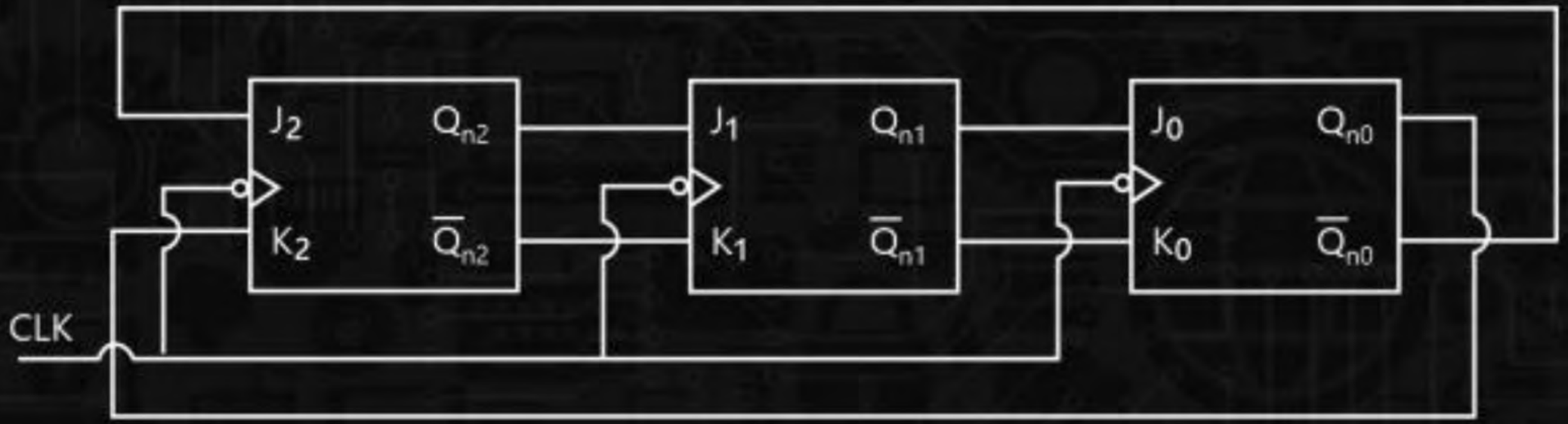
- Whenever Johnson Counter enters into its unused state then it will lock into its unused state is called lock out problem.



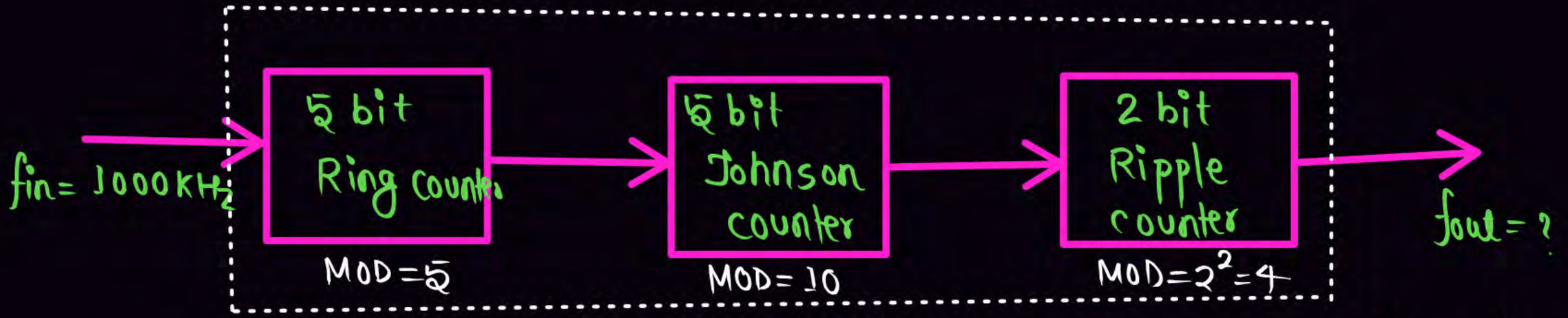
Clock	Q_2	Q_1	Q_0
0	0	1	0
1	1	0	1
2	0	1	0
3	1	0	1
4	0	1	0
5			
6			
7			
8			
9			

MOD-2

JOHNSON COUNTER BY USING JK FLIP FLOP



MOD [5x10x4] ⇒ MOD = 200



$$f_{out} = \frac{f_{in}}{MOD}$$

$$= \frac{1000\,kHz}{200}$$

$$= 5\,kHz$$

DESIGNING OF SYNCHRONOUS COUNTER

STEP 1. Write the Previous and Present State.

STEP 2. Write the Excitation Table of FF.

STEP 3. Write the Logical Expression.

STEP 4. Minimize the Logical expression.

STEP 5. Hardware Implementation.

Q. Design a Synchronous Counter by using D Flip Flop which count the sequence $0 \to 2 \to 1 \to 3 \to 0$

$\{00 \to 10 \to 01 \to 11 \to 00 \to \ldots\}$

Step 1 :→

Step 2.

Q_1	Q_0	Q_1^+	Q_0^+	D_1	D_0
0	0	1	0	1	0
0	1	1	1	1	1
1	0	0	1	0	1
1	1	0	0	0	0

Step 3.

$D_1 = \bar{Q}_1 \bar{Q}_0 + \bar{Q}_1 Q_0$

Step 4

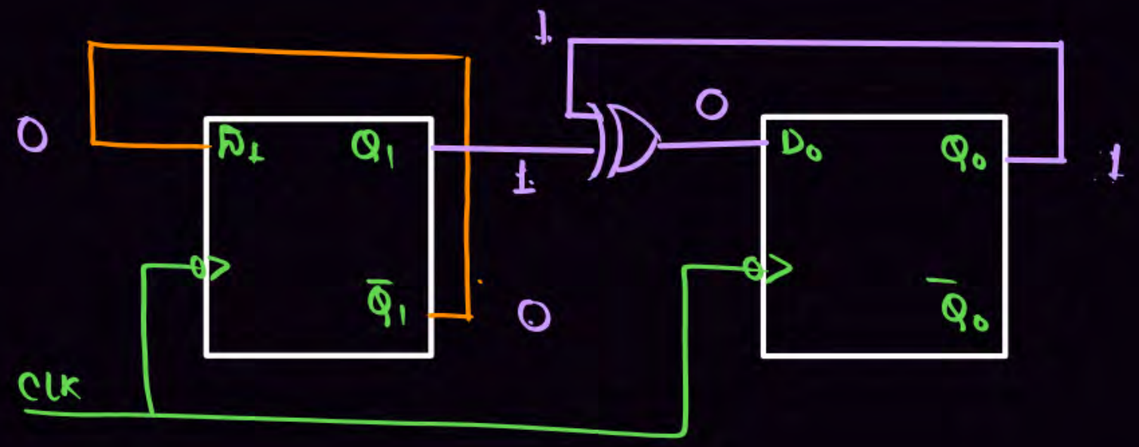
$D_1 = \bar{Q}_1 (\bar{Q}_0 + Q_0)$

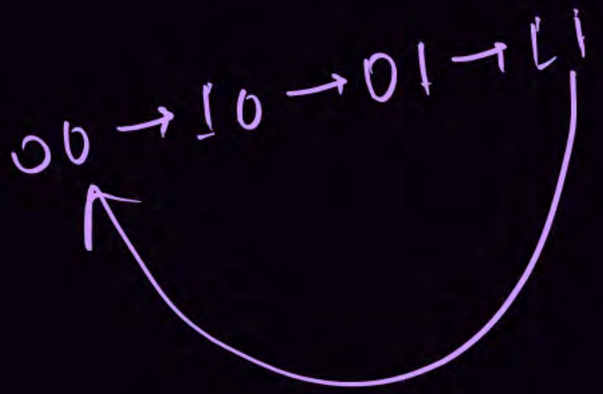
$D_1 = \bar{Q}_1$

$D_0 = \bar{Q}_1 Q_0 + Q_1 \bar{Q}_0$

$D_0 = Q_1 \oplus Q_0$

Step5.





Justification

CLK	Q_1	Q_0
0	0	0
1	1	0
2.	0	1
3.	1	1
4	0	0

MOD-4

Q. Design a Synchronous Counter by using T Flip Flop which count the sequence $0 \to 2 \to 3 \to 0$ $\{00 \to 10 \to 11 \to 00\}$

Step 1 & Step 2.

Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	1	0	1	0
0	1	x	x	x	x
1	0	1	1	0	1
1	1	0	0	1	1

Steps & Step 4.

T_1

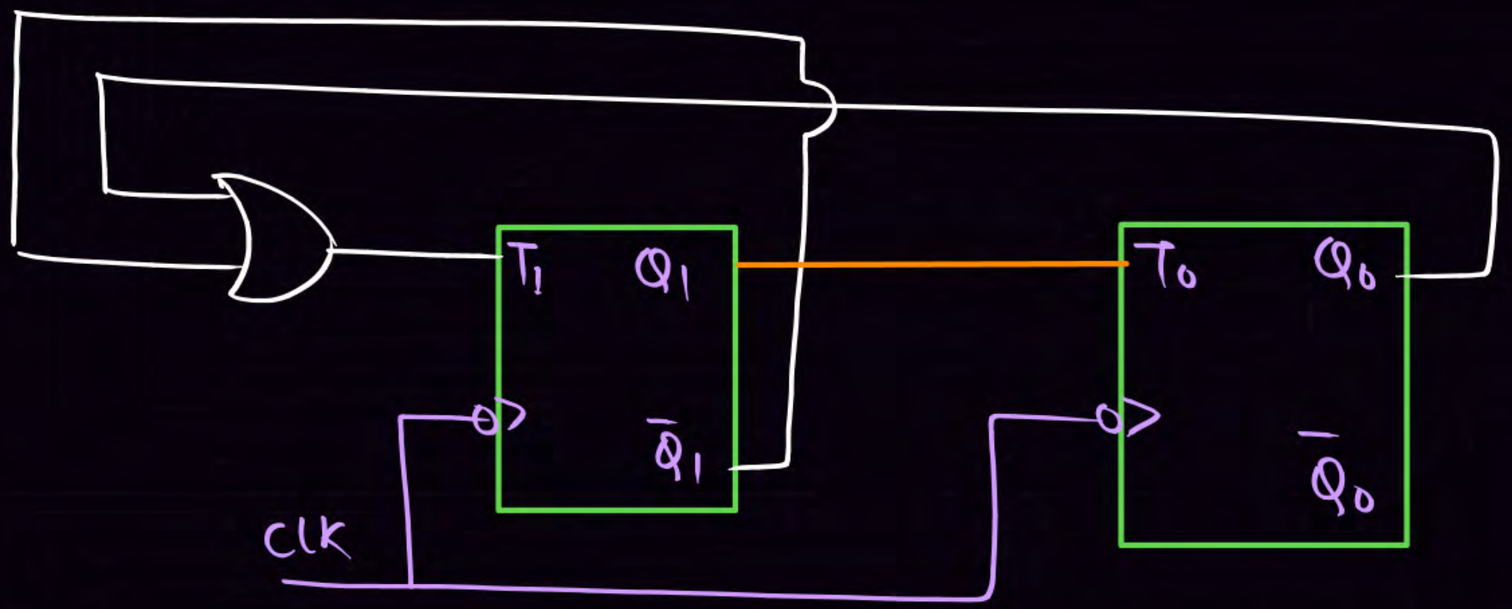
$T_1 = \bar{Q}_1 + Q_0$

Q_1 \ Q_0	0	1
0	1	X
1		1

T_0

$T_0 = Q_1$

Q_1 \ Q_0	0	1
0		X
1	1	1


T_1
Q_1
$\bar{Q}_1$
T_0
Q_0
$\bar{Q}_0$
CLK

Q.

Design a Synchronous Counter by using JK Flip Flop which count the sequence $0 \rightarrow 2 \rightarrow 3 \rightarrow 5 \rightarrow 1 \rightarrow 6 \rightarrow 0$

HW

Q.

HW

Design a Synchronous Counter by using T Flip Flop which count the sequence $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 0$


THANK YOU GW
SOLDIERS !