CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Pipeline Processing

Lecture No.- 01

By- Vishvadeep Gothi sir

Recap of Previous Lecture

Topic Disk Addressing

Topic Pipeline Processing

Topic Speed Up

Topics to be Covered

Topic Synchronous Pipeline

Topic Latency & Throughput

Topic Instruction Pipeline

	S1	S2	S3	S4
1	I1			
2	I2	I1		
3	I3	I2	I1	
4	I4	I3	I2	I1
5	I5	I4	I3	I2
				⋮

In ideal condit^n

ignoring $(k-1)$ means

ignoring $(k-1)$ cycles to fill the pipe.

$\Downarrow$

each output takes 1 cycle.

n outputs $\Rightarrow$ n cycles

$= n * t_p$ time

Topic : General Consideration About Pipeline

k segments

cycle time of pipeline $= t_p$

no. of inputs $= n$

pipeline time $= (k+n-1)\,t_p$

$t_n = 1$ operat^n time in non-pipeline

non-pipeline time $= n * t_n$

$$S = \frac{n * t_n}{(k+n-1)\,t_p}$$

$$S_{\text{ideal or max}} = \frac{t_n}{t_p}$$

special case:-

if $t_n = k * t_p$

$S_{max} = k$

If ideal or max speed up is asked $\Rightarrow$ $S_{max} = \dfrac{t_n}{t_p}$

or

If value of n is not given

[NAT]

#Q. A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns.

1. Determine the speedup ratio of the pipeline for 100 tasks.
2. What is the maximum speedup that can be achieved?

$t_n = 50\,ns$

$k = 6$

$t_p = 10\,ns$

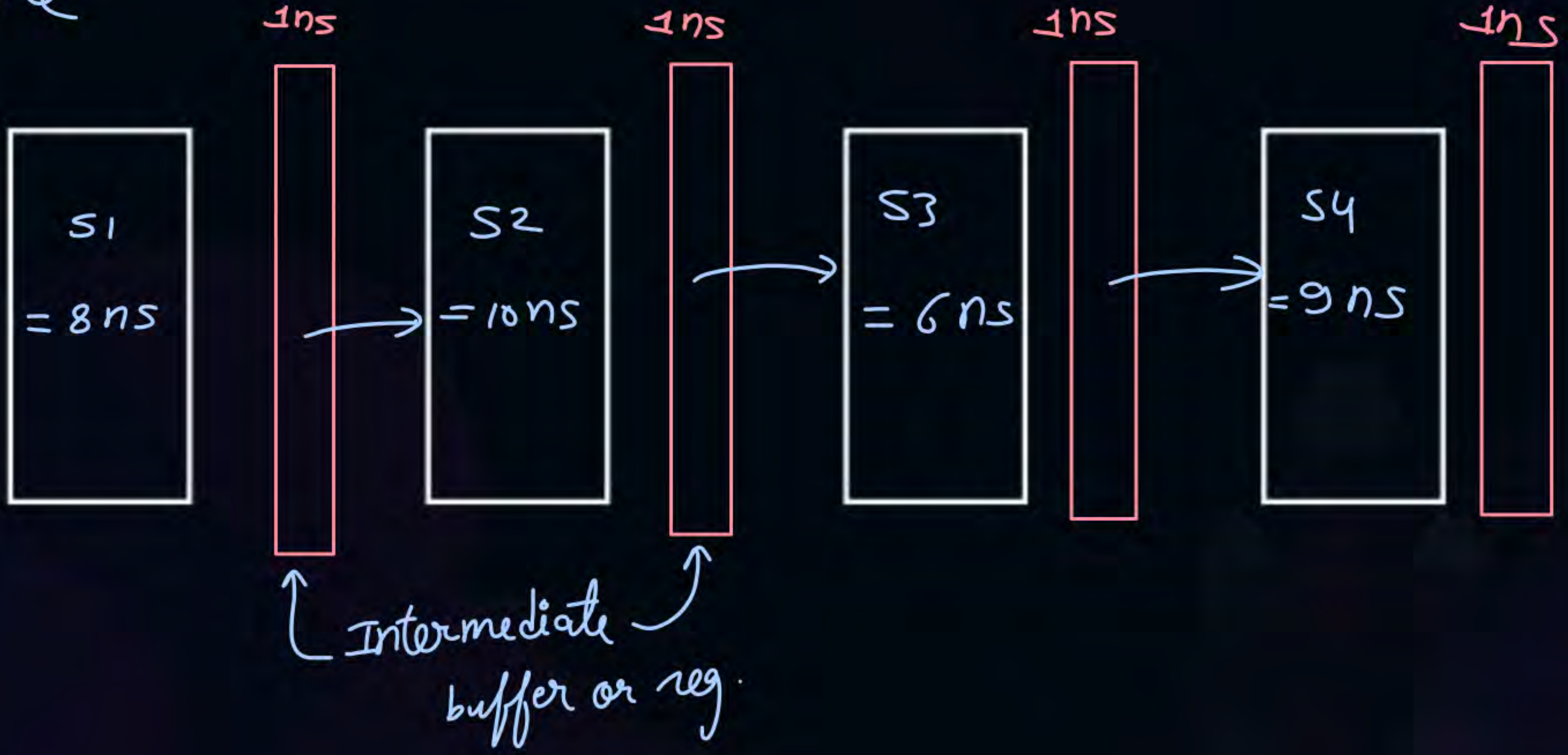
$n = 100$

1. $S = \dfrac{100 * 50\,ns}{(6 + 100 - 1)\,10\,ns} = 4.76$

2. $S_{max} = \dfrac{50}{10} = 5$

Topic : Synchronous Pipeline

Assume



Topic : Cycle Time in Synchronous Pipeline

t_p = max of all segment delays

= max of all seg. delays + Reg./buffer delay = max(8, 10, 6, 9) + 1

= 11 ns

---

t_n = sum of all segment delays

Notes :- Buffer or Reg.^s are not used in non-pipeline system.

[NAT]

#Q. Consider 6 segment pipeline with segment delay of segments as 20ns, 26ns, 21ns, 21ns, 24ns and 28ns respectively. Calculate processing time of pipeline for 1000 tasks?

$k = 6$

$t_p = max(20, 26, 21, 21, 24, 28) = 28$ ns

$n = 1000$

$t_n =$

pipeline time

$= (k + n - 1)\, t_p$

$= (6 + 1000 - 1)\, 28$

$= 28140$ ns

[NAT]

#Q. The time delay of the four segments in pipeline are as shown follows:

$t_1 = 50$ ns, $t_2 = 30$ ns, $t_3 = 95$ ns, and $t_4 = 45$ ns.

The interface registers delay time $t_r = 5$ ns.

How long would it take to process 100 tasks in the pipeline?

$k = 4$

$n = 100$

$t_p = max(50, 30, 95, 45) + 5 = 100 ns$

pipeline time $= (4 + 100 - 1)\ 100$

$= 10300$ ns

[NAT]

#Q. How can we reduce the total time about the one-half of the time calculated in above question?

Try to split segment 3 into 2 segments with delays 50, 45 ns

new pipeline:-

$t_1 = 50ns$, $t_2 = 30ns$, $t_{31} = 50 ns$, $t_{32} = 45 ns$, $t_4 = 45 ns$

$n = 100$

$k = 5$

$t_p = max(50, 30, 50, 45, 45) + 5$

$= 55 ns$

pipeline time $= (5 + 100 - 1) 55$

$= 5720 ns$

for a better pipeline design $\Rightarrow$ seg. delays must be almost equal

---

$$\text{cycle time} = \frac{1}{\text{clock rate}}$$

[NAT]

#Q. Consider a non-pipelined processor with a clock rate of 5 gigahertz and average cycles per instruction of 5. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 4 gigahertz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is ________.

$t_n = 5 * \frac{1}{5GHz} = 1 ns$

$t_p = \frac{1}{4GHz} = 0.25 ns$

$S = \frac{t_n}{t_p} = \frac{1}{0.25} = 4$

Topic : Latency and Throughput

After how much time, next input given.

no. of operations or tasks performed per unit time.

Latency of non-pipeline system $= t_n$

Latency of pipeline system $= t_p$

pipeline :-

$$\text{throughput} = \frac{n}{(k+n-1)\,t_p}$$

$$\text{throughput in ideal conditions} = \frac{1}{t_p}$$

non-pipeline :-

$$\text{throughput} = \frac{1}{t_n}$$

[NAT]

#Q. Consider 6 segment pipeline with segment delay of segments as 120ns, 126ns, 121ns, 110ns, 118ns and 120ns respectively. The intermediate buffer delay is 5ns.

Consider that the system is used for performing 100 tasks.

1. What is the latency of non-pipeline system $= t_n = 120 + 126 + 121 + 110 + 118 + 120 = 715\ ns$
2. What is the latency of pipeline system $= t_p = max(120, 126, 121, 110, 118, 120) + 5 = 131\ ns$
3. What is the throughput of pipeline system $= \frac{100}{(6+100-1)131} = 0.00727$ per ns $= 7270000$ per sec
4. What is the throughput of pipeline system in ideal case

$= \frac{1}{131}$

$= 0.00763359$ per ns

$= 7633590$ per sec

[NAT]

Ans = 33.33 %

#Q. The stage delays in a 4-stage pipeline are 60ns, 50ns, 55ns and 80ns. The last stage (with delay 80ns) is replaced with a functionally equivalent design involving two stages with respective delays 60ns and 35ns. The throughput increase of the pipeline is ______ percent?

<u>old</u>

$k = 4$

$60, 50, 55, 80 \Rightarrow t_p = 80$

n is not given

$\text{throughput} = \frac{1}{80}$

<u>new</u>

$k = 5$

$60, 50, 55, 60, 35 \Rightarrow t_p = 60$

$\text{throughput} = \frac{1}{60}$

Throughput increase

$$= \frac{\frac{1}{60} - \frac{1}{80}}{\frac{1}{80}} * 100\%$$

$$= \left(\frac{4}{3} - 1\right) * 100\%$$

$$= 33.33\%$$

[NAT]

#Q. Consider a 6-stage pipeline with delays 2, 4, 3, 5, 3 and 4 ns. This pipeline is upgraded to a new 8-segment pipeline in which each segment delay is 2 ns.

1. How much time is saved using new pipeline over old one for 100 inputs?
2. What is the speed up of new pipeline as compared to old pipeline for 100 inputs?
3. speed up of new pipeline as compared to old in ideal condition

---

old

$k = 6$

$t_p = \max(2,4,3,5,3,4)$

$= 5ns$

new

$k = 8$

$t_p = \max(2,2,2,2,2,2,2,2)$

$= 2ns$

$n = 100$

pipeline time in old $= (6 + 100 - 1)5$

$= 525\ ns$

$n = 100$

pipeline time in new $= (8 + 100 - 1)2$

$= 214\ ns$

1. Time saved by new pipeline $= 525 - 214 = 311\ ns$

2. speed up of new pipeline $= \dfrac{525}{214} = 2.45$

3. $S_{ideal} = \dfrac{t_{p_{old}}}{t_{p_{new}}} = \dfrac{5}{2} = 2.5$

If pipeline processing is implemented on Instruction Cycle

Topic : Instruction Pipeline

Assume 5-stage $inst^n$ pipeline

IF: Instruction Fetch
ID: Instruction Decode & Address Calculation
OF: Operand Fetch
EX: Execution
WB: Write Back

Topic : Instruction Pipeline

Clock Cycles

Instructions	1	2	3	4	5	6	7	8	9	10	11	12	13	14
I1	IF	ID	OF	EX	WB									
I2		IF	ID	OF	EX									
I3			IF	ID	OF									
I4				IF	ID									
I5					IF									
I6														
I7														
I8														
I9														

2 mins Summary

Topic Synchronous Pipeline

Topic Latency & Throughput

Topic Instruction Pipeline

Happy Learning

THANK - YOU