CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

CPU & Control Unit

Lecture No.- 01

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Recap of Previous Lecture

Topic Addressing Modes

Topic PC Relative Mode

Topic Questions on Addressing Modes

Topics to be Covered

- Topic: CPU
- Topic: MIPS
- Topic: Data Path

[MCQ]

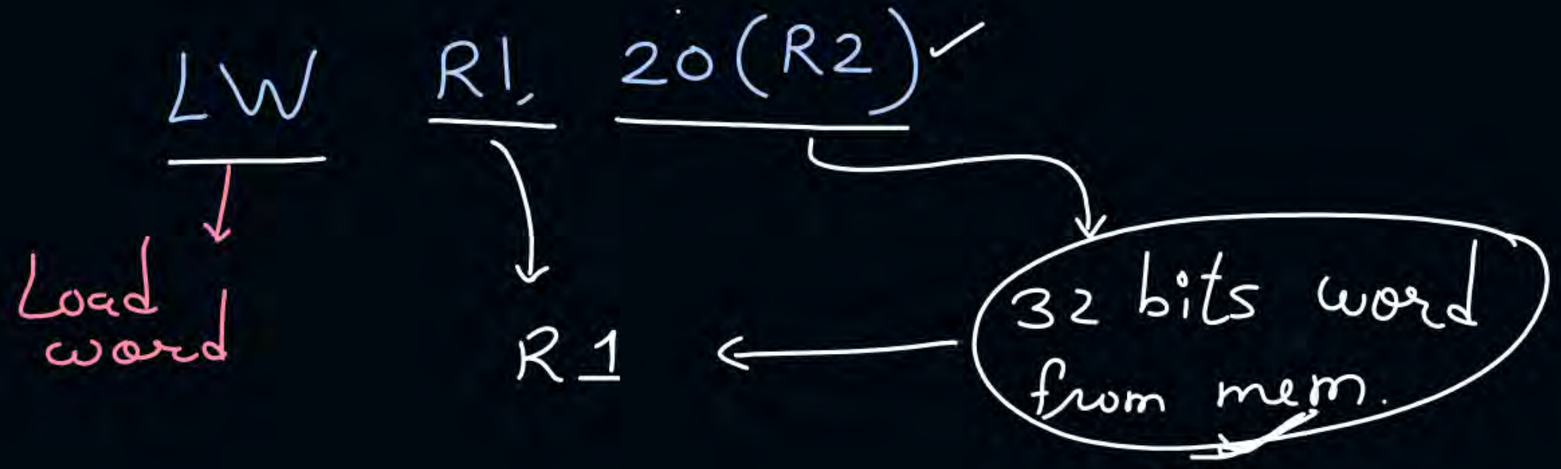
#Q. Consider a hypothetical processor with an instruction of type LW R1, 20(R2); which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for operand in memory?

A ✗ Immediate Addressing

B ✓ Register Addressing

C ✓ Register indirect and scaled addressing

D ✓ Base indexed addressing (Indexed mode)



$R1 \leftarrow M[20 + R2]$

effective add. = 20 + R2 (Reg.)

20: given in instⁿ

[NAT]

Ans = 4

#Q. Consider a three-word machine instruction

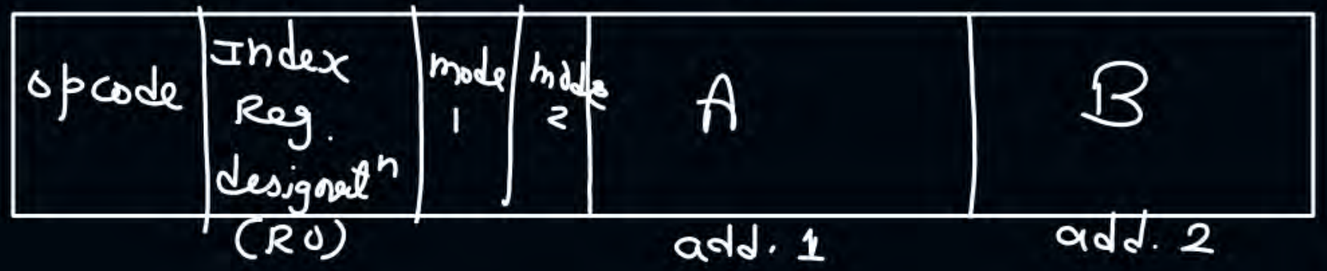
ADD A[R0], @B

The first operand (destination) "A[R0]" uses indexed addressing mode with R0 as the index register. The second operand (Source) "@B" uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).

The number of memory cycles needed during the execution cycle of the instruction is_____.

↳ no. of times memory accessed

3 word inst^n



ADD A[R0], @B

A[R0]
- source & destination
- ⇓
- indexed mode
- A ⇒ base add.
- R0 ⇒ Index Reg.

@B
- only source
- ⇓
- Indirect mode
- D ⇒ add. of e.A.

1. Inst^n fetch ⇒ not in execut^n cycle
2. Inst^n decode ⇒ 0
3. Effective add. calculat^n ⇒
   - operand 1 ⇒ 0
   - operand 2 ⇒ 1

   Total ⇒ 4
4. operand fetch ⇒
   - operand 1 ⇒ 1
   - operand 2 ⇒ 1
5. Execution ⇒ 0
6. Write back ⇒ 1

#Q No. of mem. cycles for inst^{n} cycle in prev. Quest^{n} ?

Ans:-

Soln:- for 3 word inst^{n} fetch ⇒ 3

execution cycle ⇒ 4

Total ⇒ 7

If one mem. cycle is 200 ns then total mem. access time _____ ns ?

Ans:- 7 * 200 ns

= 1400 ns

[NAT]

H.W.

#Q. Consider a 6-words instruction, which is of the following type:

Opcode	Mode1	Mode2	Address1	Address2

The first operand (destination) uses register indirect mode and second operand uses indirect mode. Assume each operand is of size 2 words, each address is of 2 words and main memory takes 50ns for 1 byte access. Further assume that the opcode denotes addition operation which copies result of addition of 2 operands. One word size is 4 bytes. Total time required in:

1. Fetch cycle of instruction
2. Execution cycle of instruction
3. Instruction cycle of instruction

Topic : CPU

1. CPU Cycle ⇒ Time in which CPU can perform smallest micro-operations

2. CPU Clock rate (frequency) $= \frac{1}{\text{CPU cycle time}}$

3. CPI (cycles Per Instruction) :- no. of CPU cycles needed to execute an instruction.

4. Execution Time :-

1 inst^n execution time = CPI$_{avg}$ * CPU cycle time

$= \frac{\text{CPI}_{avg}}{\text{clock rate}}$

$$n \text{ no. of inst}^n \text{ execution time} = n * CPI_{avg} * \text{CPU cycle time}$$

$$= \frac{n * CPI_{avg}}{\text{clock rate}}$$

$K = 10^3$	$milli = 10^{-3}$
$M = 10^6$	$micro = 10^{-6}$
$G = 10^9$	$nano = 10^{-9}$

#a clock rate = 2 GHz

CPU cycle time = $\frac{0.5}{}$ ns

Soln cycle time = $\frac{1}{2\,GHz} = \frac{1 * sec}{2 * 10^9} = \frac{10^{-9}\,sec}{2}$

$= 0.5\,ns = 0.0005\,\mu sec$

Topic : MIPS

(Million inst^ns per second)

in t time no. of inst^ns executed by CPU = n

in 1 —— 11 —————— $= \frac{n}{t}$

$= \frac{\cancel{n} * \text{clock rate}}{\cancel{n} * CPI_{avg}}$

$= \frac{\text{clock rate}}{CPI}$

$$MIPS = \frac{\text{clock rate}}{CPI * 10^6}$$

Topic : Average CPI

Consider computing the overall CPI for a machine A for which the following performance measures were recorded when executing a set of benchmark programs. Assume that the clock rate of the CPU is 200 MHz

Instruction Category	Number of Instructions	No. of cycles per Instruction	Total cycles
ALU	48	1	48 * 1 = 48
Load & Store	10	3	10 * 3 = 30
Branch	39	4	39 * 4 = 156
Other	3	5	3 * 5 = 15
Total	100	Total	249

$$\text{Avg. CPI} = \frac{249}{100} = 2.49$$

$$\text{MIPS} = \frac{200 \text{ MHz}}{2.49 * 10^6}$$

$$= \frac{200}{2.49} \text{ MIPS}$$

$$= 80.32 \text{ MIPS}$$

[NAT] GATE-2014 PYQ

Ans = 1.6

#Q. Consider two processors P1 and P2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P1. If the clock frequency of P1 is 1GHz, then the clock frequency of P2 (in GHz) is _____?

	P1	P2
Time	t_1	$t_2 = 0.75 t_1$
CPI	C_1	$C_2 = 1.2 C_1$
freq.	$f_1 = 1GHz$	$f_2 =$ ___ ?
no. of instns	n_1	n_2

$$t = \frac{n * CPI}{f}$$

$$n = \frac{t * f}{CPI}$$

$$n_1 = n_2$$

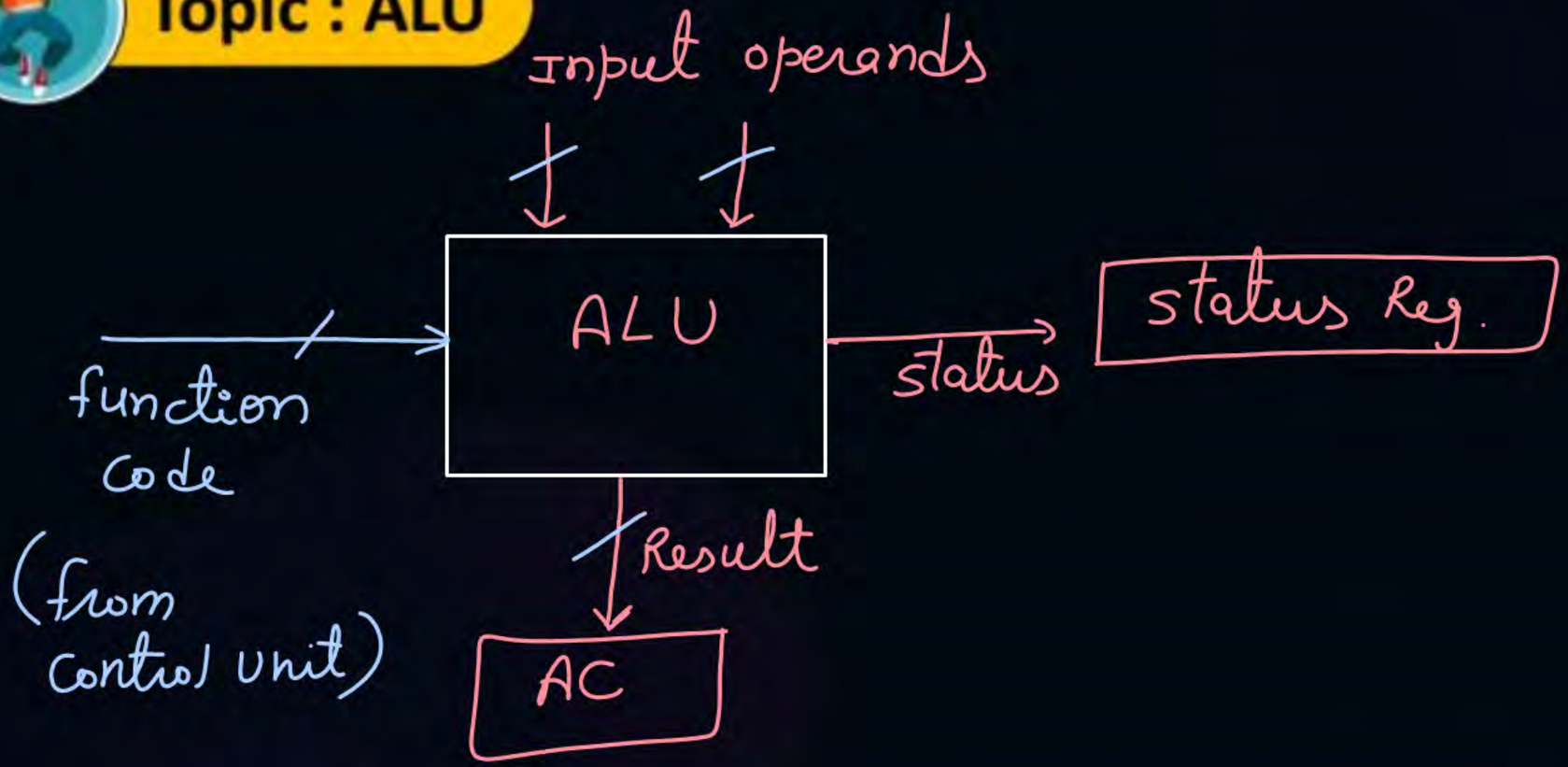
$$\frac{t_1 * f_1}{C_1} = \frac{t_2 * f_2}{C_2}$$

$$\frac{t_1 * 1GHz}{C_1} = \frac{0.75 t_1 * f_2}{1.2 C_1}$$

$$f_2 = \frac{1.2}{0.75} * 1GHz$$

$$= 1.6\ GHz$$

Topic : ALU


Input operands
ALU
status Reg.
status
function code
(from control unit)
Result
AC

2 mins Summary

Topic CPU

Topic MIPS

Topic Data Path

Happy Learning

THANK - YOU