CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Floating Point Representation

Lecture No.- 01

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Recap of Previous Lecture

Topic Hardwired Control Unit

Topic Microprogrammed Control Unit

Topic Control Word Sequencing

Topics to be Covered

- **Topic** RISC vs CISC
- **Topic** Byte Ordering
- **Topic** Floating Point Representation

Topic : Types of Microprogrammed Control Unit

Horizontal

In control word one bit per signal is stored

---

control word size is large

---

no any decoder needed.

vertical

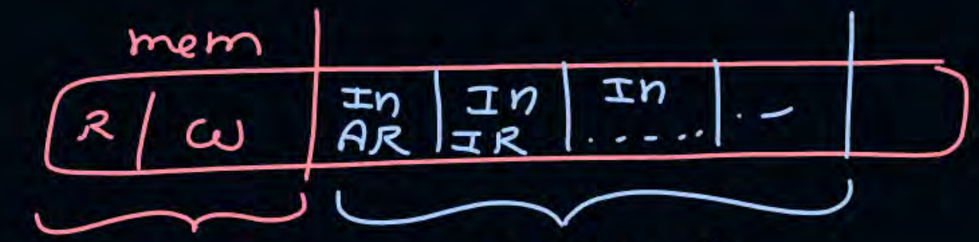
Control word is stored in encoded form to reduce it's size.

All signals are divided into multiple groups in such a way that from one group only one signal is active at time.

Decoder needed to generate signals.

Horizontal	Vertical
→ max no. of signals active at a time (max degree of parallism) is more.	max degree of parallelism is limited by no. of groups.
→ Faster	→ slower because of signal decoders.

Vertical microprogrammed C.U.:-



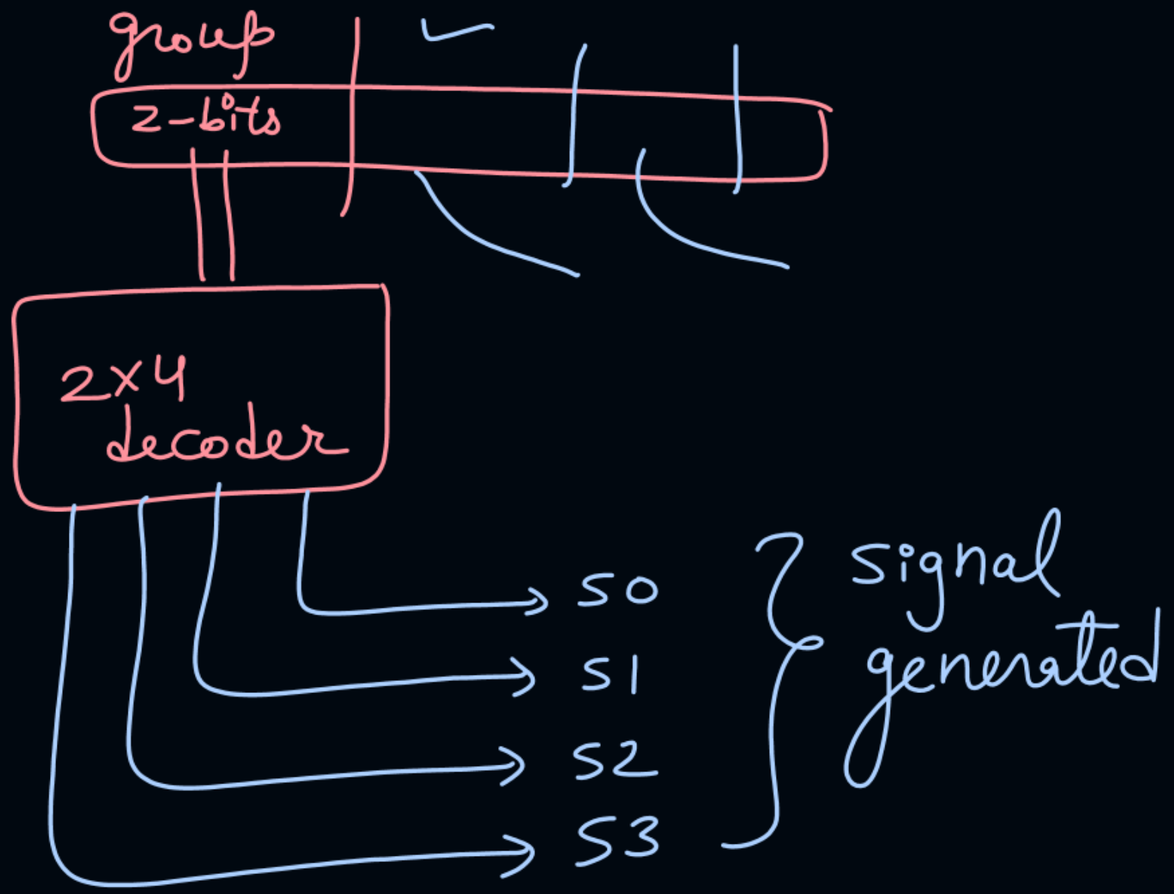
ex:- 4 signals S0, S1, S2, S3 are grouped in single group

	S3	S2	S1	S0
S0 active	0	0	0	1
S1	0	0	1	0
S2	0	1	0	0
S3	1	0	0	0

Horizontal

⇒

vertical	stored
S0 active	00
S1	01
S2	10
S3	11


group
2-bits
2X4
decoder
S0
S1
S2
S3
signal
generated

Topic : Speed Comparison

Fastest

Hardwired > Horizontal micro-prog. > vertical micro-prog.

slowest

[NAT]

#Q. A control unit generates 120 control signals, which are divided into 6 groups of mutually exclusive signals as below:

Group1 = 30 $\Rightarrow \lceil \log_2 30 \rceil = 5$ bits

Group2 = 13 $\Rightarrow$ 4 bits

Group3 = 12 $\Rightarrow$ 4 bits

Group4 = 3 $\Rightarrow$ 2 bits

Group5 = 27 $\Rightarrow$ 5 bits

Group6 = 35 $\Rightarrow$ 6 bits

Horizontal = 120 bits

Vertical = 5 + 4 + 4 + 2 + 5 + 6 = 26 bits

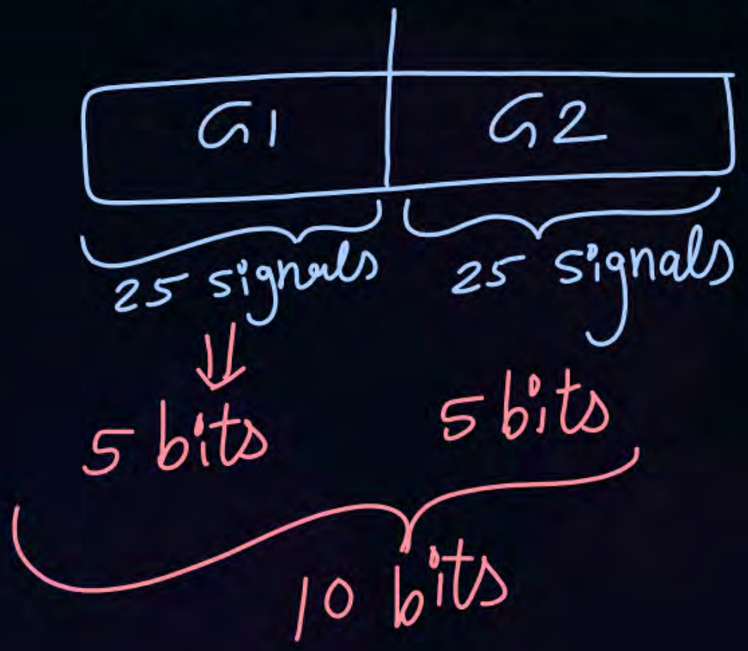
94 bits saved

How many bits can be saved by using vertical micro-programmed control unit as compared to horizontal one? Ans = 94

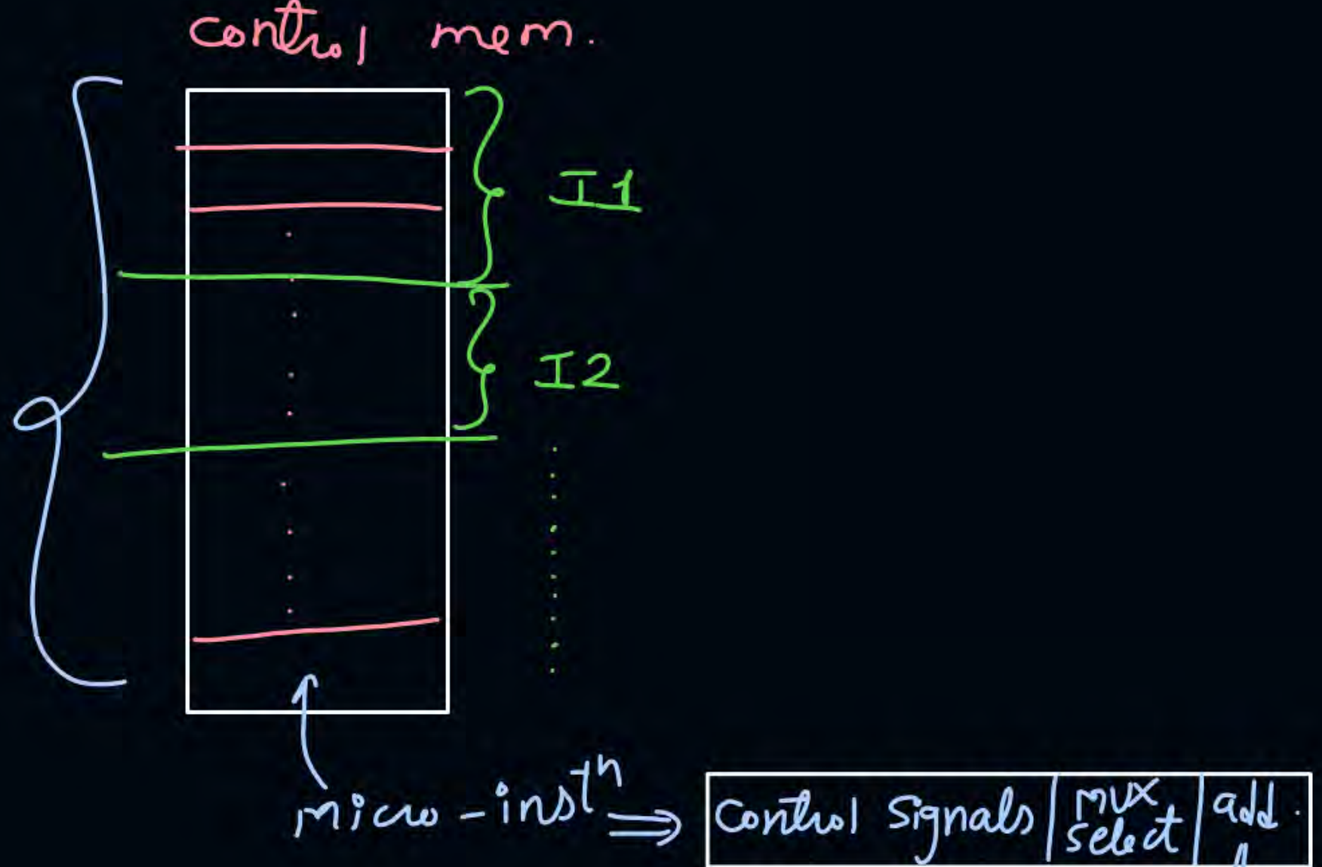
[NAT]

vertical ⇒ 2 groups

#Q. A micro-programmed control unit is required to generate a total of 25 control signals. Assume that during any microinstruction at most 2 control signals are active. Minimum number of bits required in the control word to generate the required control signals will be?



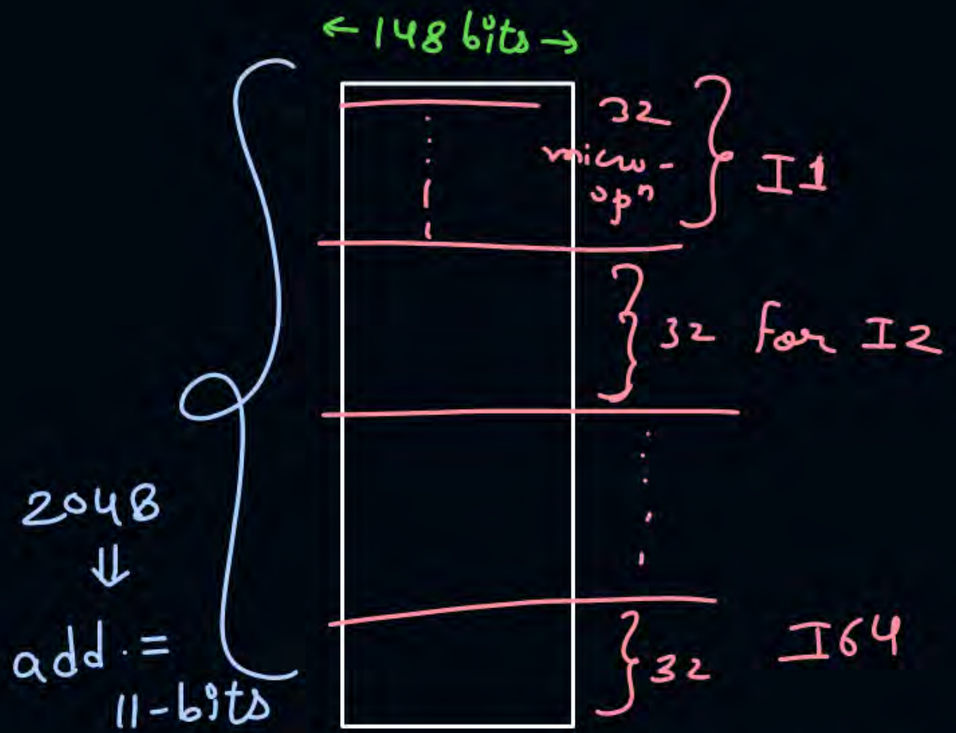
Ans = 10

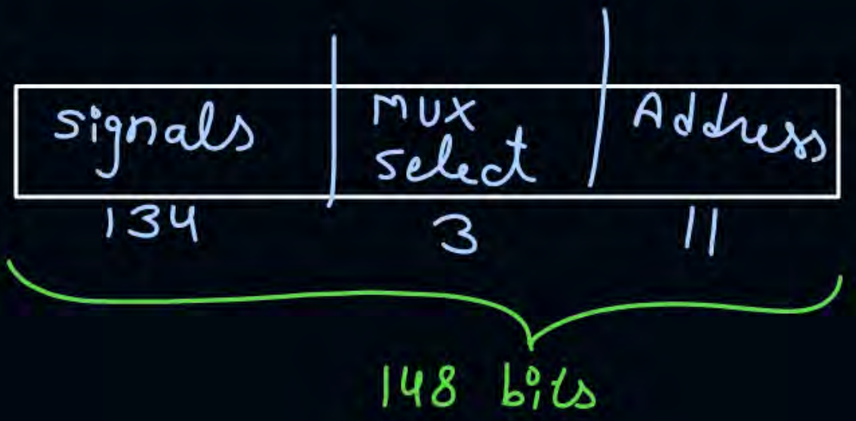

control mem.
I1
I2
micro-instn
Control Signals
mux select
add.
depends on
no. of micro-instns

[NAT]

#Q. A micro-programmed control unit is required to support 64 instructions with each instruction need a sequence of 32 microoperations to execute completely. The control unit has microinstruction format with 3 fields: control signals, MUX select and next address field. The control unit has 134 signal to be stored in horizontal manner. The MUX has 8 inputs. The size of control memory to support such control unit is 296 k bits?

mux select = 3 bits





No. of micro-instns stored = $64 * 32$

$= 2^6 * 2^5$

$= 2^{11}$

$= 2048 \Rightarrow$ add. = 11-bits

Control mem. size $= 2^{11} * 148$ bits

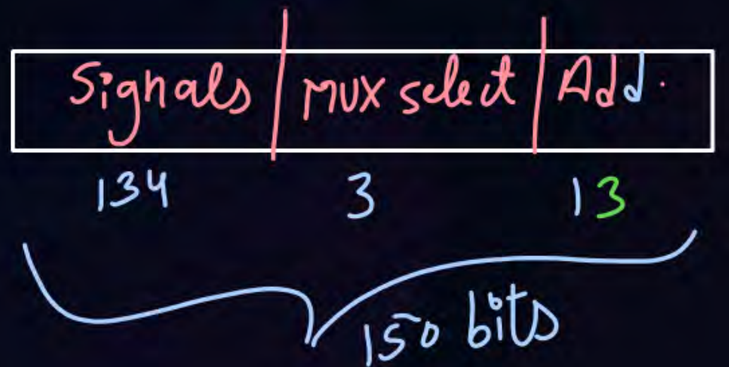
$= 2 * 2^{10} * 148$ bits

$= \underline{296}$ k bits

[NAT]

#Q. A micro-programmed control unit is required to support 128 instructions with each instruction need a sequence of 64 microoperations to execute completely. The control unit has microinstruction format with 3 fields: control signals, MUX select and next address field. The control unit has 134 signal to be stored in horizontal manner. The MUX has 8 inputs. The size of control memory to support such control unit is 150 k bytes?

no. of microinst^{ns} $= 64 * 128 = 2^{13} \Rightarrow$ add. $= 13$ bits



mem size $= 2^{13} * 15$ bits
$= 2^3 * 2^{10} * 150$ bits
$= 150$ k bytes

Topic : RISC vs CISC

S. No.	RISC (Reduced Instruction-Set Computer)	CISC (Complex Instruction-Set Computer)
1.	Less Number of Instructions Supported	More Number of Instructions
2.	Fixed Length Instructions	Variable Length Instructions
3.	Simple Instructions	Complex Instructions
4.	Simple and less number of addressing Modes	Complex and More number of addressing Modes
5.	Easy to implement using hardwired control unit	Difficult to implement using hardwired control unit

Topic : RISC vs CISC

S. No.	RISC (Reduced Instruction-Set Computer)	CISC (Complex Instruction-Set Computer)
6.	One Cycle per instruction	More than one cycle per instruction
7.	Register-to-Register arithmetic operation only (Reg.-based architecture)	Register-to-Memory & Memory-to-Register arithmetic operations possible
8.	More Number of Registers (GPRs)	Less Number of Registers

[MCQ]

#Q. Consider the following processor design characteristics.

I. Register-to register arithmetic operations only

II. Fixed-length instruction format

III. Hardwired control unit

Which of the characteristics above are used in the design of a RISC processor?

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A I and II only

B II and III only

C I and III only

D I, II and III

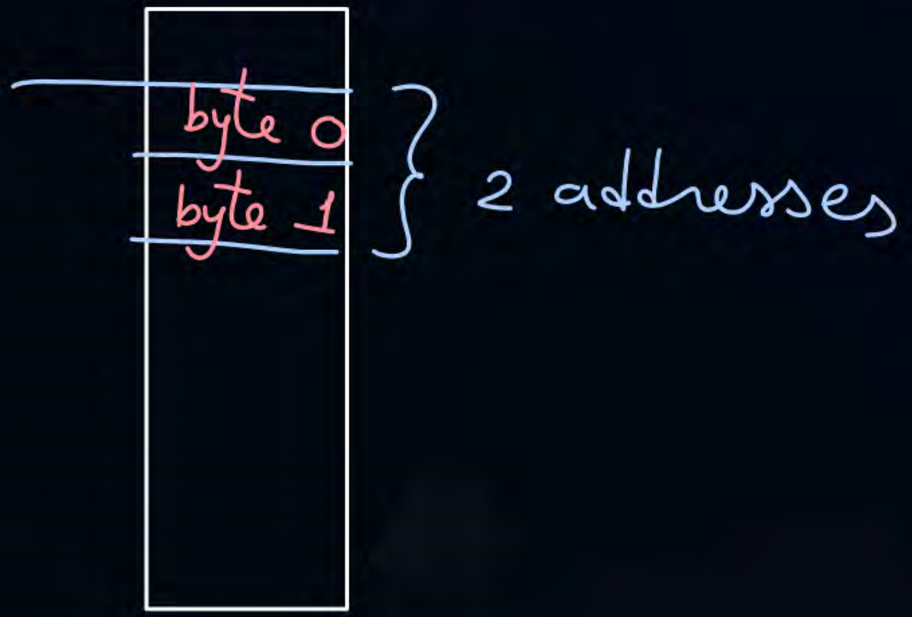
Topic : Byte Ordering

2 bytes instⁿ

16-bits

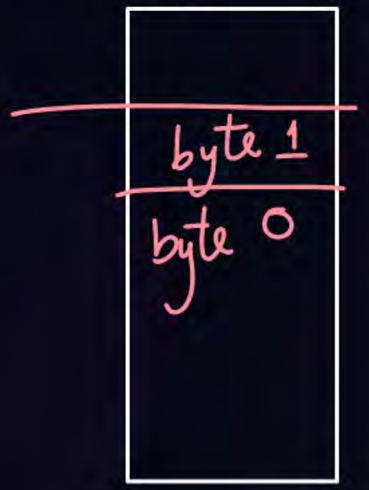
byte 1	byte 0

⇒ store in byte addressable memory

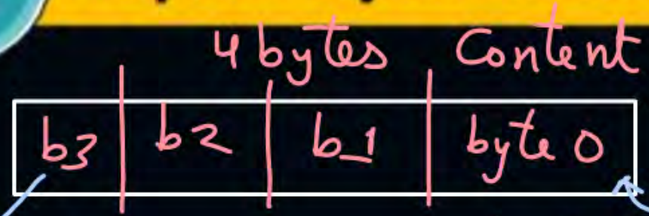


little endian

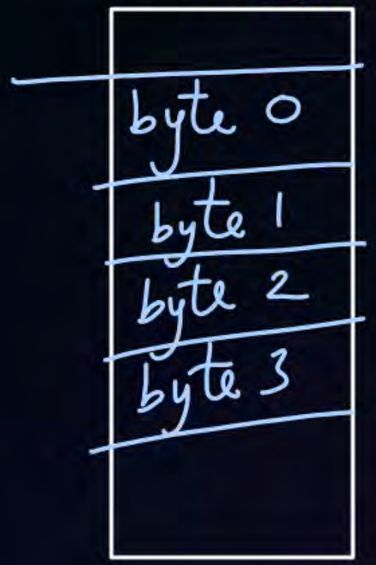
Big endian



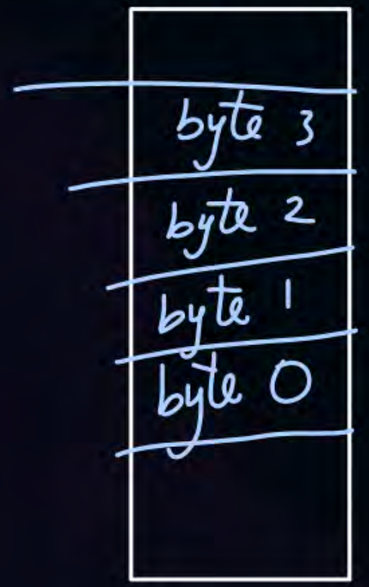
Topic : Byte Ordering



Little endian

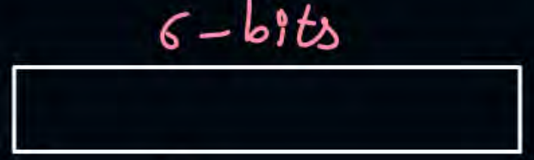


Big endian



Floating point Representat^n

In fixed point representat^n



⇓

Unsigned ⇒ Range 0 to 63

Signed ($2^{'s}$ Comp.) ⇒ −32 to +31

⇒ limited range of numbers represented.

⇓

so^n ⇒ floating point representat^n can provide longer range of numbers

Topic : Floating-Point Numbers

- The number is represented in format:

Sign Exponent Mantissa

S	E	M

- Mantissa is signed normalized (implicit/explicit) fraction number
- Exponent is stored in biased form.

sign ⇒ alway 1 bit → 0 ⇒ +ve, 1 ⇒ -ve

Exponent ⇒ power of 2.

Topic : Biased Exponent

↳ Convert exponent into unsigned value and store

S	E	M

⇓

stored in 4 bits

⇓

signed numbers ⇒ −8 to +7 (Range) —Transform→ unsigned 0 to 15

original exponent (e)	stored exponent (E) excess-8 code
−8	0
−7	1
−6	2
⋮	⋮
0	8
⋮	⋮
7	15

$E = e + 8$

↳ bias = 8

$E = e + \text{bias}$

If k-bits are used to store E.

$$\text{Bias} = 2^{k-1}$$

Topic : Mantissa

Mantissa (M) = Number after point

101.1

Explicit normalizat^{n} $\Rightarrow 0.1011 * 2^{3}$

should be '1'

M = 1011

e = 3

E = 3 + bias

S	E	M = 1011

Implicit normalizat^{n} $\Rightarrow 1.011 * 2^{2}$

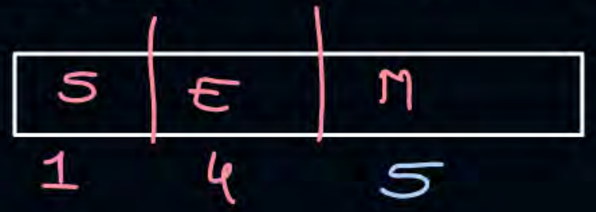
should be '1'

M = 011

e = 2

E = 2 + bias

example:- (Explicit normalizat^n)



Number $\Rightarrow$ $+(101.11)_2 \Rightarrow$ Explicit normalizat^n $\Rightarrow 0.10111 * 2^3$

$M = 10111$

$e = 3$

$E = 3+8 = (11)_{10} = (1011)_2$

for E of 4 bits

$\Downarrow$

$bias = 2^{4-1} = 2^3 = 8$

for S = 0 for +ve number

S	E	M
0	1011	10111

Topic : Value Formula

S	E	M

$$\text{Value (Explicit)} = (-1)^{S} * 0.M * 2^{E-\text{bias}}$$

$$\text{Value (Implicit)} = (-1)^{S} * 1.M * 2^{E-\text{bias}}$$

[MCQ]

bias = 64

#Q. A certain well-known computer family represents the exponents of its floating-point numbers as "excess-64" integers; i.e., a typical exponent $e_6e_5e_4e_3e_2e_1e_0$ represents the number:

A $e = -64 + \sum_{i=0}^{6} 2^i ei$

B $e = -64 + \sum_{i=0}^{6} 2e_i$

C $e = 64 - \sum_{i=0}^{6} 2^i ei$

D $e = 64 - \sum_{i=0}^{6} 2e_i$

binary to decimal

$$e_6 e_5 \cdots e_0 \Rightarrow (e_6 * 2^6) + (e_5 * 2^5) + \cdots + (e_0 * 2^0)$$

$$\Downarrow$$

$$\text{original exponent} = \text{value} - \text{bias} \Rightarrow \sum_{i=0}^{6} e_i * 2^i - 64$$

2 mins Summary

Topic RISC vs CISC

Topic Byte Ordering

Topic Floating Point Representation

Happy Learning

THANK - YOU