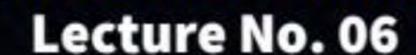
CS & IT

ENGINEERING



Combinational Circuit





By- CHANDAN SIR



TOPICS TO BE COVERED 01 HS

02 FS

03 SERIAL ADDER

04 PARALLEL ADDER

HA

Sum=ABB

(arry = AB

NAND/NOR= 5

FA

Sum = A & B & C

$$= (A \oplus B) (+ AB)$$

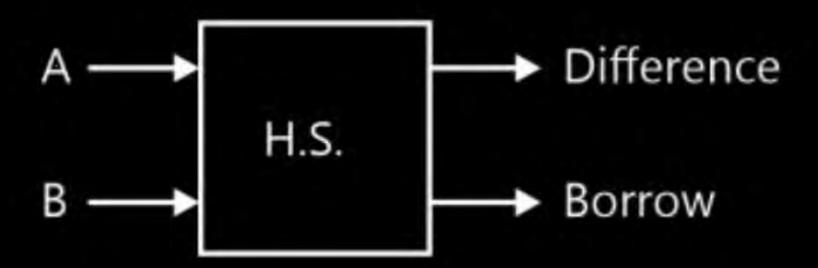
NAND/NOR= 9





HALF SUBTRACTOR - Two bit subtractor

Step - 1



Pw

HALF SUBTRACTOR

Step - 1

A	В	Diff.	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

HALF SUBTRACTOR

Borrow -



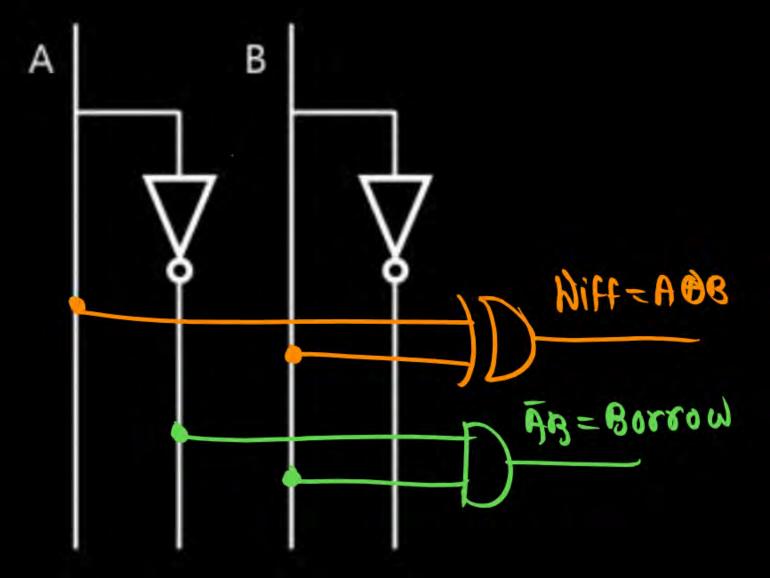
HALF SUBTRACTOR

Step - 4: Minimization

La Already minimized

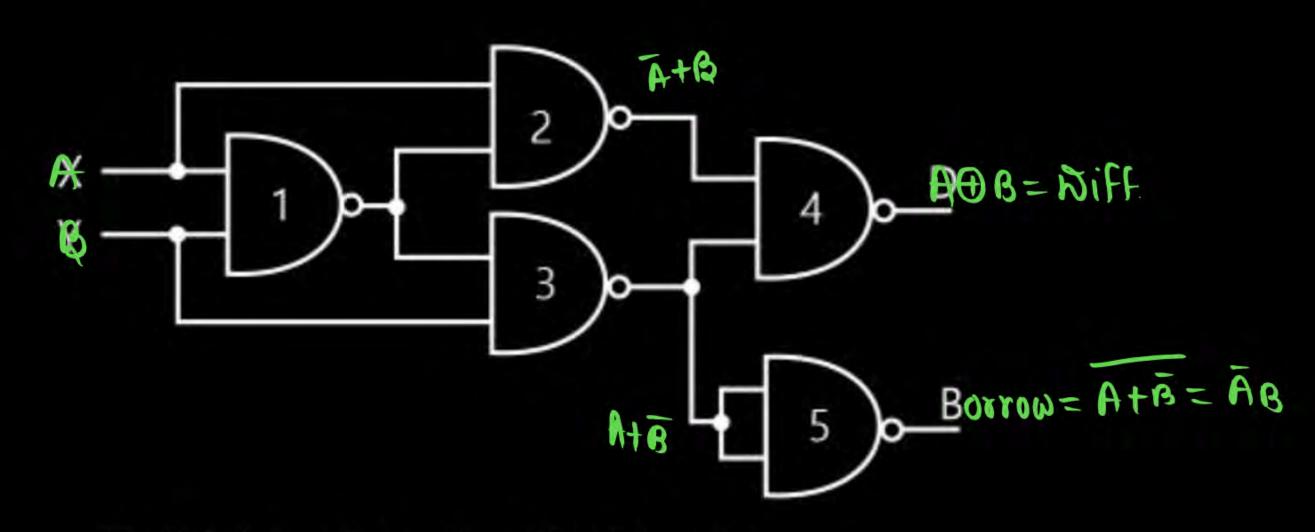
Step - 5: Hardware Implementation





Pw

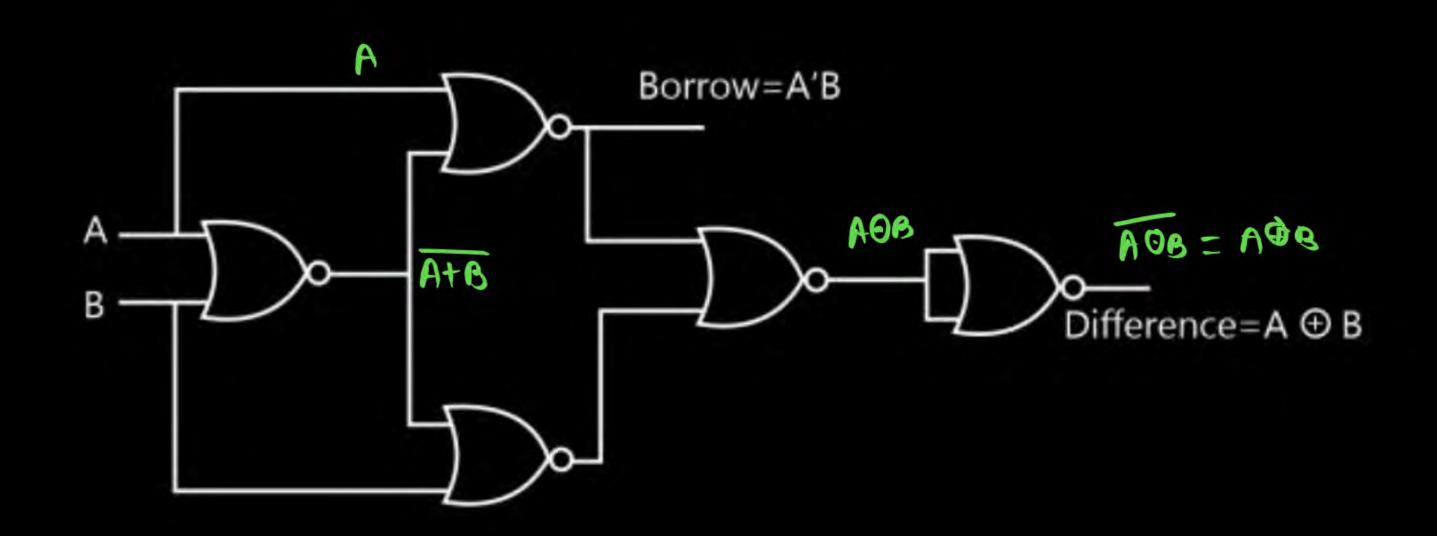
HALF SUBTRACTOR

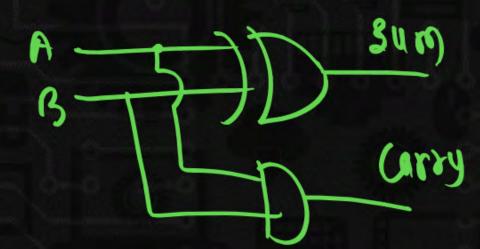


Half-Subtractor using NAND gates

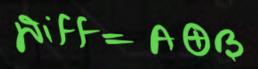
Pw

HALF SUBTRACTOR

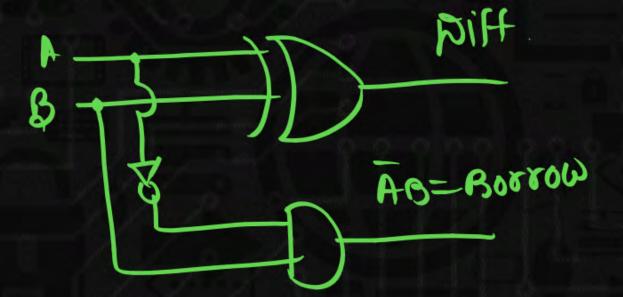




H.S.



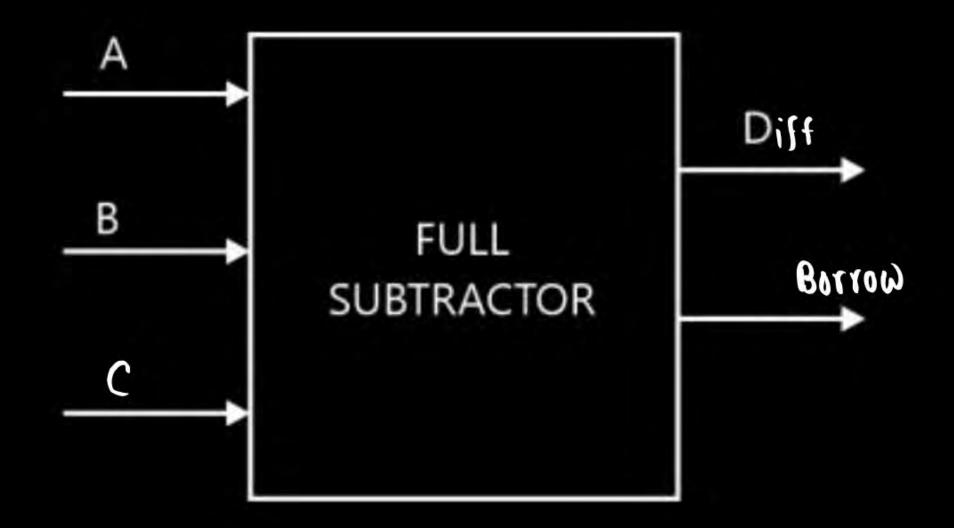
Borrow = AB



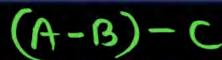


Pw

FULL SUBTRACTOR - Three bit subtractor



FULL SUBTRACTOR



TRACTOR	(4-13)			
INPUT			OUTPUT	
Α	В	С	Diff.	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



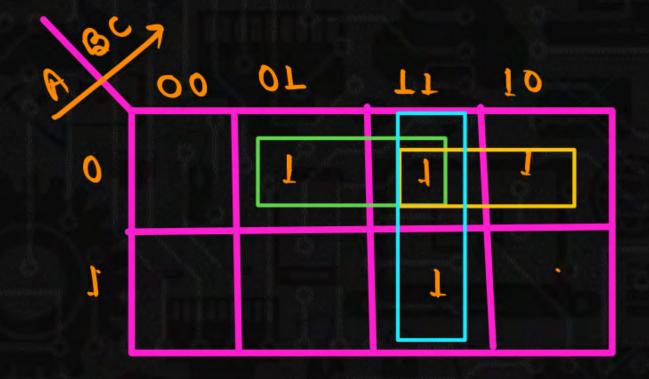
Step4

Biff = ABBBC =
$$\leq m(\Gamma'3'4'+)$$



$$= (\bar{A}\bar{B} + \bar{A}\bar{B})C + \bar{A}\bar{B}(\bar{c}+\bar{c})$$

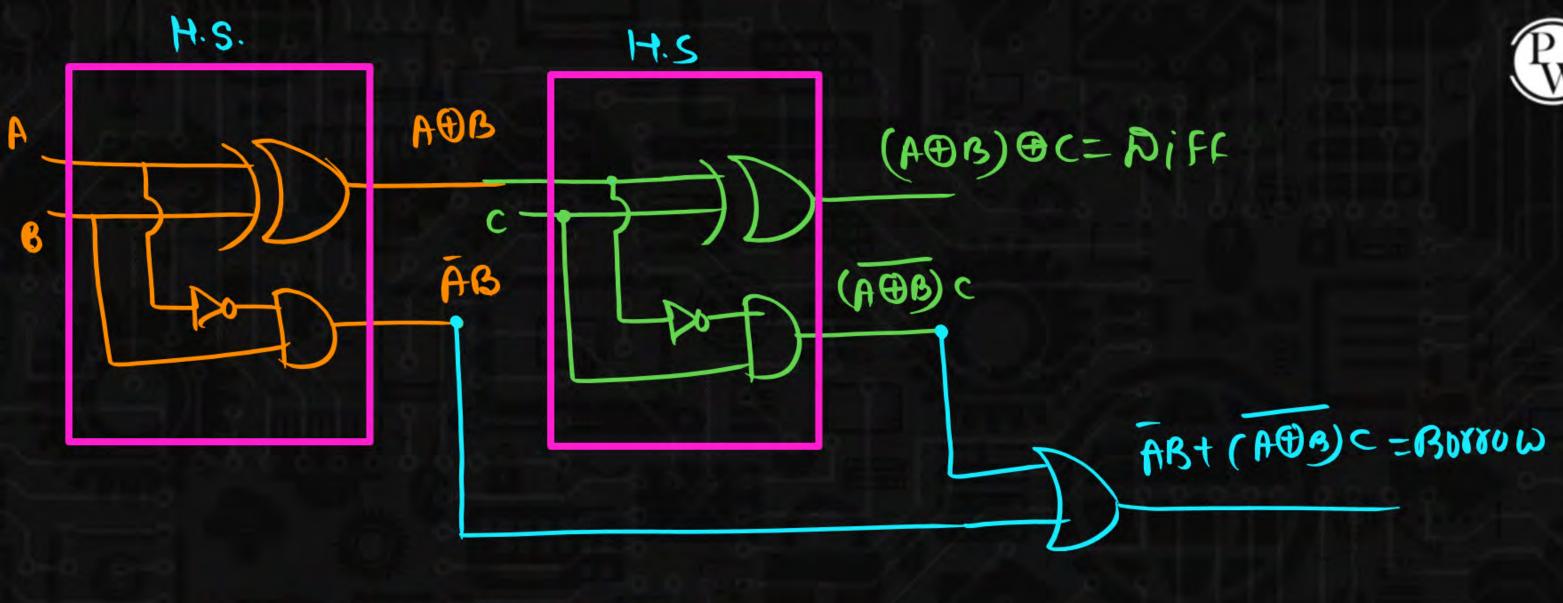




$$= \bar{A}B + \bar{A}C + BC$$

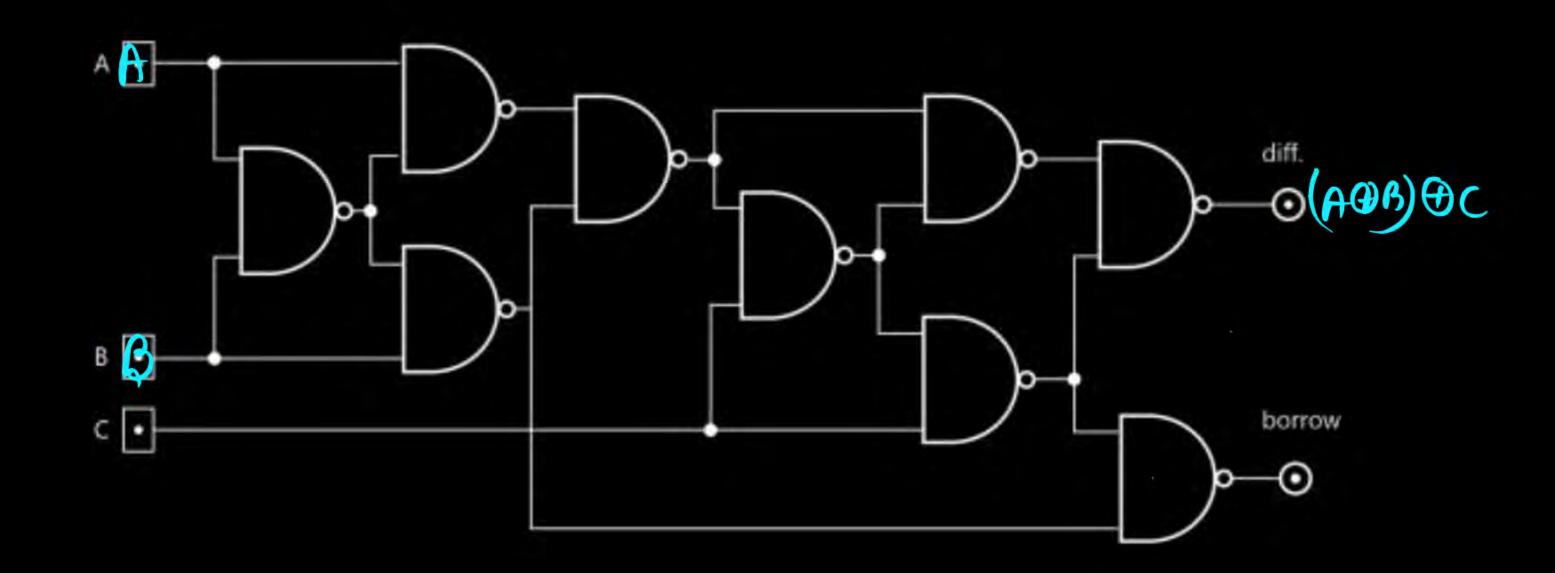
FULL SUBTRACTOR



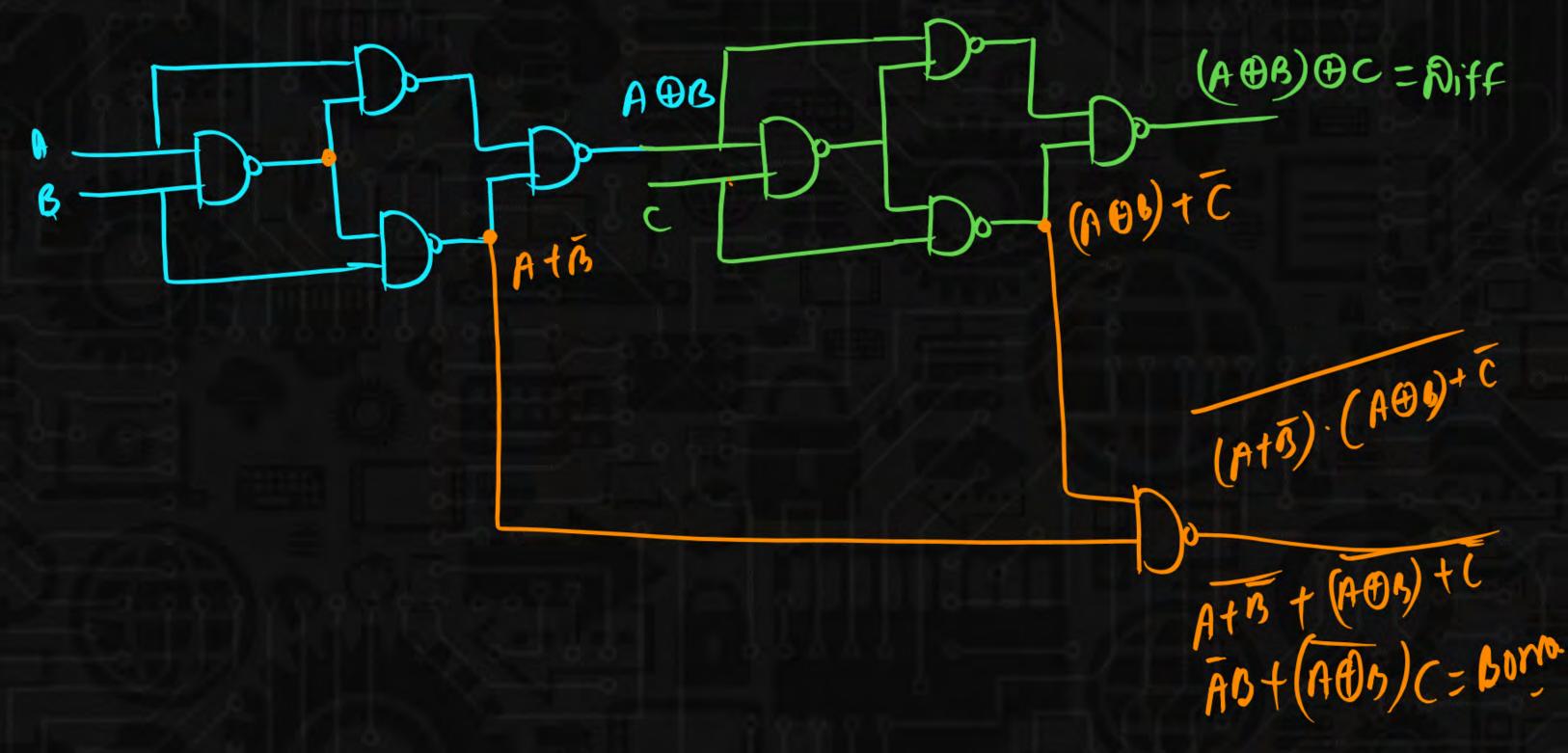


Pw

FULL SUBTRACTOR







FA

NAND/NOR=9

F.\$.



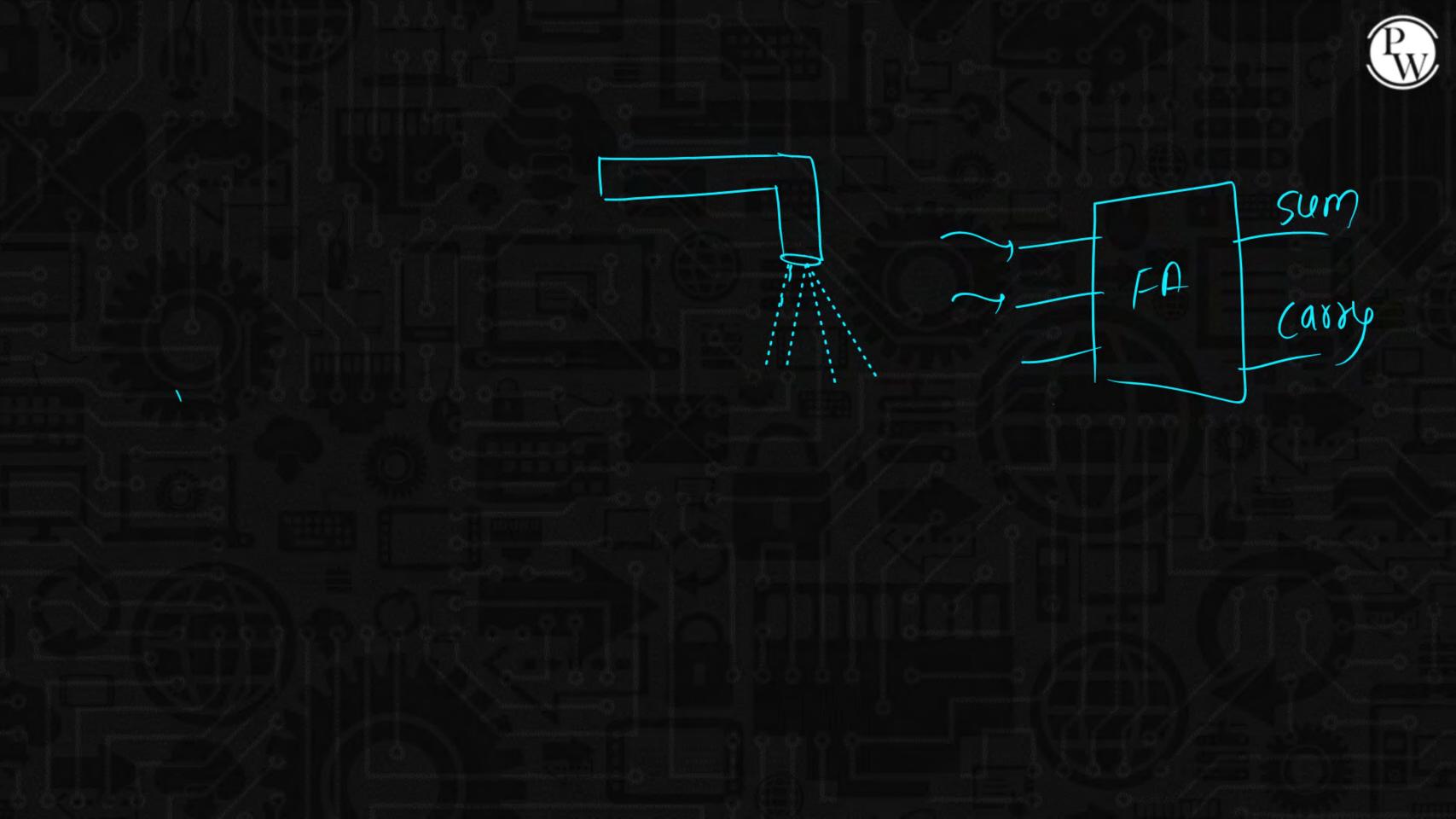


Comparator

MUX DE-MUX

Encoder, Decoder.

HA, FA Itis, F-S.

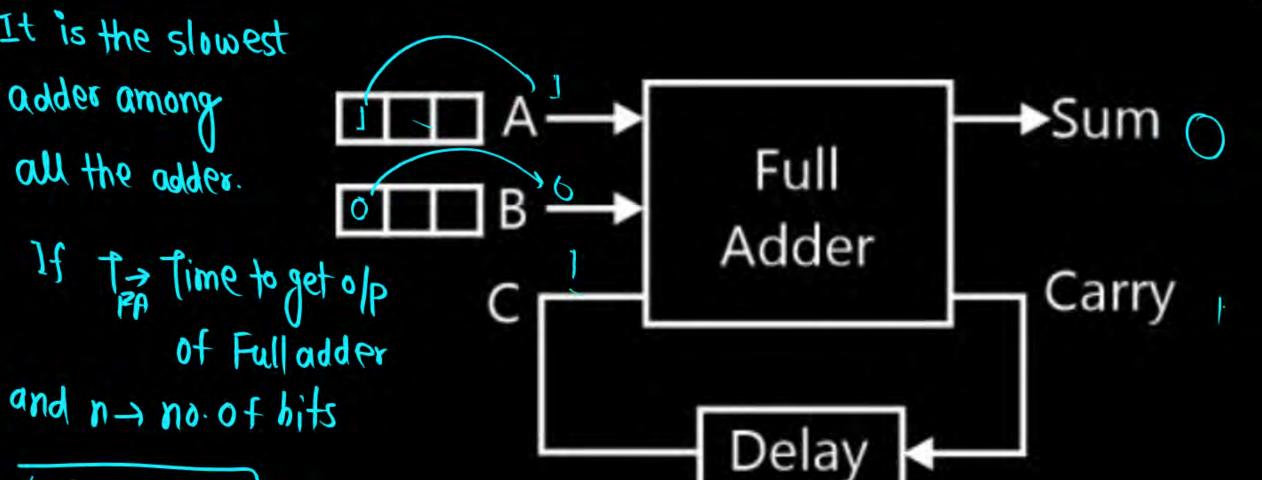




- one by one.

Curry

It is the slowest adder among all the adder.



T= n-TFA V

PARALLEL ADDER



-> Inputs are connected simultaneously

4 bits

'h' bit parallel adder

$$\Rightarrow$$
 $(n-1)$ FA + 1 HA

1 FA = 2HA+10R CHATE

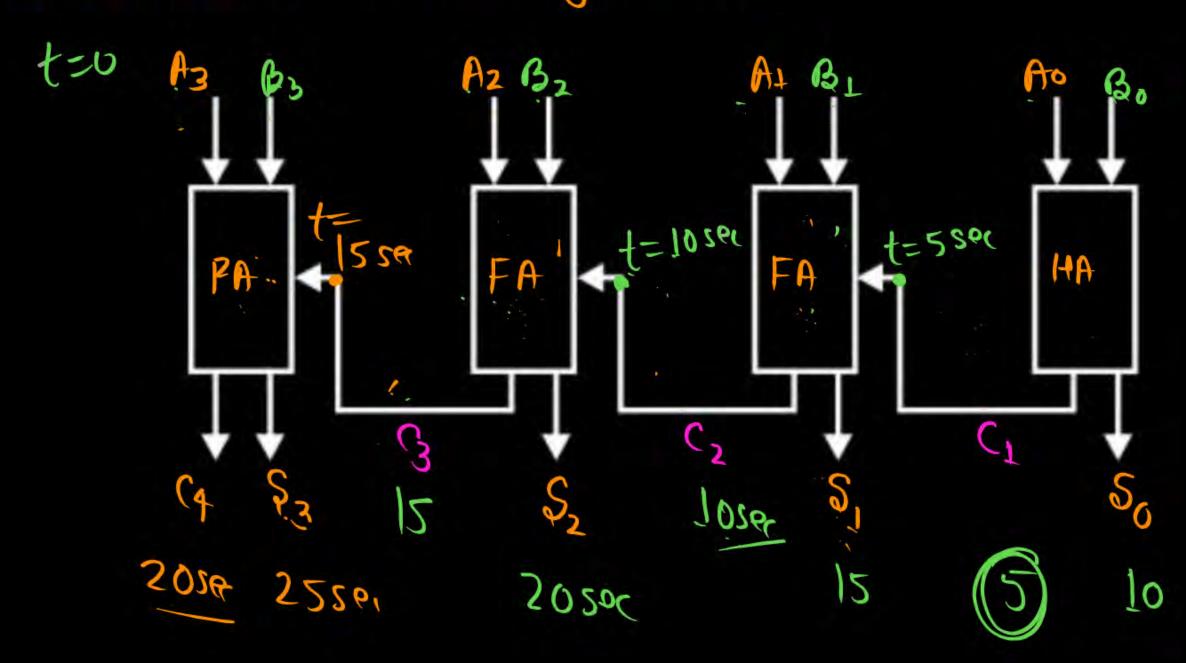


$$(n-1)(FA) + LHA$$

 $(n-1)(FA) + LHA$
 $(n-1)(FA) + LHA$
 $(gn-2) + HA + (n-1)OR + LHA$
 $(gn-1)HA + (n-1)OR$
 $(gn-1)HA + (n-1)OR$

PARALLEL ADDER, LACA

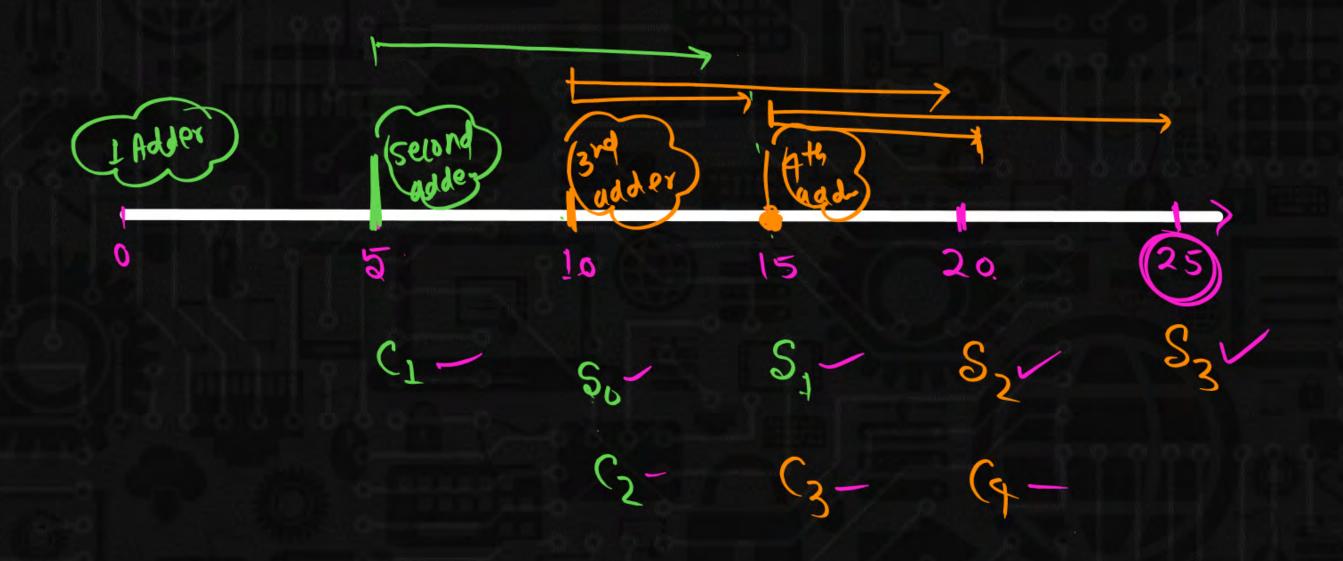
PARALLEL ADDER [Ripple Corry addes]





Tsum=10sec
Tcarry=5 sec











Thank you

Seldiers!

