CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

IO Organization

Lecture No.-01

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Recap of Previous Lecture

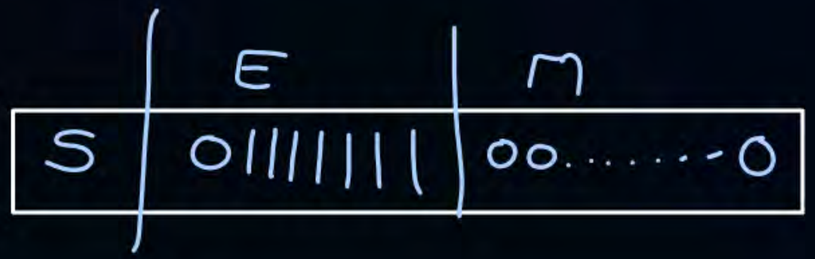
- Topic: Floating-Point Numbers
- Topic: Biased Exponent
- Topic: Number Range
- Topic: IEEE-754 Floating Point Representation
- Topic: Denormalized Number

Topics to be Covered

- **Topic** Peripheral Device
- **Topic** IO vs Memory Buses
- **Topic** Memory Mapped IO vs IO Mapped IO
- **Topic** Asynchronous Data Transfer

[NAT]

#Q. How to represent +1 and -1 in IEEE-754 single precision floating point number?



$(1.0)_{10} = (1.0)_2$

⇓

Implicit normalizat^n

⇓

$1.0 * 2^0$

$M = 000\ldots0$

$e = 0$

$E = 0 + 127 = (127)_{10} = (01111111)_2$

[NAT]

#Q. How to represent $+(0.0000101)_2$ in IEEE-754 single precision floating point number?

$\Downarrow$

Implicit normalizath

$\Downarrow$

$1.01 * 2^{-5}$

S	E	M
0	01111010	01000...0

$m = 0100\cdots0$

$e = -5$

$E = -5 + 127 = 122 = (01111010)_2$

[MCQ]

GATE - PYQ

#Q. The value of a float type variable is represented using the single- precision 32-bit floating point format IEEE-754 standard that uses 1bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A float type variable X is assigned the decimal value of −14.25. The representation of X in hexadecimal notation is

A ✓ C1640000H

B 416C0000H

C 41640000H

D C16C0000H

S = 1

$(14.25)_{10} = (1110.01)_2$

$= 1.11001 * 2^3$

M = 11001000...0

e = 3

E = 3 + 127 = 130

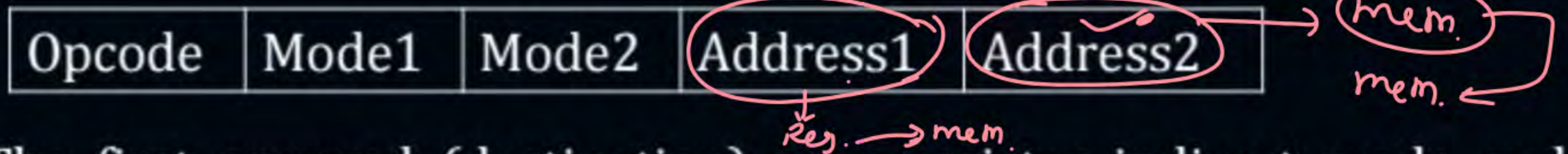
$= (10000010)_2$

S	E	M
1	10000010	11001000...0

C 1 6 4 0 0 0

[NAT]

#Q. Consider a 6-words instruction, which is of the following type:



The first operand (destination) uses register indirect mode and second operand uses indirect mode. Assume each operand is of size 2 words, each address is of 2 words and main memory takes 50ns for 1 byte access. Further assume that the opcode denotes addition operation which copies result of addition of 2 operands. One word size is 4 bytes. Total time required in:

1. Fetch cycle of instruction = 1200ns
2. Execution cycle of instruction 1600ns
3. Instruction cycle of instruction => 1200 + 1600 = 2800 ns

Inst^n size = 6 words = 6 * 4 = 24 bytes

Add. size = 2 words = 2 * 4 = 8 bytes

operand size = 2 words = 2 * 4 = 8 bytes

---

1. Fetch time = 24 bytes read time from mem.

= 24 * 50 ns

= 1200 ns

---

2. Execution cycle :-

	operand 1	operand 2
E.A. calculat^n	0	8 * 50 = 400 ns
operand fetch	8 * 50 = 400	8 * 50 = 400 ns
write back	8 * 50 = 400	

Total = 1600 ns

Topic : Peripheral Device

Input/output device (I/O device)

All devices which are connected to CPU externally apart from main memory.

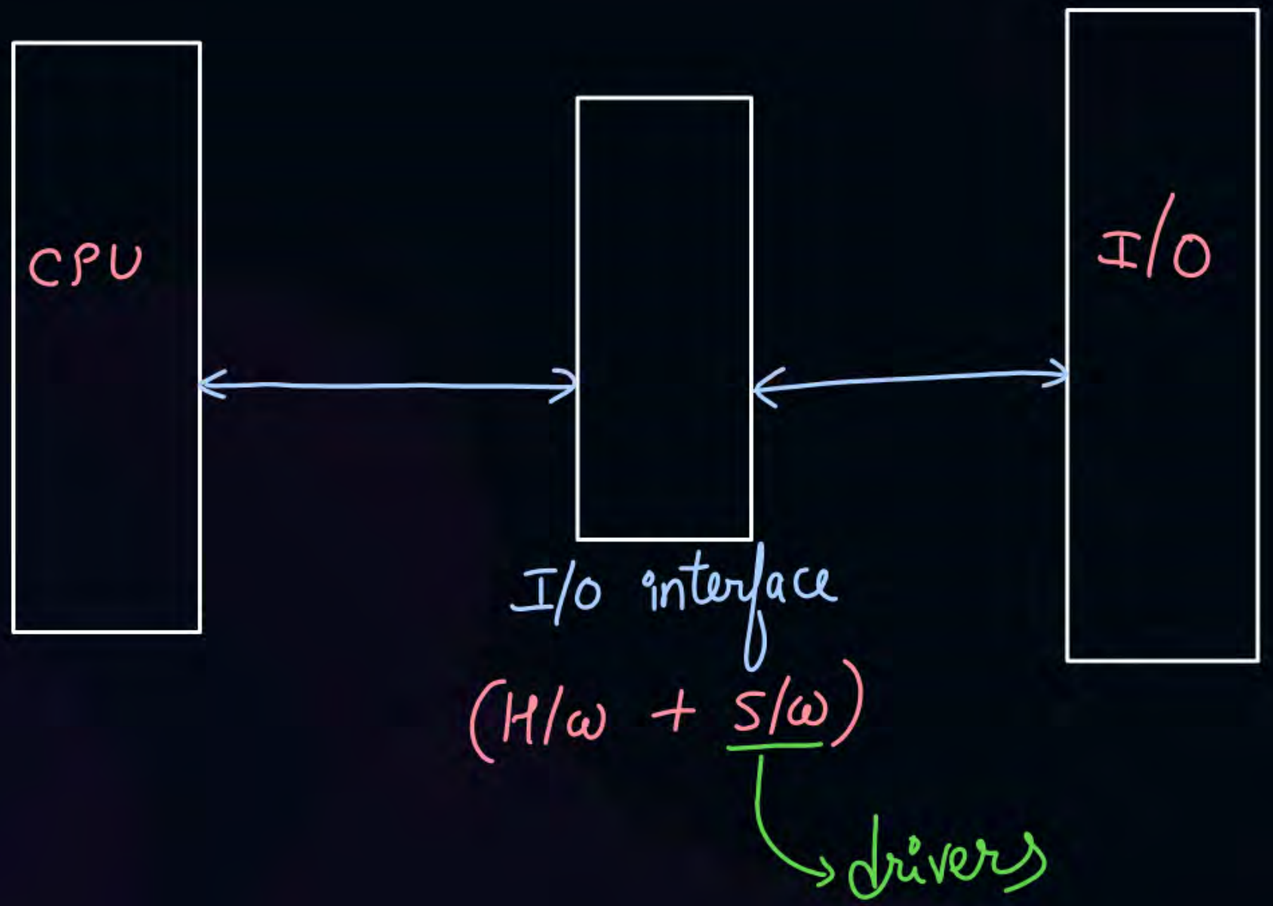
Types:-

1:- Input devices

2:- output devices

3:- storage devices

Topic : CPU Connected to IO Directly?



versions of I/O interfaces	operat^{n}
I/O interface	Interfacing
DMA Controller	Interfacing + DMA transfer
I/O processor	Interfacing + DMA transfer + I/O instruction Execution

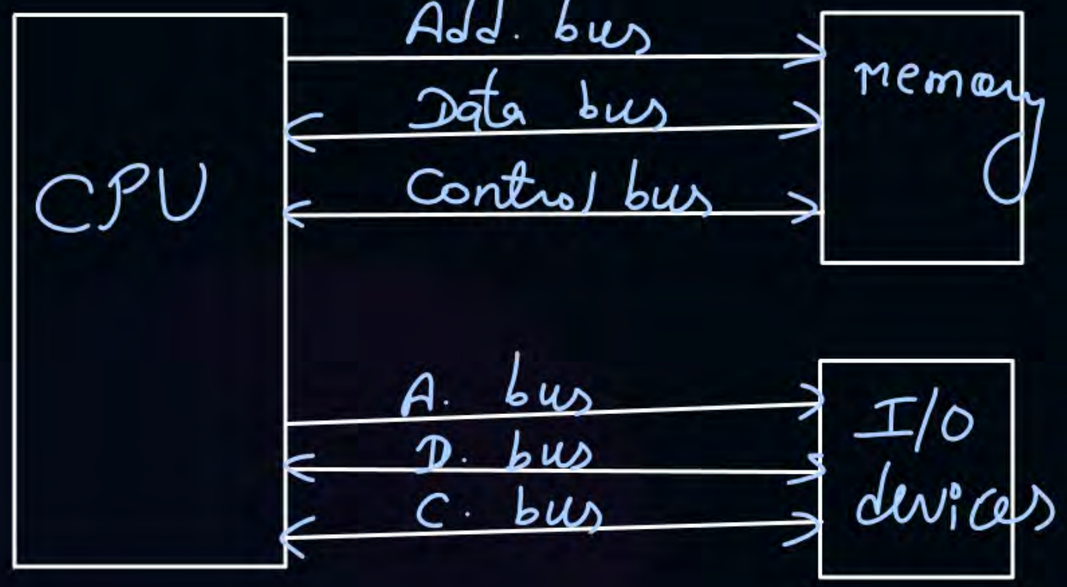
Topic : Need For Interface

1. Peripherals are electromechanical or electromagnetic devices; and their manner of operation is different from the operation of the CPU and memory. Which are electronic devices. So conversion of signal required.
2. The data transfer rate of peripherals is usually slow. So synchronization is required.
3. Data codes and format in peripherals differ from the word format in the CPU and memory. So conversion of formats is required.
4. The operating modes of peripherals are different from each other and each must be controlled so a peripheral does not disturb the operation of other peripherals.

Topic : IO vs Memory Buses

There are 3 way to connect CPU with memory & I/O

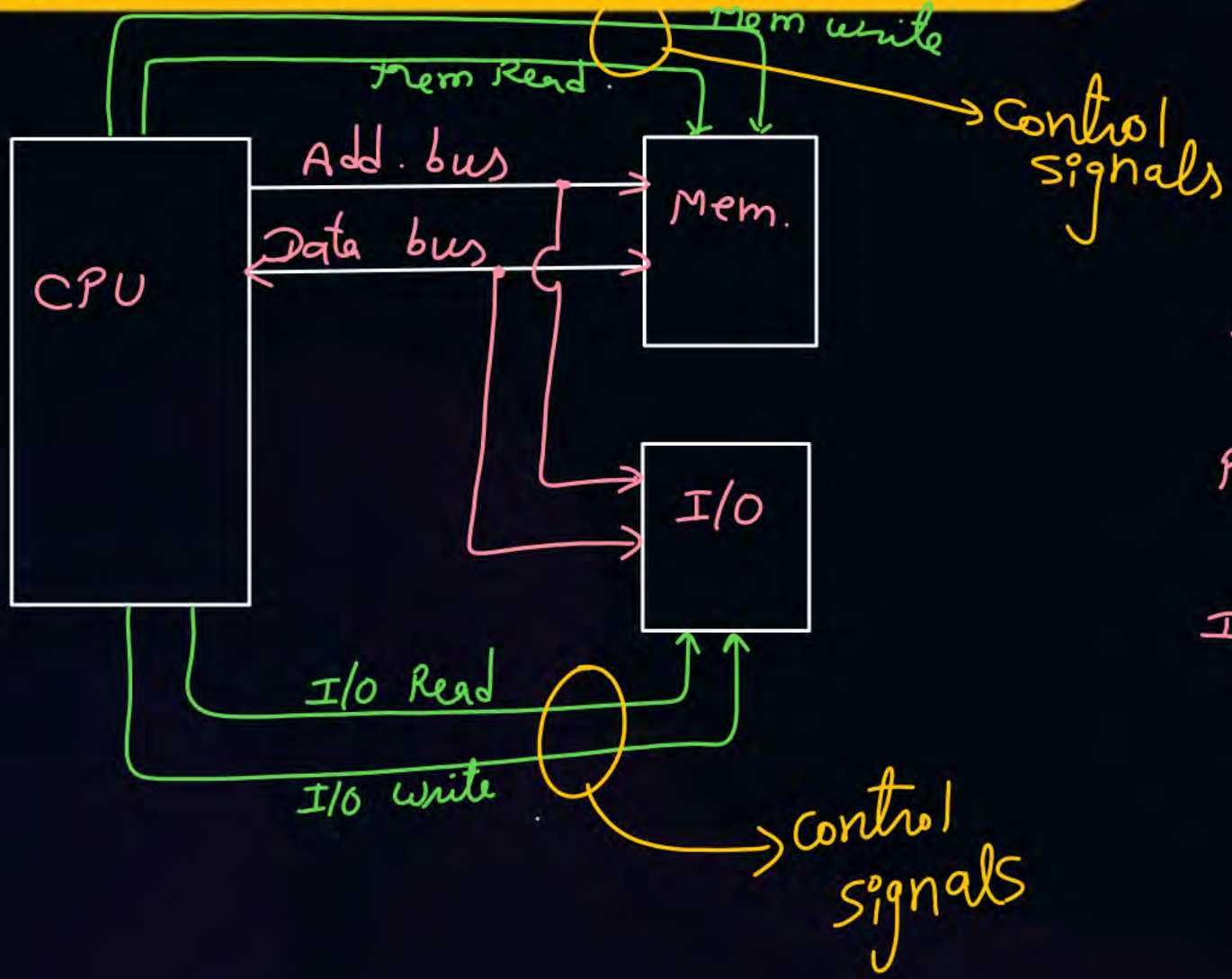
Topic : 1. Separate Buses for Both



Disadv :-

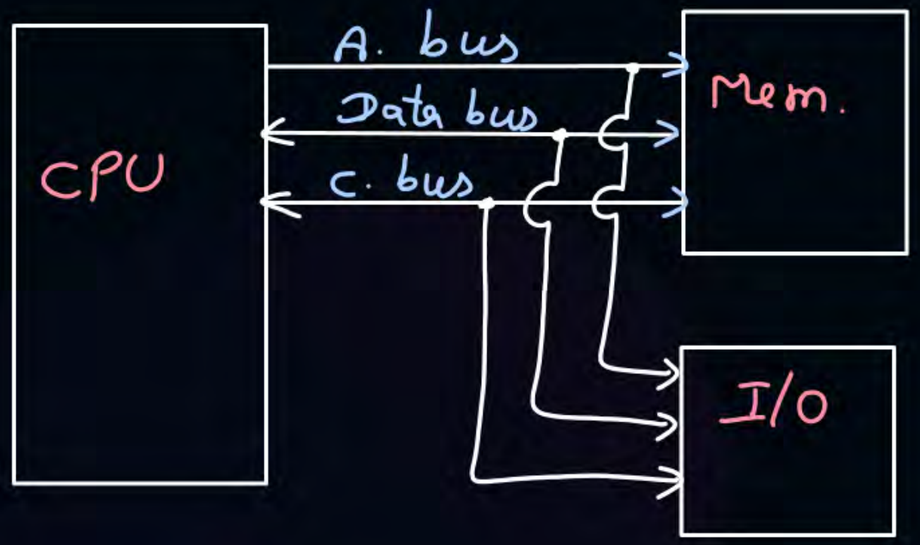
→ costly

Topic : 2. Common Data, Address Bus → Used



Isolated I/O
or
Port - mapped I/O
or
I/O - mapped I/O

Topic : 3. Common Address, Data & Control Bus

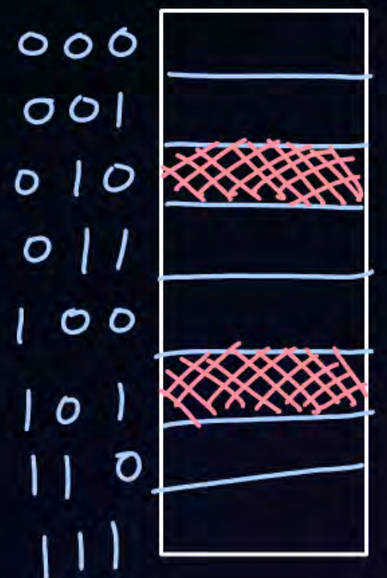


Memory – Mapped I/O

Topic : 3. Common Address, Data & Control Bus

ex:- There is a byte addressable mem. of size = 8 bytes and 2 I/O devices d1 and d2

2 addresses are allocated to devices from mem.



assume	allocated add.
d1	101
d2	010

Topic : Memory Mapped IO vs IO Mapped IO

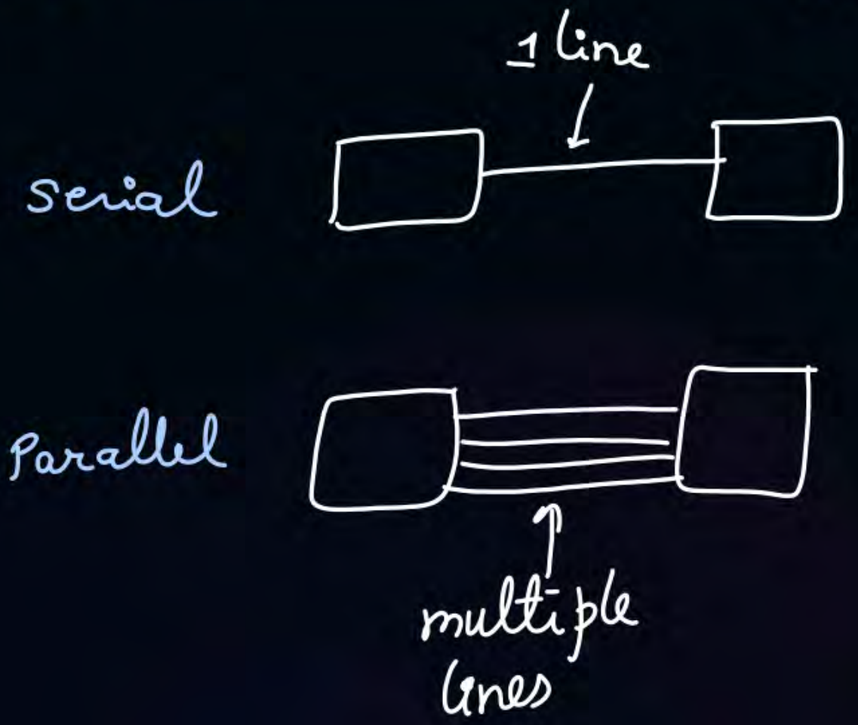
Memory Mapped IO	IO Mapped IO
1. Some part of mem. wastage	1. No mem. wastage
2. I/O devices do not have their own address space.	2. I/O devices have their own address space
3. All mem. access instns can be used to access I/O also.	3. I/O access instns and mem. access instns are different - different
4. More no. of instns and modes to access I/O.	4. Lesser no. of instns and addressing modes to access I/O devices.

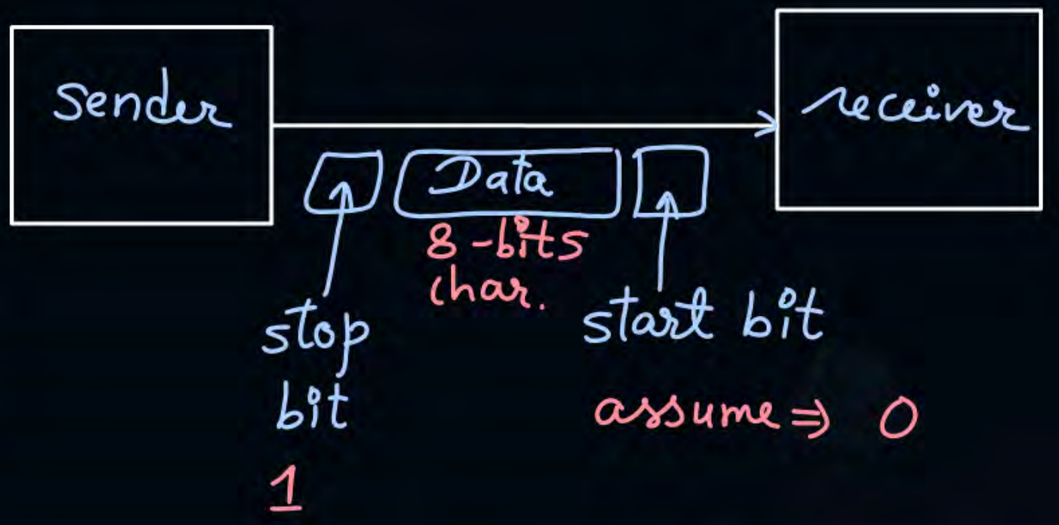
Topic : Memory Mapped IO vs IO Mapped IO

Memory Mapped IO	IO Mapped IO
5. More no. of I/O devices can be connected.	5. Less no. of I/O devices connected.

Topic : Asynchronous Data Transfer

serial





→ when there is no any data transfer then receiver always detects '1' on the line.

→ As soon as receiver get '0' (start bit), it will be ready to receive data.

$$\text{Efficiency of line} = \frac{\text{Char Size}}{\text{Total bits per char}}$$

Effective transmission rate = efficiency * Actual transfer rate

[NAT]

#Q. How many 8-bit characters can be transmitted per second over 9600 bits/sec. serial communication link using a parity synchronous mode of transmission with 1 start bit, 8 data bits, 2 stop bits and 1 parity bit?

for 1 char no. of bits = 1 + 8 + 2 + 1 = 12 bits

$$\text{no. of char/sec} = \frac{9600}{12} = 800 \text{ char/sec.}$$

$$\text{Efficiency} = \frac{8}{12}$$

[NAT]

#Q. An asynchronous serial communication is employing 8 character bits, 1 parity bit, 2 start bits and 1 stop bit. To maintain a rate of 700 char/sec. The minimum transfer rate should be required is 8400 bits/sec?

for 1 char = 8 + 1 + 2 + 1 = 12 bits

for 700 char = 700 * 12

= 8400 bits/sec

[NAT]

#Q. 8-bit characters can be transmitted using a parity synchronous mode of transmission with 1 start bit, 8 data bits, 2 stop bits and 1 parity bit.

1. What is the efficiency of the transmission line? $\frac{2}{3} = 0.66 = 66.67\ \%$
2. If the transfer rate of the line is 3000 bits per second, then effective transfer rate is? $= 2000$ bits/sec.

1. $\text{Efficiency} = \frac{8}{1+8+2+1} = \frac{8}{12} = \frac{2}{3} = 0.66 = 66.67\ \%$

2. Effective transmission rate $= \frac{2}{3} * 3000$ bits $= 2000$ bits/sec

2 mins Summary

Topic Peripheral Device

Topic IO vs Memory Buses

Topic Memory Mapped IO vs IO Mapped IO

Topic Asynchronous Data Transfer

Happy Learning

THANK - YOU