CS & IT ENGINEERING

DIGITAL LOGIC

Combinational circuit

Lecture No. 8

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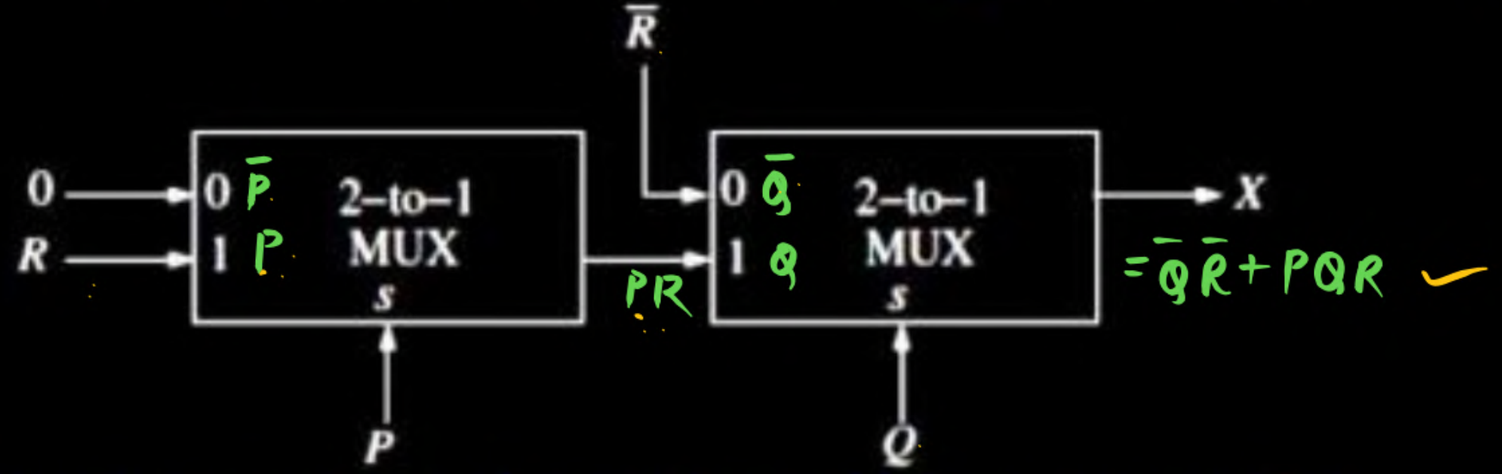
01 HW Discussion

02 PRACTICE

04 DISCUSSION

MCQ

Consider the two cascaded 2 to 1 multiplexers as shown in the figure.



The minimal sum of products form of the output X is

[GATE-2016-CS: M]

A $\overline{P}\overline{Q} + PQR$

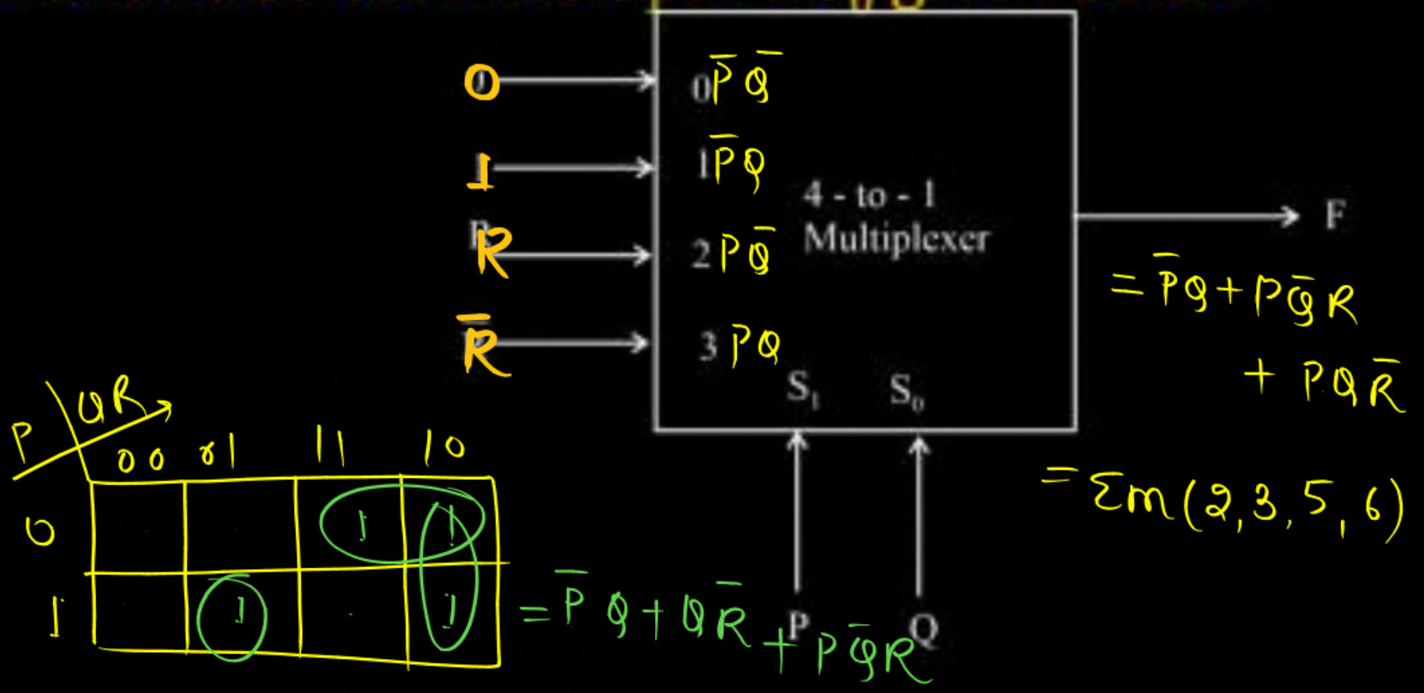
B $\overline{P}$Q+QR

C PQ+ $\overline{P}\overline{Q}$R

D $\overline{Q}\overline{R}$ +PQR

MCQ

Consider the 4–to–1 multiplexer with two select lines S_1 and S_0 given below.



The minimal sum–of–products form of the Boolean expression for the output F of the multiplexer is

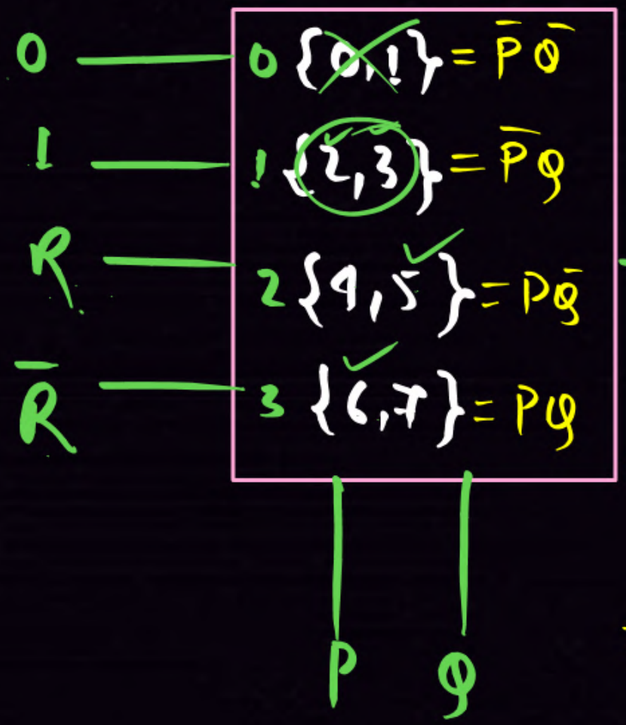
GATE-2014-CS:2M

(A) $\bar{P}Q + Q\bar{R} + P\bar{Q}R$

(B) $\bar{P}Q + \bar{P}Q\bar{R} + PQ\bar{R} + P\bar{Q}R$

(C) $\bar{P}QR + \bar{P}Q\bar{R} + Q\bar{R} + P\bar{Q}R$

(D) $PQ\bar{R}$



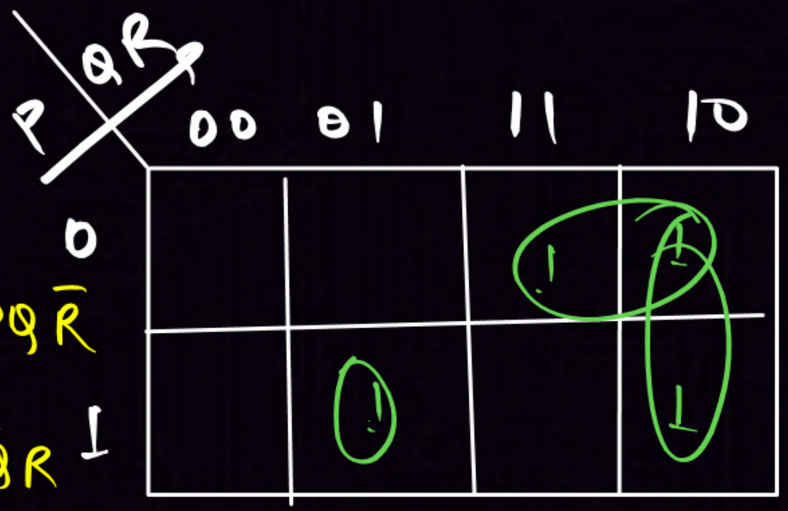
$f(P,Q,R)$

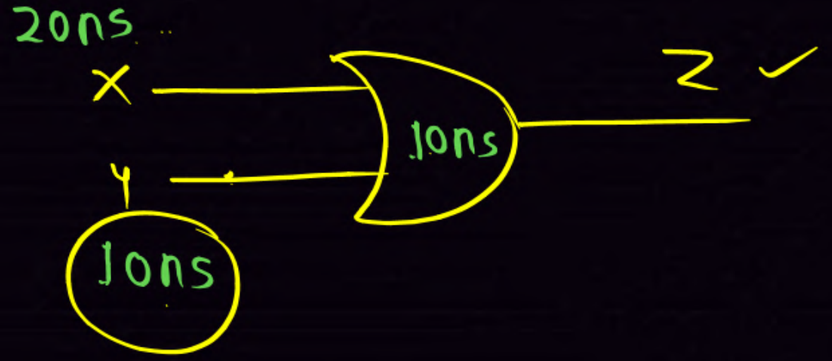
$= \bar{P}Q + P\bar{Q}R + PQ\bar{R}$

$= \bar{P}Q(\bar{R}+R) + P\bar{Q}R + PQ\bar{R}$

$= \bar{P}Q\bar{R} + \bar{P}QR + P\bar{Q}R + PQ\bar{R}$

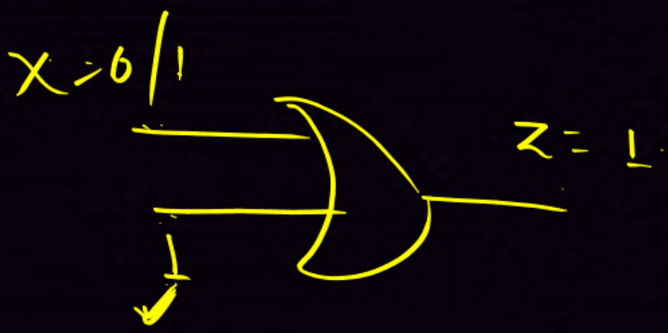
$= \Sigma m(2,3,5,6)$





minimum = 20ns

Maximum = 30ns

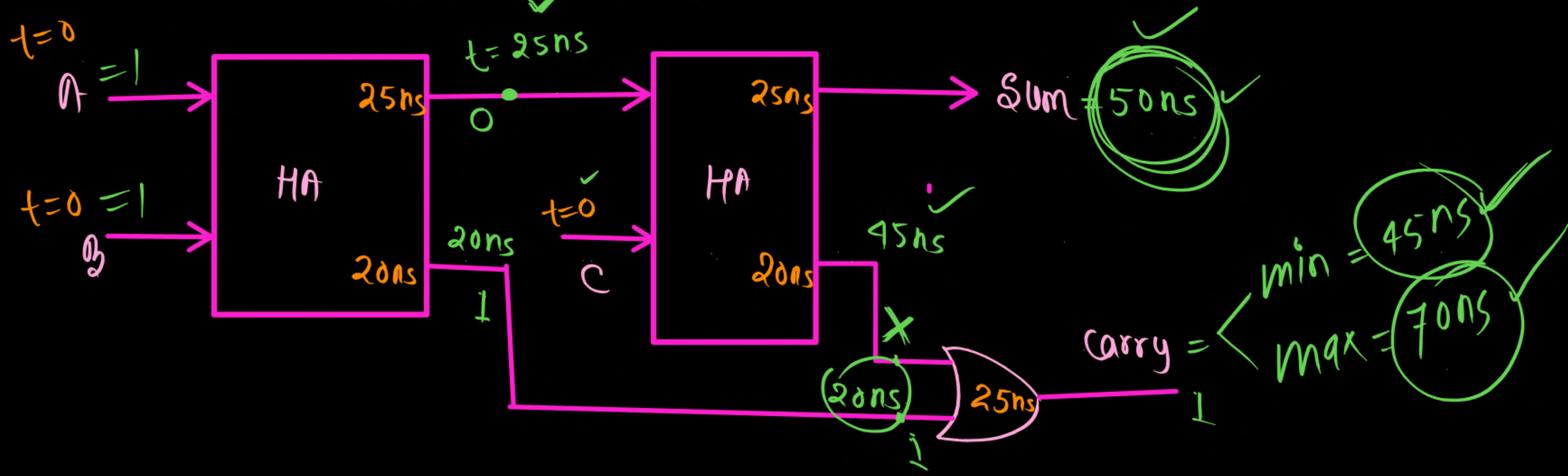


Q.1

$T_{sum} = 25ns$ $T_{carry} = 20ns$ $T_{OR} = 25ns$

A full adder is implemented with two half adders and one OR gate. OR gate is used to derive the final carry function of full adder. In each half adder, T_{sum} = 25 ns and T_{carry} = 20 ns and T_{OR} = 25 ns. The minimum time required to derive both the sum and carry function of a full adder after applying the inputs is ____ ns

50ns



$T_{sum} = 50ns$ ✓

$t_{carry} = 45ns$

$T_{min} = 50ns$.

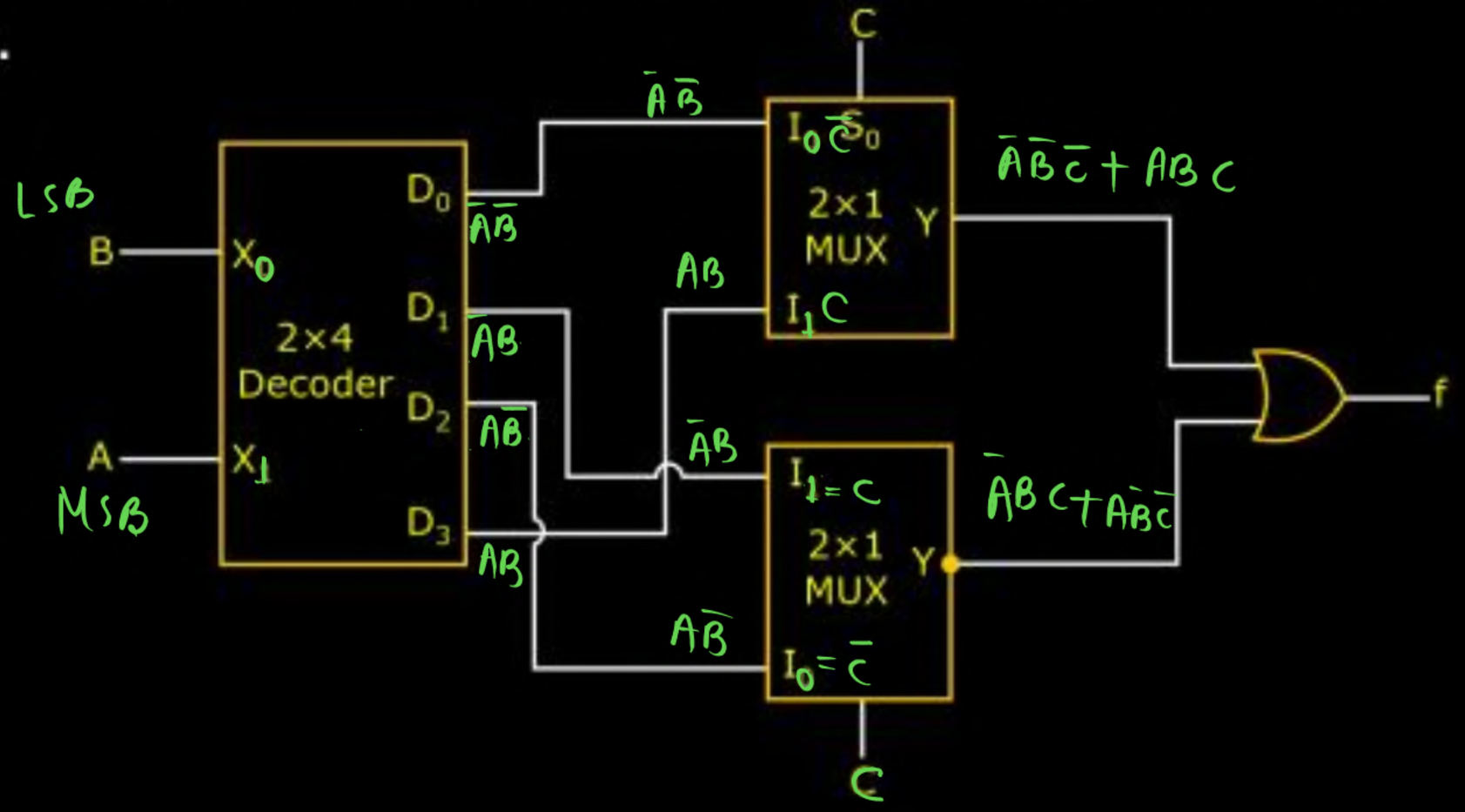
$T_{sum} = 50ns$

$T_{max} = 70ns$

$T_{carry} = 70ns$ ✓

Q.2

A logic function 'f' is implemented by the circuit shown in the figure below. The circuit consists of one 2×4 decoder, two 2×1 multiplexers and a two input or gate connected in cascade. Then the function f is equal to.



(A) $A \oplus B$

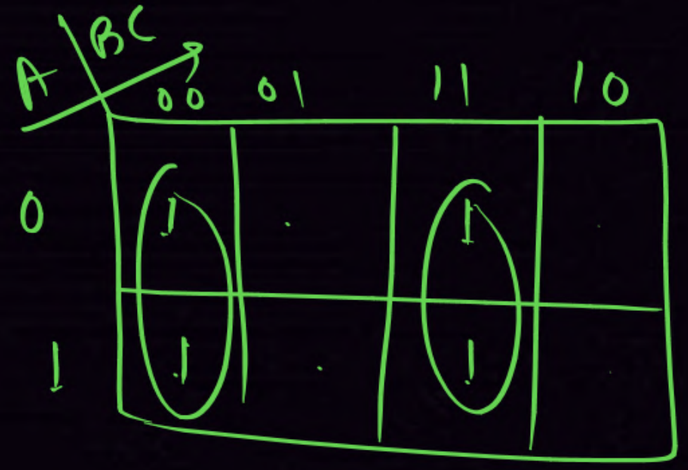
(B) $A \oplus B \oplus C$

(C) $B \odot C$

(D) $A \odot B$

$$f = \bar{A}\bar{B}\bar{C} + ABC + \bar{A}BC + A\bar{B}\bar{C}$$

$$= \Sigma m(0, 3, 4, 7)$$



$$\bar{B}\bar{C} + BC = B \odot C$$

Q.4

The combinational circuit given below implements which of the following

A NOR gate

B XOR gate

C NAND gate

D None of these

$f = \overline{BC} \cdot \overline{BC} + \bar{A} \cdot BC$

$BC = x$

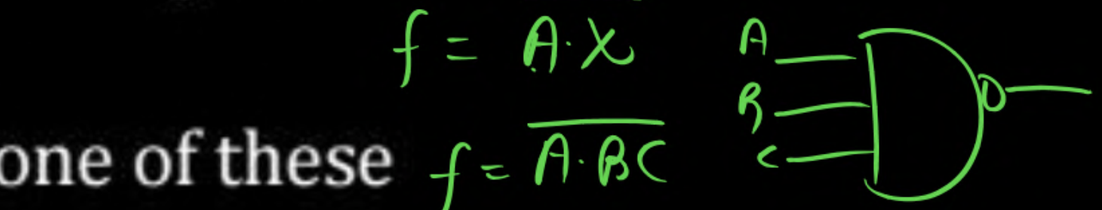
$f = \bar{x} + \bar{A}x$

$f = (\bar{x} + \bar{A}) \cdot (\bar{x} + x)$

$f = \bar{A} + \bar{x}$

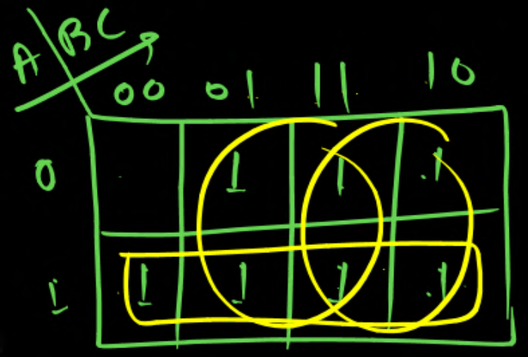
$f = \overline{A \cdot x}$

$f = \overline{A \cdot BC}$

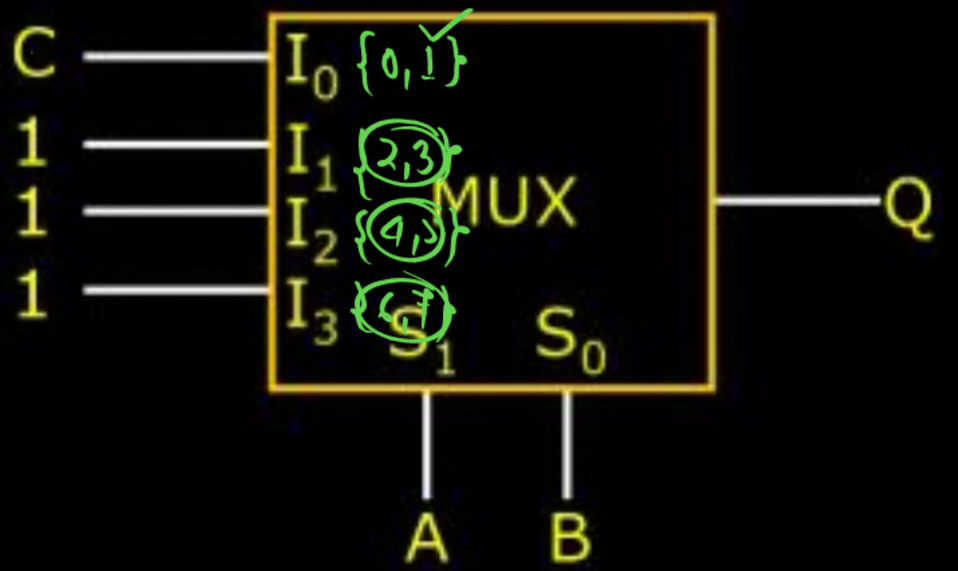


Q.5

The combinational logic circuit shown in the given figure has an output Q which is



A + B + C

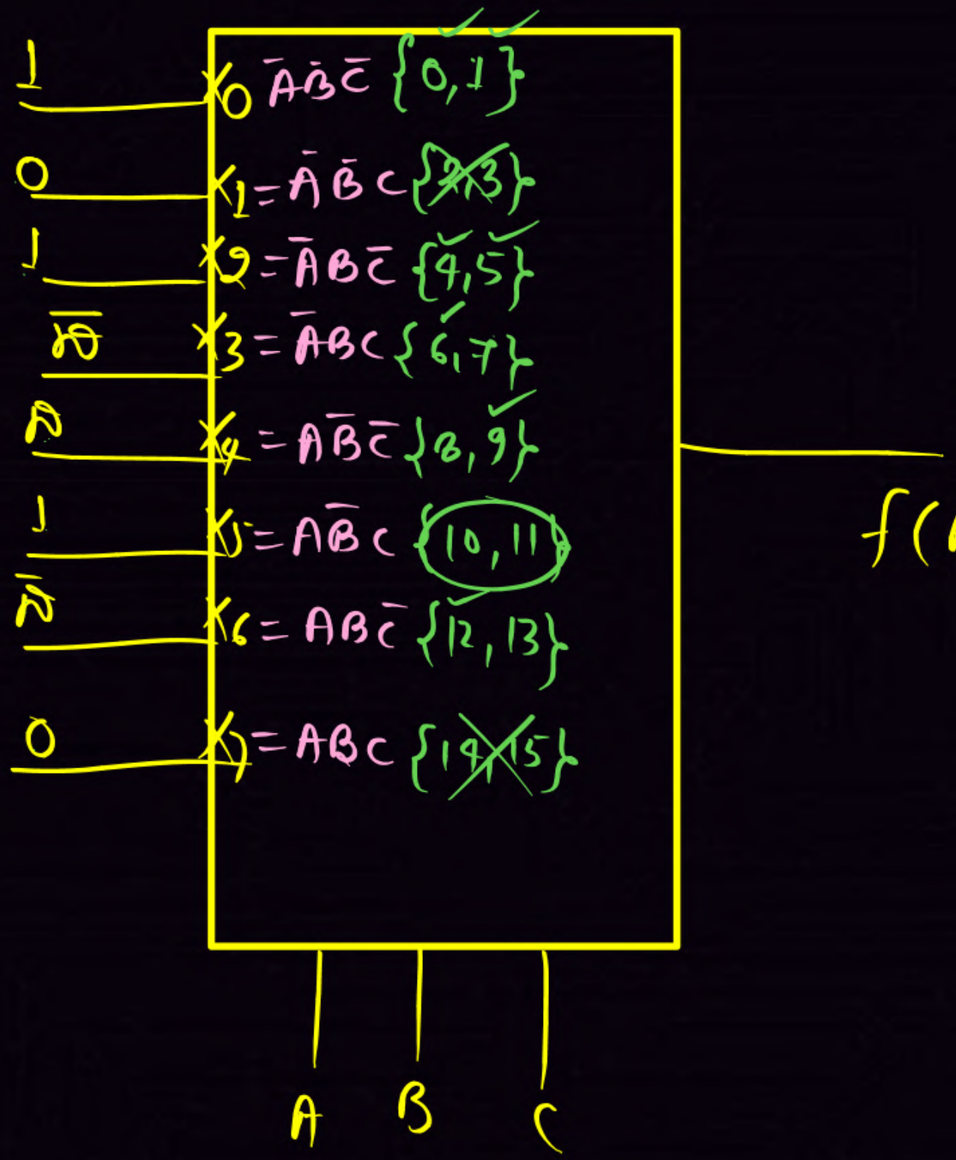


(A) ABC

(B) A + B + C

(C) $A \oplus B \oplus C$

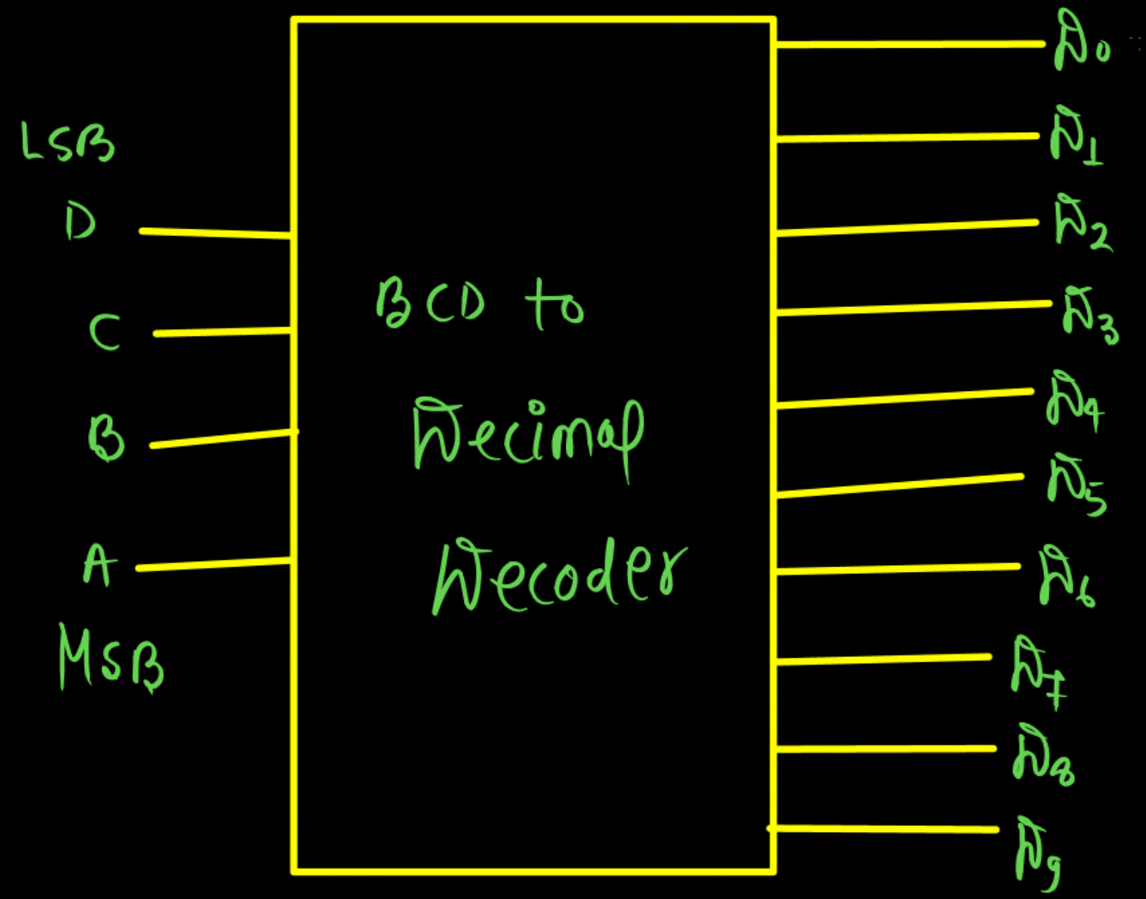
(D) A.B + C



$$f(A,B,C,D) = \Sigma m(0,1,4,5,6,9,10,11,12)$$

Questions Practice

BCD to Decimal

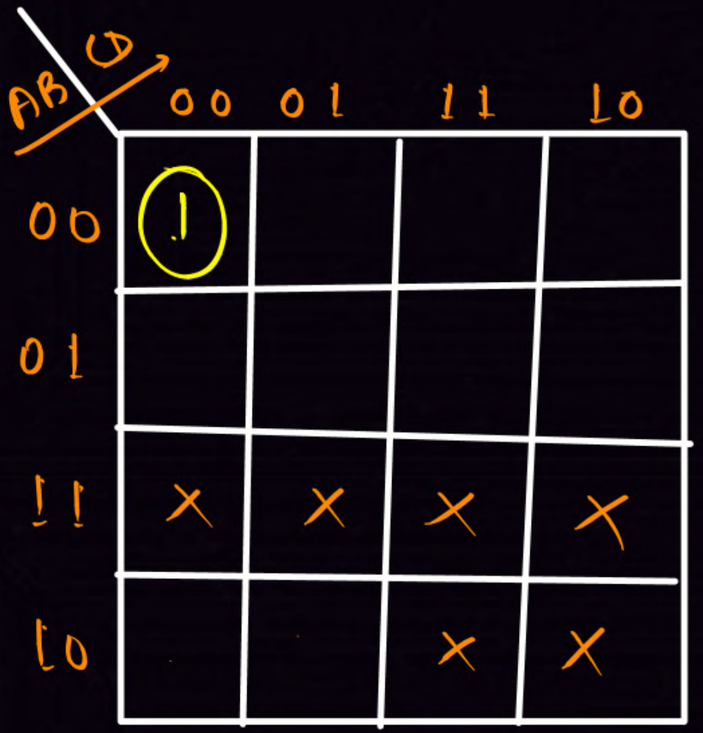


A	B	C	D	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0

$$P_0(A,B,C,D) = \Sigma m(0) + \Sigma d(10,11,12,13,14,15)$$

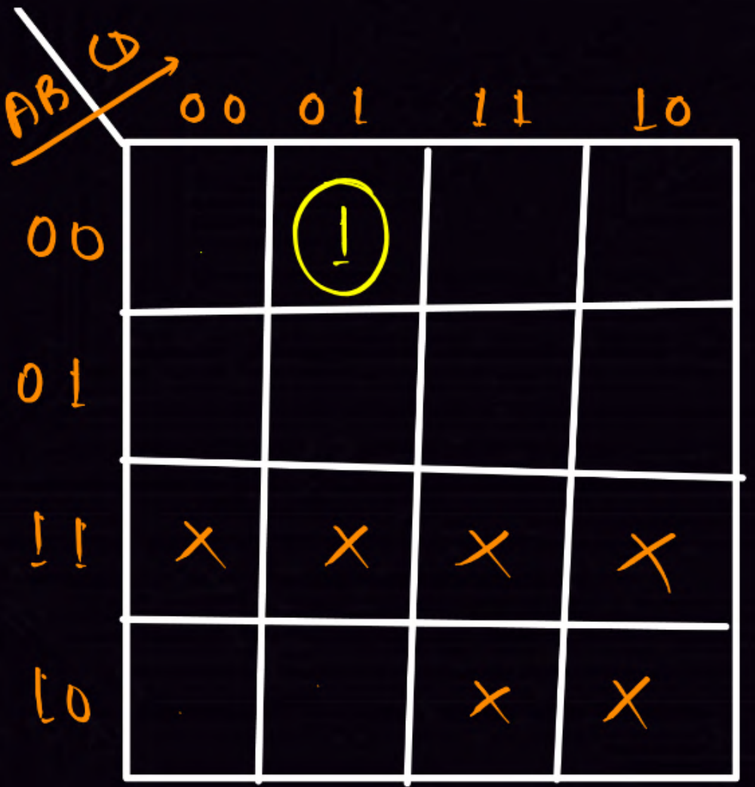
$$P_1(AB,C,D) = \Sigma m(1) + \Sigma d(10,11,12,13,14,15)$$

FOR D_0



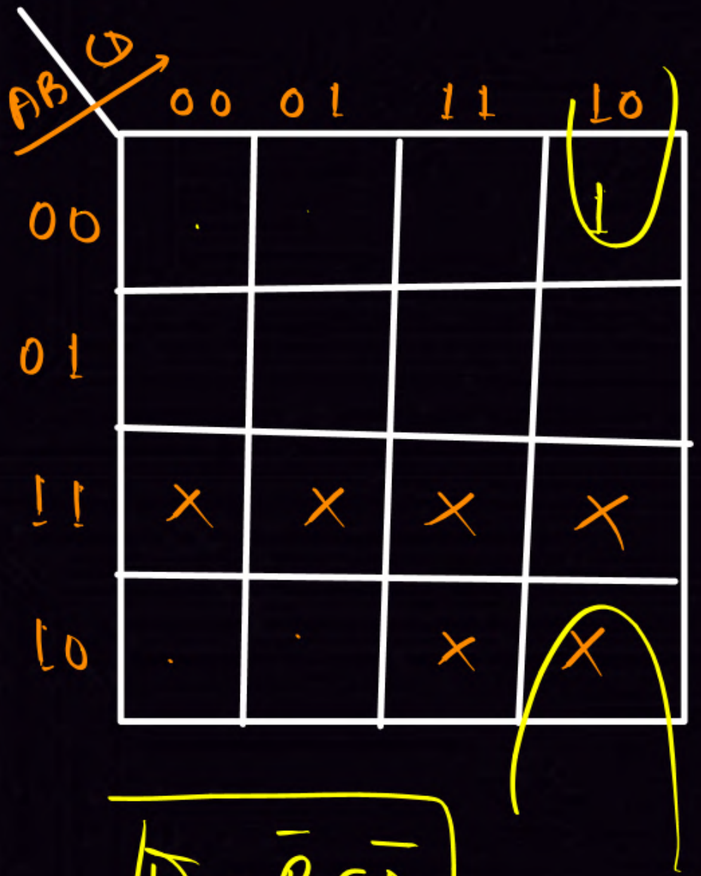
$$D_0 = \bar{A}B\bar{C}\bar{D}$$

FOR D_1



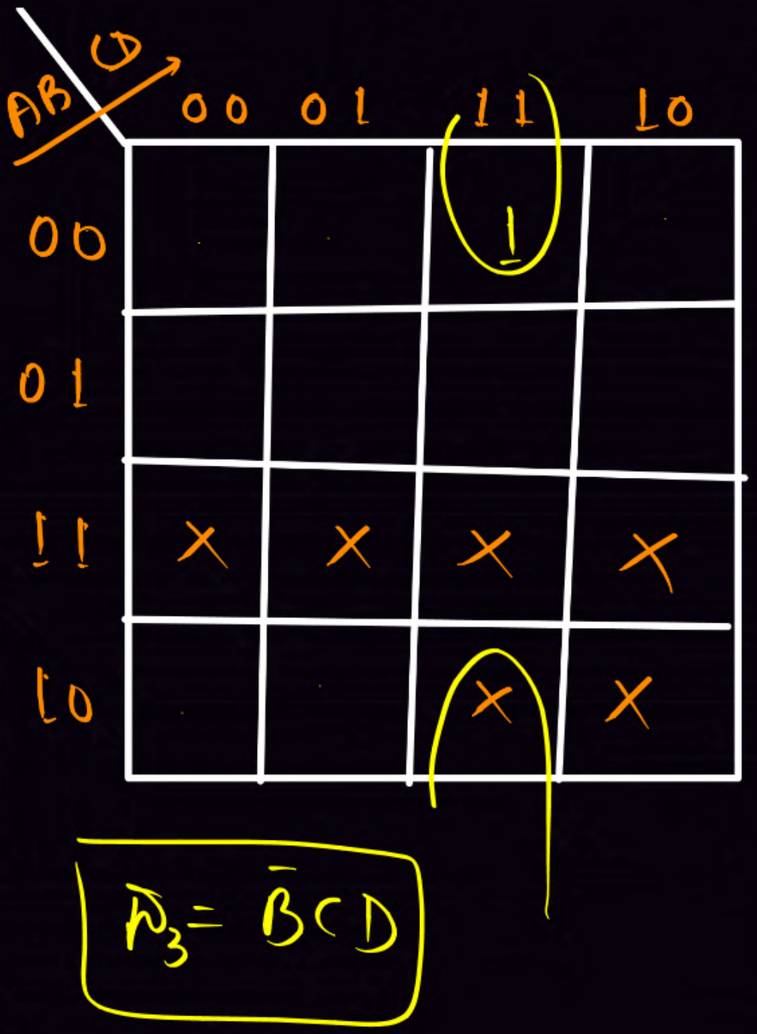
$$D_1 = \bar{A}B\bar{C}D$$

FOR A_2



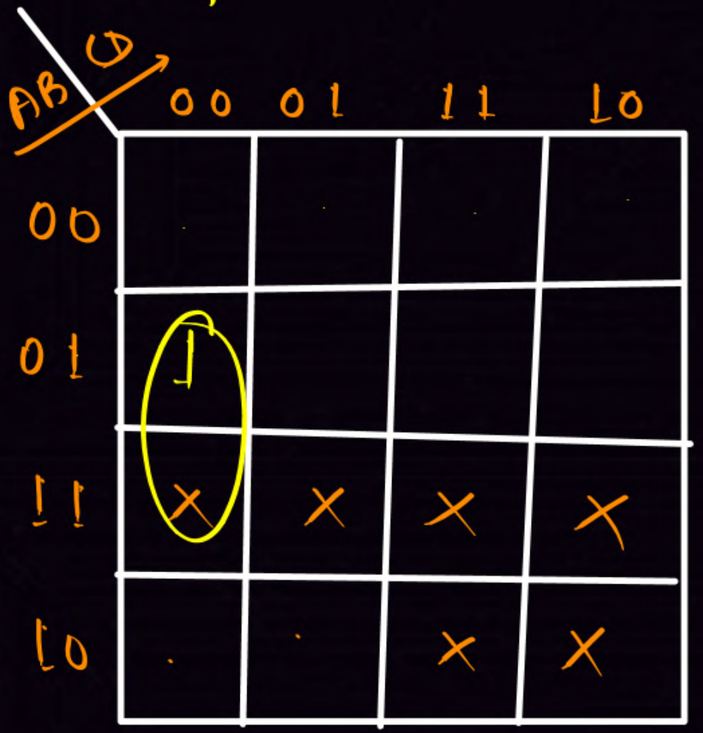
$A_2 = \bar{B}C\bar{D}$

FOR A_3



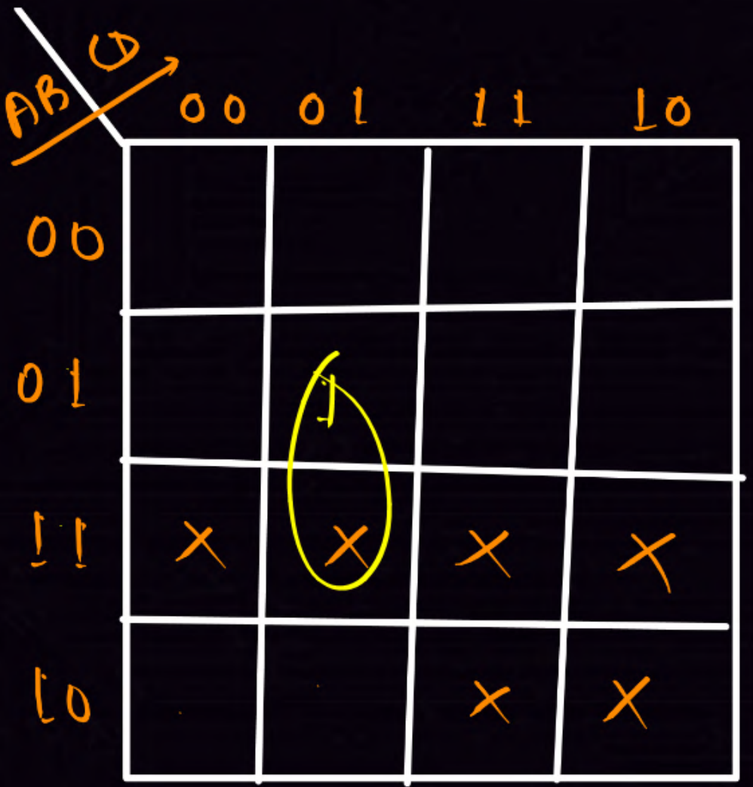
$A_3 = \bar{B}CD$

FOR W_4



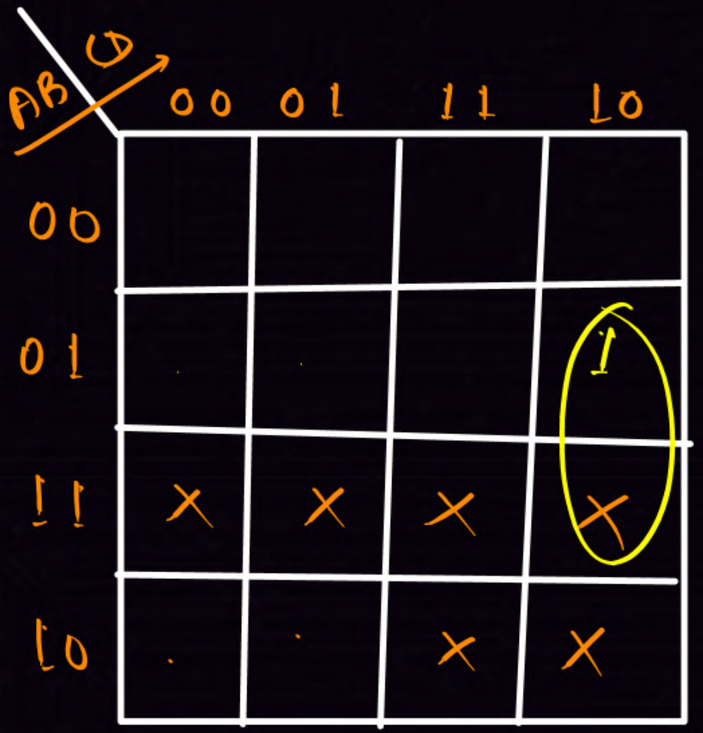
$$W_4 = B\bar{C}\bar{D}$$

For W_5



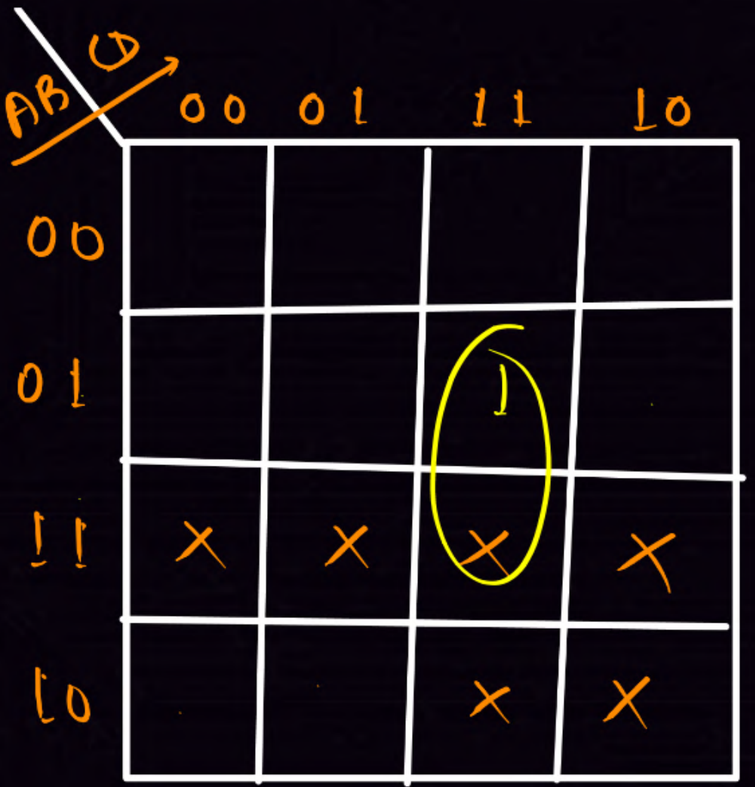
$$W_5 = B\bar{C}D$$

FOR D_6



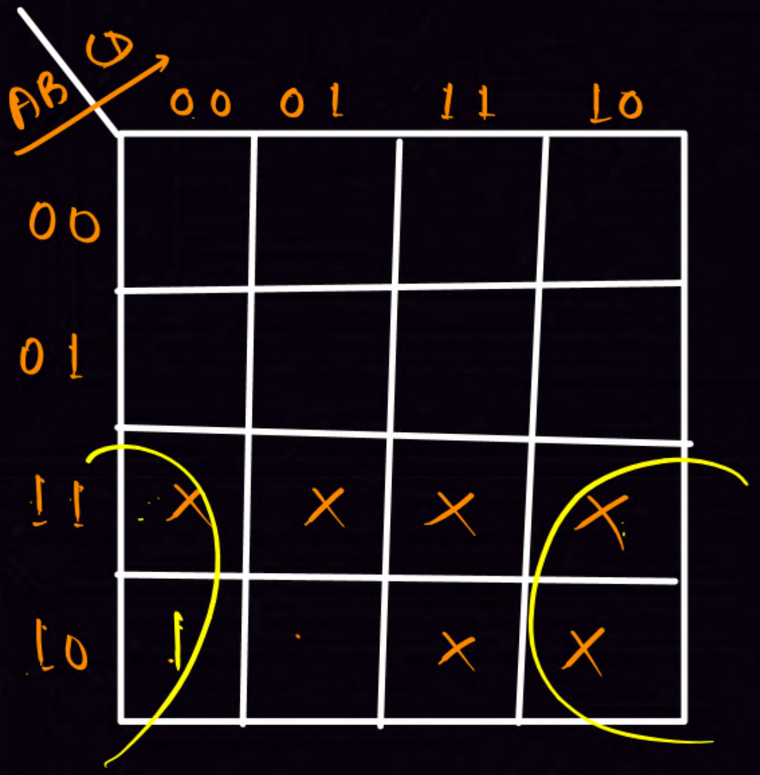
$D_6 = B\bar{C}\bar{D}$

For D_7



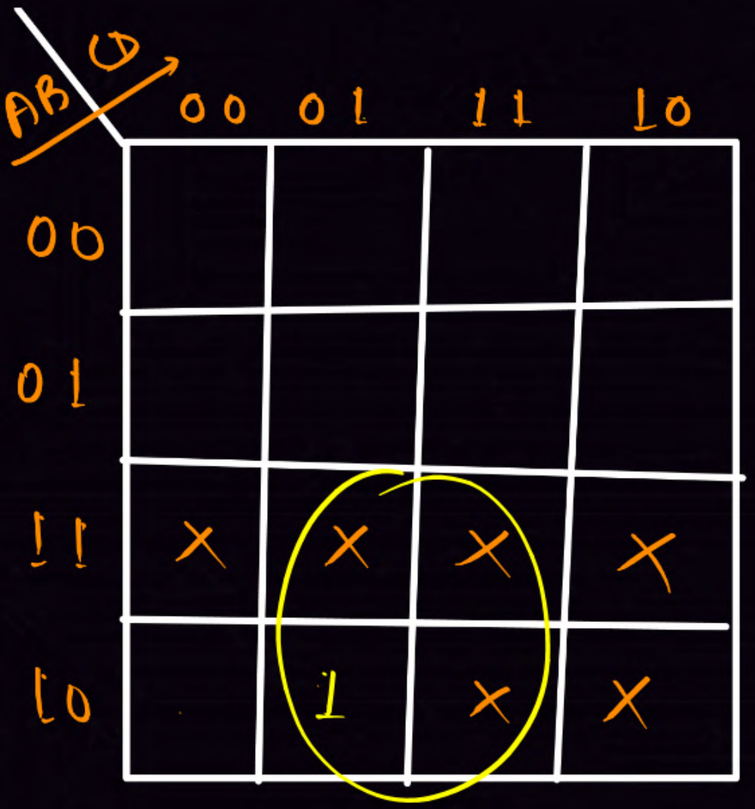
$D_7 = BCD$

FOR D_8



$D_8 = A\bar{D}$

For D_9



$D_9 = AD$

$D_0 = \bar{A}\bar{B}\bar{C}\bar{D}$

$D_1 = \bar{A}\bar{B}\bar{C}D$

$D_2 = \bar{B}C\bar{D}$

$D_3 = \bar{B}CD$

$D_4 = B\bar{C}\bar{D}$

$D_5 = B\bar{C}D$

$D_6 = BC\bar{D}$

$D_7 = BCD$

$D_8 = A\bar{D}$

$D_9 = AD$

AB \ CD	00	01	11	10
00	D_0	D_1	D_3	D_2
01	D_4	D_5	D_7	D_6
11	X	X	X	X
10	D_8	D_9	X	X

Thank you

GW

Soldiers !