CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

IO Organization

Lecture No.- 02

By- Vishvadeep Gothi sir

Recap of Previous Lecture

- **Topic** Peripheral Device
- **Topic** IO vs Memory Buses
- **Topic** Memory Mapped IO vs IO Mapped IO
- **Topic** Asynchronous Data Transfer

Topics to be Covered

- **Topic** Modes of Transfer
- **Topic** Programmed IO
- **Topic** Interrupt IO

Topic : Modes of Transfer

1. Programmed I/O or Program Controlled I/O
2. Interrupt Initiated I/O or Interrupt Driven I/O

→ transfer b/w CPU & I/O

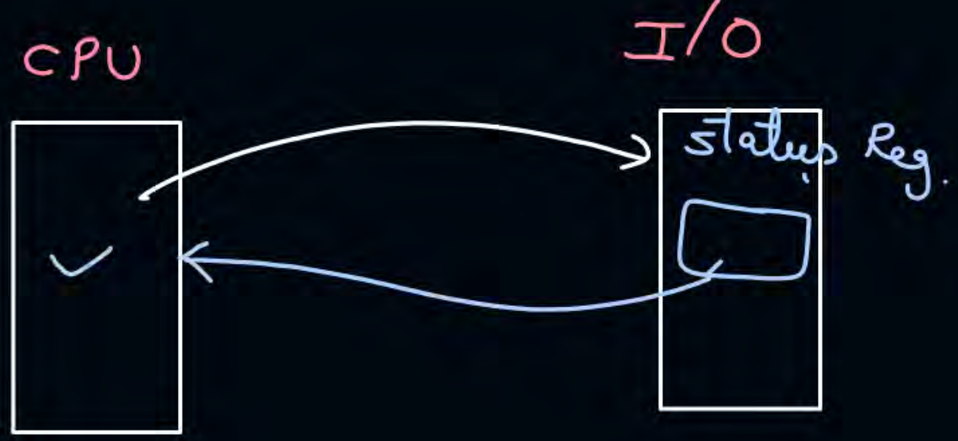
3. Direct memory Access (DMA) → transfer b/w memory & I/O

Topic : Programmed IO

- There is no any provision through which IO can inform to CPU about data transfer
- IO sets its own status and waits
- CPU runs program periodically and checks the status of each device one-by-one
- If any device has its status set then CPU performs data transfer for it.

Polling

Disadv:-
wastage of CPU time for checking status of devices periodically



Time needed by I/O device to send status Reg. to CPU

Total time required in data transfer = (time needed to check status of I/O device) + data transfer time

based on I/O speed

Topic : Interrupt Initiated IO

- IO device has a provision (Interrupt Signal) to inform to CPU about communication.

Topic : Interrupt Initiated IO

- IO device has a provision (Interrupt Signal) to inform to CPU about communication.
- When CPU receives interrupt:
  - It completes execution of current instruction
  - Saves the status (PC, PSW etc.) of current process onto the stack
  - Branches to service the interrupt PC = by the starting add. of that prog.
  - Resumes the previous process by taking out the values from stack

[MCQ] GATE_PYQ

QPTRS

#Q. The following are some events that occur after a device controller issues an interrupt while process L is under execution.

P. The processor pushes the process status of L onto the control stack

Q. The processor finishes the execution of the current instruction

R. The processor executes the interrupt service routine

S. The processor pops the process status of L from the control stack

T. The processor loads the new PC value based on the interrupt

Which of the following is the correct order in which the events above occur?

A QPTRS

B PTRSQ

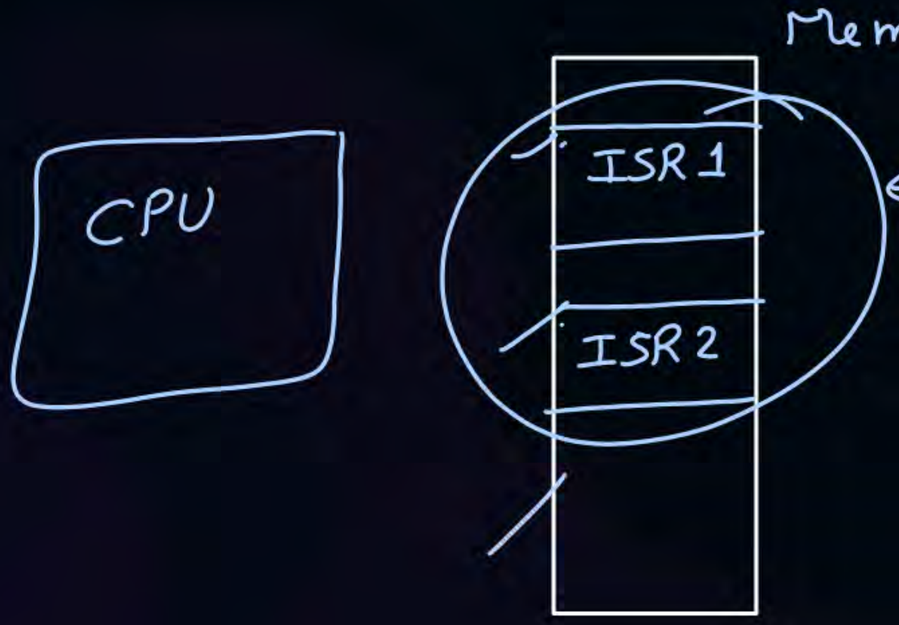
C TRPQS

D QTPRS

Topic : Interrupt Initiated IO

Interrupt Service Routine :-

A function, execution of which services the interrupt.



How CPU gets add. of ISR

Topic : Vectored vs Non-Vectored (scalar)

Device sends reference of ISR to CPU along with interrupt.

Device sends only interrupt
⇓
CPU runs Default Service Routine.
⇓
CPU obtains location of actual ISR by executing default service routine

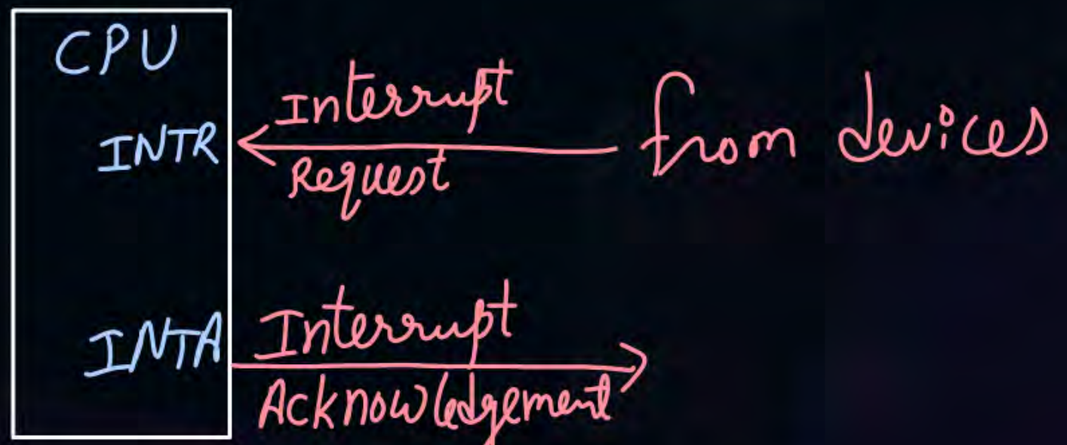
Topic : Maskable vs Non-Maskable

CPU can accept or can reject

CPU will always accept

CPU is not accepting interrupt

- Interrupt signal discarded
- Interrupt in pending



Topic : Internal Vs External

(Hardware)

software

Interrupt generated during inst^n execut^n due to some unexpected situat^n for inst^n execut^n.

generated by devices

All internal interrupts

- Non-maskable
- vectored

Topic : Simultaneous Interrupts

when multiple devices send interrupt simultaneously then CPU services interrupt of highest priority device first.

Priority based interrupt handling

- Software soln
- Hardware solution
  - Serial (daisy chaining)
  - Parallel

fixed priority of devices

Topic : Time Required in Interrupt IO

= Interrupt overhead time + Interrupt service time

[NAT]

#Q. Consider a CPU which takes 0.05 microseconds as interrupt overhead time when a device generates interrupt for CPU, and CPU accepts it. After that CPU takes 6 cycles to service the interrupt. If CPU runs on 10MHz clock rate then total time CPU spends for interrupt service is 0.65 microseconds?

$$\text{CPU cycle time} = \frac{1}{10\text{MHz}} = 0.1\ \mu\text{sec}$$

$$\text{Total time} = 0.05\ \mu\text{sec} + (6 * 0.1)\ \mu\text{s}$$

$$= 0.65\ \mu\text{sec}$$

[NAT]

H. W.

#Q. A device with data transfer rate 20 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 10 microsecond.

1. Total time required in programmed IO for 10 bytes data transfer?
2. Total time required in interrupt IO for 10 bytes data transfer?
3. What is the minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode?

2 mins Summary

Topic Modes of Transfer

Topic Programmed IO

Topic Interrupt IO

Happy Learning

THANK - YOU