CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Memory Organization

Lecture No.- 03

By- Vishvadeep Gothi sir

Recap of Previous Lecture

- **Topic** Memory Address Decoder
- **Topic** Main Memory: RAM, ROM
- **Topic** RAM Chip
- **Topic** ROM Chip

Topics to be Covered

Topic Multiple Chips in Single Memory System

Topic DRAM Refresh

Topic : Multiple Chips in Single Memory System

Total mem. capacity = no. of chips * 1 chip capacity

[NAT]

#Q. How many 64 bytes RAM chips are needed to provide a memory capacity of 1Kbytes?

$$= \frac{1\text{k bytes}}{64 \text{ bytes}}$$

$$= \frac{2^{10}}{2^6}$$

$$= 2^4 = \underline{\underline{16}} \text{ Ans.}$$

[NAT]

Ans = 8

#Q. Total memory capacity is ____ Mbytes, if we use 16 chips of size 512Kbytes each?

$= 16 * 512k$ bytes

$= 2^4 * 2^9 * 2^{10}$ bytes

$= 2^{23}$ bytes

$= 8$ M bytes

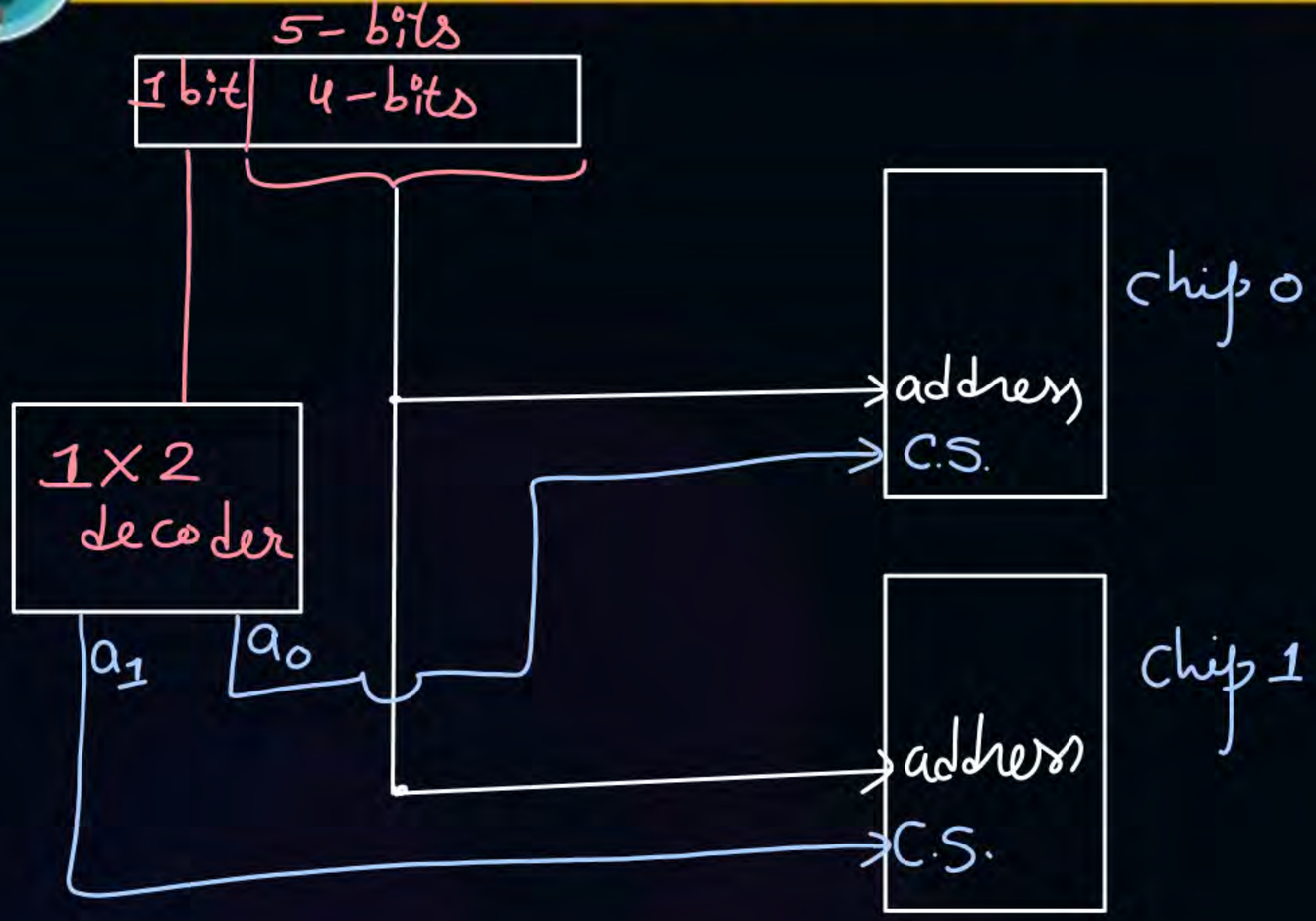
Topic : Multiple Chips in Single Memory System

ex:- A mem. system is built using 2 chips of size 16 bytes each.

chip 0 ⇒ 16×8 bits ⇒ 4 bits
chip 1 ⇒ 16×8 bits ⇒ 4 bits
Total ⇒ 32×8 bits ⇒ 5 bits

	5 bits address range
$(0)_{10}$	00000
	⋮
$(15)_{10}$	01111
$(16)_{10}$	10000
	⋮
$(31)_{10}$	11111

Topic : Multiple Chips in Single Memory System



vertical arrangement of chips

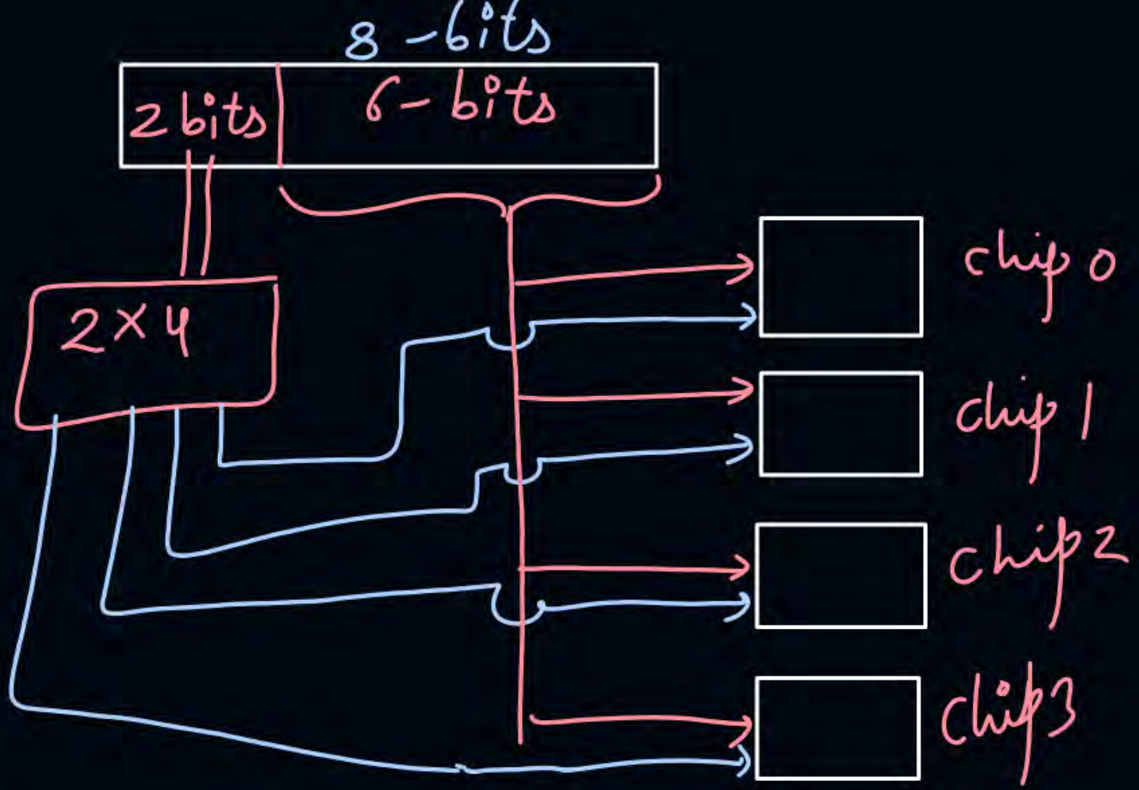
⇓

when no. of addresses required more than addresses one chip

ex:- ②

4 chips of size 64 x 8 bits (64 bytes) ⇒ add. = 6-bits

Total capacity = 4 * 64 = 256 bytes ⇒ add. = 8 bits



[NAT]

2^7 — 1 byte

#Q. (a) How many 128×8 bits RAM chips are needed to provide a memory capacity of 2048 bytes?

2^{11} B

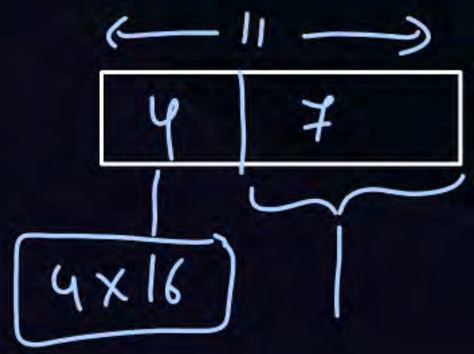
(b) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?

(c) How many lines must be decoded for chip select? Specify the size of decoder?

a) no. of chips $= \frac{2048\ B}{128\ Bytes} = \frac{2^{11}}{2^7} = 2^4 = 16$

b) add. = 11 lines

Common = 7 lines



c. 4 lines go for chip select decoder

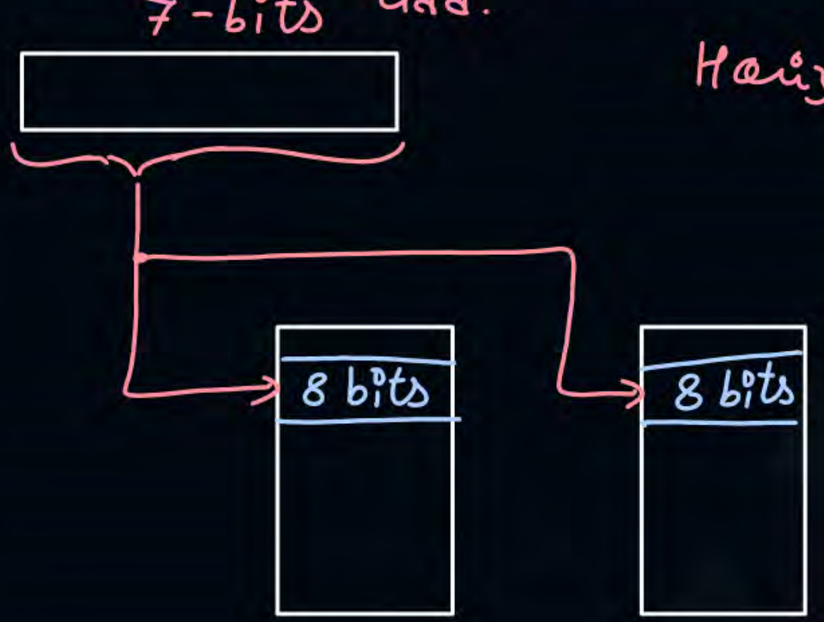
Decoder size = 4×16

[NAT]

#Q. How many 128×8 bits RAM chips are needed to provide a memory capacity of 128 ×16 bits?

$$= \frac{\cancel{128} \times \overset{2}{\cancel{16}} \text{ bits}}{\cancel{128} \times \cancel{8} \text{ bits}}$$

= 2 chips



Horizontal arrangement

⇓

when data per address is required more than the one chip data per address.

[NAT]

#Q. How many 128×8 bits RAM chips are needed to provide a memory capacity of 256×16 bits?

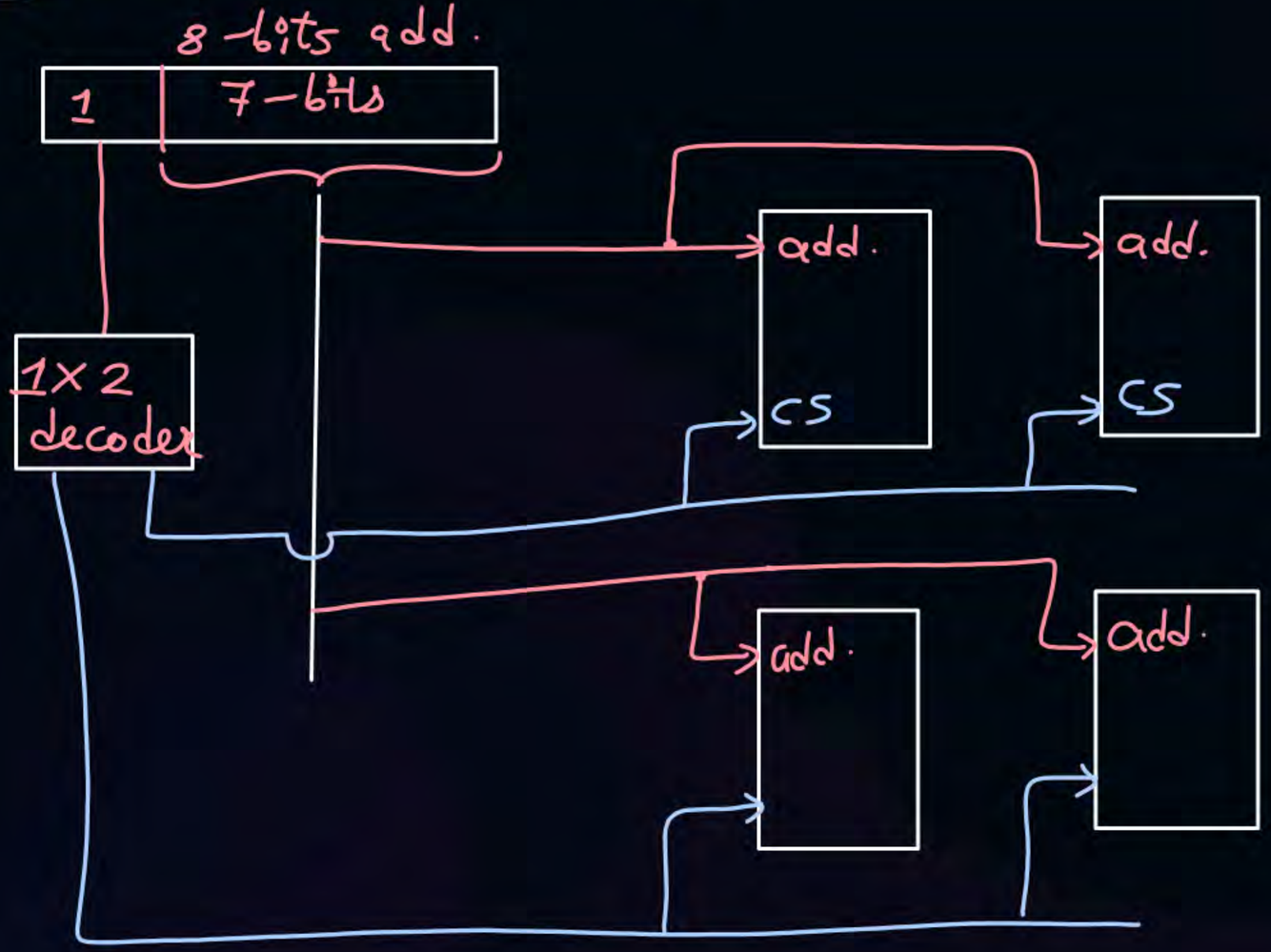
$$= \frac{256 \times 16}{128 \times 8} = 4 \text{ chips}$$

for mem 256×16 bits,
CPU generates add. = 8 bits

for chip 128×8 bits, each chip
can understand add. = 7 bits

Topic : Solution

Hybrid arrangement



[MCQ] GATE- 2009

#Q. How many 32K × 1 RAM chips are needed to provide a memory capacity of 256K bytes?

A 8

B 32

C ✓ 64

D 128

$$= \frac{256K \text{ bytes}}{32k \times 1 \text{ bit}}$$

$$= \frac{2^8 * 8 \text{ bits}}{2^5 * 1 \text{ bits}}$$

$= 64$ → chip arrangement (hybrid)

Note :-
default storage unit is bits

Topic : DRAM Refresh

In single refresh time entire row of cells can be refreshed.

1 chip refresh time = No. of rows of cells * 1 refresh time

n- chip refresh time = 1 chip refresh time

(entire mem. system)

because each chip can be refreshed in parallel to other chip.

Note:- during refresh, read/write can not be done in DRAM.

ex:-

% of time available for Read/write $= \frac{18}{20} * 100\%$

$= 90\%$

[NAT]

#Q. Consider a DRAM which can be refreshed in 10ns. The refresh period is 0.05 microseconds. $= 50\,ns$

1. % of time taken in refresh? $\frac{10}{50} * 100\% = 20\%$
2. % of time remaining for read write is? $\frac{40}{50} * 100\% = 80\%$

[MCQ] GATE- 2010 PYQ

#Q. A main memory unit with a capacity of 4 megabytes is built using 1M × 1-bit DRAM chips. Each DRAM chip has 1K rows of cells with 1K cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is?

total refresh time = 1k * 100 ns

A 100 nanoseconds

B ✓ 100×2^{10} nanoseconds

C 100×2^{20} nanoseconds

D 3200×2^{20} nanoseconds

[NAT]

17.00.

#Q. A 32–bit wide main memory unit with a capacity of 1 GB is built using 256M X 4-bit DRAM chips. The number of rows of memory cells in the DRAM chip is 2^{14}. The time taken to perform one refresh operation is 50 nanoseconds. The refresh period is 2 milliseconds. The percentage (rounded to the closet integer) of the time available for performing the memory read/write operations in the main memory unit is _____?

[NAT]

H.W.

#Q. A DRAM chip of $256K \times 8$ bits has x rows of cells with y cells in each row? If DRAM takes 20ns for 1 refresh and 2.56 milliseconds for entire chip refresh then the value of x + y is _____?

2 mins Summary

Topic Multiple Chips in Single Memory System

Topic DRAM Refresh

Happy Learning

THANK - YOU