CS & IT ENGINEERING

DIGITAL LOGIC

Combinational Circuit

Lecture No. 5

By- CHANDAN SIR

01 DECODER

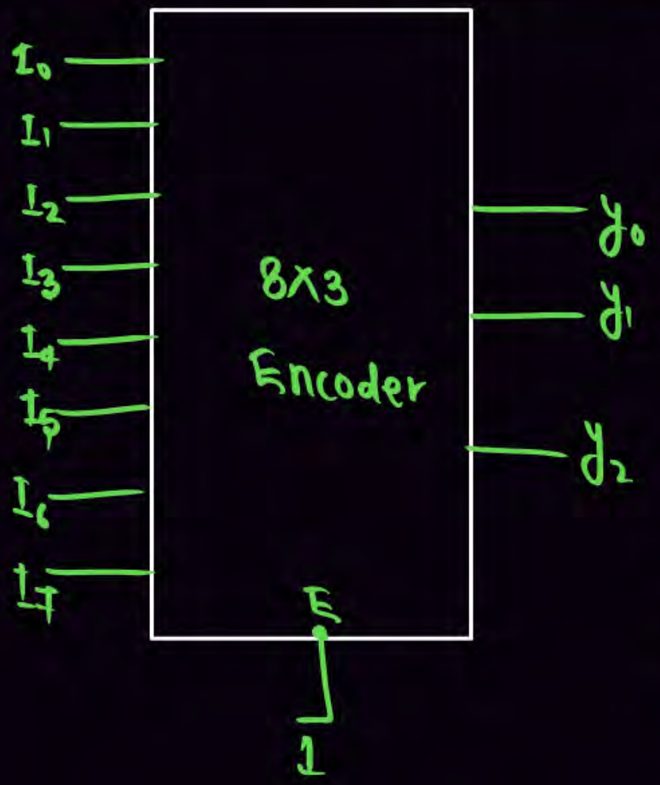
02 Question Practice

03 HA

04 FA

05 Discussion

8X3 Encoder

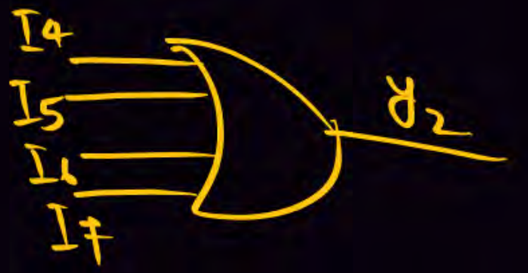


I7	I6	I5	I4	I3	I2	I1	I0	y2	y1	y0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

$$y_2 = \bar{I}_4 + \bar{I}_5 + \bar{I}_6 + \bar{I}_7$$

$$y_1 = \bar{I}_2 + \bar{I}_3 + \bar{I}_6 + \bar{I}_7$$

$$y_0 = \bar{I}_1 + \bar{I}_3 + \bar{I}_5 + \bar{I}_7$$



LSB Priority Encoder :→

MSB LSB

I_3	I_2	I_1	I_0	y_1	y_0
X	X	X	1	0	0
X	X	1	0	0	1
X	1	0	0	1	0
1	0	0	0	1	1

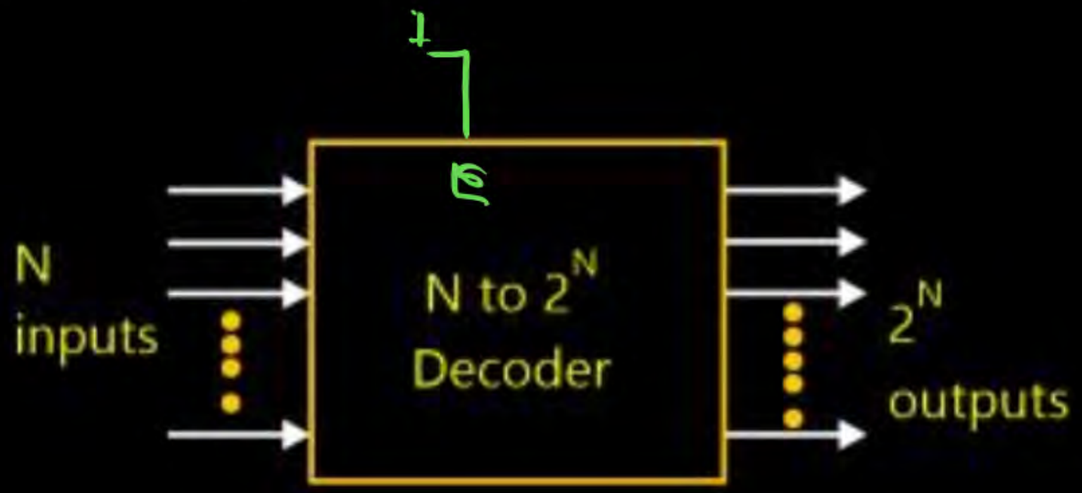
DECODER, HA, FA

Decoder :→ A circuit which is use to convert Binary into any other code are called Decoder

DECODER, HA, FA

DECODER

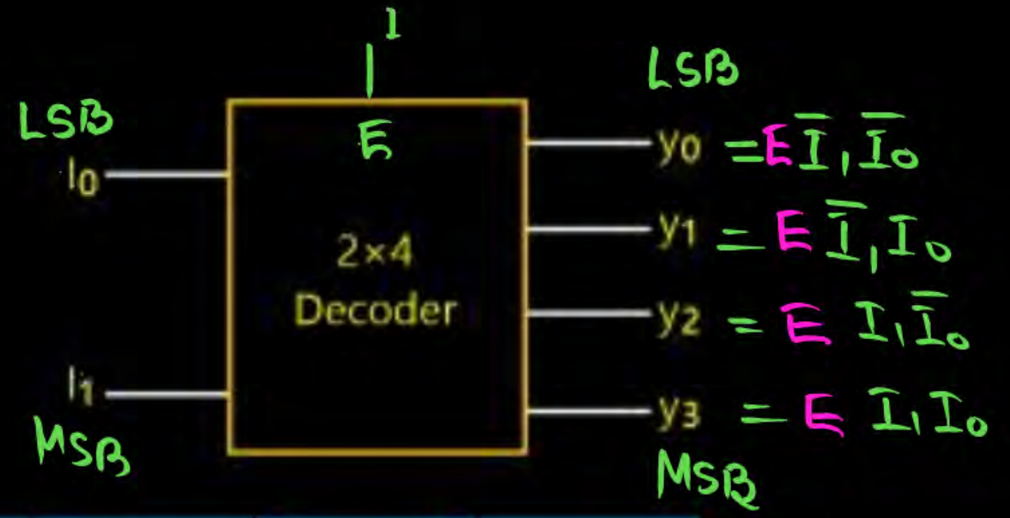
1. 2 × 4 Decoder
2. 3 × 8 Decoder
3. 4 × 16 Decoder



DECODER, HA, FA

2 × 4 DECODER

Step 1.



Step 2.

I_1	I_0	y_3	y_2	y_1	y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

DECODER, HA, FA

2 × 4 DECODER

$y_0 = \bar{I}_1 \bar{I}_0$

$y_1 = \bar{I}_1 I_0$

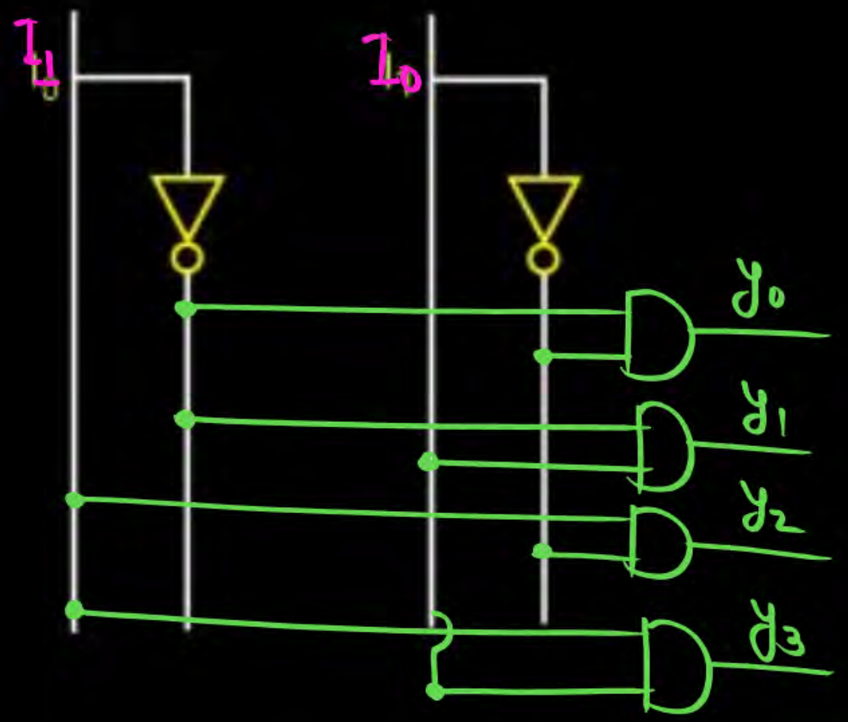
$y_2 = I_1 \bar{I}_0$

$y_3 = I_1 I_0$

Step 3.

Step 4. Minimization

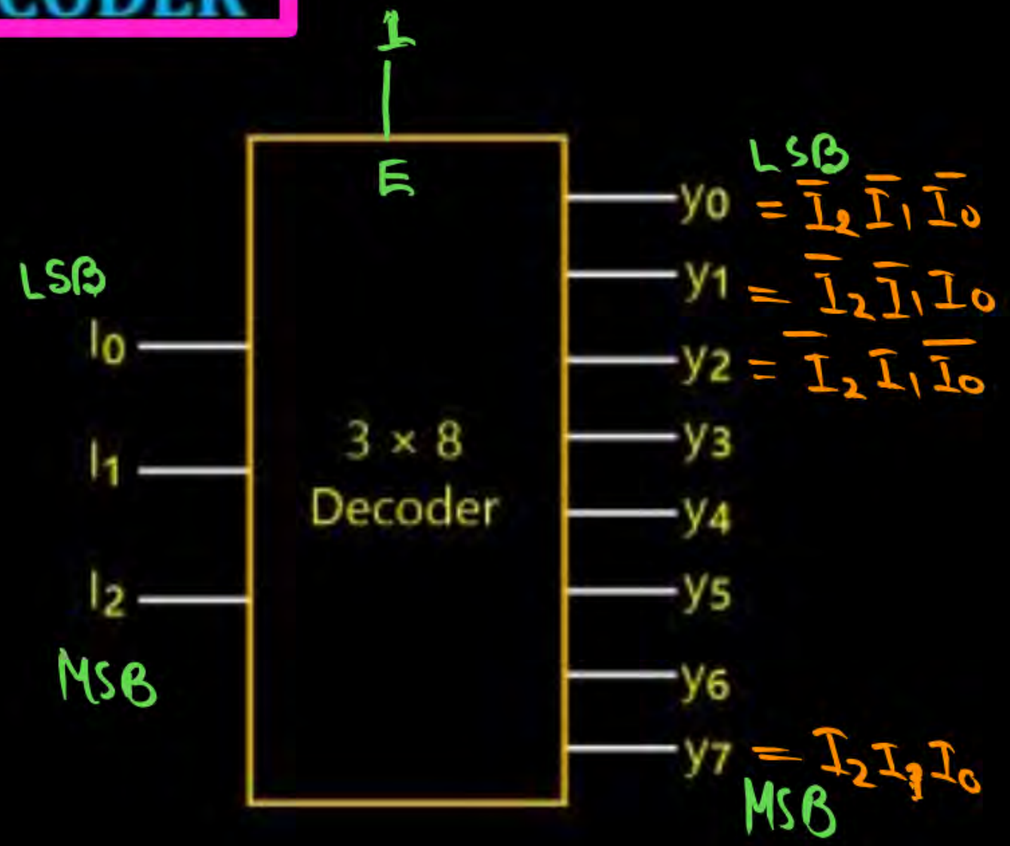
Step 5. Hardware Implementation



DECODER, HA, FA

3 × 8 DECODER

Step 1.



DECODER, HA, FA

3 × 8 DECODER

Step 2.

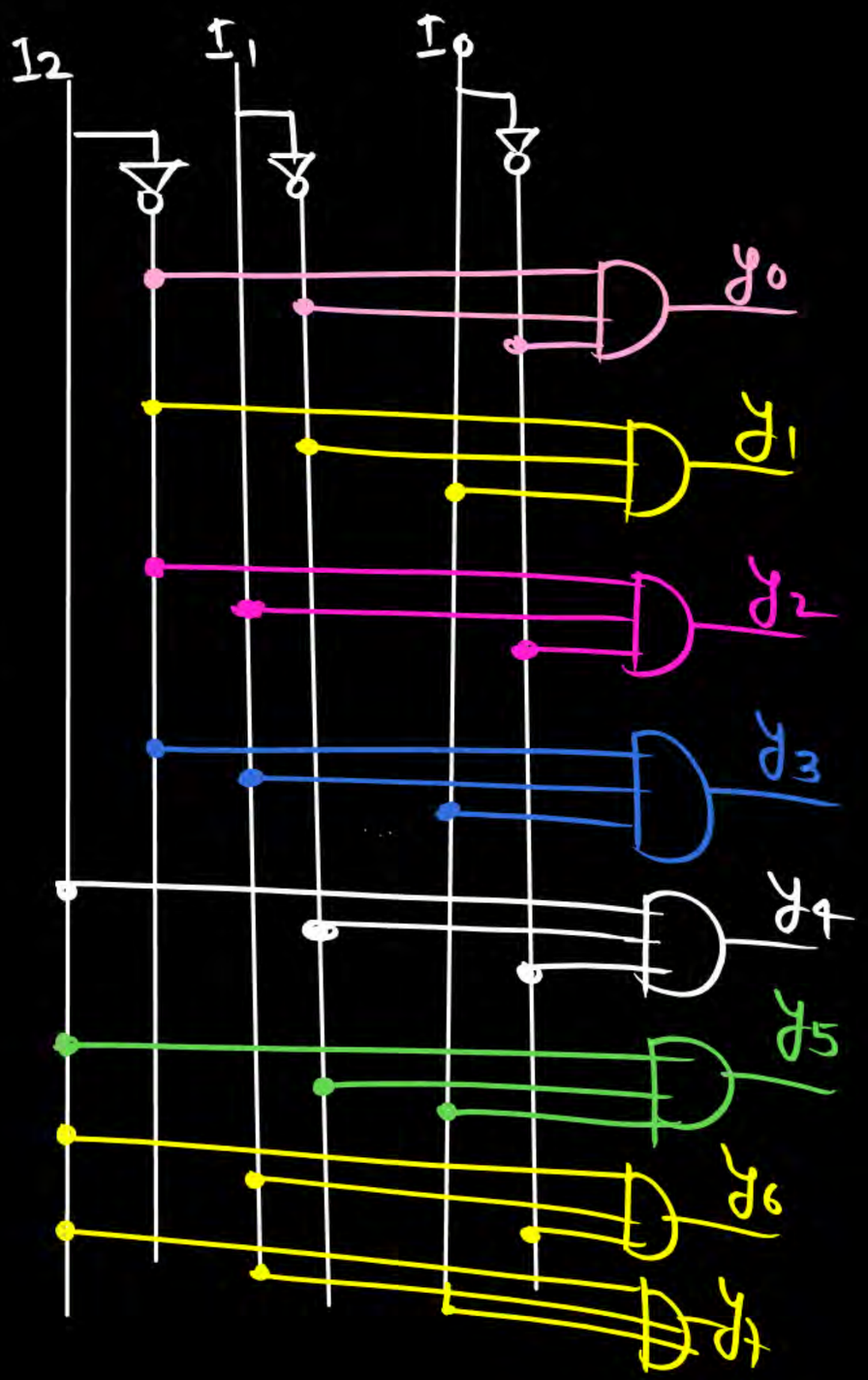
I_2	I_1	I_0	y_7	y_6	y_5	y_4	y_3	y_2	y_1	y_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

DECODER, HA, FA

3 × 8 DECODER

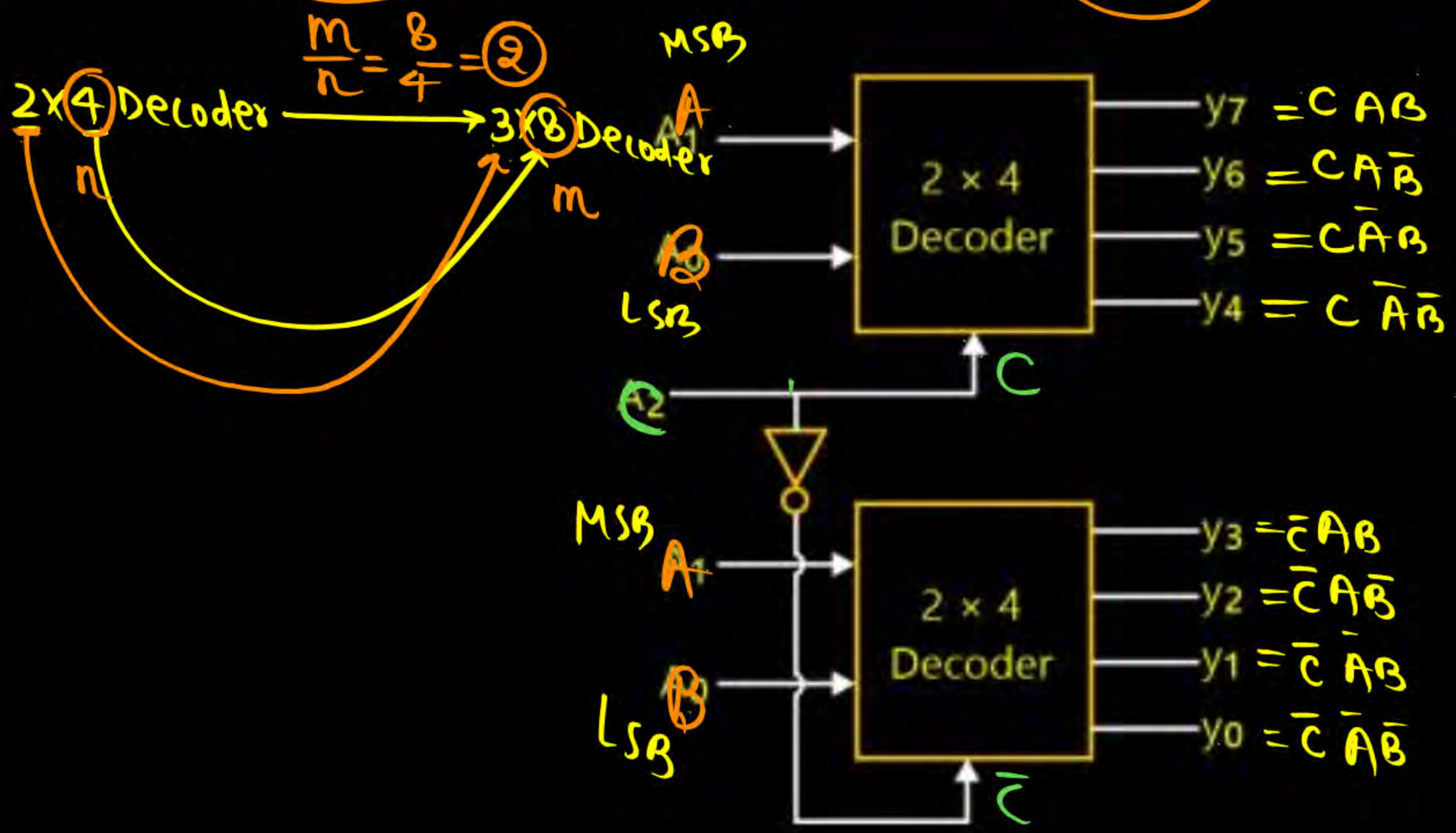
Step 4. Minimization

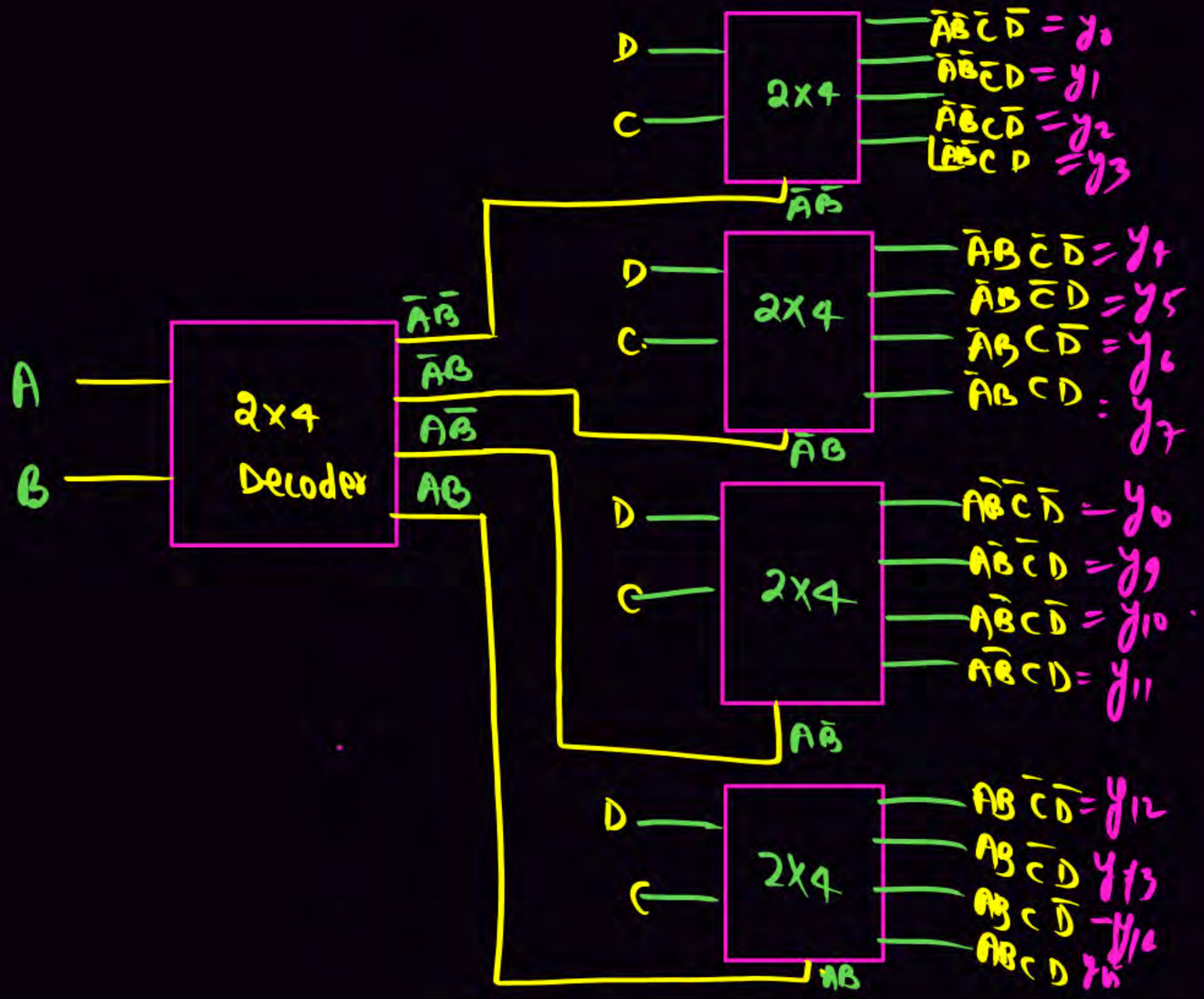
Step 5. Hardware Implementation

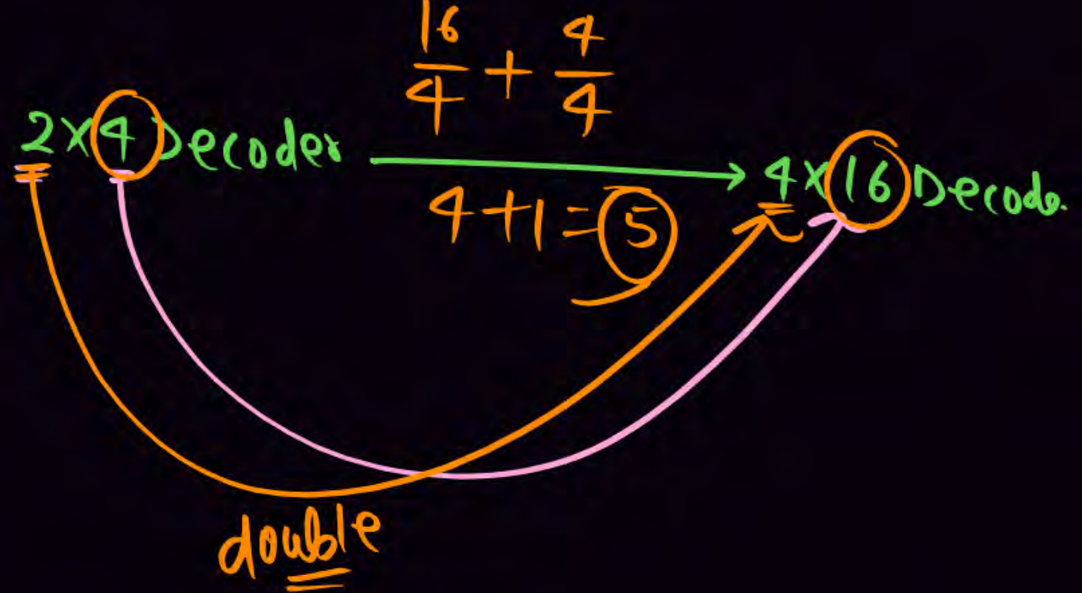


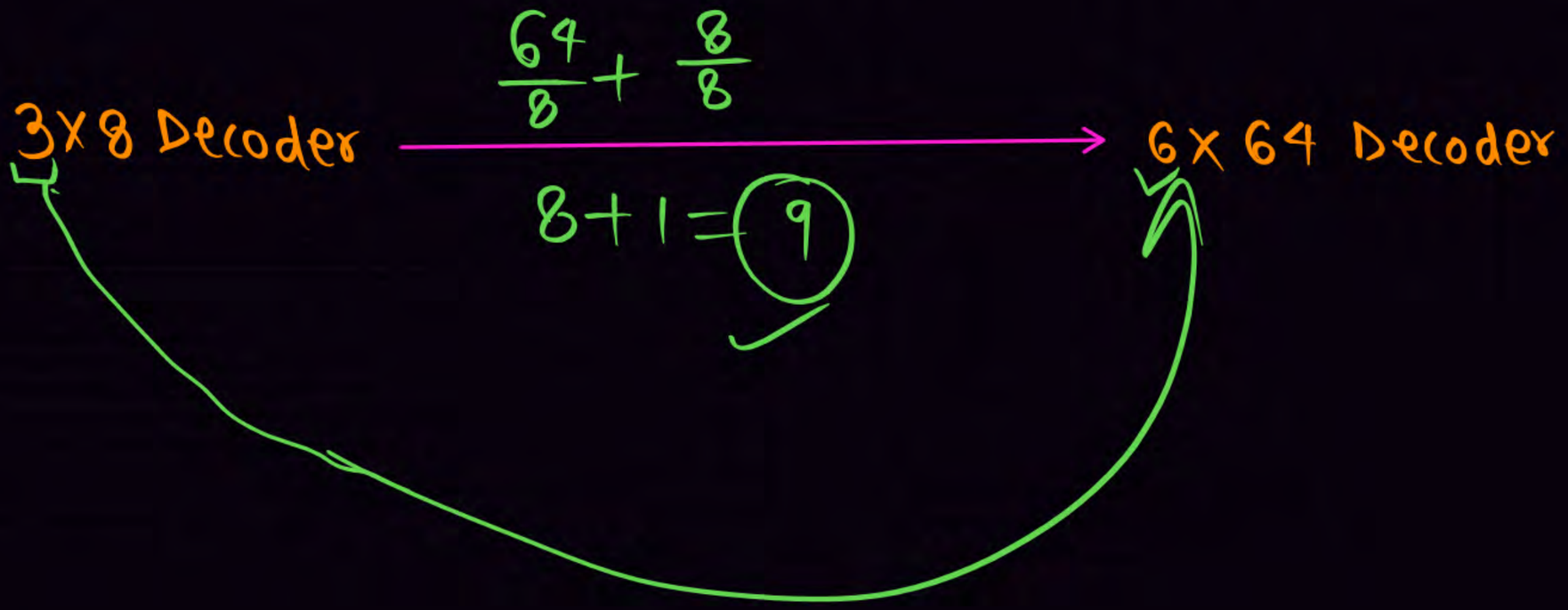
DECODER, HA, FA

DESIGN 3 × 8 DECODER BY USING 2 × 4 DECODER



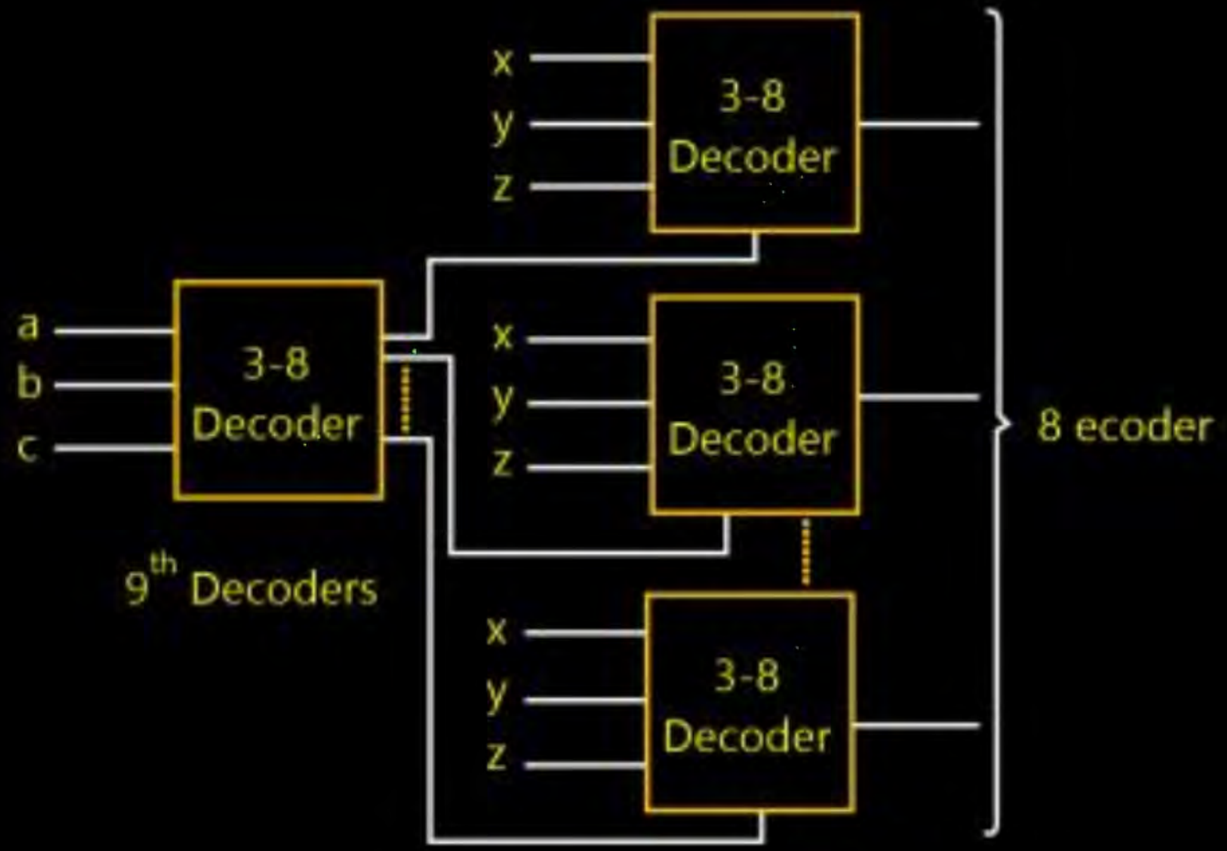

A
B
2x4 Decoder
$\bar{A}\bar{B}$
$\bar{A}B$
$A\bar{B}$
AB
D
C
2x4
$\bar{A}\bar{B}\bar{C}\bar{D} = y_0$
$\bar{A}\bar{B}\bar{C}D = y_1$
$\bar{A}\bar{B}C\bar{D} = y_2$
$\bar{A}\bar{B}CD = y_3$
$\bar{A}B\bar{C}\bar{D} = y_4$
$\bar{A}B\bar{C}D = y_5$
$\bar{A}BC\bar{D} = y_6$
$\bar{A}BCD = y_7$
$A\bar{B}\bar{C}\bar{D} = y_8$
$A\bar{B}\bar{C}D = y_9$
$A\bar{B}C\bar{D} = y_{10}$
$A\bar{B}CD = y_{11}$
$AB\bar{C}\bar{D} = y_{12}$
$AB\bar{C}D = y_{13}$
$ABC\bar{D} = y_{14}$
$ABCD = y_{15}$


2x4 Decoder
$\frac{16}{4} + \frac{4}{4}$
4+1=5
4x16 Decoder
double


3 X 8 Decoder
64/8 + 8/8
8 + 1 = 9
6 X 64 Decoder

DECODER, HA, FA

DESIGN 3 × 8 DECODER BY USING 2 × 4 DECODER



Q.1

A logic circuit consist of two 2 × 4 decoders as shown in the figure. The output of decoder are as follow:

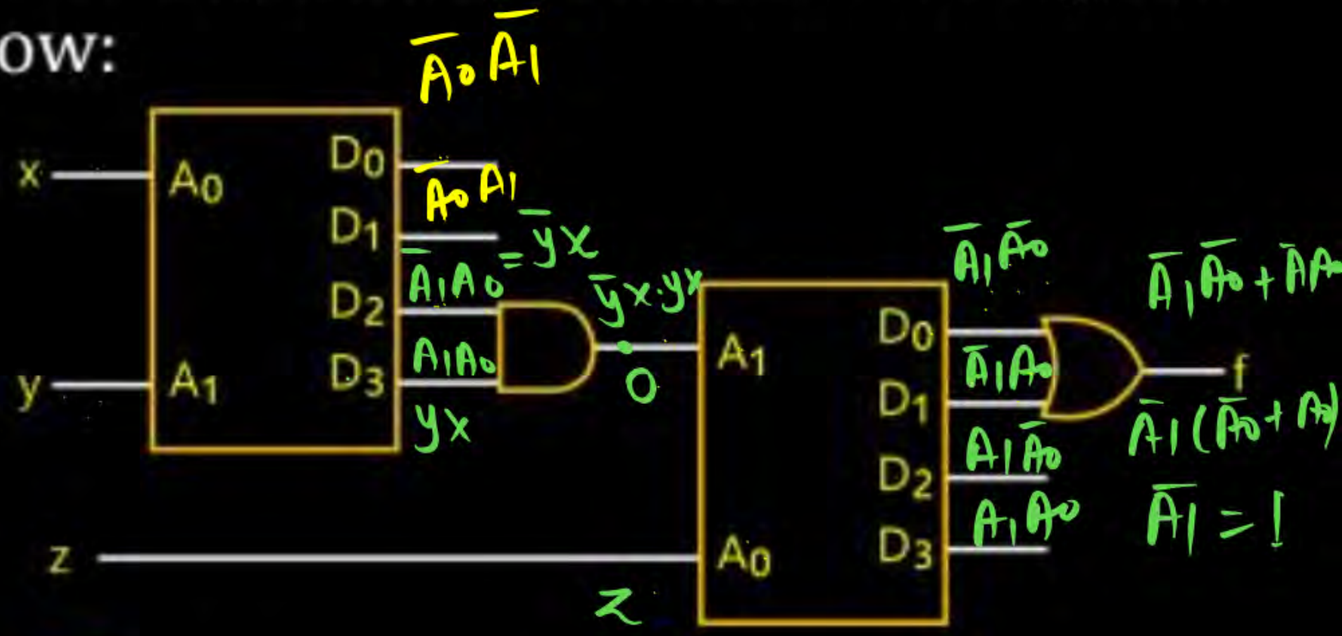
D0 = 1 when A0 = 0, A1 = 0

D1 = 1 when A0 = 1, A1 = 0

D2 = 1 when A0 = 0, A1 = 1

D3 = 1 when A0 = 1, A1 = 1

The value of f(x, y, z) is



A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

$A_1 = 0$

$\bar{A}_1 = 1$ ✓

(A) 0

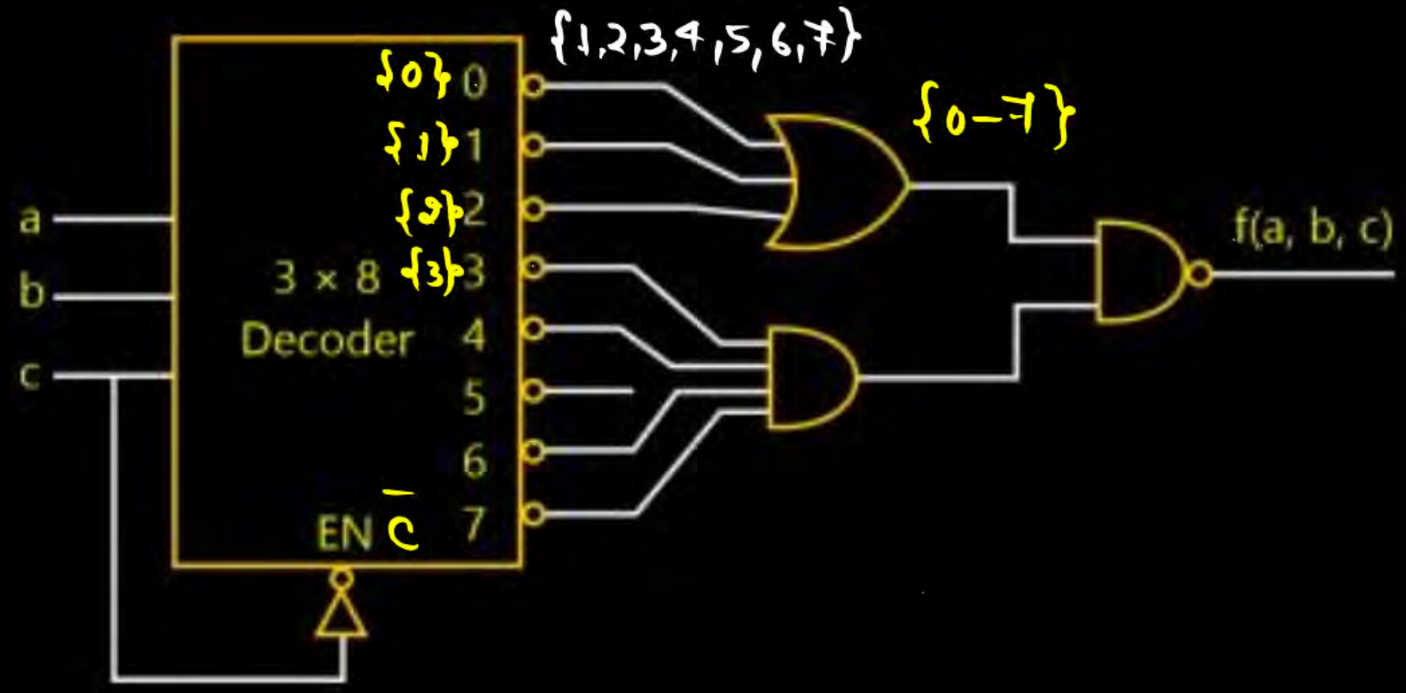
(B) z

(C) $\bar{z}$

(D) 1

Q.2

The Boolean expression f(a, b, c) in its canonical form for the decoder circuit shown below is

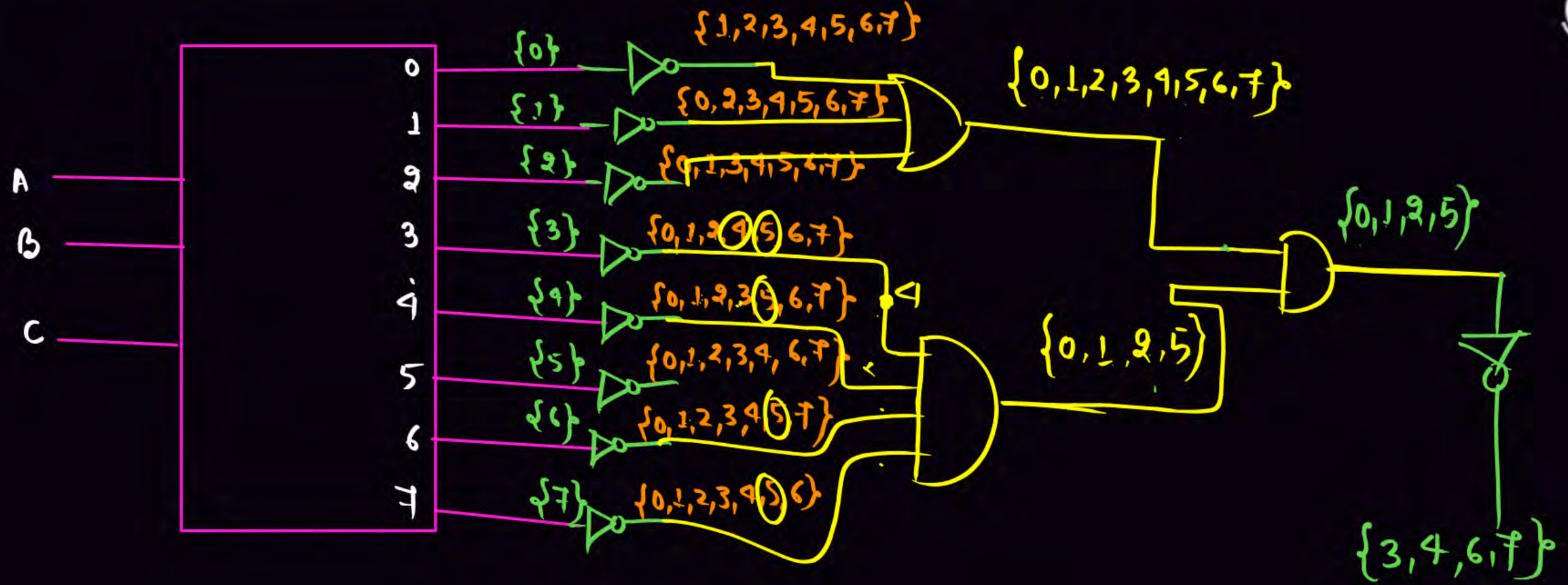


A. $\Pi M(4, 6)$

B. $\Sigma m(0, 1, 2, 3, 5, 7)$

C. $\Sigma m(4, 6)$ ✓

D. $\Pi M(0, 1, 2, 3, 5)$ ✗


A
B
C
0
1
2
3
4
5
6
7
{0}
{1}
{2}
{3}
{4}
{5}
{6}
{7}
{1,2,3,4,5,6,7}
{0,2,3,4,5,6,7}
{0,1,3,4,5,6,7}
{0,1,2,4,5,6,7}
{0,1,2,3,5,6,7}
{0,1,2,3,4,6,7}
{0,1,2,3,4,5,7}
{0,1,2,3,4,5,6}
{0,1,2,3,4,5,6,7}
{0,1,2,5}
{0,1,2,5}
{3,4,6,7}

$$f = \bar{C}\,\Sigma m(3,4,6,7)$$

$$f = \bar{C}\left[\cancel{\bar{A}BC} + A\bar{B}\bar{C} + AB\bar{C} + \cancel{ABC}\right]$$

$$\underset{4}{A\bar{B}\bar{C}} + \underset{6}{AB\bar{C}}$$

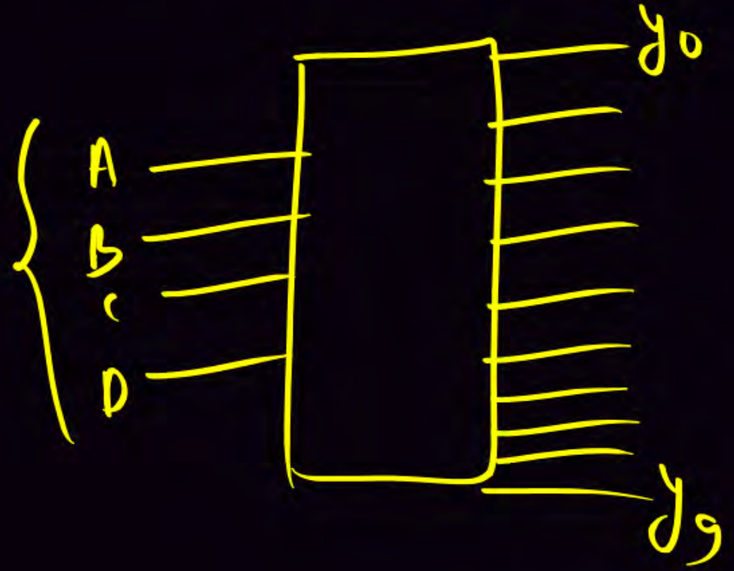
$$f = A\bar{B}\bar{C} + AB\bar{C}$$

✓ $f = \Sigma m(4,6)$

✓ $f = \Pi M(0,1,2,3,5,7)$

HW

Design Binary to Decimal Decoder?

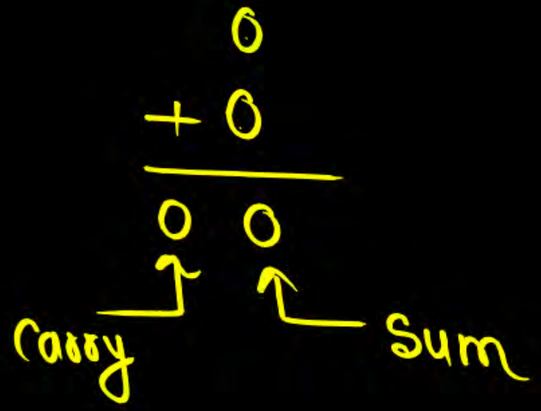


DECODER, HA, FA

HALF ADDER

0	0	1	1
+0	+1	+0	+1
00	01	01	10

carry — sum



- Two bit adder are known as half adder.

DECODER, HA, FA

HALF ADDER

Step 1.

DECODER, HA, FA

HALF ADDER

Step 2. Truth table.

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

DECODER, HA, FA

HALF ADDER

Step 3.

$$\text{sum} = \overline{A}B + A\overline{B} = A \oplus B$$

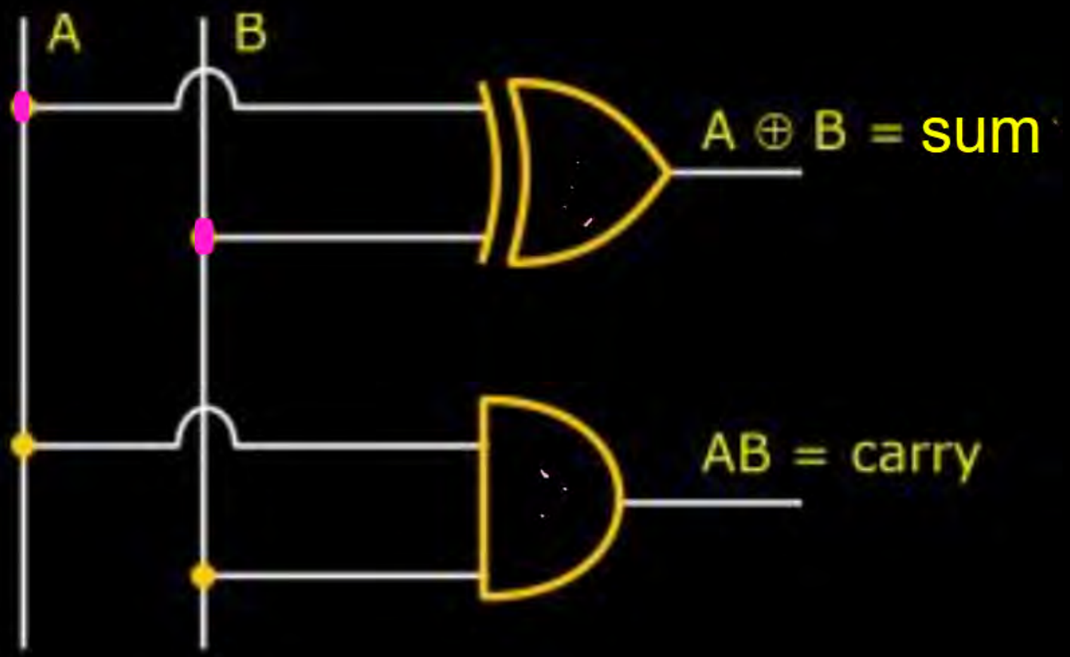
$$\text{carry} = AB$$

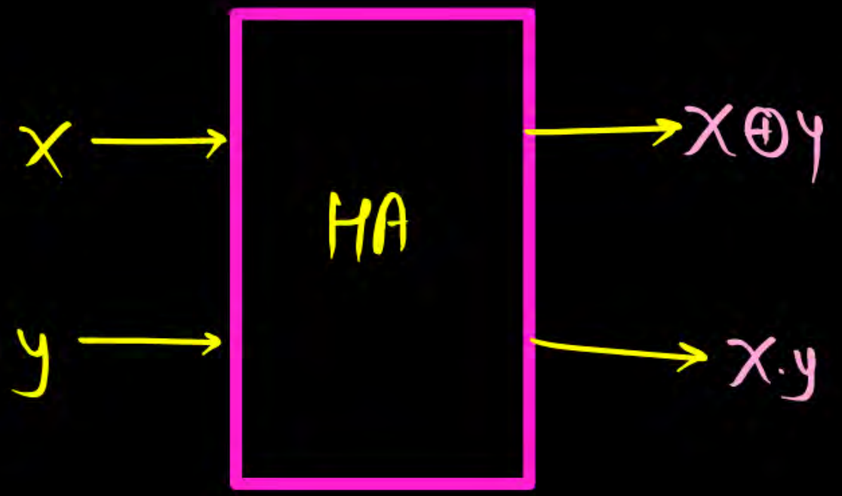
Step 4. Minimization

DECODER, HA, FA

HALF ADDER

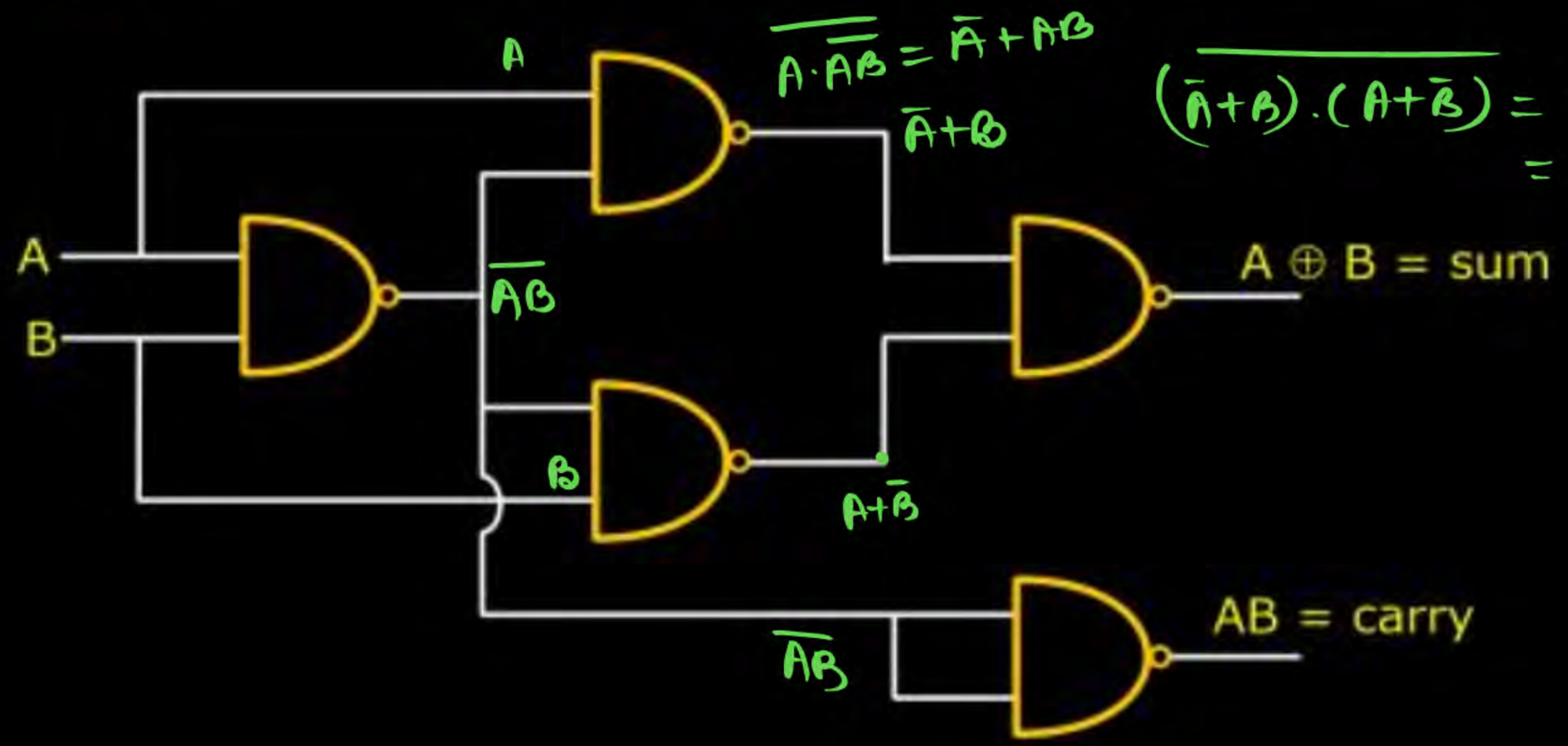
Step 5.





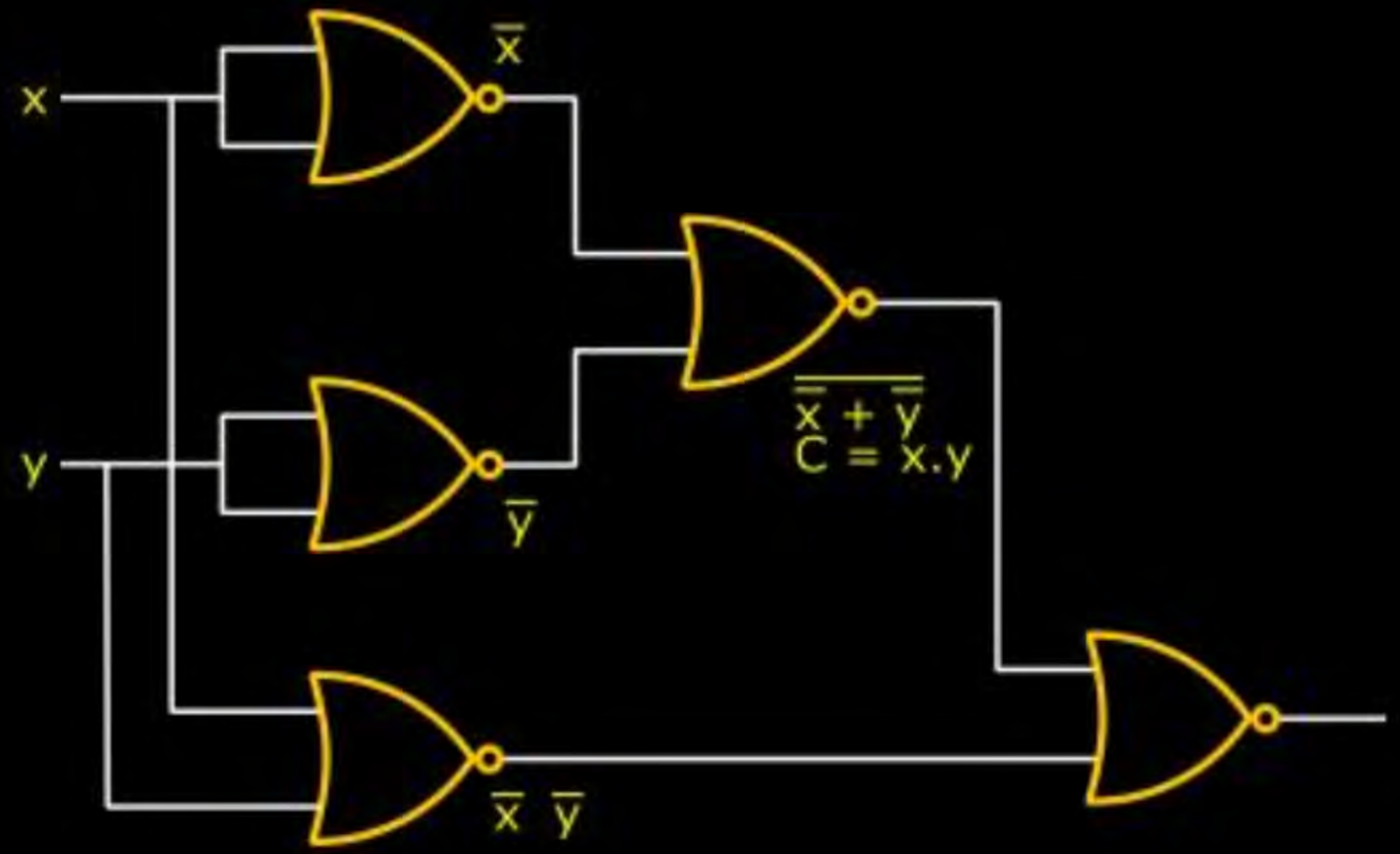
DECODER, HA, FA

By NAND GATE

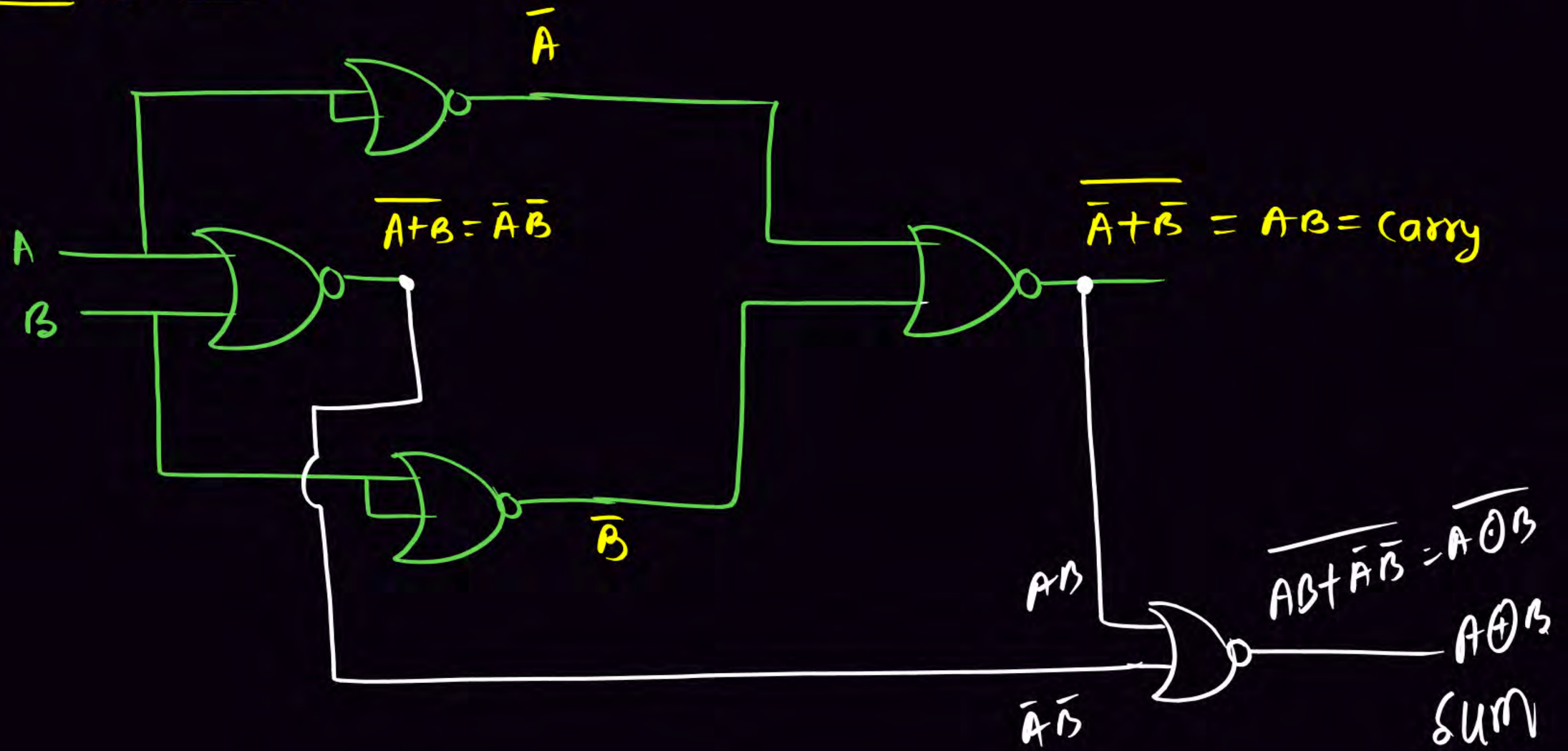


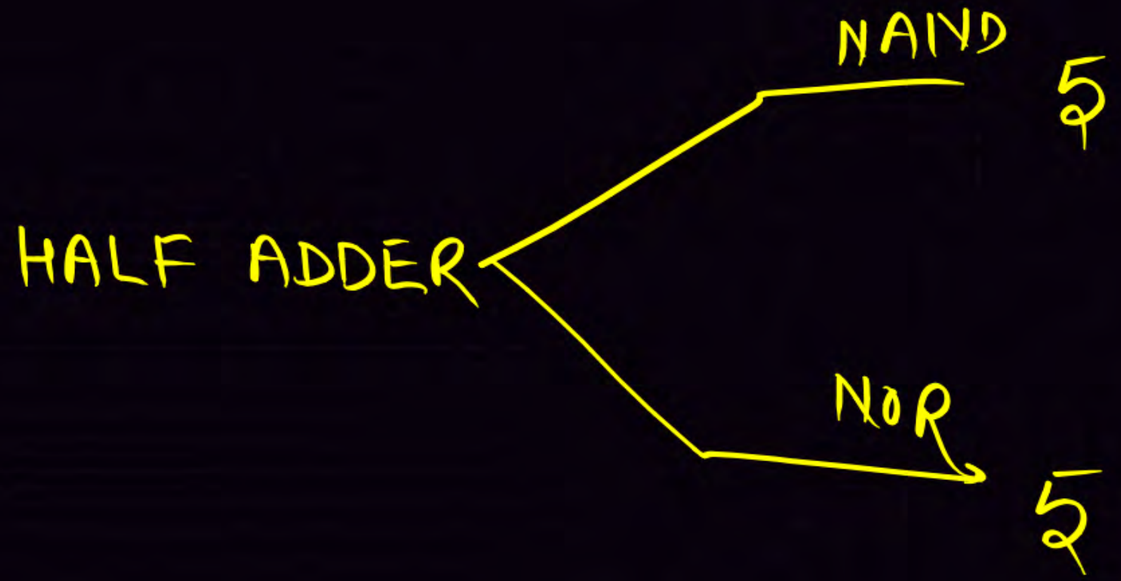
DECODER, HA, FA

By NAND GATE

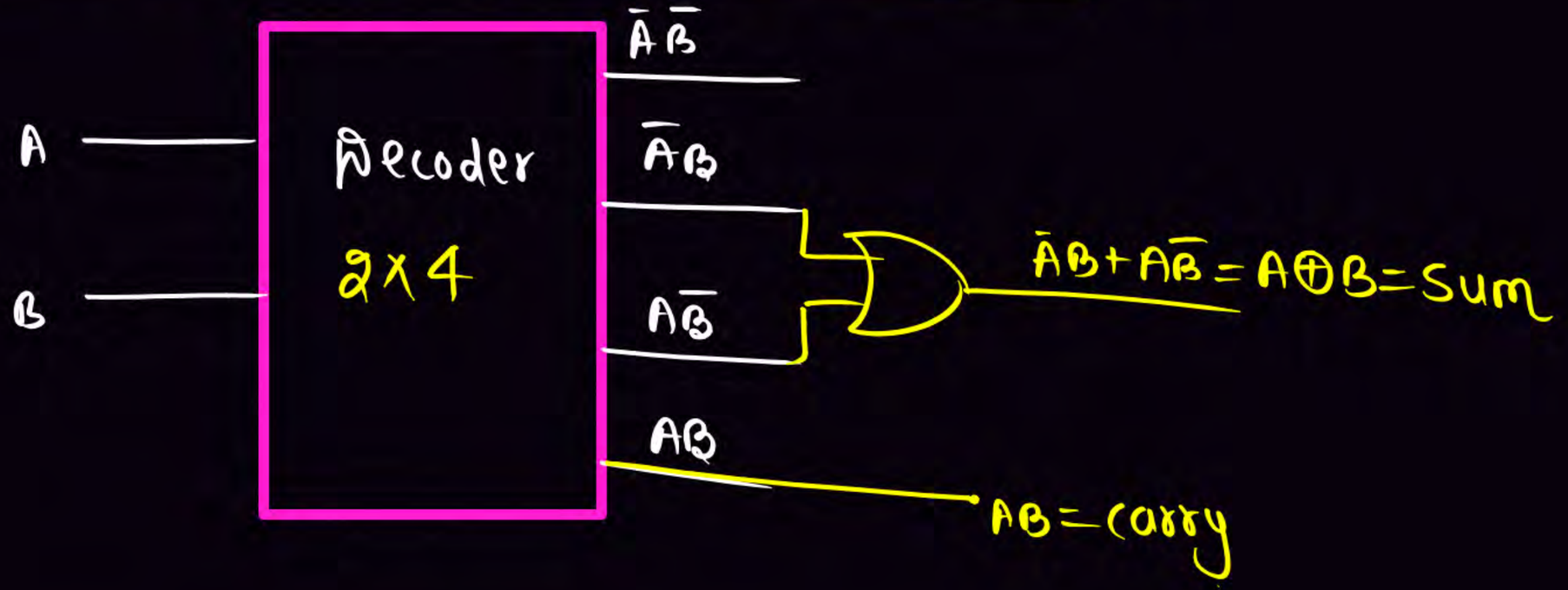


By NOR GATE


$\bar{A}$
$\overline{A+B} = \bar{A}\bar{B}$
A
B
$\overline{\bar{A}+\bar{B}} = AB$ = Carry
$\bar{B}$
AB
$\overline{AB+\bar{A}\bar{B}} = \overline{A \odot B}$
$A \odot B$
SUM
$\bar{A}\bar{B}$


HALF ADDER
NAND
5
NOR
5̄

HALF ADDER BY Using 2x4 Decoder →

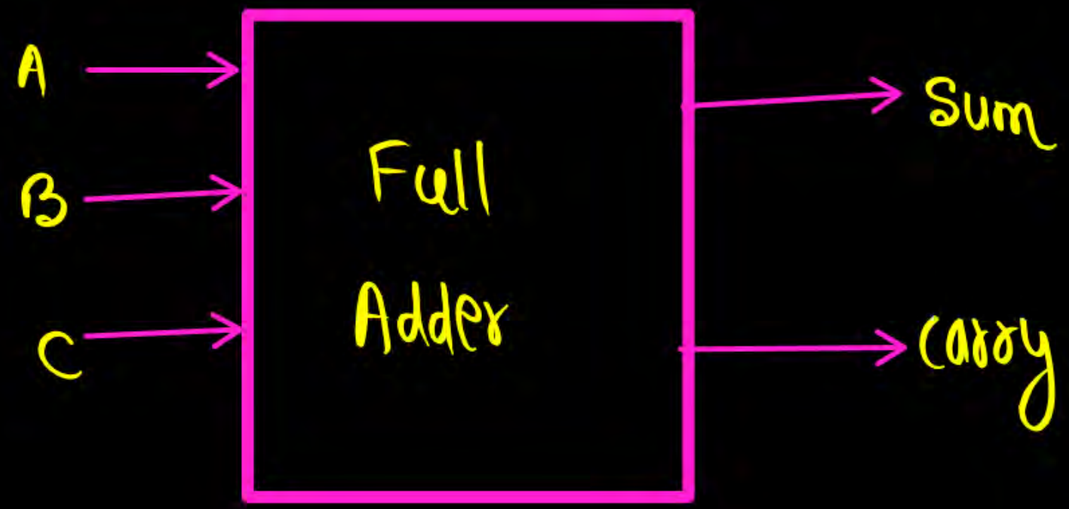


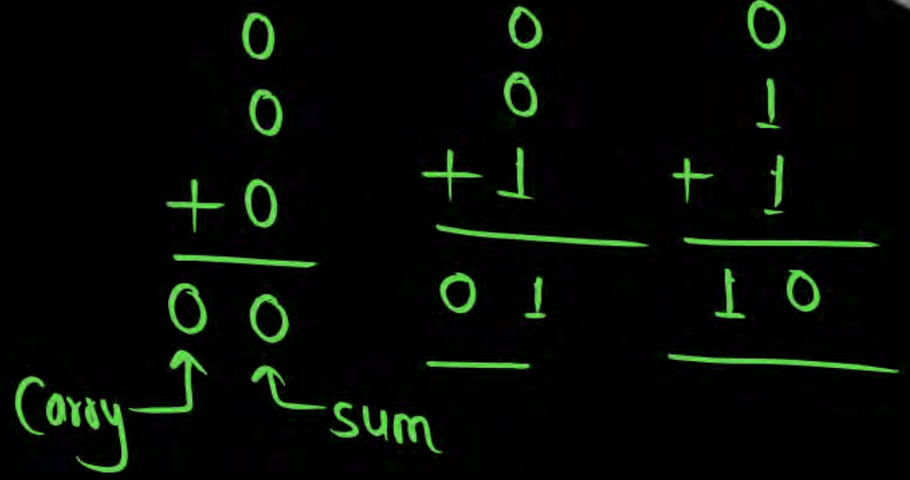
DECODER, HA, FA

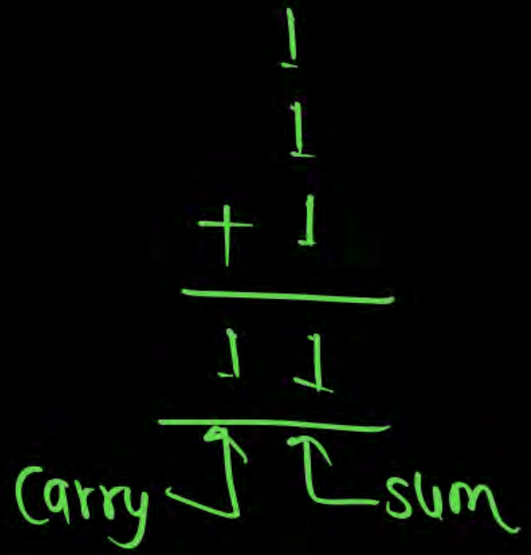
FULL ADDER

Three bit adder are known as full adder

Step 1.







DECODER, HA, FA

FULL ADDER

Step 2.

When majority of the inputs are high.

	A	B	C	Sum	Carry
0→	0	0	0	0	0
1→	0	0	1	1	0
2→	0	1	0	1	0
3→	0	1	1	0	1
4→	1	0	0	1	0
5→	1	0	1	0	1
6→	1	1	0	0	1
7→	1	1	1	1	1

DECODER, HA, FA

FULL ADDER

Step 3. Sum (A, B, C) $= \Sigma m(1,2,4,7) = A \oplus B \oplus C = (A \oplus B) \oplus C$

Step 4. Carry (A, B, C) $= \Sigma m(3,5,6,7) = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$

$= (\bar{A}B + A\bar{B})C + AB(\bar{C} + C)$

$= (A \oplus B)C + AB$

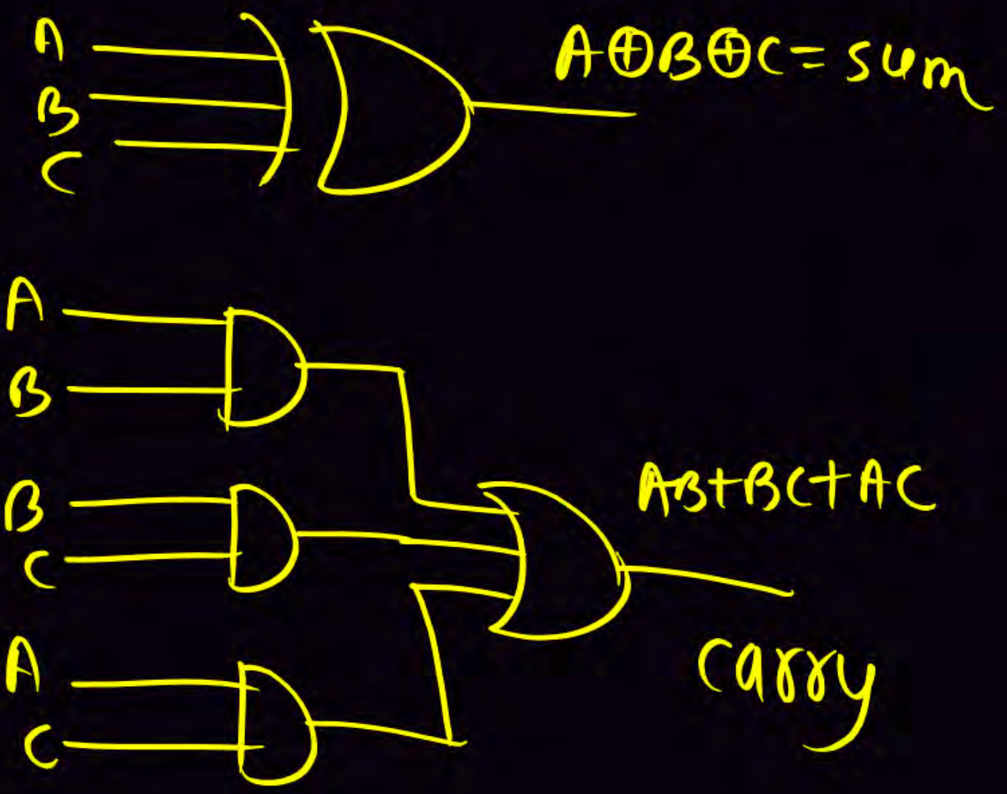
$= AB + BC + AC$

Sum = $A \oplus B \oplus C$

Carry = $\Sigma m(3,5,6,7)$

$= (A \oplus B)C + AB$

$= AB + BC + AC$



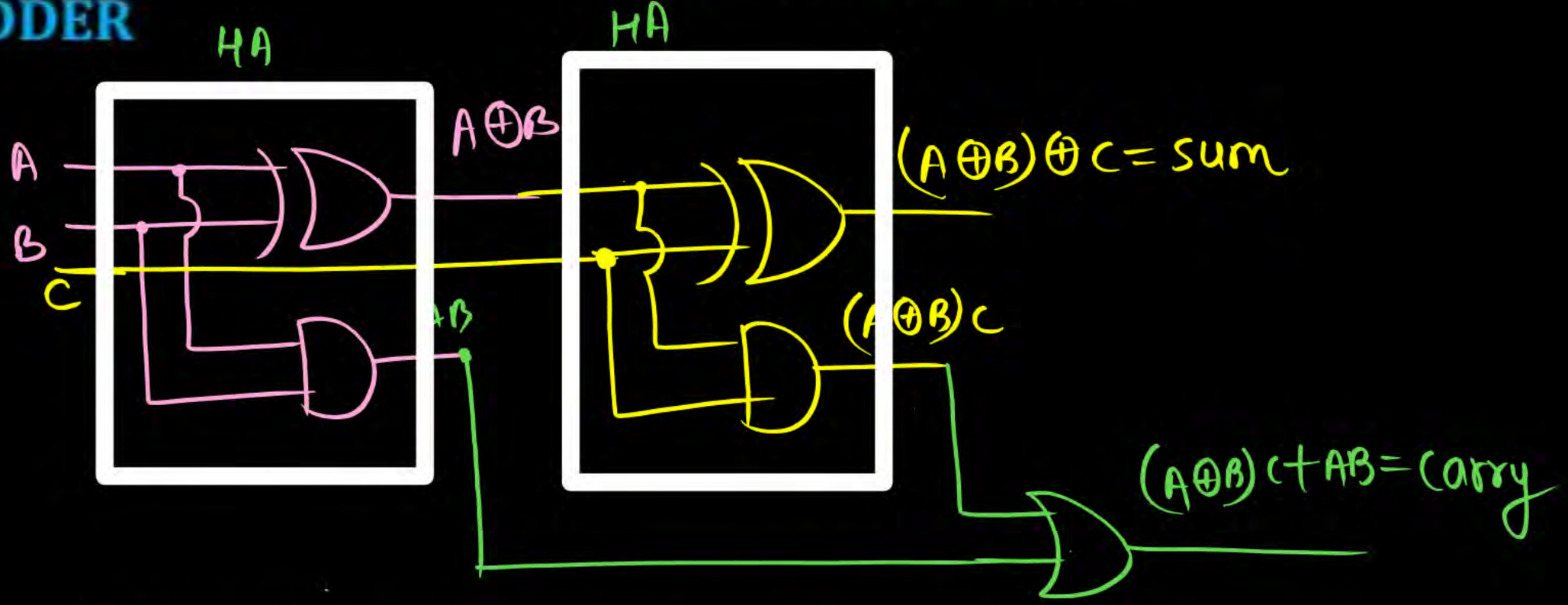
DECODER, HA, FA

Sum = $(A \oplus B) \oplus C$

Curry = $(A \oplus B)C + AB$

FULL ADDER

Step 5.

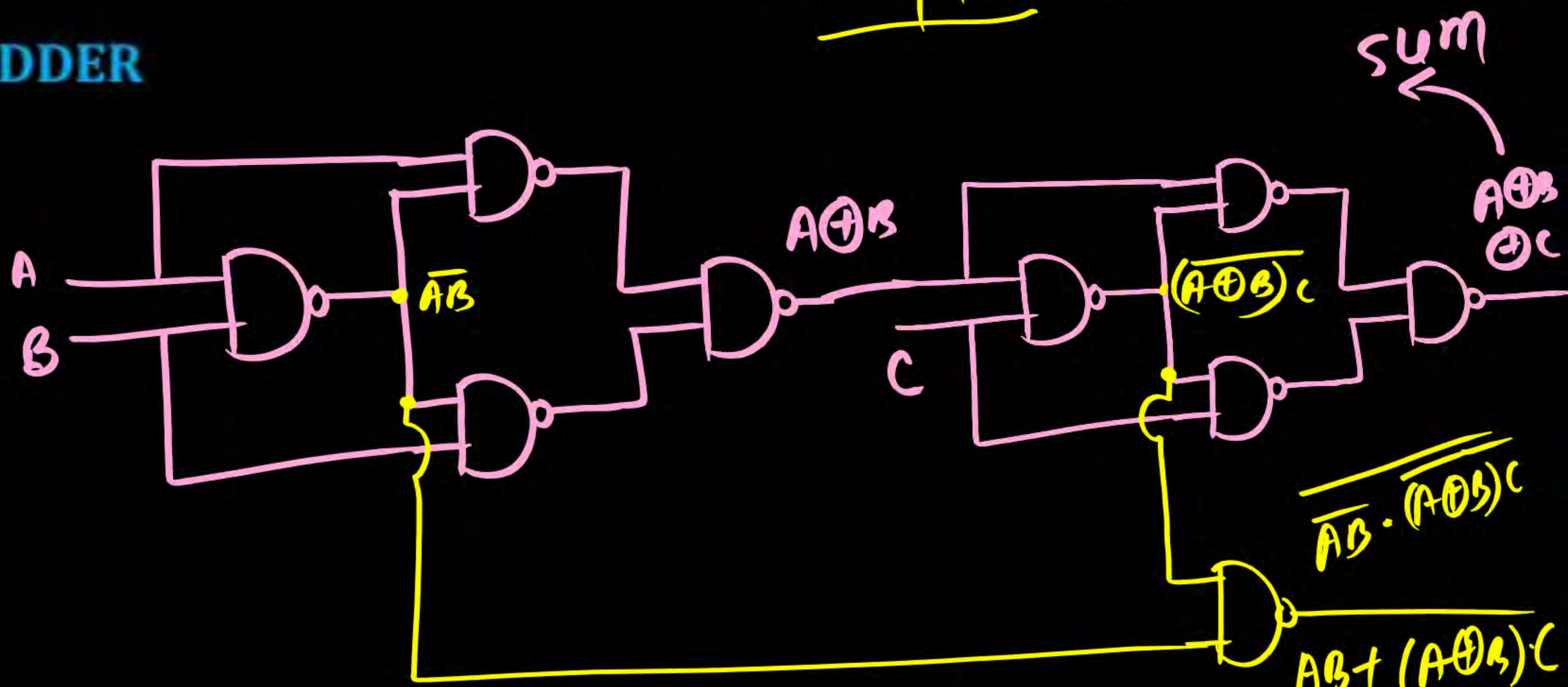


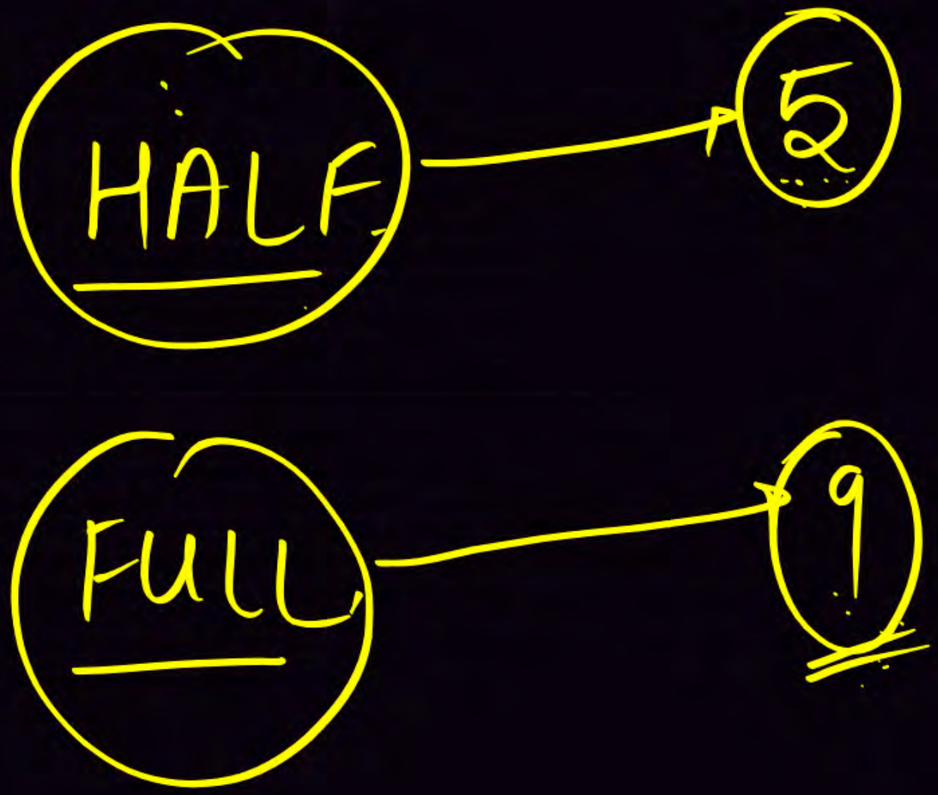
FA = 2HA + 1 OR GATE

DECODER, HA, FA

FA = (9) → NAND / NOR

FULL ADDER




HALF
5
FULL
9

Q.1

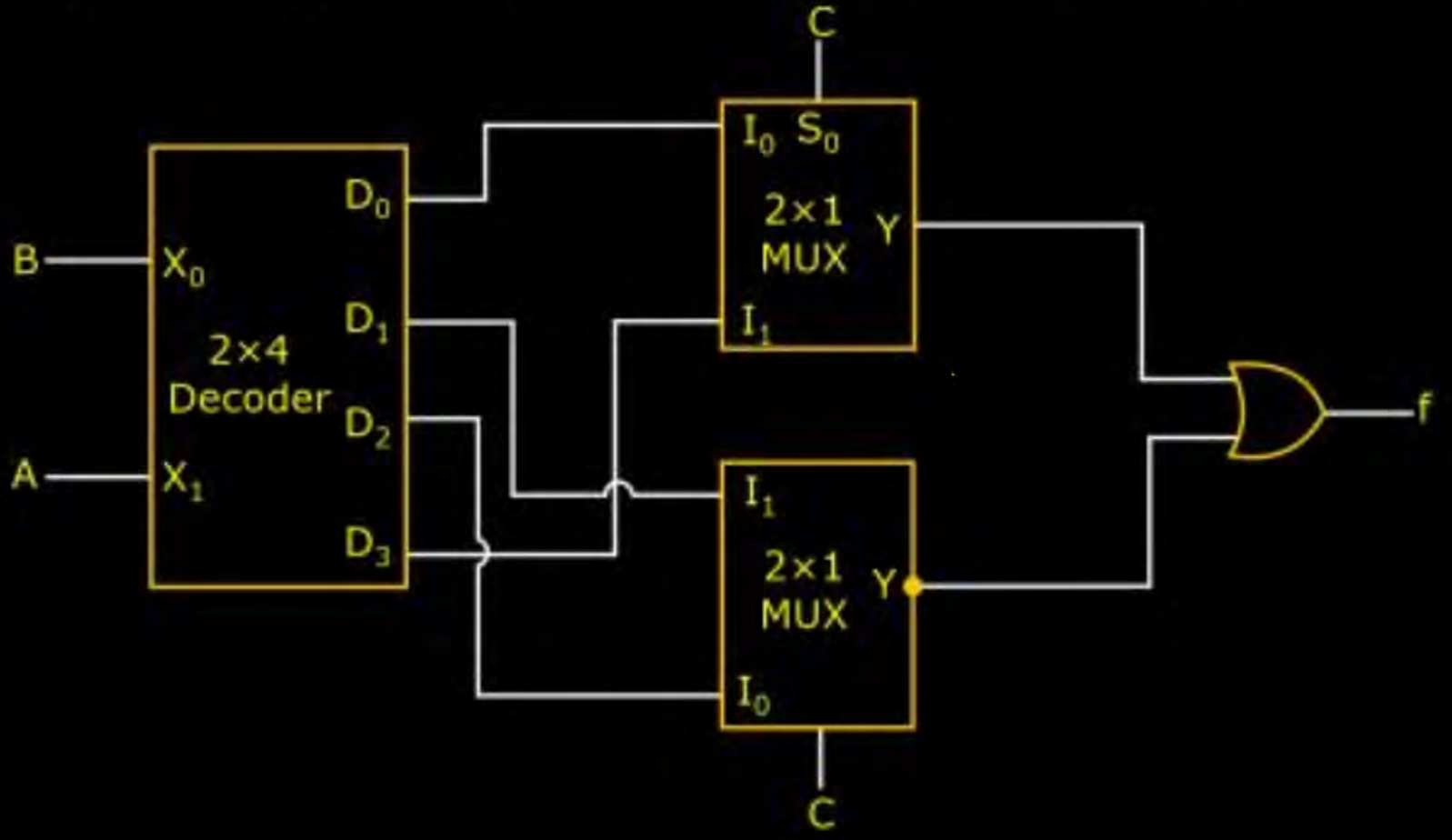
HW

A full adder is implemented with two half adders and one OR gate. OR gate is used to derive the final carry function of full adder. In each half adder, T_{sum} = 25 ns and T_{carry} = 20 ns and T_{OR} = 25 ns. The minimum time required to derive both the sum and carry function of a full adder after applying the inputs is ____ ns

Q.2

HW

A logic function 'f' is implemented by the circuit shown in the figure below. The circuit consists of one 2×4 decoder, two 2×1 multiplexers and a two input or gate connected in cascade. Then the function f is equal to.



(A) $A \oplus B$

(B) $A \oplus B \oplus C$

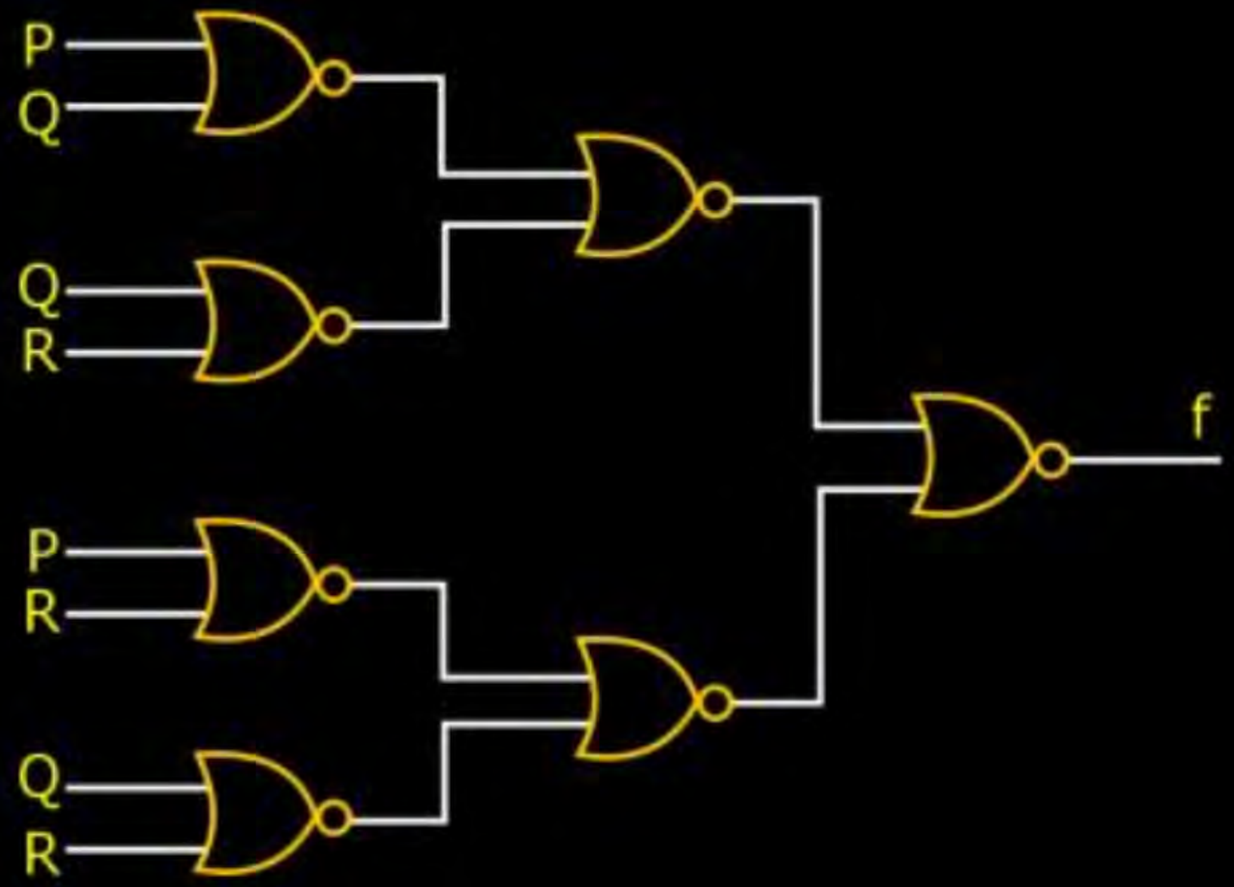
(C) $B \odot C$

(D) $A \odot B$

Q.3

HW

What is the Boolean expression for the output f of the combinational logic circuit of NOR gates given below?



A $\overline{Q+R}$

B $\overline{P+Q}$

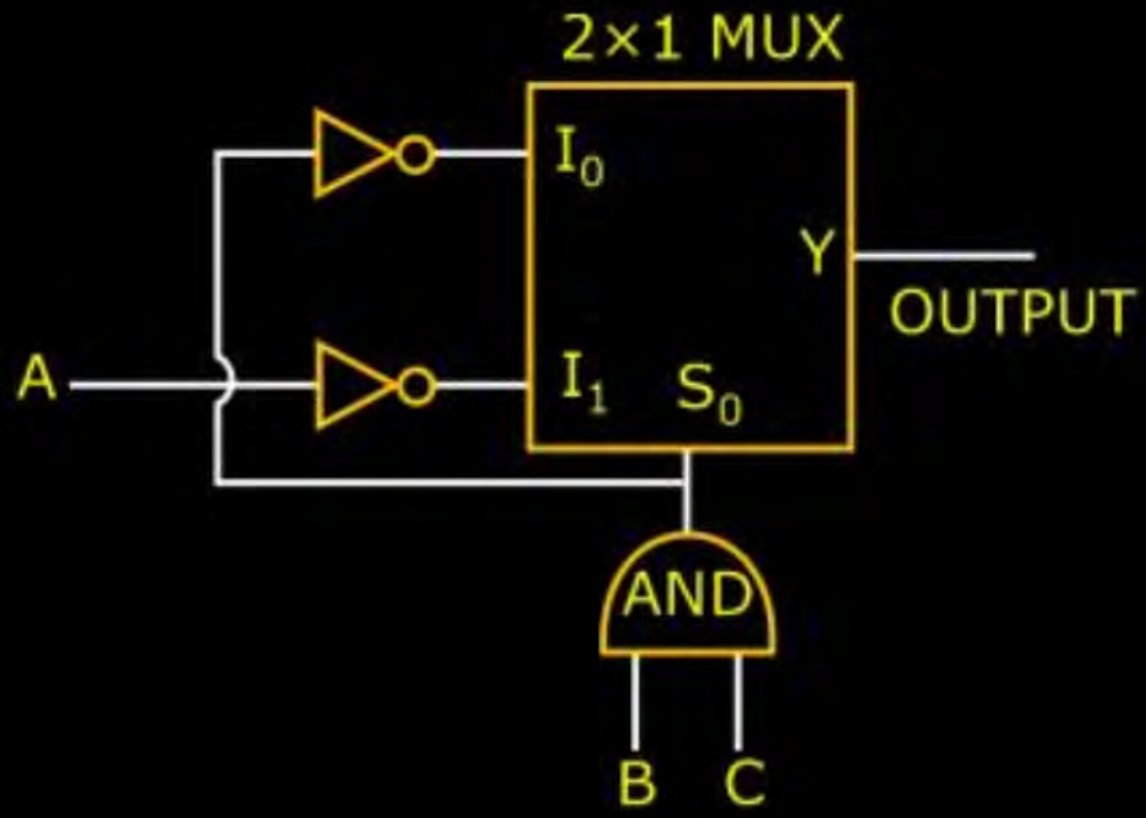
C $\overline{P+R}$

D $\overline{P+Q+R}$

Q.4

HW

The combinational circuit given below implements which of the following



(A) NOR gate

(B) XOR gate

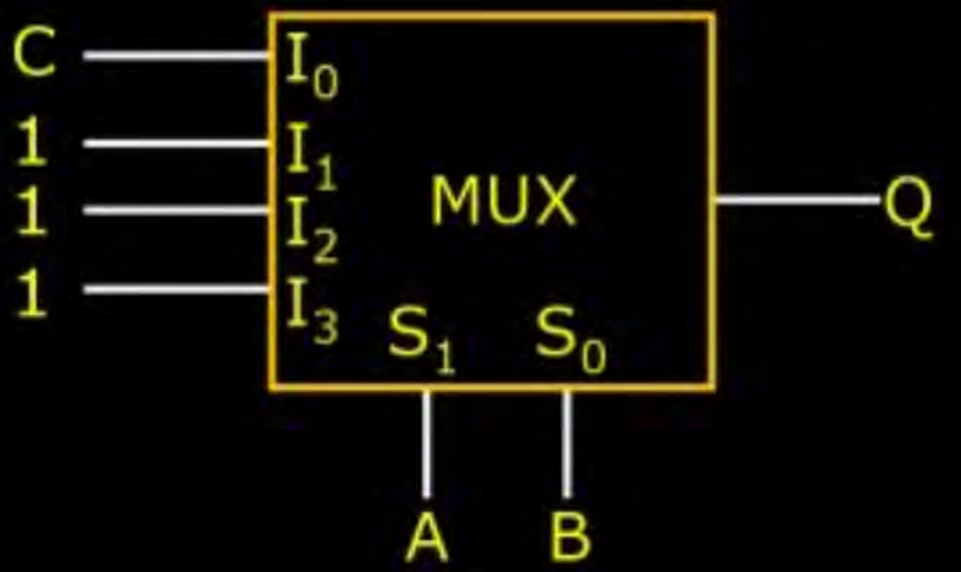
(C) NAND gate

(D) None of these

Q.5

HW.

The combinational logic circuit shown in the given figure has an output Q which is



(A) ABC

(B) A + B + C

(C) $A \oplus B \oplus C$

(D) A.B + C

$18

Thank you

GW

Soldiers !