CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Memory Organization

Lecture No.- 02

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Eraser

Recap of Previous Lecture

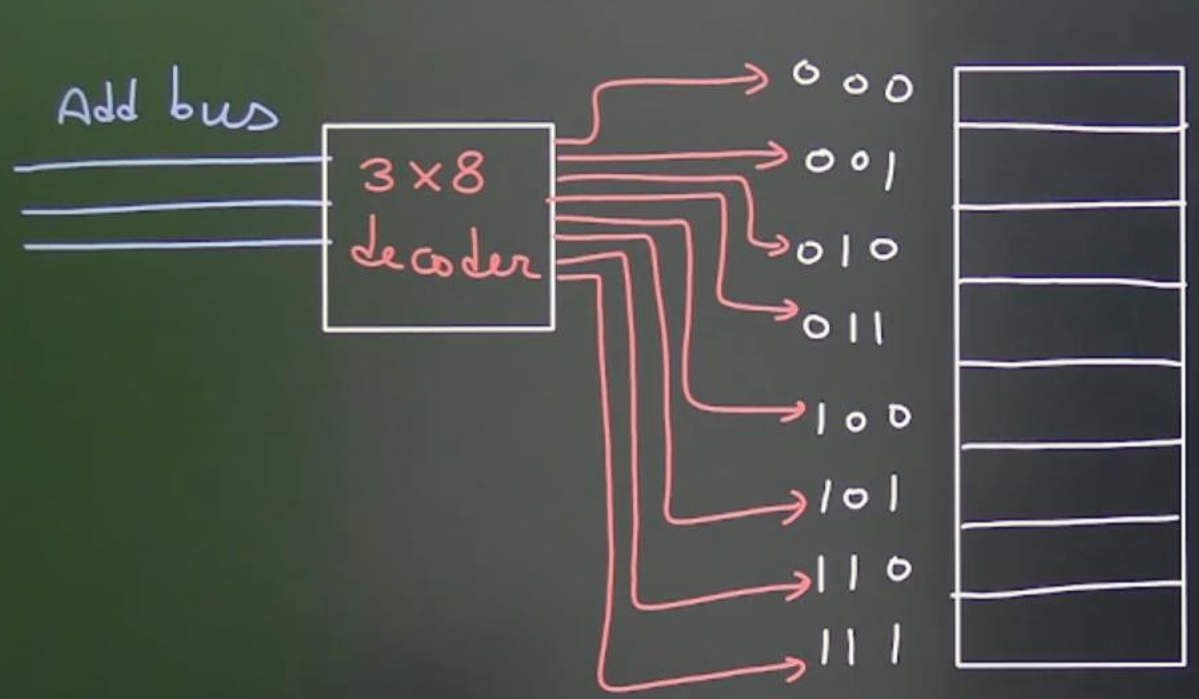
Topic Memory Hierarchy

Topic Memory Presentation

Topics to be Covered

- Topic: Memory Address Decoder
- Topic: Main Memory: RAM, ROM
- Topic: RAM Chip
- Topic: ROM Chip

Topic : Memory Address Decoder



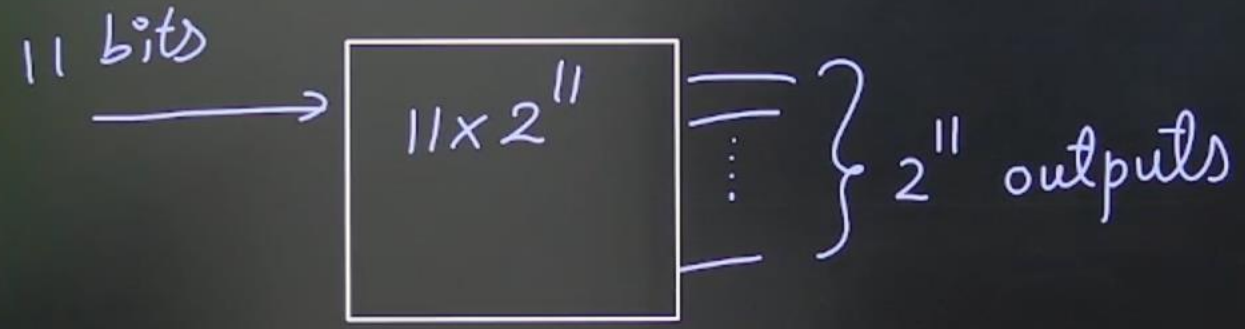
assume, 8 byte memory

[NAT]

Ans = 11×2^{11} or $11 \times 2k$

#Q. Consider a memory of size 2K × 8-bits. What is the size of decoder needed to access the cells of the memory uniquely?

no. of cells = $2k = 2^{11}$ ⇒ add. size = 11 bits

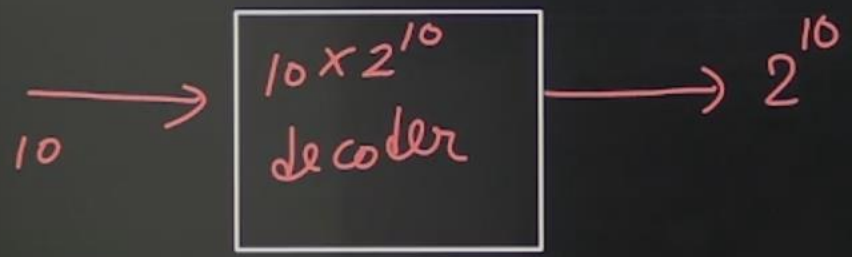


[NAT] GATE-PYQ

#Q. If there are m input lines n output lines for a decoder that is used to uniquely address a byte addressable 1 KB RAM, then the minimum value of m + n is _____?

RAM = 1kB = 1k x 1B

no. of cells = 1k = 2^{10} ⇒ add. = 10 bits



m = 10

n = 2^{10} = 1024

m+n = 10 + 1024 = 1034

Topic : Main Memory

Used to store current running programs and their data.

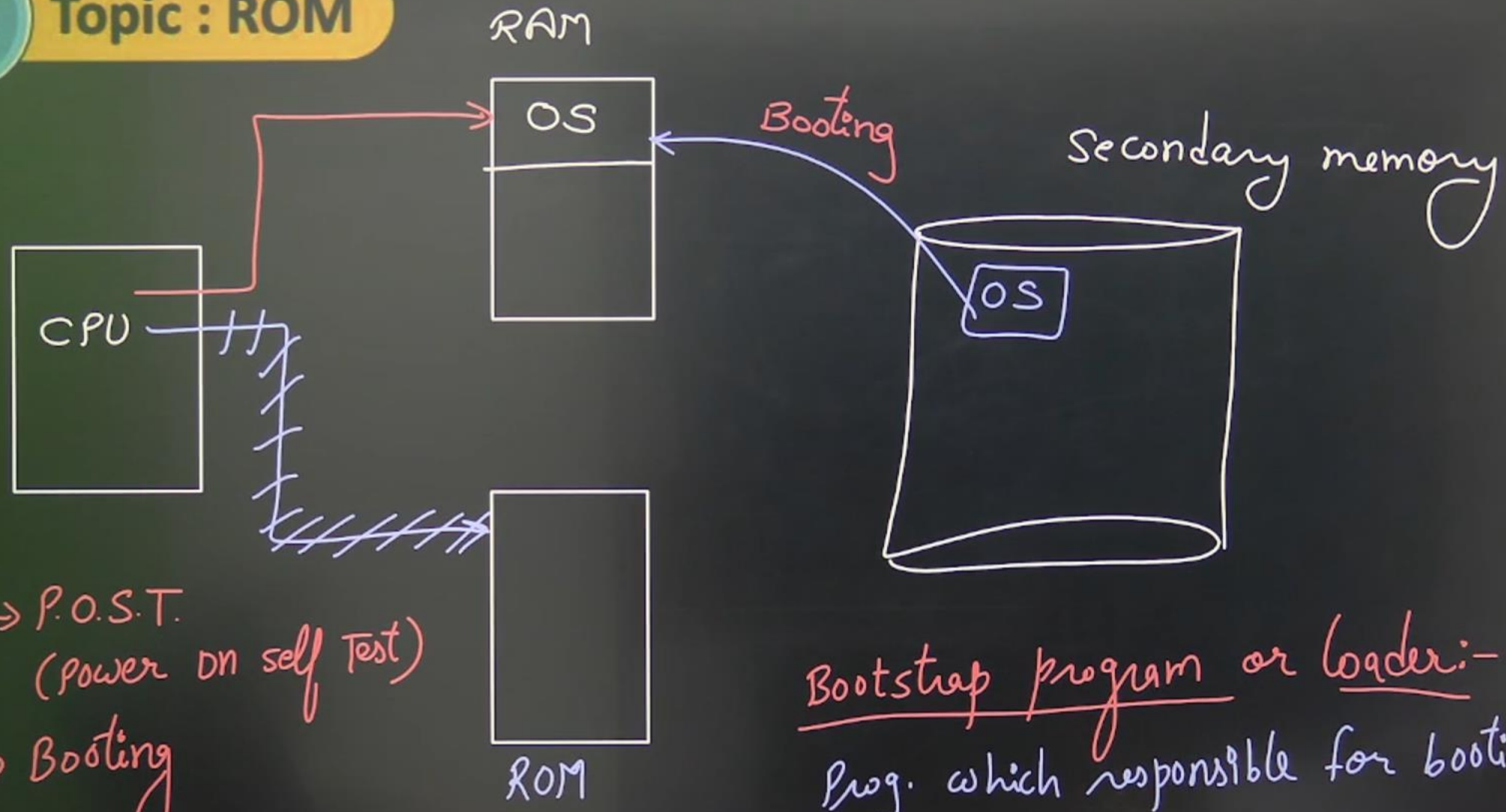
or

CPU takes instns & data for execution from main memory.

Types:-

1. ROM (non-volatile)
2. RAM (volatile) ⇒ when power supply is cut then the memory is flushed out (the content of memory is not persisted)

Topic : ROM



→ P.O.S.T.
(Power On self Test)

→ Booting

Bootstap program or loader:-

Prog. which responsible for booting

Topic : RAM

Used to store OS programs and current running program's inst^{ns} + data.

Topic : Types of RAM

Hardware

Static (SRAM)	Dynamic (DRAM)
1. Built using flip-flops	1. Built using capacitors store content in the form of electric charges
2. No refresh needed	2. Periodic refresh/recharge is required.
3. faster	3. slower
4. Expensive	4. Less expensive
5. Used for cache memory	5. used for main memory

static	Dynamic
6. Less idle power Consumption	6. More idle power Consumption
7. More operational power Consumptn	7. Less operational power Consumption

[NAT]

#Q. Consider 2 4-bits unsigned values A and B. What will be the maximum size of result for:

1. Addition of A and B $\Rightarrow$ 5-bits
2. Multiplication of A and B $\Rightarrow$ 8-bits

A, B

0000 to 1111

or

0 to 15

extreme case

A = 15

B = 15

A + B = $(30)_{10}$

$\Downarrow$

5-bits

A = 15

B = 15

A * B = $(225)_{10}$

$\Downarrow$

8-bits

[MCQ]

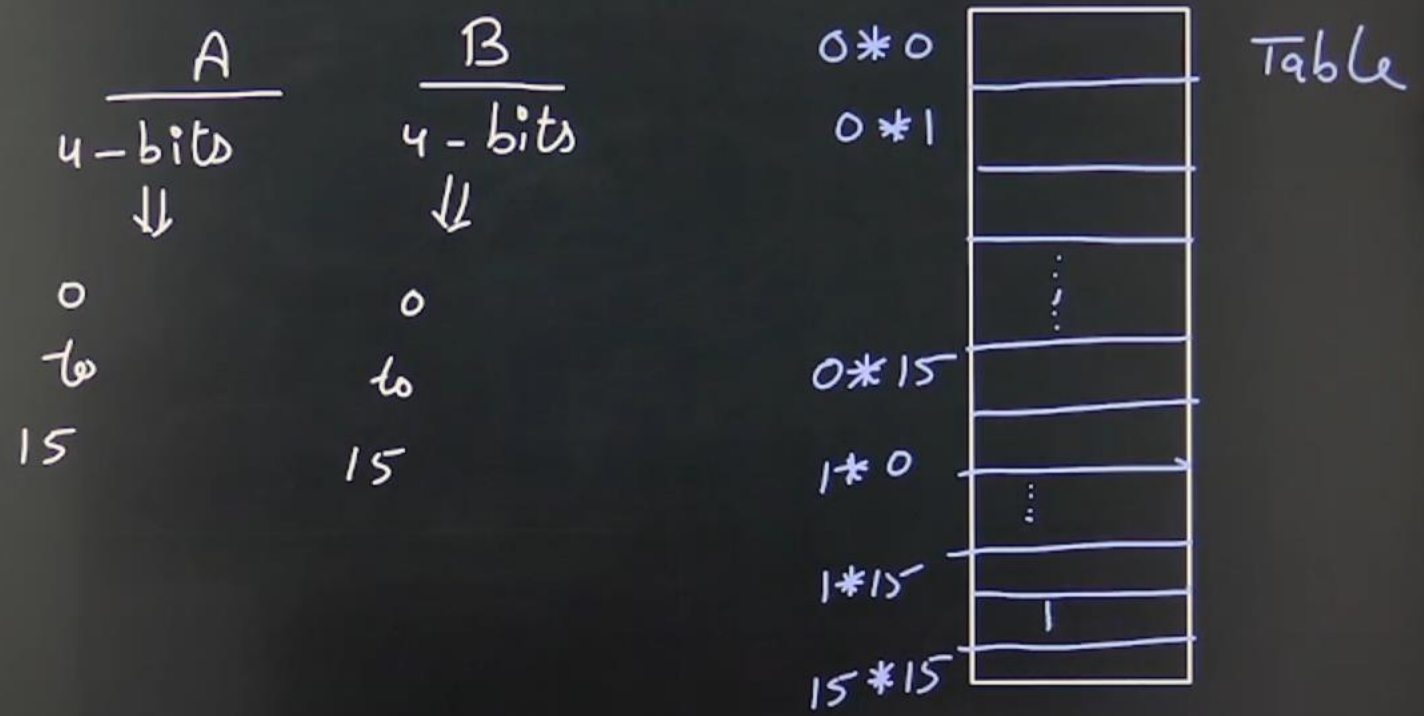
#Q. The amount of ROM needed to store the table for multiplication of two 4-bit unsigned integer is?

A. 64 bits

B. 128 bits

C. 1K bits

D. 2K bits



memory size needed $= 2^8 * 8$ bits

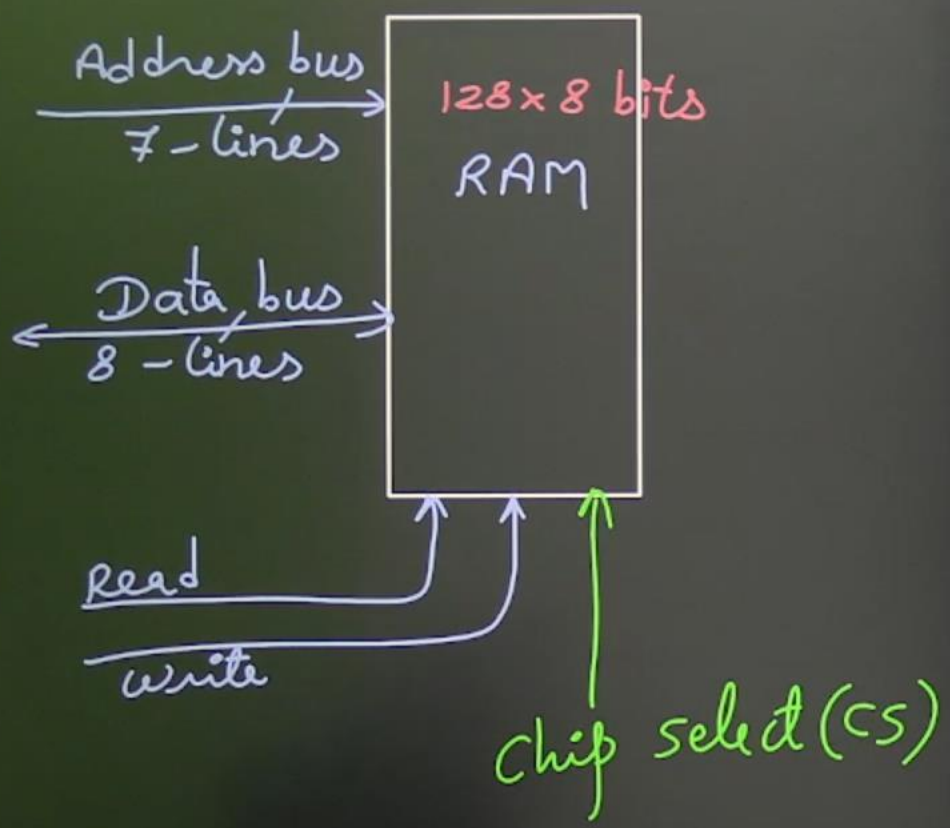
$= 2^8 * 2^3$ bits

$= 2^{11}$ bits

$= 2k$ bits

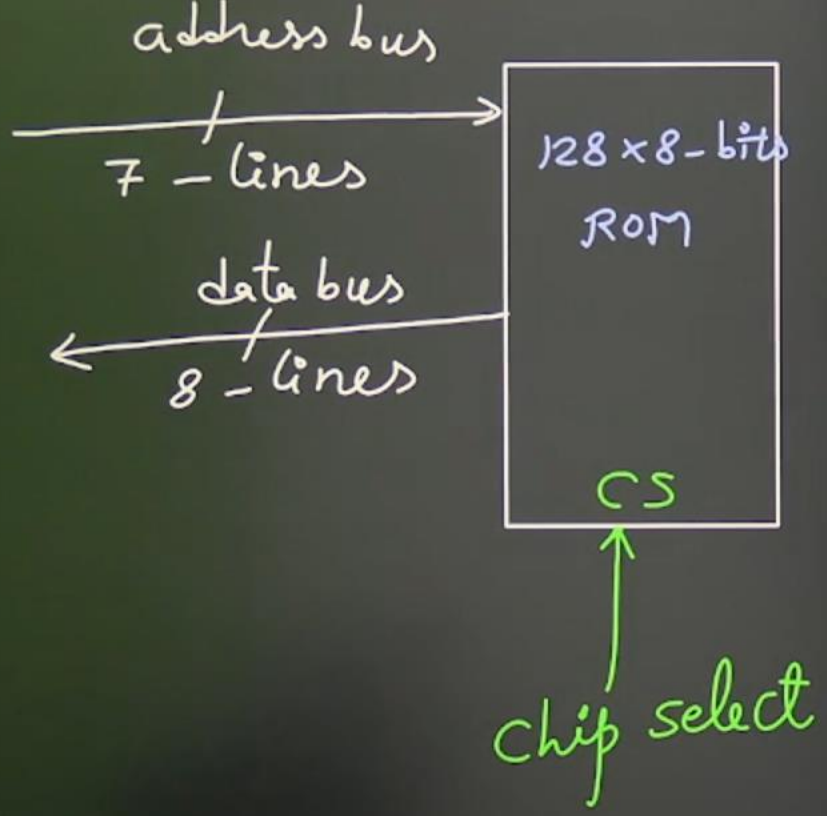
size of input	size of multiplicat^{n} table	size of addition table
4-bits	$2^8 \times 8$ bits	$2^8 \times 5$ bits
n-bits	$2^{2n} \times 2n$ bits	$2^{2n} \times (n+1)$ bits

Topic : RAM Chip



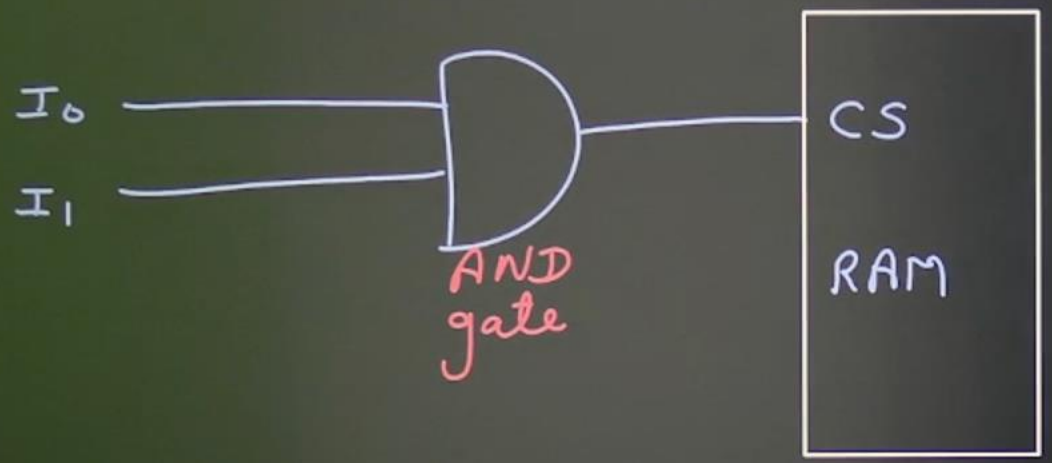
CS	Read	write	operation
0	x	x	No operation
1	0	0	No operation
1	0	1	write
1	1	x	Read

Topic : ROM Chip



CS	operation
0	No- operation
1	Read

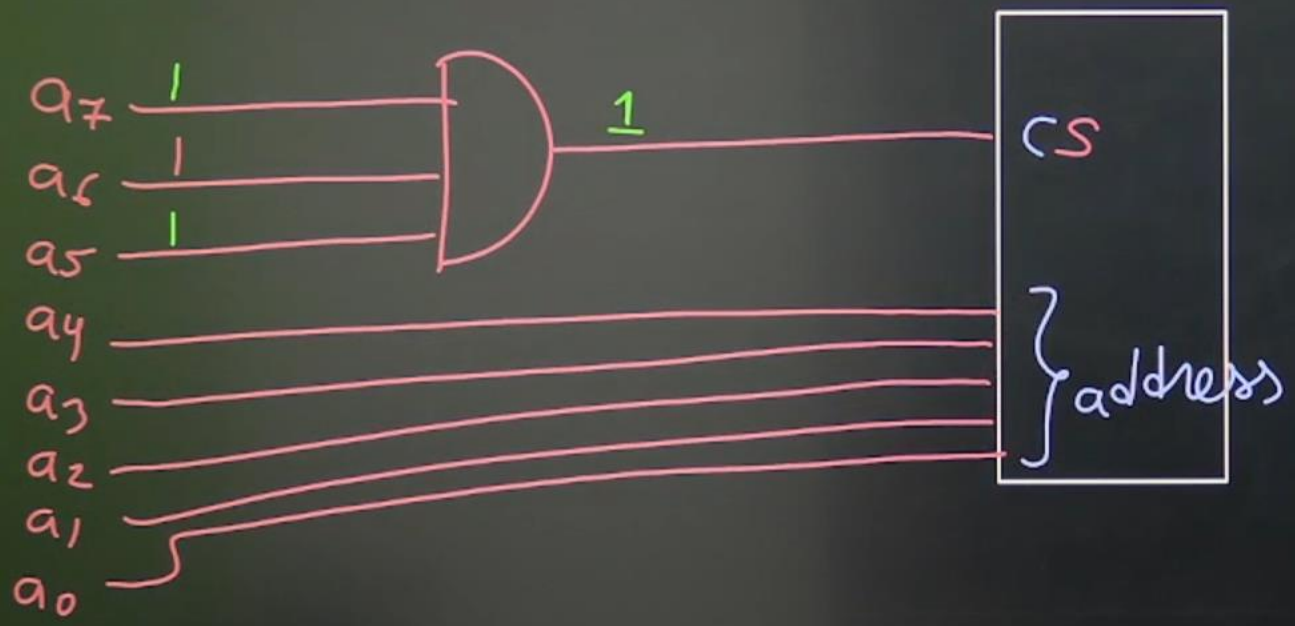
Topic : Chip Select



I_1	I_0	CS
1	1	1

I_1	I_0	CS
1	0	1

Assume a mem takes 8-bit address $a_7\ a_6 \cdots a_1\ a_0$



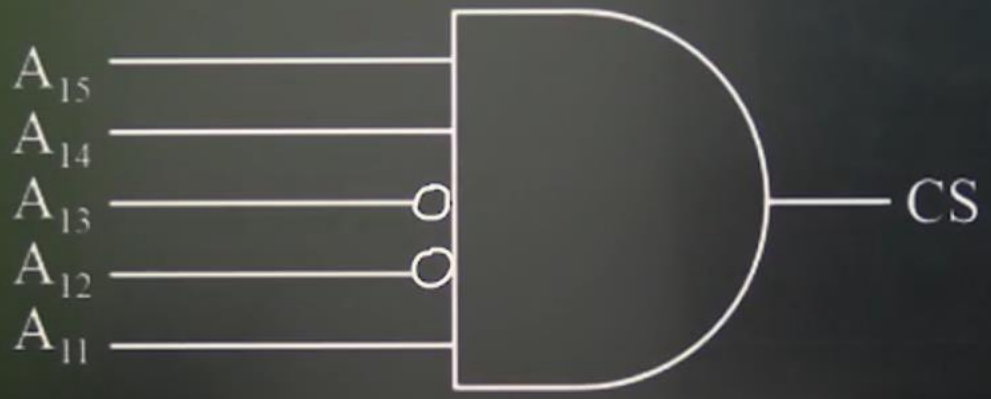
for CS = 1

a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0
1	1	1	0	0	0	0	0
			0	0	0	0	1
⋮							
1	1	1	1	1	1	1	1

address Range ⇐ E0 to FF

[MCQ]

#Q. The chip select logic for a certain DRAM chip in a memory system design is shown below. Assume that the memory system has 16 address lines denoted by A_{15} to A_0. What is the range of address (in hexadecimal) of the memory system that can get enabled by the chip select (CS) signal?



A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 ..... A_0

1 1 0 0 1 0 0 ... 0

C 8 0 0

1 1 0 0 1 1 1 ... 1

C F F F

(A) C800 to CFFF

(B) CA00 to CAFF

(C) C800 to C8FF

(D) DA00 to DFFF

Happy Learning

THANK - YOU