CS & IT ENGINEERING

DIGITAL LOGIC

Extra Practice session

By- CHANDAN SIR

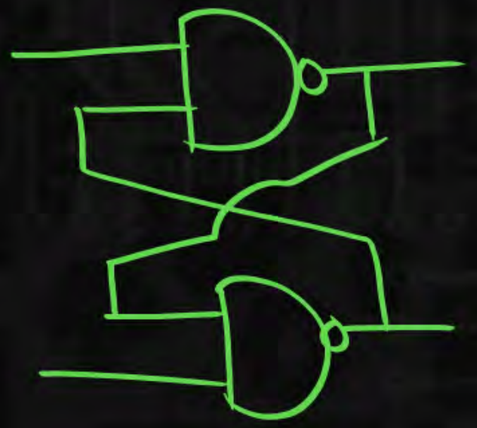
01 Revesion

02 QUESTION PRACTICE

03 DISCUSSION

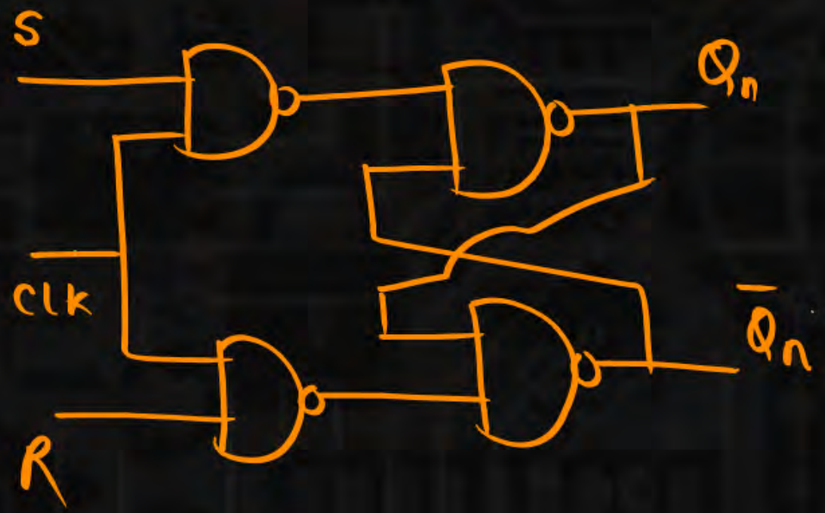
Recap of Sequential Circuit

Latches



Flip-Flop

① SR-FF

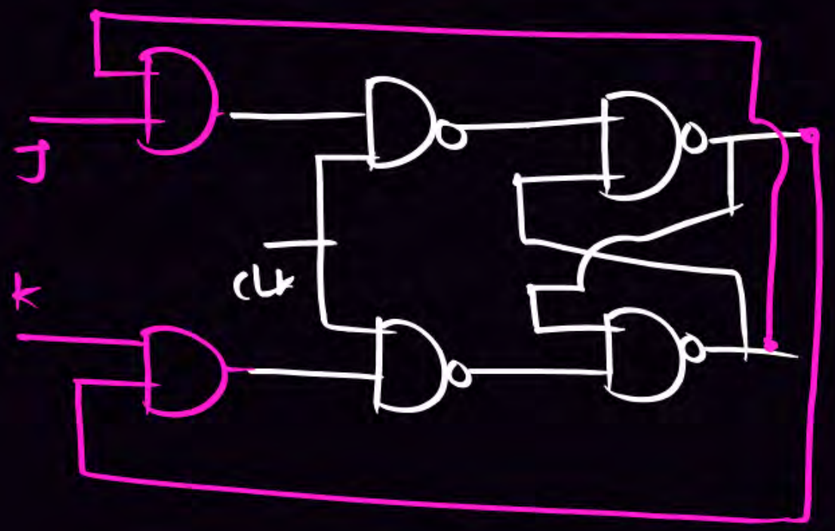


S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

$$Q_{n+1} = S + \bar{R}Q_n$$

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

JK FF



J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

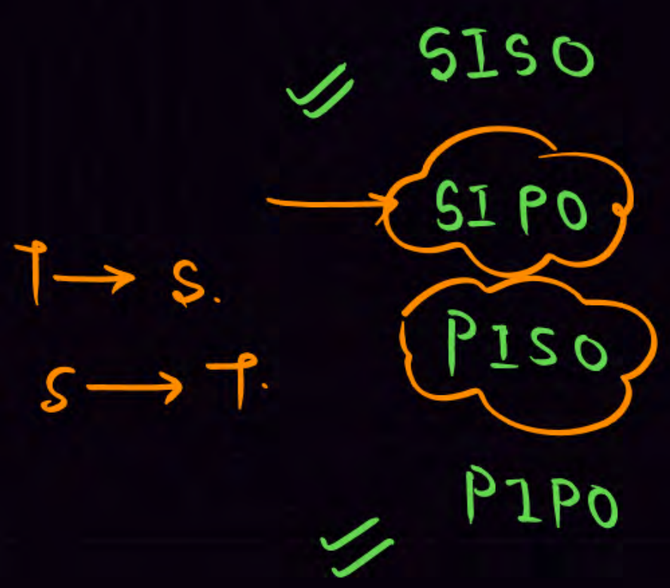
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D-FF

$$Q_{n+1} = D$$

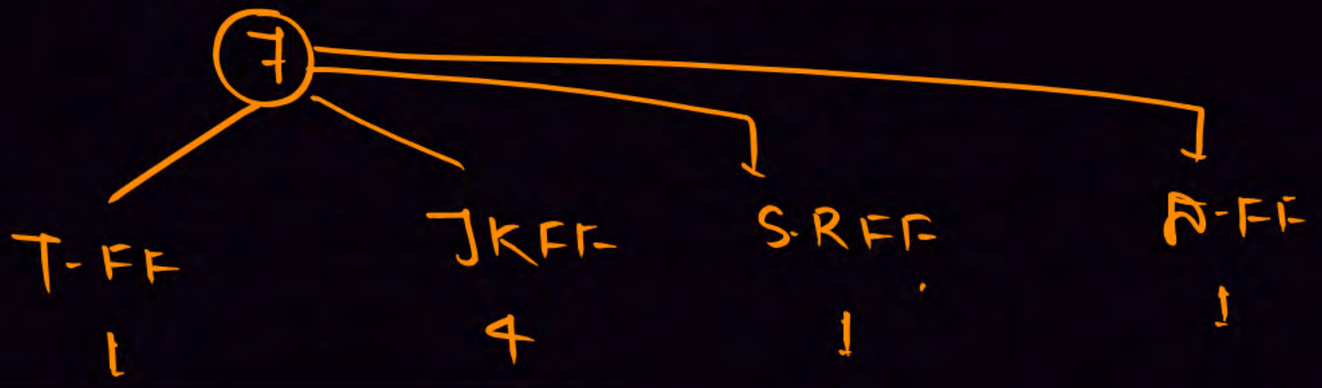
T-FF

$$Q_{n+1} = T \oplus Q_n$$



	Store	Retrive
SISO	n	n-1
SIPO	n	0
PISO	1	n-1
PIPO	1	0

Toggle Mode of FF :→



COUTERS

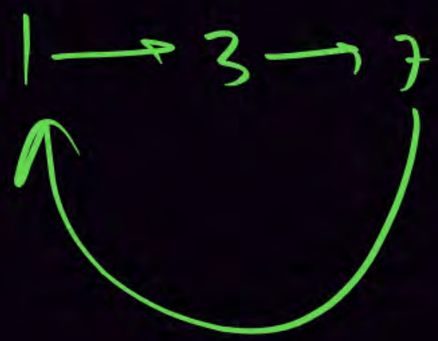
Maximum no. of states $= 2^n$ ← no. of FF's.

$M \leq 2^n$

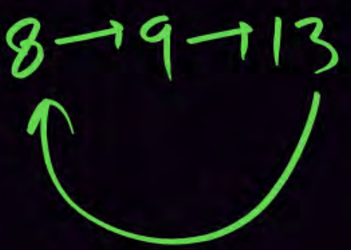
↑

Modulus

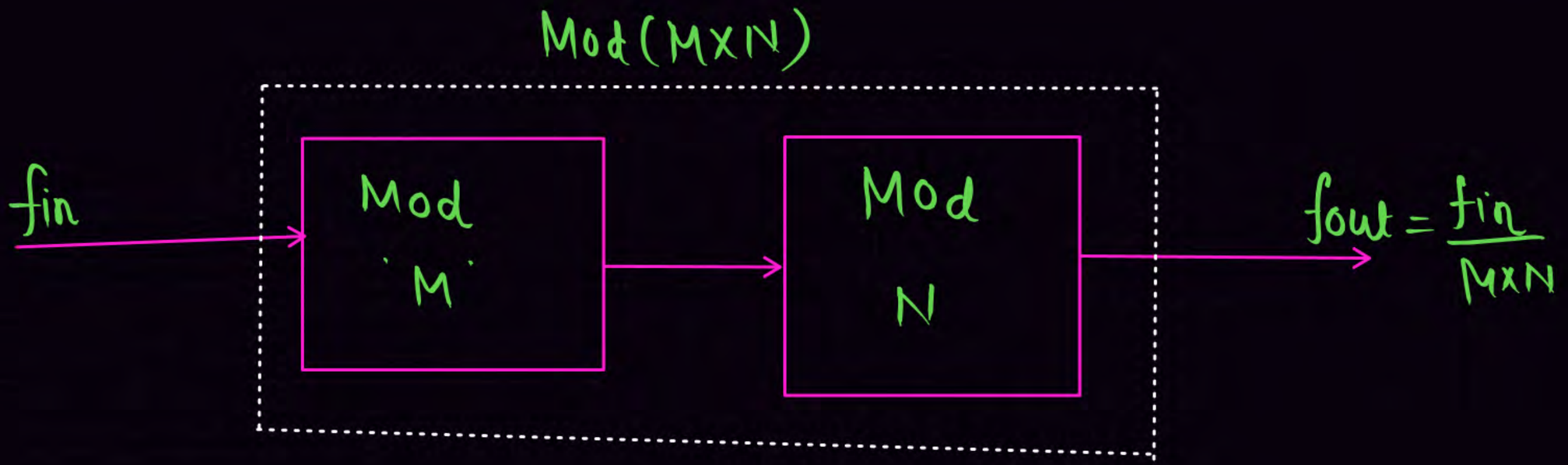
$n \geq \log_2 M$



Mod = 3



Mod = 3.


Mod (M x N)
fin
Mod M
Mod N
fout = fin / M x N

Counter

Synchronous counter

- fast
- all counting

Ring
Johnson.

Asynchronous counter

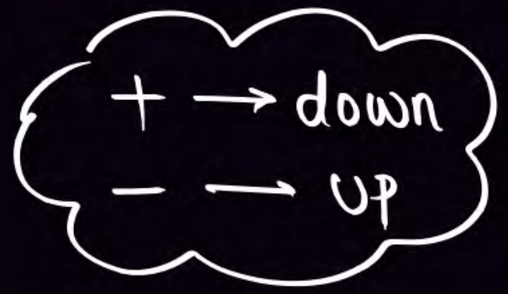
slow

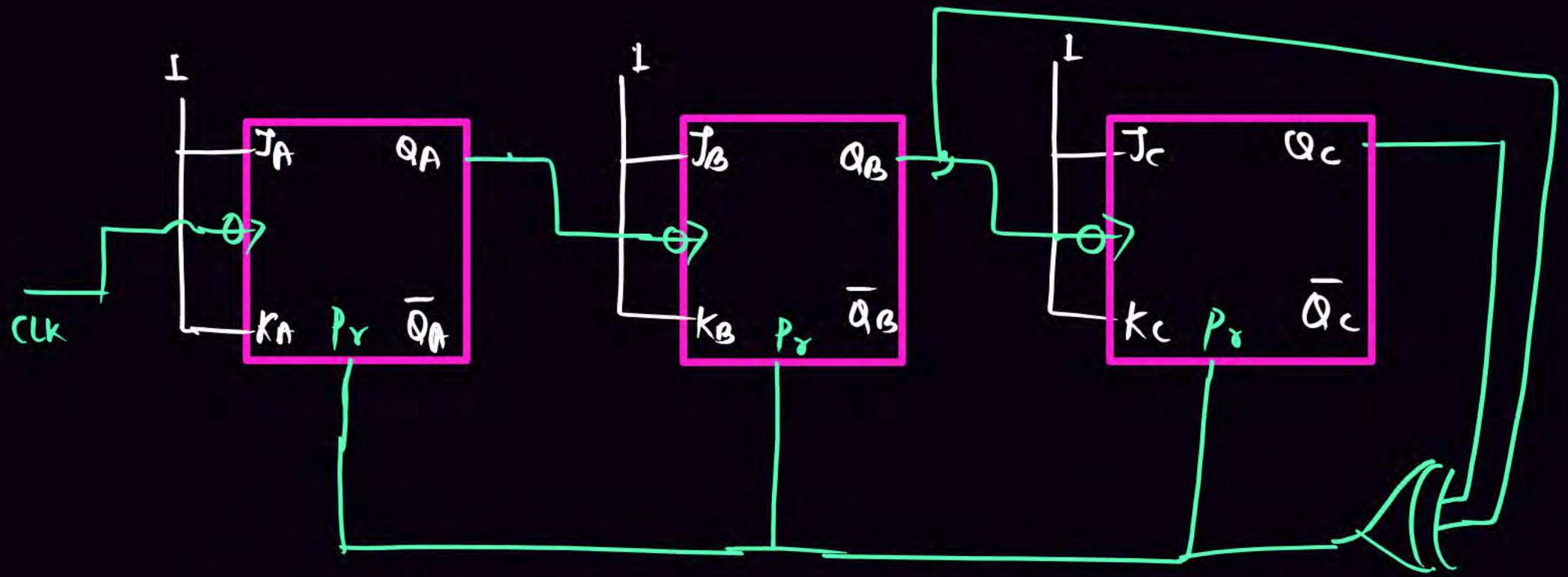
↑ ↓

Ripple counter.

Asynchronous counter :→

↳ Full mod.



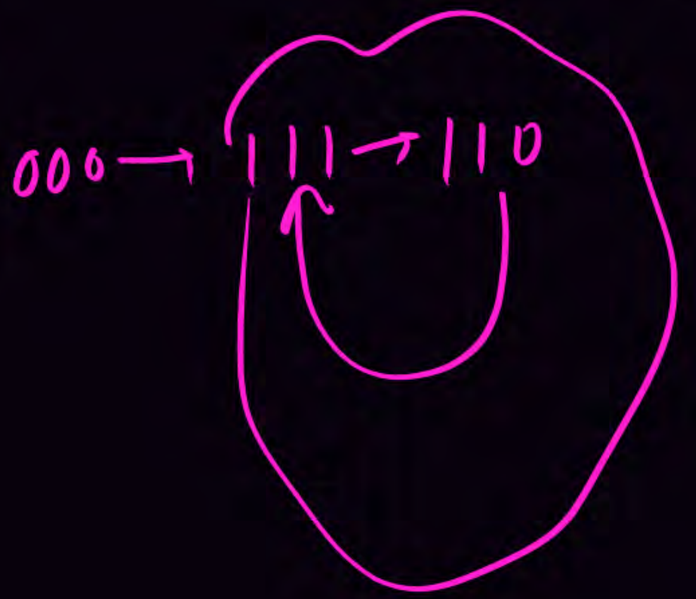


CLK	Q_C Q_B Q_A	$P_r = Q_C \oplus Q_B$
0	0 0 0	0
1	0 0 1	0
2.	0 1 0	1
3.	0 0 0	0

$000 \rightarrow 001 \rightarrow 111$

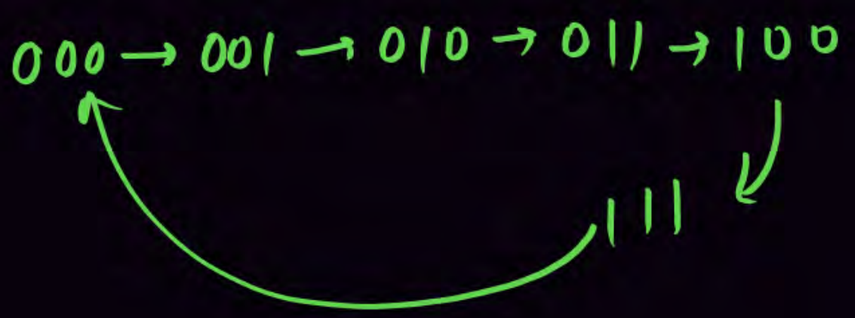
Mod = 3

CLK	Q_C	Q_B	Q_A	$P_r = Q_C \bar{Q}_B Q_A$
0	0	0	0	0
1	1	1	1	0
2	1	1	0	0
3	1	0	1	1 → 0
4	1	1	0	0
5	1	0	1	1 → 0



Mod = 2

CLK	Q_C Q_B Q_A	$P_X = Q_C \bar{Q}_B Q_A$
0	0 0 0	0
1	0 0 1	0
2.	0 1 0	0
3.	0 1 1	0
4	1 0 0	0
5	1 0 1	1 → 0
6.	0 0 0	0
7	0 0 1	0



Mod- 6

$$T_{clk} \geq n \cdot \tau_{pd_{ff}}$$

$$f_{clk} \leq \frac{1}{n \cdot \tau_{pd_{ff}}}$$

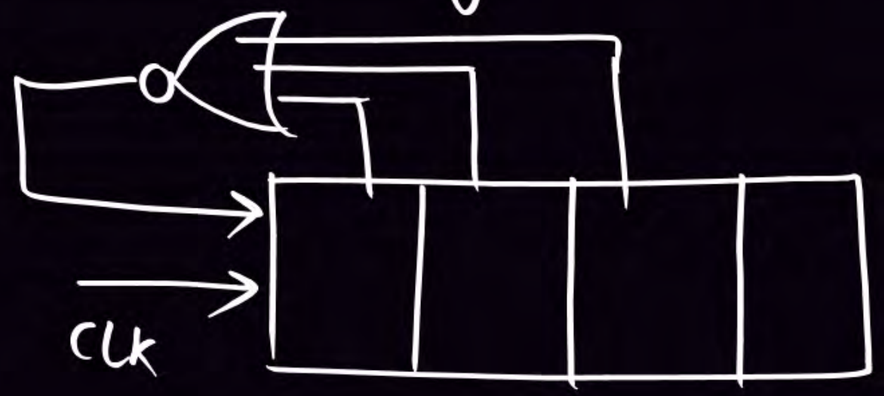
$n \rightarrow$ no. of FF's

$\tau_{pd_{ff}} \rightarrow$ propagation delay of FF

Synchronous counter

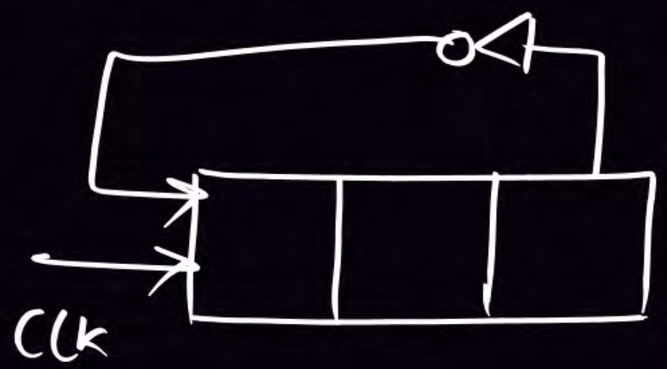
① Ring counter

n bit Ring counter ⟶ Mod = n



② Johnson counter :→

Mod = 2n



Lockout problem

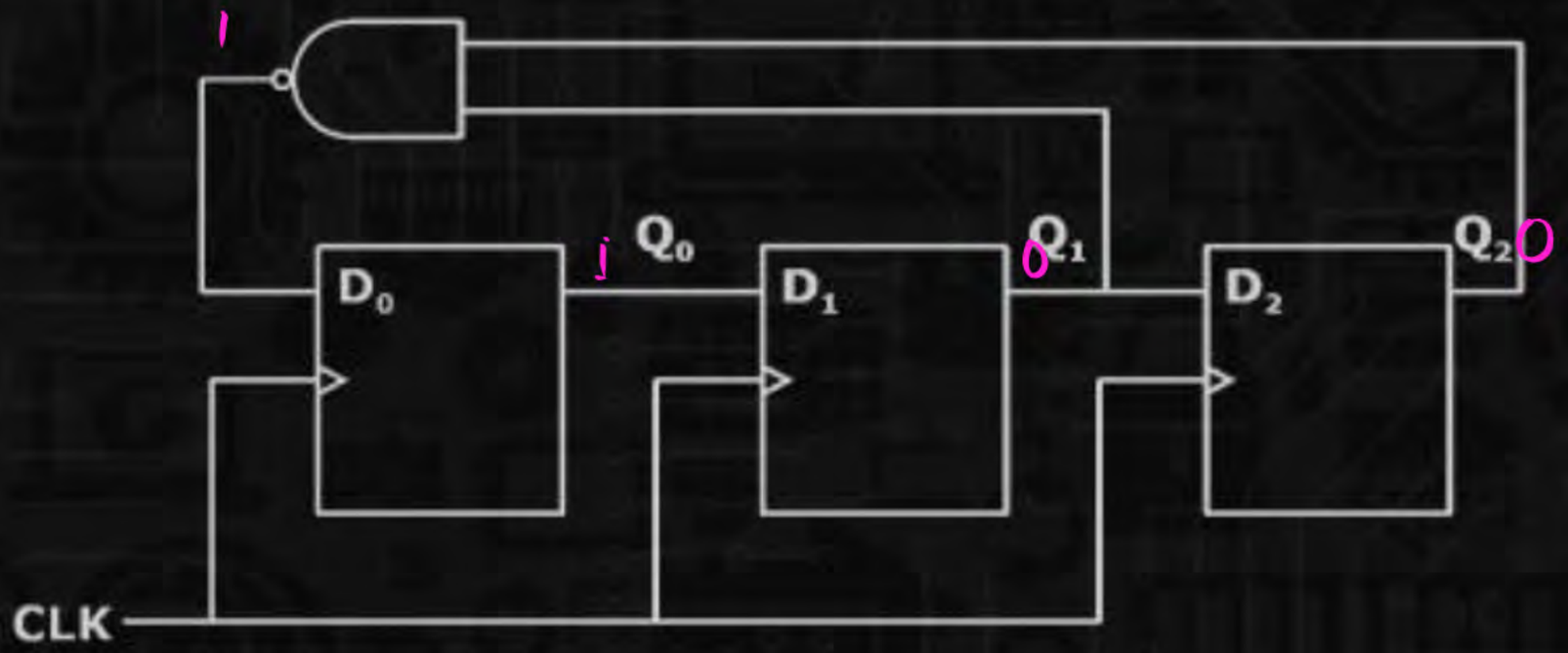
$$\left\{\begin{matrix} 0 & 1 & 0 \\ 1 & 0 & 1 \end{matrix}\right\} \text{MOD-}\underline{2}$$

0 1 0

1 0 1

Synchronous counter design :→

1. In the circuit shown below, initially all flip-flops are reset. The output $Q_2\ Q_1\ Q_0$ after four clock pulses is _____.



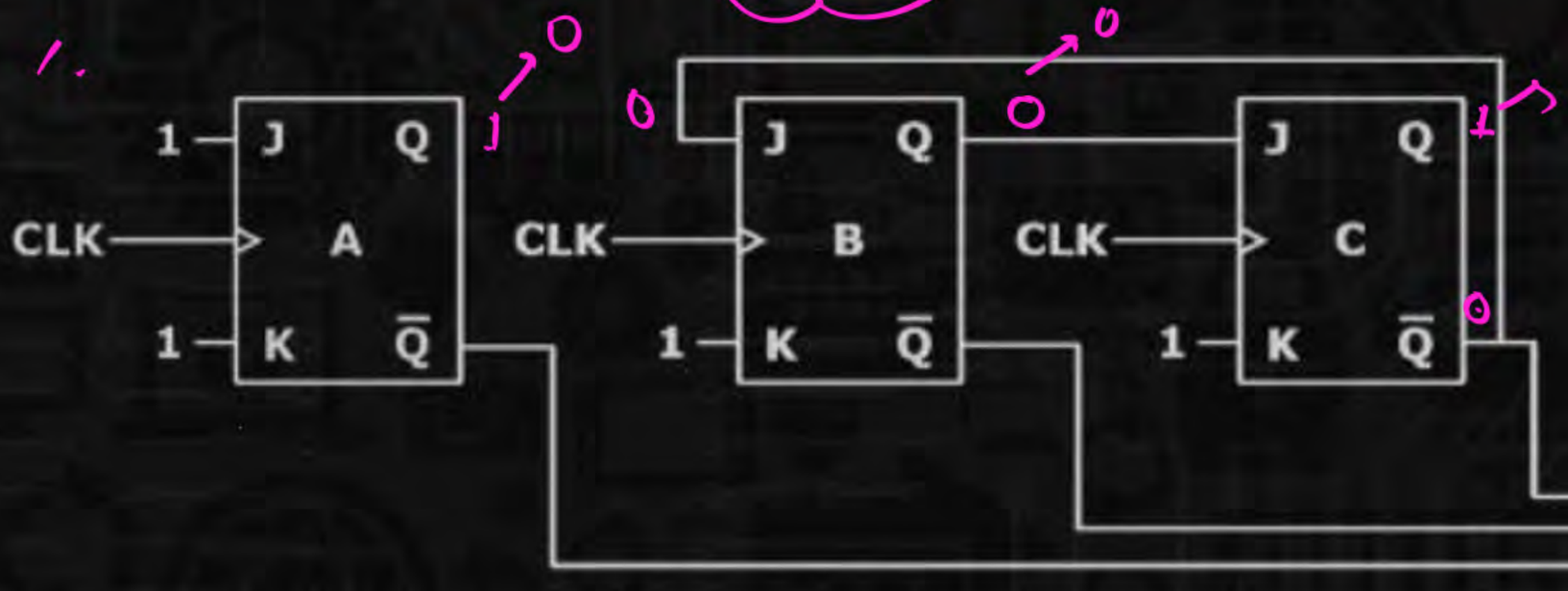
$\overline{Q_1 Q_2}$

CLK	Q_0	Q_1	Q_2
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1

$Q_2 Q_1 Q_0 = 110$

2. Consider a sequential circuit using three J-K flip-flops and one AND gate shown in figure. Output of the circuit becomes '1' after every N-clock cycles. The value of N is

N = 6



CLK	Q_A	Q_B	Q_C	Z
0	0	0	0	1
1	1	1	0	0
2	0	0	1	0
3	1	0	0	0
4	0	1	0	0
5	1	0	1	0
6	0	0	0	1
7	1	1	0	0
8	0	0	1	0
9	1	0	0	0
10	0	1	0	0
11	1	0	1	0
12	0	0	0	1

3. If we are designing the counter by using DFF which count 0 → 1 → 2 → 4 → 0 →..... The unused state must go to zero (000) on the next clock pulse, if output is considered as $Q_3Q_2Q_1$ then expression for D_1 will be –

A. $\bar{Q}_3Q_2\bar{Q}_1$

B. $\bar{Q}_3\bar{Q}_2Q_1$

C. $\bar{Q}_3\bar{Q}_2\bar{Q}_1$

D. $Q_3\bar{Q}_2Q_1$

Q_3 Q_2 Q_1	Q_3^+ Q_2^+ Q_1^+			
0 0 0	0 0 1			
0 0 1	0 1 0			
0 1 0	1 0 0			
0 1 1	0 0 0			
1 0 0	0 0 0			
1 0 1	0 0 0			
1 1 0	0 0 0			
1 1 1	0 0 0			

$D_1 = Q_1^+ = \bar{Q}_3\bar{Q}_2\bar{Q}_1$

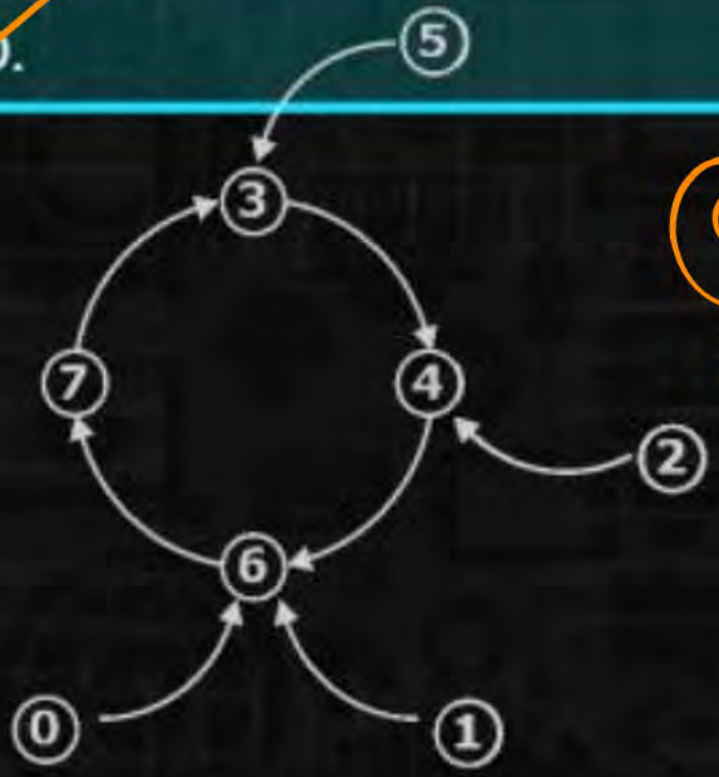
4. Which is/are correct for the given circuit-

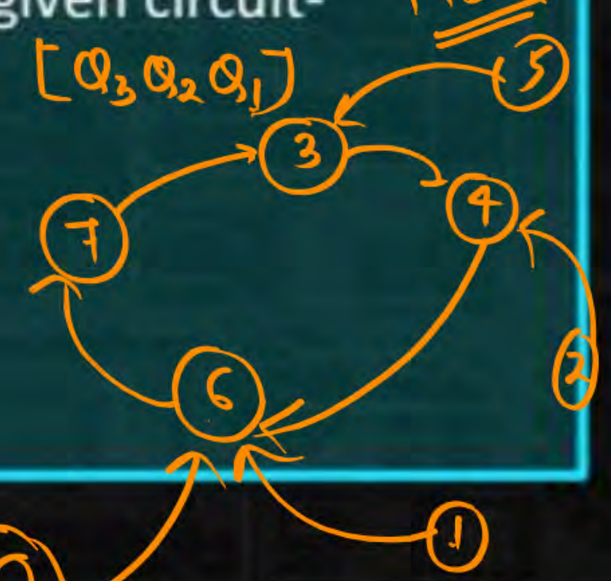
A. If is self starting counter

B. It have mod 4

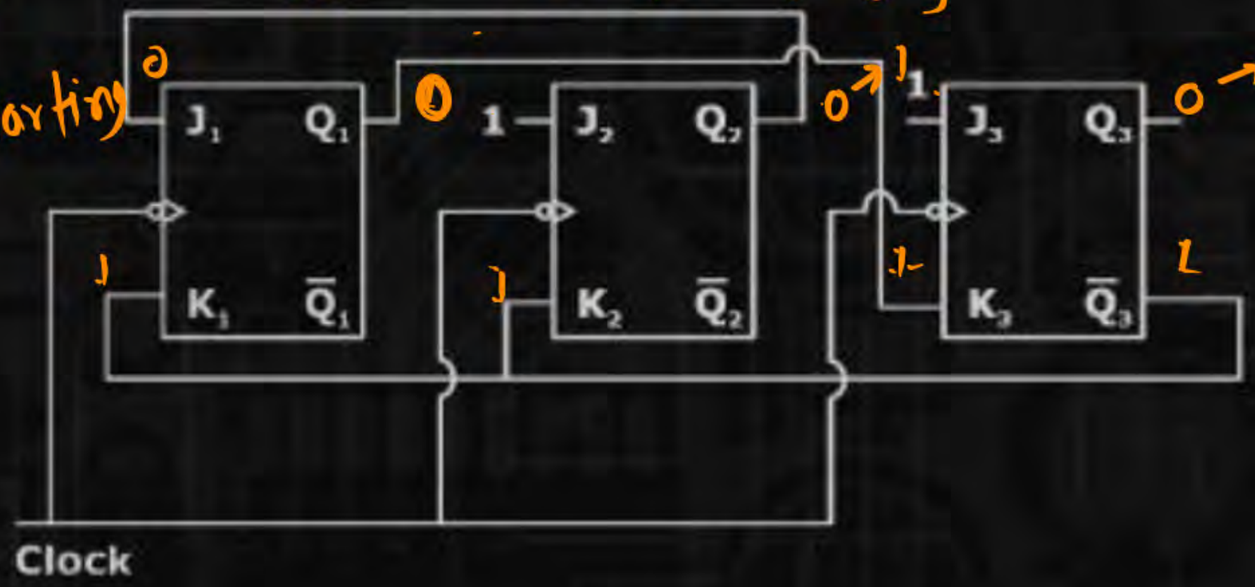
C. 5 is a invalid state

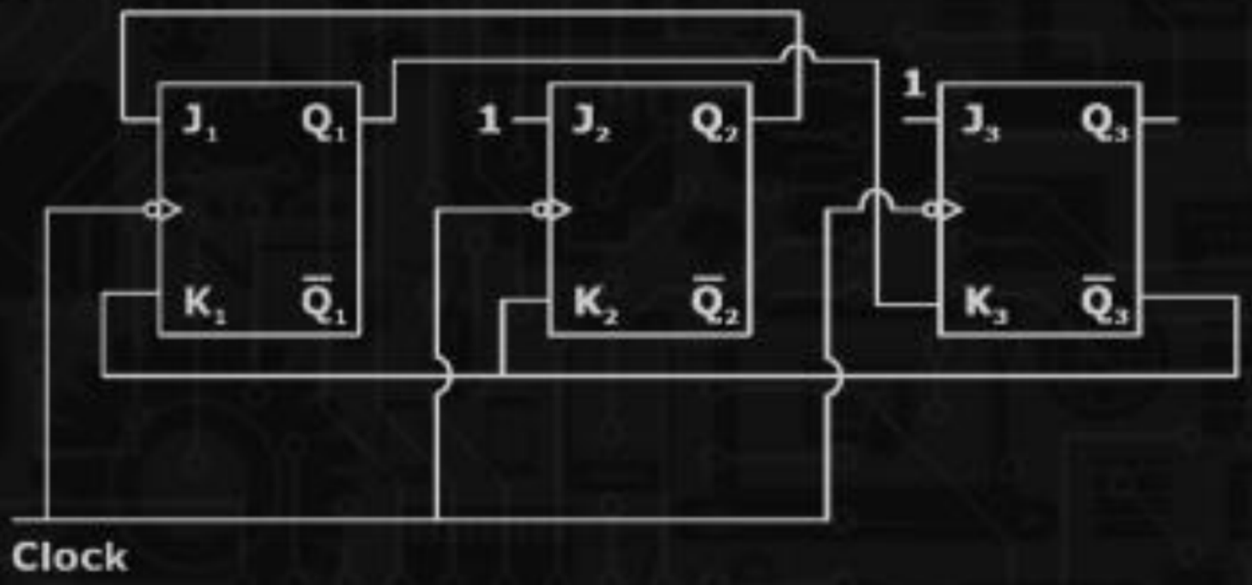
D.





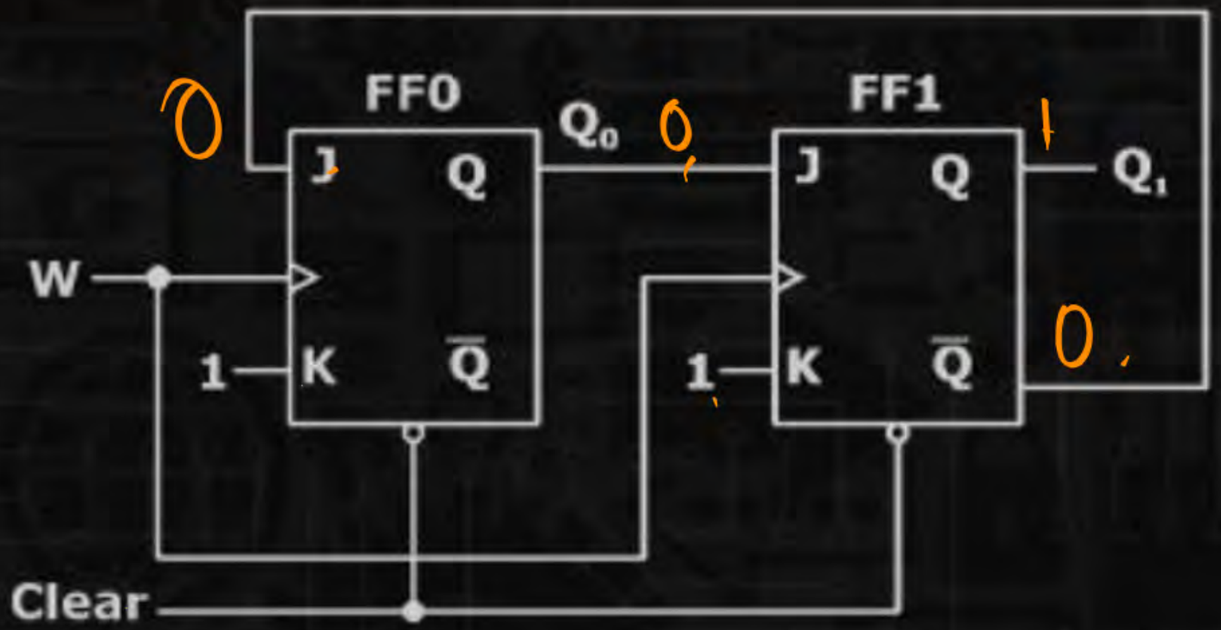
clk	Q_3 Q_2 Q_1
0	0 0 0
1	1 1 0
2.	1 1 1
3.	0 1 1
4	1 0 0
5	1 1 0




J1
Q1
K1
Q̄1
1
J2
Q2
K2
Q̄2
1
J3
Q3
K3
Q̄3
Clock

5. What function is implemented by the circuit shown below? Assume the signal w is driven by a square wave signal.

A. Modulo-3 counter
B. Modulo-4 counter
C. Modulo-5 counter
D. Modulo-6 counter



CLK	Q_1	Q_0
0	0	0
1	0	1
2	1	0
3	0	0

Mod = 3

6. Output is considered as Q3Q2Q1 and initially all the FF's are in rest condition.

MSQ.

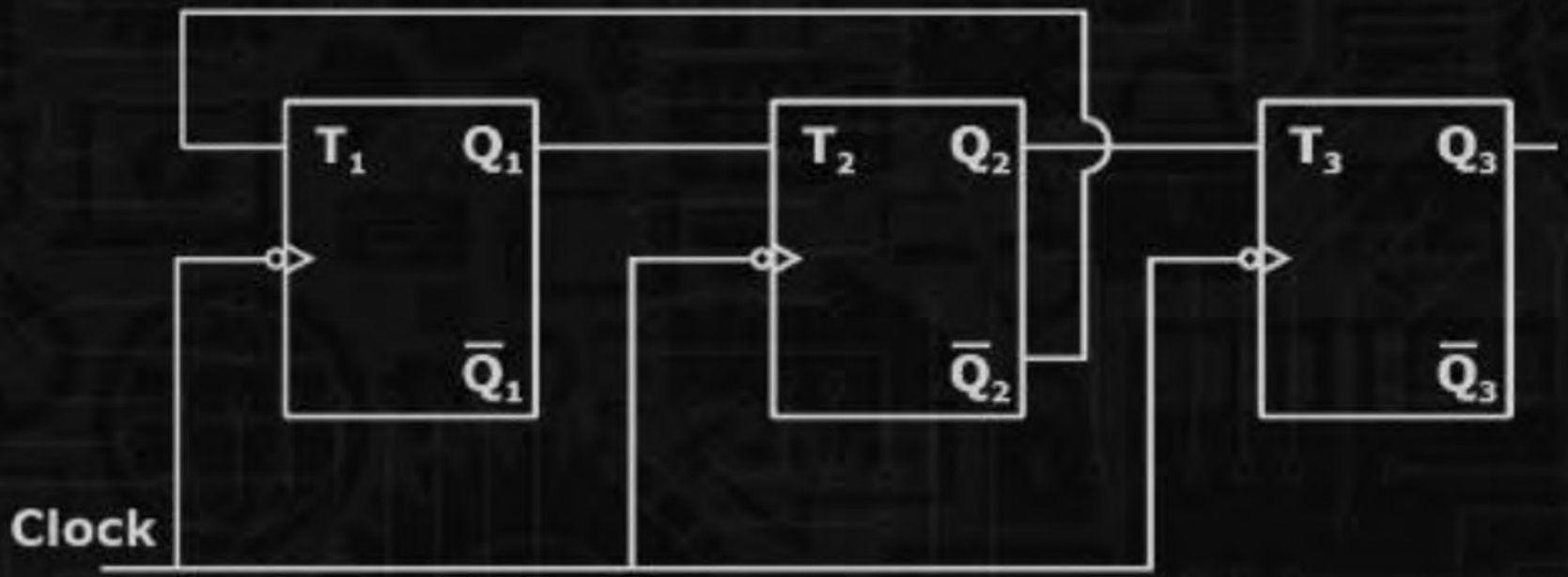
Which is/are correct for the given circuit?

A. MOD 4

B. It has lock out problem.

C. It will count 0 → 3 → 5 → 6 → 0

D. It will count 0 → 4 → 3 → 6 → 0



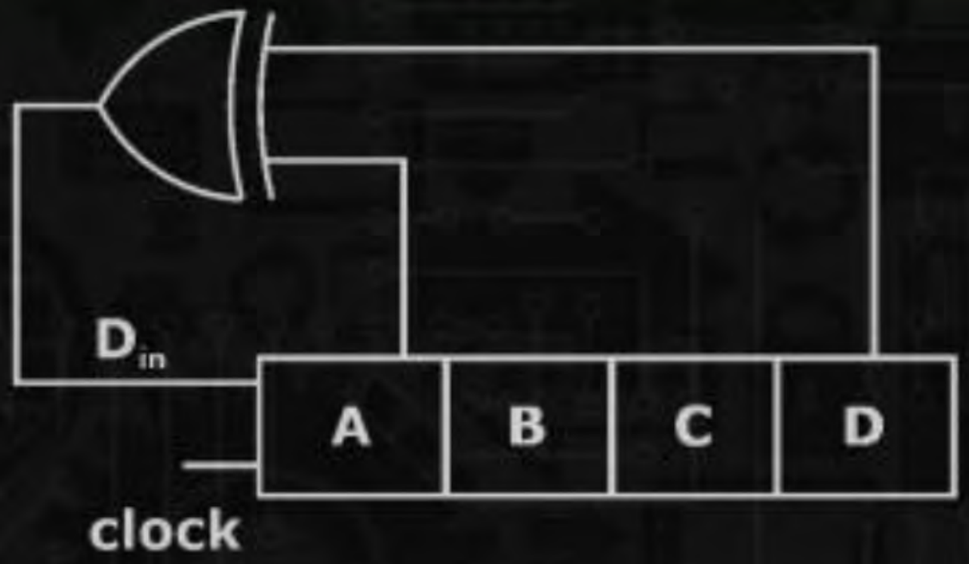
7. A 4-bit shift register circuit configured for right-shift operation (D_{in}-> A, A-> B , B-> C, C -> D), is shown. If the present state of the shift register is ABCD = 1101, the number of clock cycles required to reach the state ABCD = 0100 is

A. 3

B. 7

C. 4

D. 5



8. If 5 toggle mode FF are used to design asynchronous counter, starting 2 FF having propagation delay 2 ns and last 3 FF having propagation delay 3ns, then maximum clock frequency for reliable operation will be_____.

9. Three binary ripple counters, modulo-A, modulo-B and modulo-C respectively, are connected in cascade. For counting modulo-500, which of the following are correct solutions?

A. A = 10, B = 10, C = 5

B. A = 150, B = 200, C = 150

C. A = 25, B = 2, C = 10

D. A = 10, B = 20, C = 25

10. –13 in 2's complement will be-

A. 1 1 1 0 1

B. 0 1 1 0 1

C. 1 0 0 1 0

D. 1 1 0 0 1 0

E. None

11. –24 in 2's complement form is

A. 11101000

B. 01001000

C. 01111111

D. 00111111


THANK YOU GW
SOLDIERS !