CS & IT



ENGINEERING



Combinational Circuit



Lecture No. 07



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TOPIC,S TO B,E COVER1ED 01 HS

02 FS

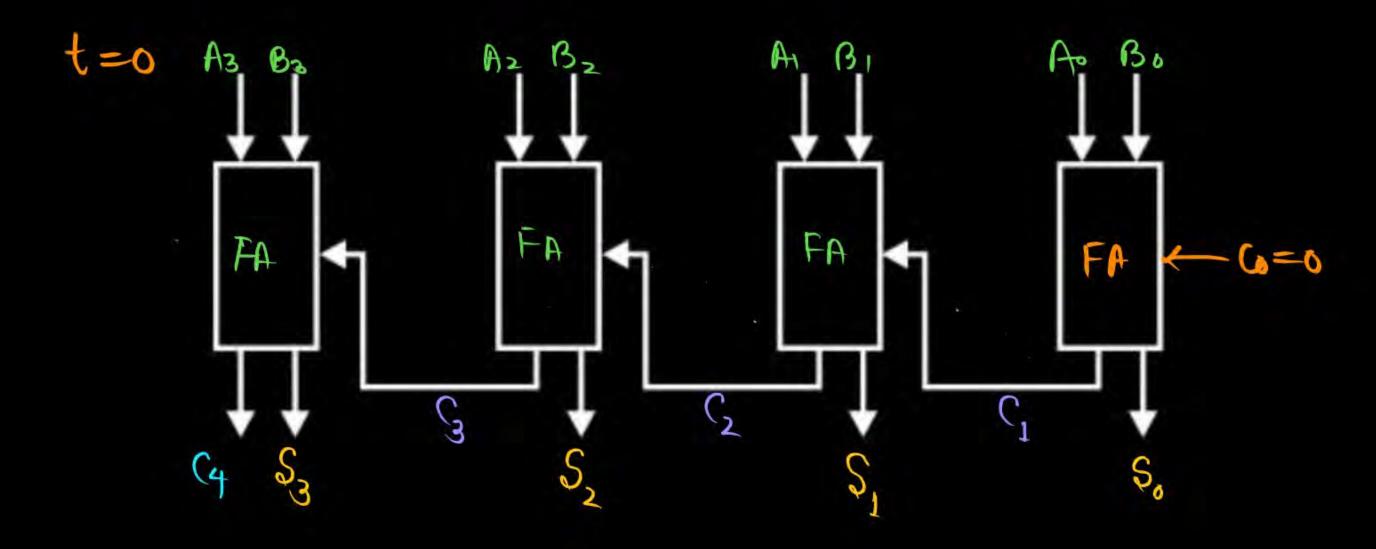
03 SERIAL ADDER

04 PARALLEL ADDER

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PARALLEL ADDER [Ripple Carry Adder]:-



n bit Parallel adder

Pw

- (n-1) FA + 1 HA
- (2) N-FA
- (3) (2n-1) HA+ (n-1) OR

Relay

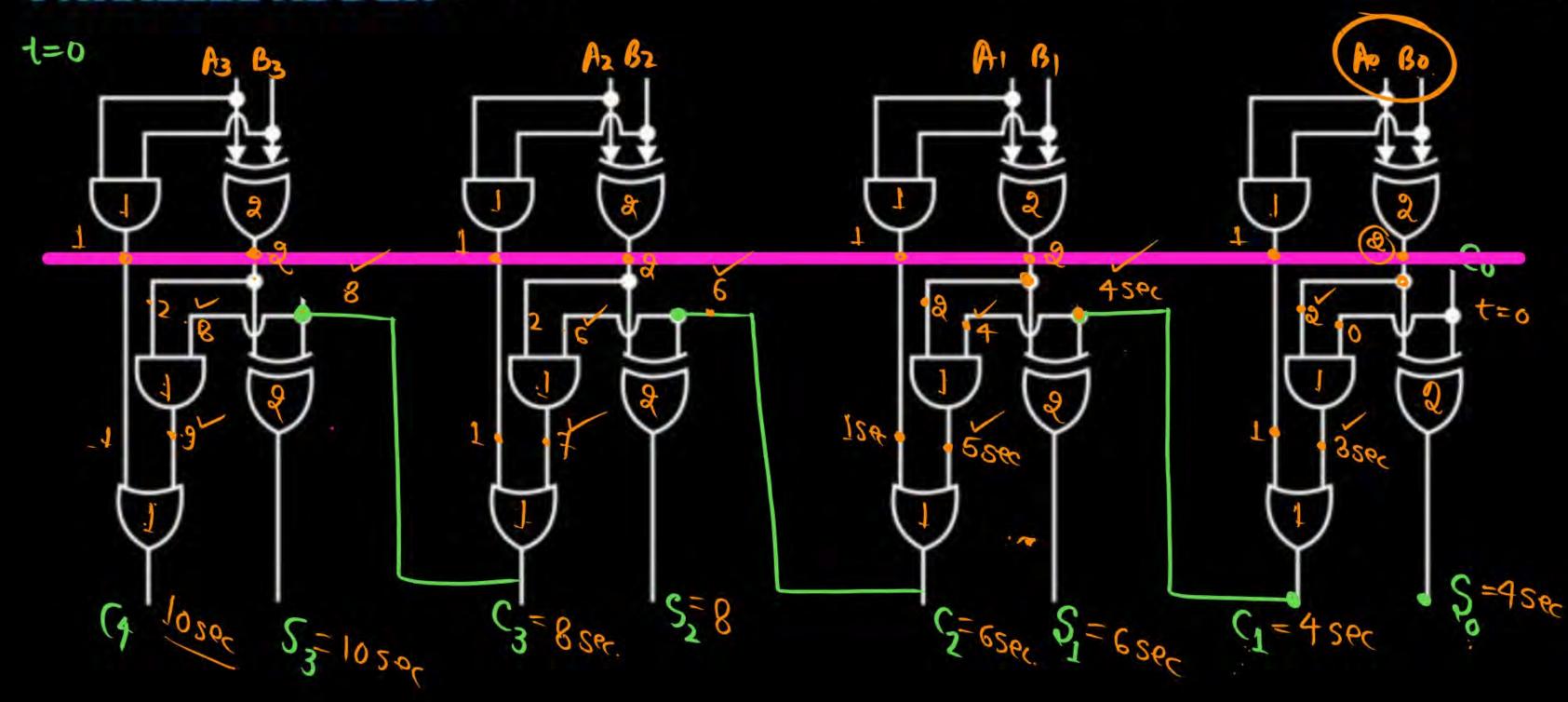




TXOR = 2 second TAND=TOR=1 second



PARALLEL ADDER [46it]



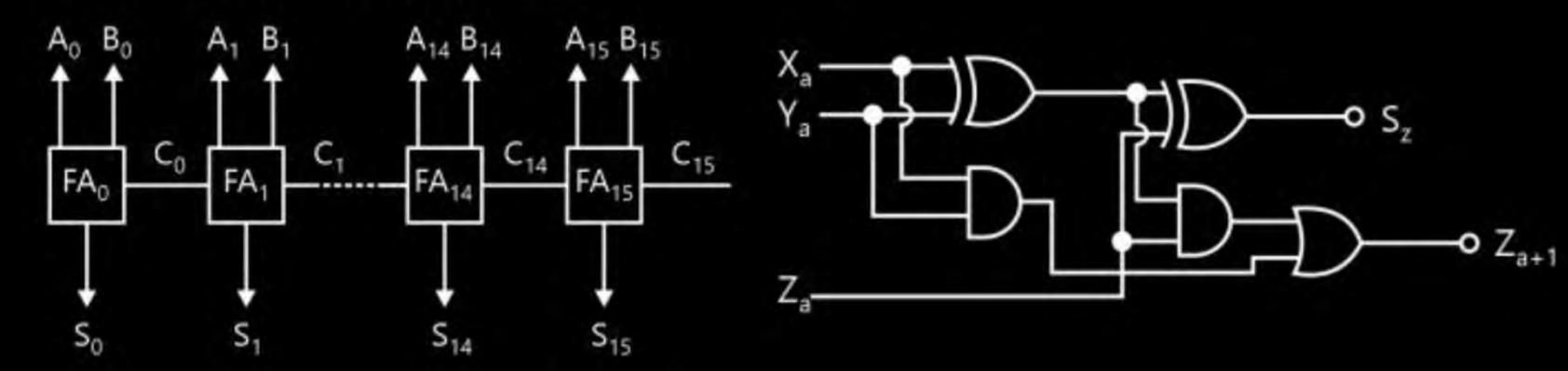


$$T=(4-1)\{1+1\}+ Mox\{4,4\}$$
 $T=3x2+4$
 $=10\mu s$



Q.3

A 16-bit ripple carry adder is realized using 16 identical full adders (FA) as shown in the figure. The carry-propagation delay of each FA is 12 ns and the sum-propagation delay of each FA is 15 ns. The worst case delay (in ns) of this 16-bit adder will be ____.





$$T = Cn-1)Tcarry + Max {Tsum, Tcarry}$$

$$= (16-1) \times 12ns + Max { 15ns, 12ns}$$

$$= 15 \times 12 + 15$$

$$= 195 \text{ ns}$$



Q.4

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple-carry binary adder is implemented by using full adders. The total propagation time of this 4-bit binary adder in microseconds is,

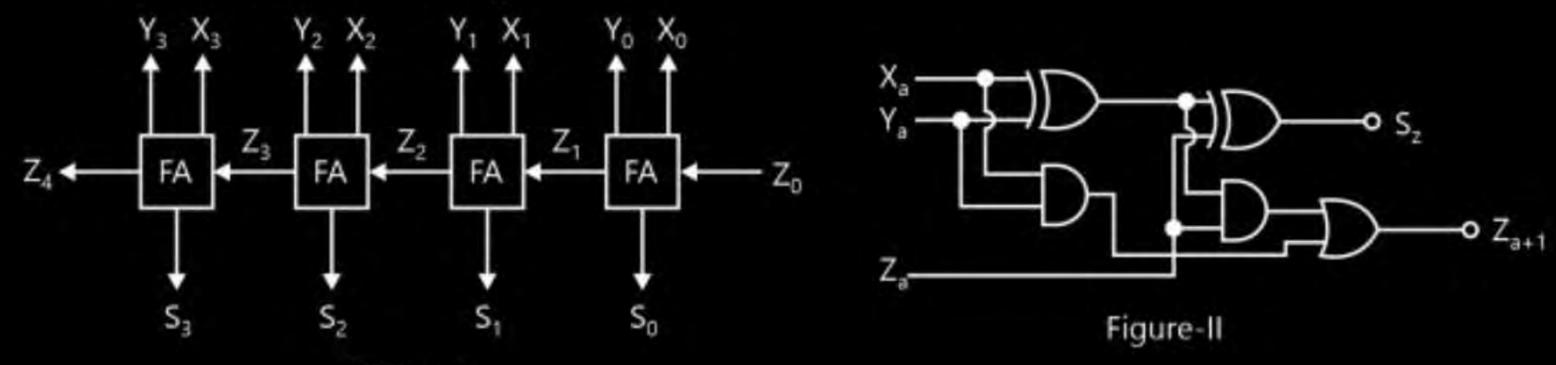


Figure-I



Tsum=2 TxoR

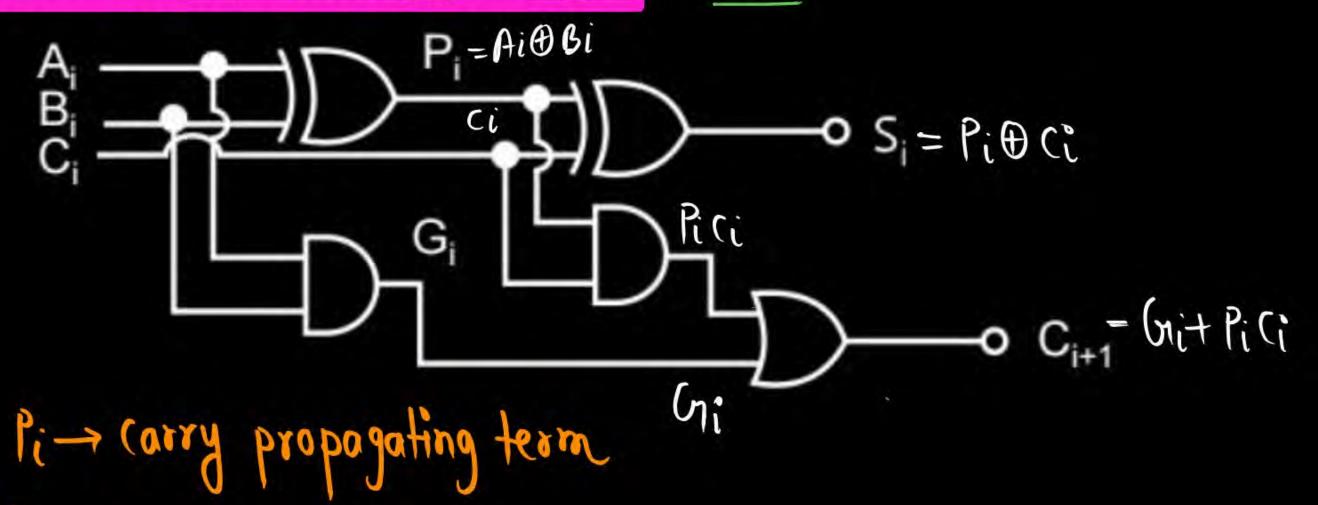
- = 3x {1.2+1.2}+2x2.4
- = 3×2-4+4.8
- = 12 ms

LOOK AHEAD CARRY ADDER [LACA]

(ni-) (arry generating term

7 fastest Adder among all the





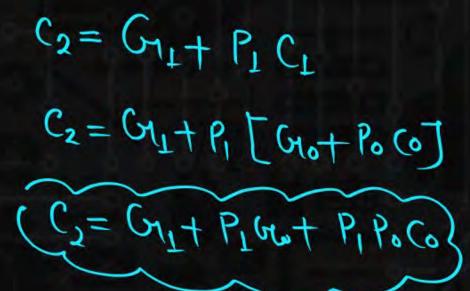
$$P_1 = A_1 \oplus B_1$$

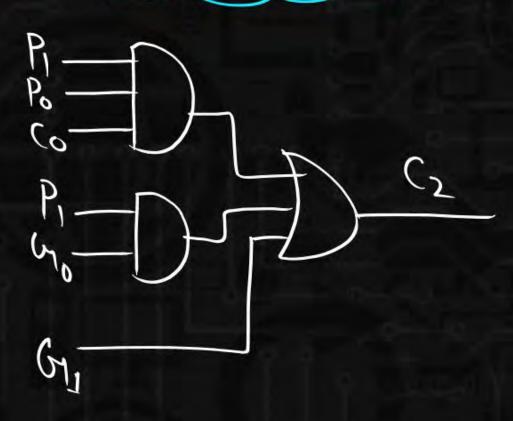
Voi= Ai Bi

$$M^{5} = H^{5}B^{5}$$

$$S_1 = P_1 \oplus C_1$$

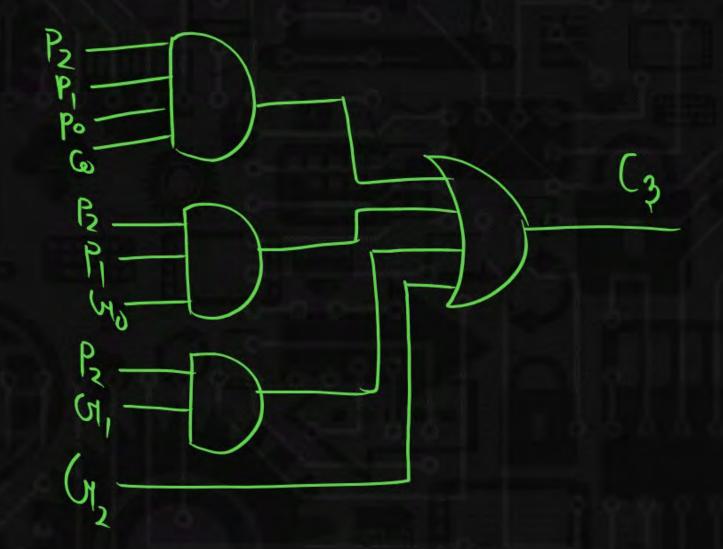
City = Gnit Pi Ci



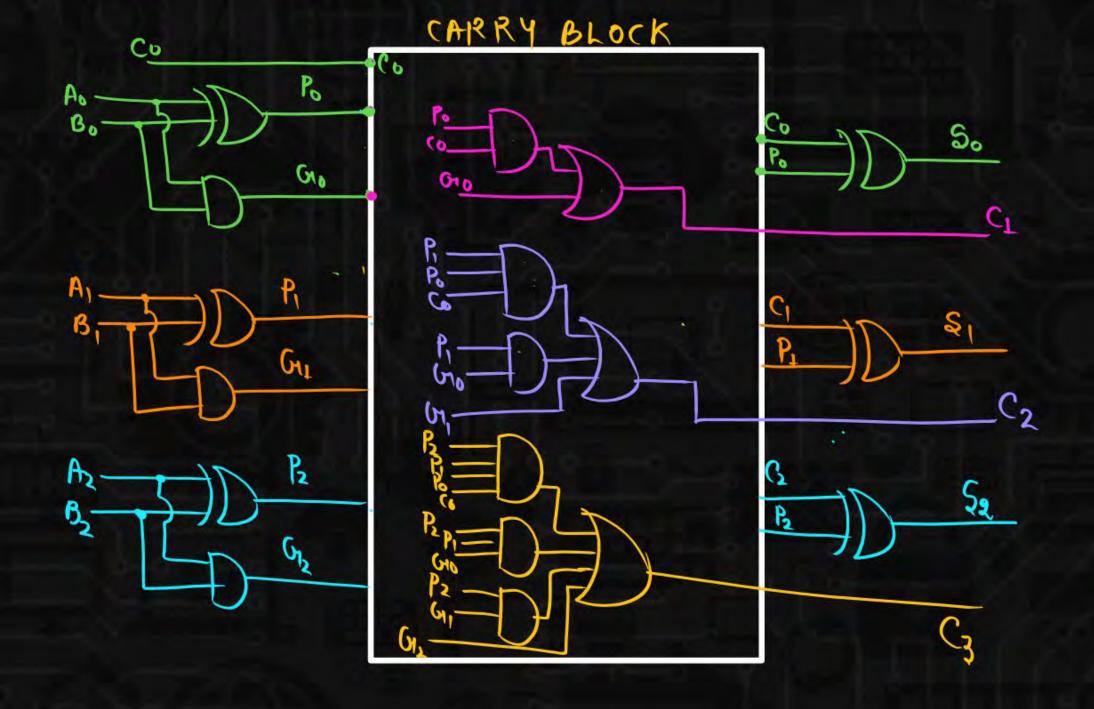




(3= M2+ P2 C2 (3= M2+ P2 [M1+ P1M0+ P1P0 (0)] (3= M2+ P2 M1+ P2 P1 M0+ P2 P1P0 (0)









CARRY Brock will be always two Level implementation.

Delay for corry Block

H For entire Circuit

47

'h' bit LACA

Pw

For Carry Block

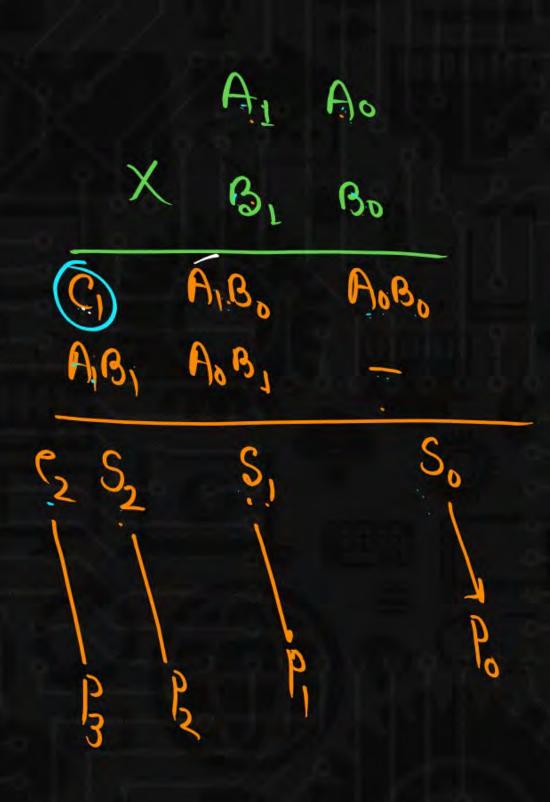
No of AND GIATE =
$$\frac{n(n+1)}{2}$$

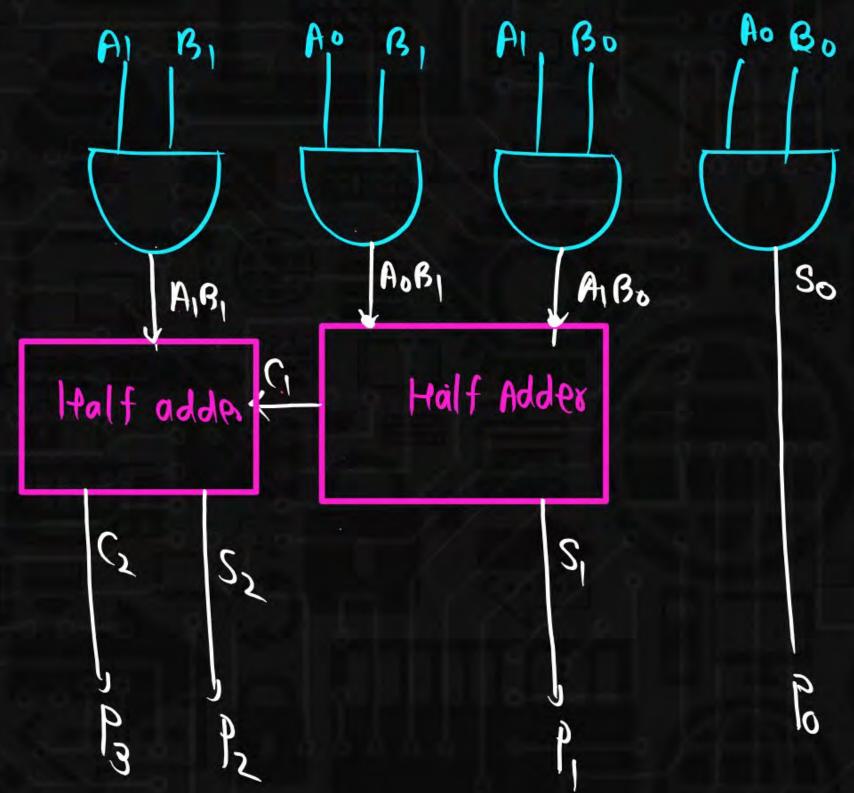
Multiplier:>

Pw

2bit







His
Besign
$$A = A_2 A_1 A_0$$

 $X B = B_1 B_0$



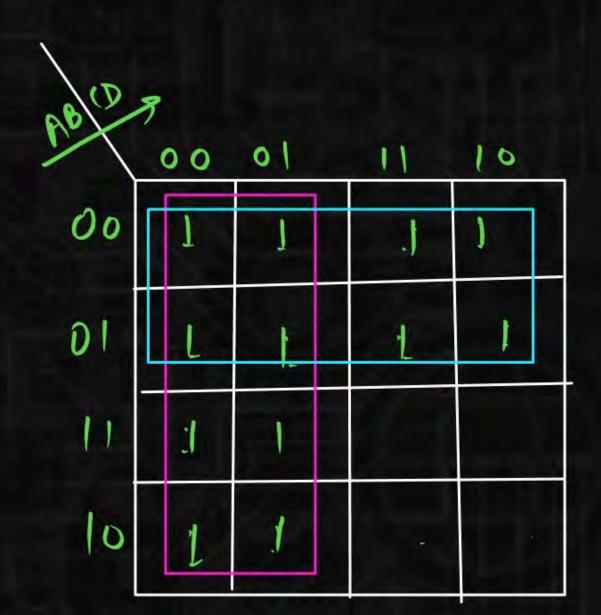


Q Resign a circuit in which 4 inputs A,B,C,D are there.

if in decimal AB=X and (D=Y) Then if X,Y < 3 Then ofp
will be high otherwise Low.

X:Y < 0

A	В	C :	1	X.y	7
0	0	0	0	0	1
0	0	D	1	0	1.
0	O	1	0	0	1.
0	0	1)	0	1.
0	1	0	0	0	1.
0	Į	D	J	1	4
0	1	j.		2	1
0	1	1	J	3	1
1.	0	0	0	0	1
1	Ó	0	1	2	1.
1	0	Į.	0	4	٥
1	0	1	1	6	0
1	Į	0	0	0	J
1	J	6	Ţ	3	1
1	J	1	0	6	0
1-	1	1	1	9	0





combinational circuit { static circuit }



MUX DE-MUX

Encoder, Decoder

99

F.S



HA

S= ADB

G= AB

(5)

FA

SUM= ABBOC

Carry= Em (3,5,6,7)

=(AAB) (+ AB

= AB+AC+BC

9

H5

DIHE-ABB

CORTY = AB

DIFFLAGBE

(arm = Em (1,2,3,7)

= AB+ (ABB) (

= AB+AC+BC

(5)

9



Serial adder

Parallel add

T= (n-1) Tearry + Max & Tsum, Tearry &

T= (n-1) & Tant Top & + Max & Tsum, Tearry &



LACA
Toto Delay = 47
Carry Block = 27



Thank you

GW Soldiers!

