CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

CPU & Control Unit

Lecture No.- 02

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Recap of Previous Lecture

Topic CPU

Topic MIPS

Topics to be Covered

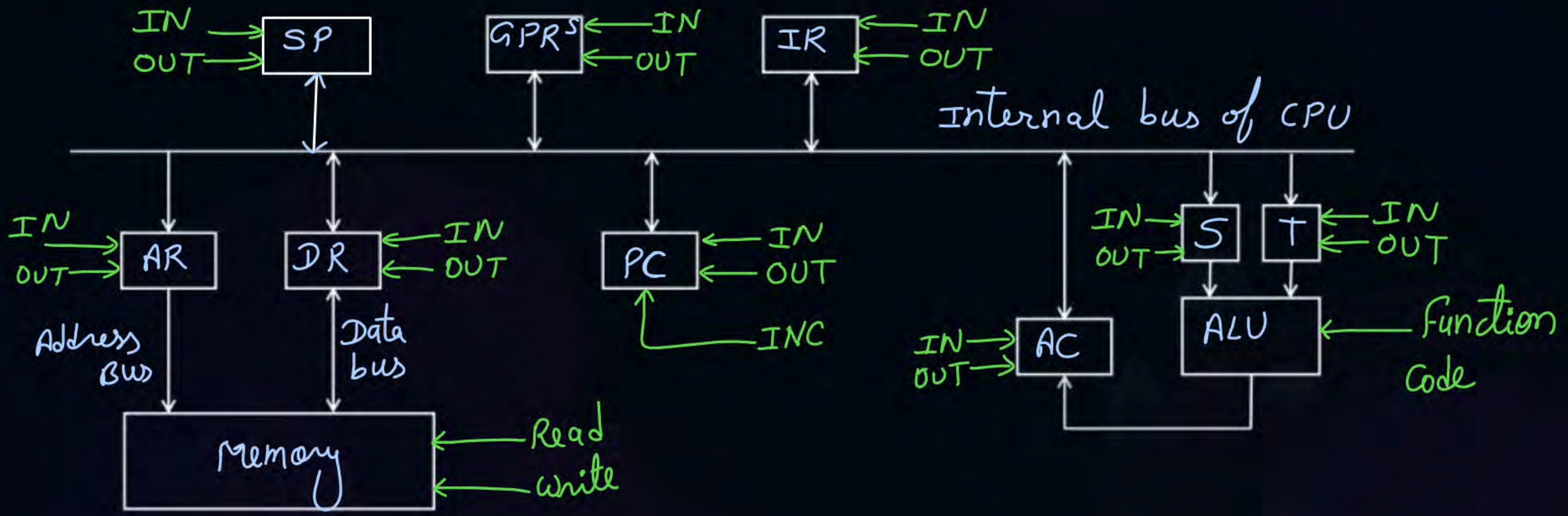
- **Topic** Data Path
- **Topic** Control Unit
- **Topic** Hardwired Control Unit

Topic : Datapath

Collection of functional units such as arithmetic logic units or ~~multipliers~~ multiplexers

to Perform data processing operations

Topic : Datapath



Topic : Datapath

assume all micro-operations take one CPU cycle except mem. access. mem. access takes 4 cycles

Instruction Fetch :-

$AR \leftarrow PC$ — 1

$DR \leftarrow M[AR]$ — 4

$IR \leftarrow DR$, $PC \leftarrow PC + 1$ — 1

no. of CPU cycles = 1 + 4 + 1 = 6

store current value of PC on stack in mem :-

$AR \leftarrow SP$ — 1

$DR \leftarrow PC$ — 1

$M[AR] \leftarrow DR$ — 4

no. of CPU cycles = 1 + 1 + 4 = 6

$R2 \leftarrow R0 + R1$

$S \leftarrow R0$

$T \leftarrow R1$

$AC \leftarrow S + T$

$R2 \leftarrow AC$

no. of CPU cycles = 4

Topic : Control Unit

It generates control signals and sends those signals to the components of Computer.

The Components will perform operation accordingly.

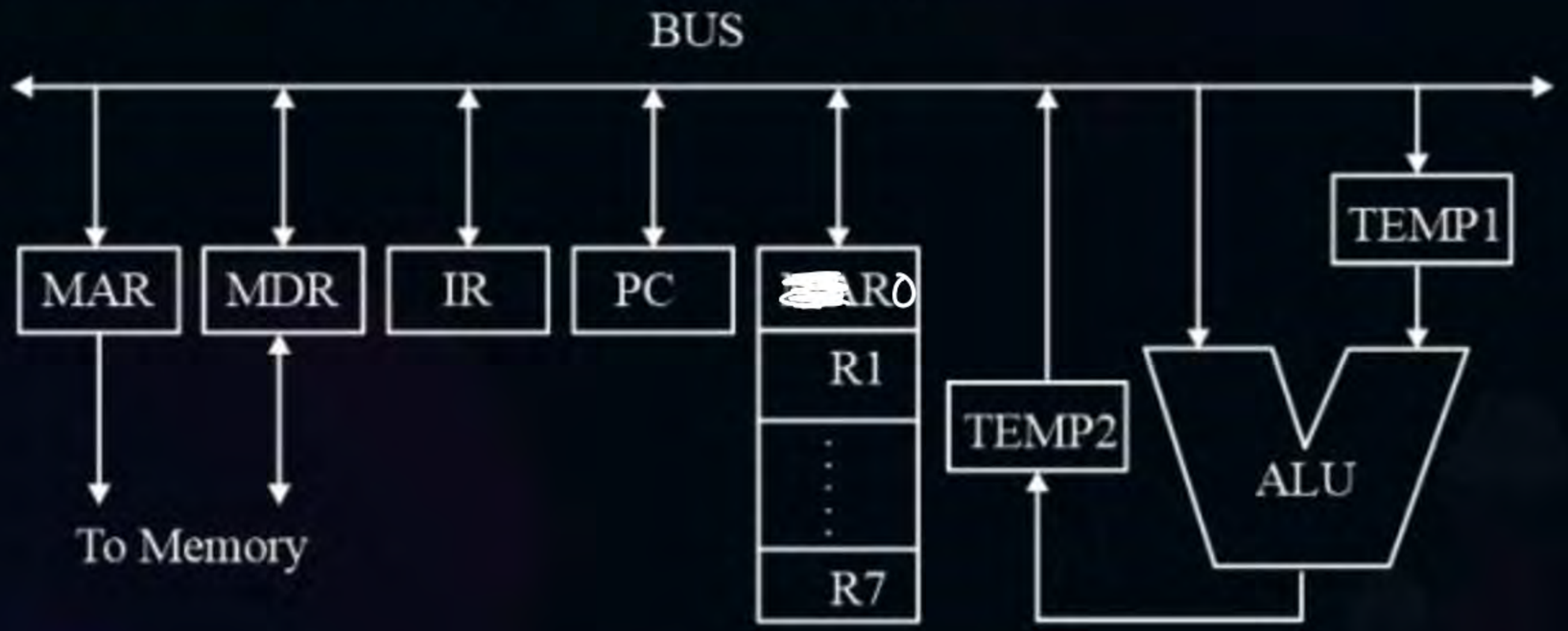
Instⁿ fetch :-

$AR \leftarrow PC$	PC_{out} , AR_{In}
$DR \leftarrow M[AR]$	AR_{out} , $Memory_{Read}$, DR_{In}
$IR \leftarrow DR$, $PC \leftarrow PC+1$	DR_{out} , IR_{In} , PC_{Inc}

[~~NAT~~]
MCQ

GATE PYQ – 2020

#Q. Consider the following data path diagram



[MCQ]

Consider an instruction: R0 ← R1 + R2. The following steps are used to execute it over the given data path. Assume that PC is incremented appropriately. The subscripts r and w indicate read and write operations, respectively.

1. $R2_r$, $TEMP1_r$, ALU_{add}, $TEMP2_W$
2. $R1_r$, $TEMP1_w$
3. PC_r, MAR_W, MEM_r
4. $TEMP2_r$, $R0_w$
5. MDR_r, IR_W

Which one of the following is the correct order of execution of the above steps

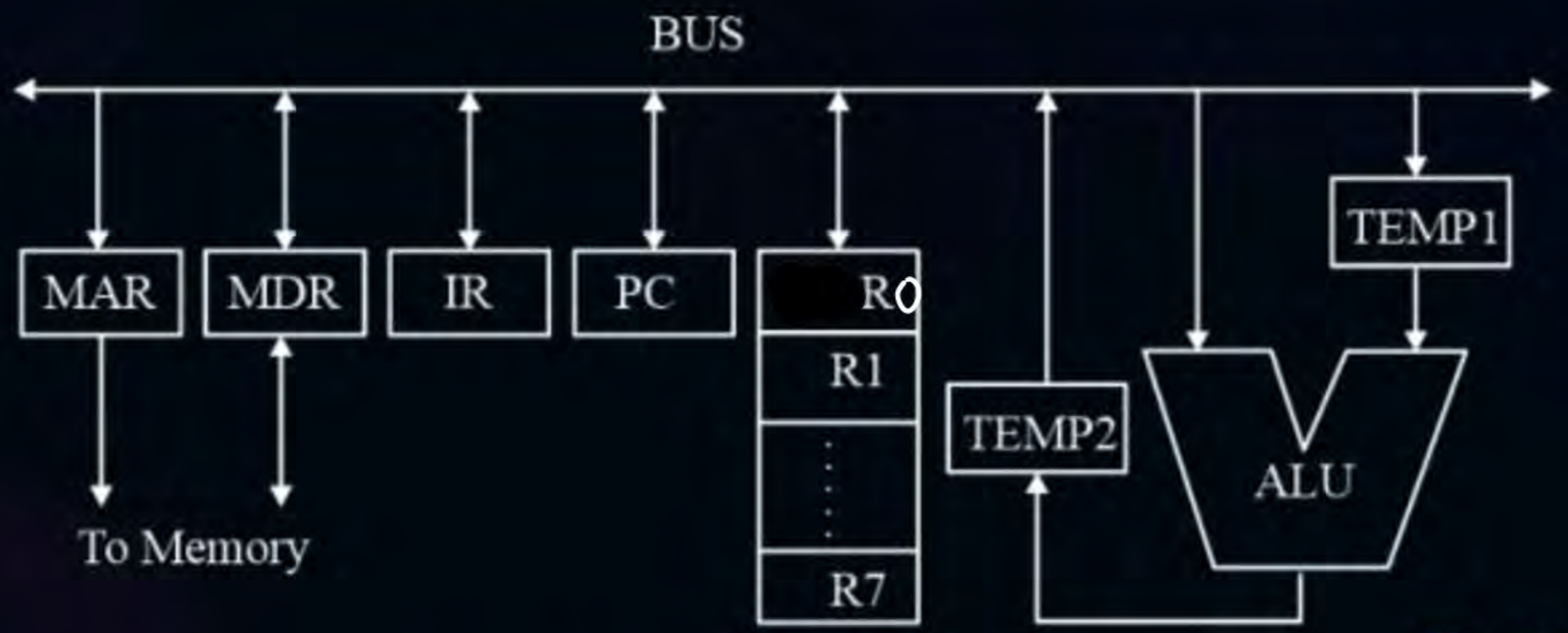
A 2, 1, 4, 5, 3

B 1, 2, 4, 3, 5

C 3, 5, 2, 1, 4

D 3, 5, 1, 2, 4

$R0 \leftarrow R1 + R2$



1. $R2_r, TEMP1_r, ALU_{add}, TEMP2_w$
2. $R1_r, TEMP1_w$
3. PC_r, MAR_w, MEM_r
4. $TEMP2_r, R0_w$
5. MDR_r, IR_w

Temp2 ← R2 + Temp1

Temp1 ← R1

MAR ← PC

MDR ← M[MAR]

R0 ← Temp2

IR ← MDR

3, 5, 2, 1, 4

Control Unit :-

Control variable:- Name of a control signal

Control word:- Collection of all control signals generated at a time.

A control word is responsible for one (or more if done in parallel) microoperation(s).

AC		S		T		IR		PC			AR	DR	Mem	GPR	ALU	SP	
IN	OUT	IN	OUT	IN	OUT	I	0	I	0	Inc	I/0	I/0	R/W	....	funct^n code	I	0

Assume 5-bits

$AR \leftarrow PC$

Control word

0 0 0 0 0 0 0 0 01 0 1 0 00 0 0 0....0 XXXXX 00

don't care

$DR \leftarrow M[AR]$

00 00 00 00 000 01 10 10 0...0 XXXXX 00

$IR \leftarrow DR,\ PC \leftarrow PC + 1$

00 00 00 10 001 00 01 00 0....0 XXXXX 00

Topic : Control Unit Organization

The way control unit is designed

1. Hardwired control unit
2. Microprogrammed control unit
   - → Horizontal Microprogrammed control unit
   - → Vertical " " "

Topic : Hardwired Control Unit

Control logic is implemented with Gates, flip-flops, decoders and other digital circuits.

Advantage: Can be optimized to produce a faster mode of operation.

Disadvantage: Rearranging the wires among various components is difficult.

→ Updation in control logic is difficult.

2 mins Summary

Topic Data Path

Topic Control Unit

Topic Hardwired Control Unit

Happy Learning

THANK - YOU