CS & IT ENGINEERING

DIGITAL LOGIC

Sequential Circuit

Lecture No. 1

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01 LATCHES

02 PRACTICE

04 DISCUSSION

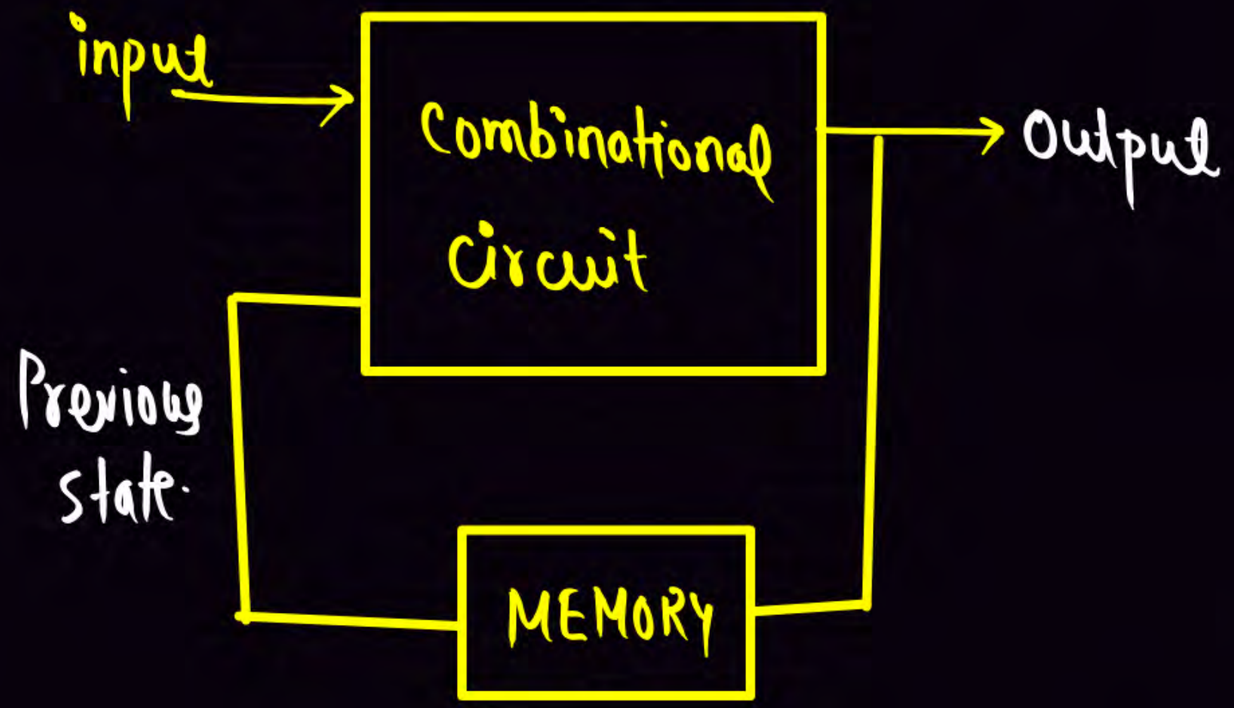
Logic GATE

Minimization → Boolean algebra
Minimization → K-MAP

Combinational circuit

Comparator, MUX, DE-MUX, Encoder, Decoder, HA
FA, H.S, F.S, Serial adder, parallel adder, LACA,
Multiplier

SEQUENTIAL CIRCUIT



SEQUENTIAL CIRCUIT → 1º , 2º

- ✓ A circuit with feedback and memory are called sequential circuit.
- ✓ Output of the sequential circuit depends on previous output as well as present state of input.

↳ Dynamic circuit

Latches

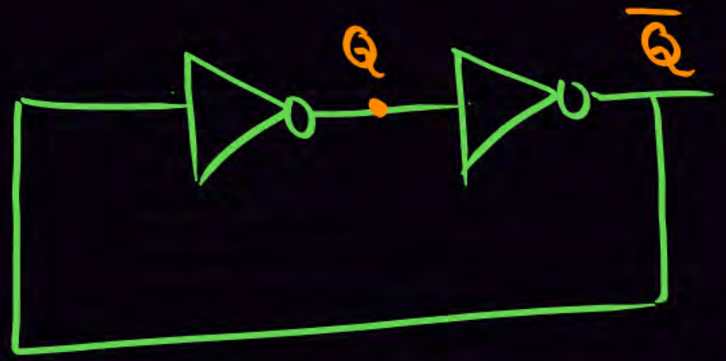
Flip-Flops

Registers

Counters

LATCHES

↳ Basic memory element.



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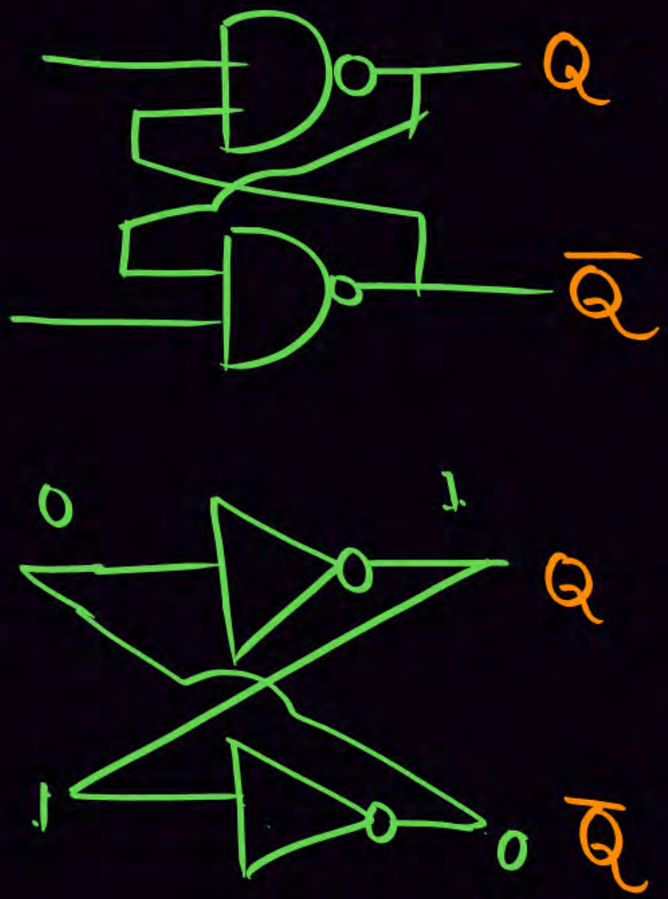
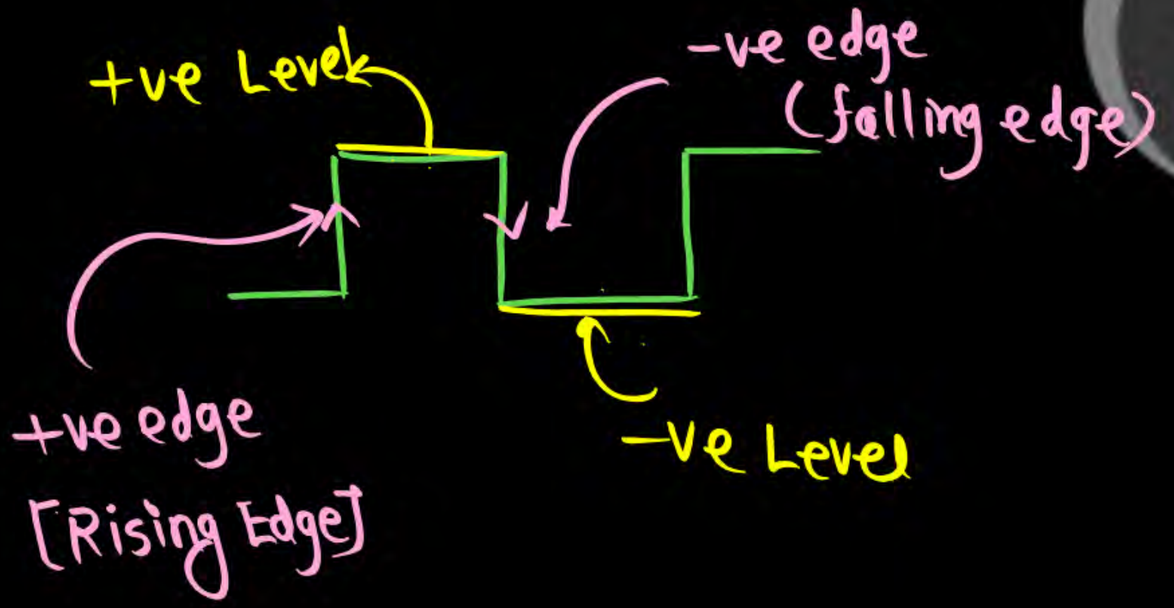
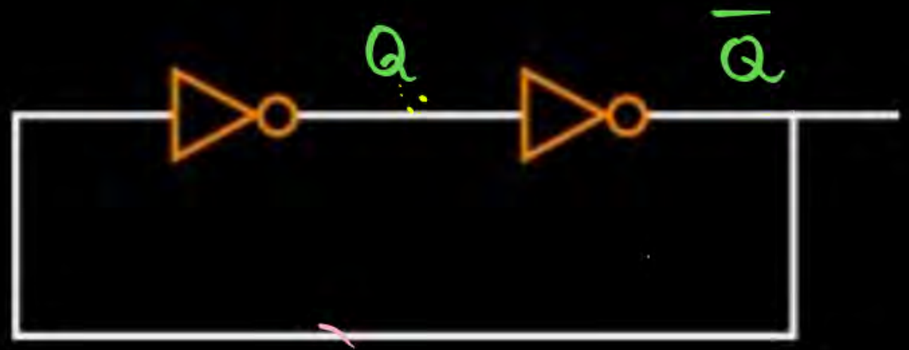
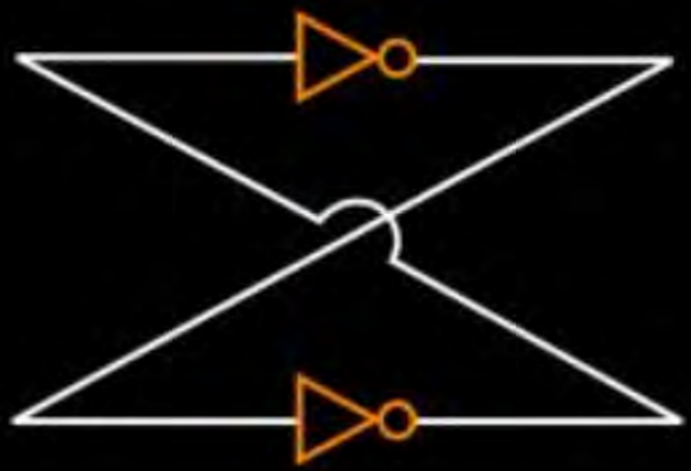


LATCHES

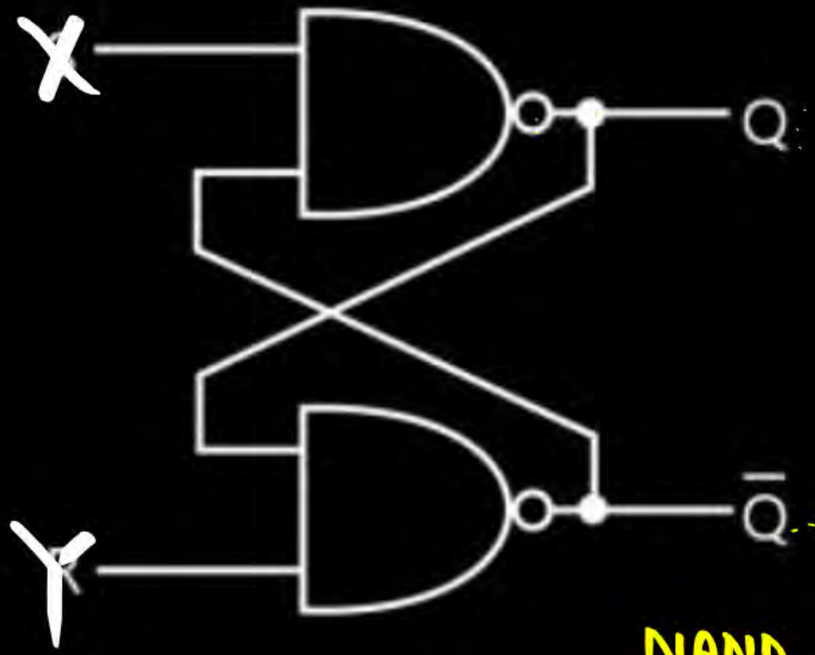
- ✓ Basic memory element ✓
- ✓ Latches are level triggered
- ✓ Latches has two output which is complement of each other







LATCHES



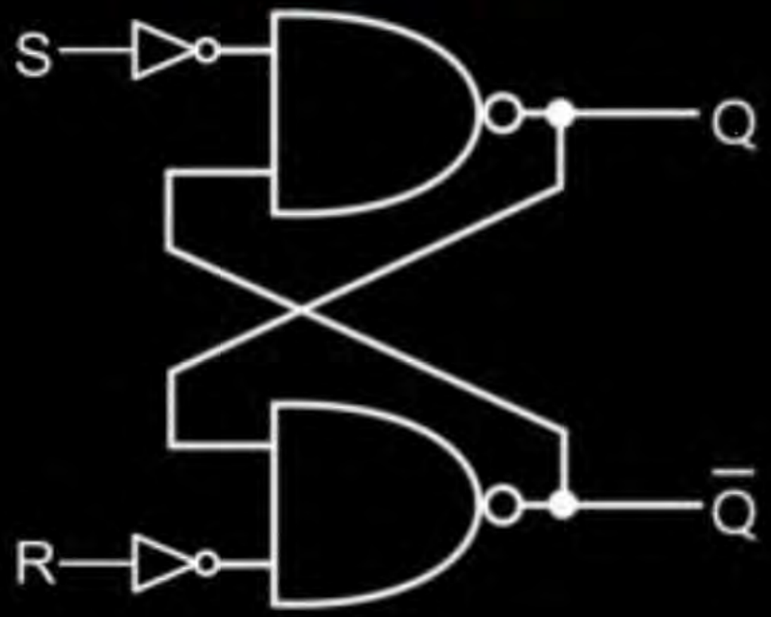
X	Y	Q	$\overline{Q}$	
0	0	1	1	Invalid (forbidden)
0	1	1	0	
1	0	0	1	
1	1	Q	$\overline{Q}$	(HOLD)

NAND

A	B	$Y=\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

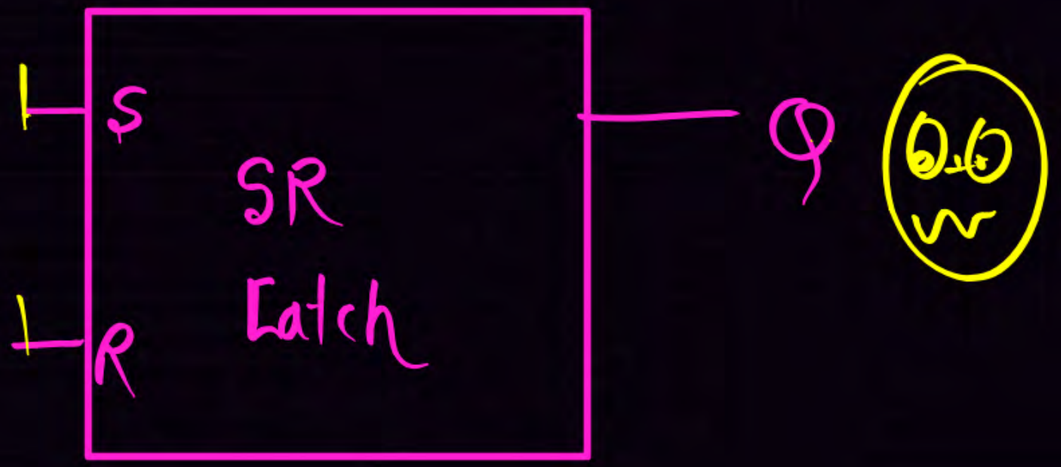
LATCHES

S-R Latch :→



SR Latch.

S	R	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	(HOLD)
0	1	0	1	(RESET)
1	0	1	0	(SET)
1	1	1	1	(InValid)

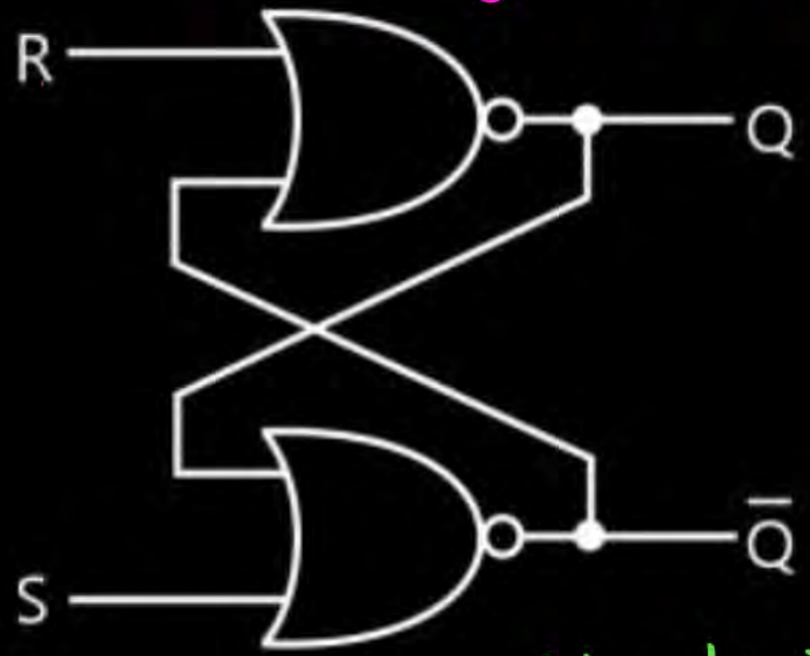

S
R
SR
Latch
Q

LATCHES

Note : Whenever S = R = 1 is applied and invalid condition occurs than a NAND having lower propagation delay first change its output and other remain on its previous state are called racing problem or raising problem.

LATCHES

SR latch by NOR GATE

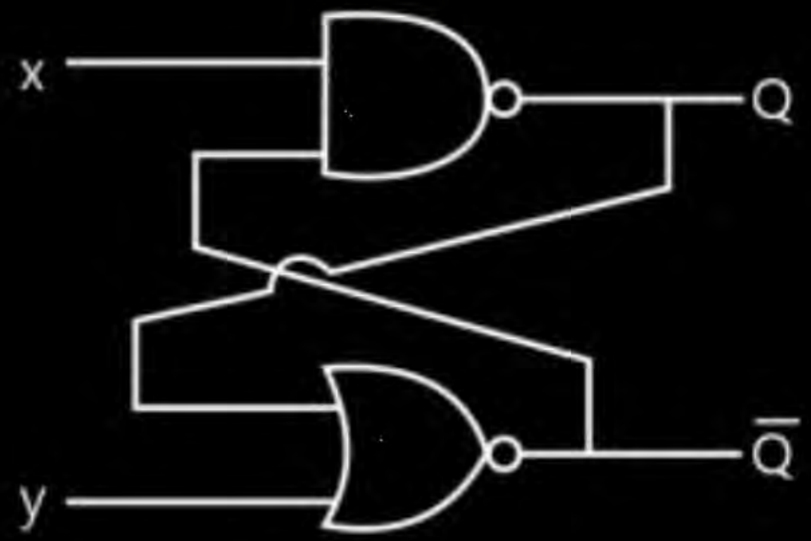


A	B	$Y=\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

SR Latch (SR)

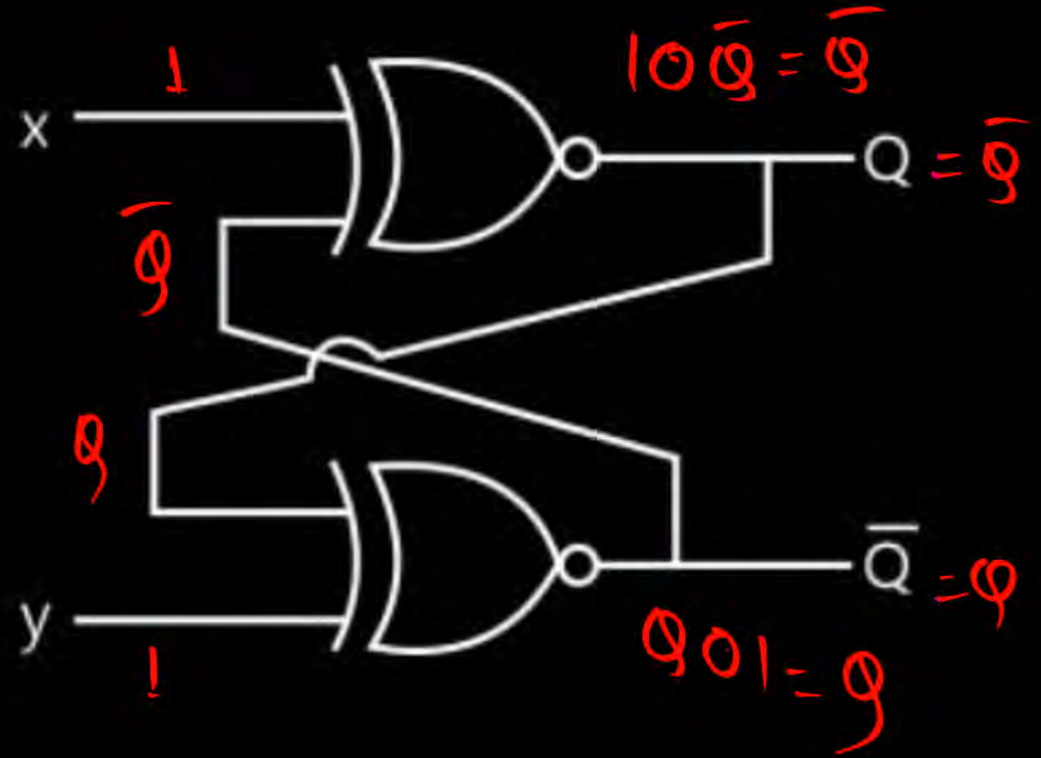
S	R	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$ (HOLD)
0	1	0	1 (RESET)
1	0	1	0 (SET)
1	1	0	0 (Invalid)

LATCHES



X	Y	Q	$\overline{Q}$
0	0	1	0
0	1	1	0
1	0	Q	$\overline{Q}$
1	1	!	0

LATCHES



X	Y	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$ (HOLD)
0	1	Q	Q (Invalid)
1	0	$\bar{Q}$	$\bar{Q}$ (Invalid)
1	1	$\bar{Q}$	Q (Toggle)

Q ⊙ Q = 1

$\bar{Q}$ ⊙ $\bar{Q}$ = 1

Q ⊙ 1 = Q

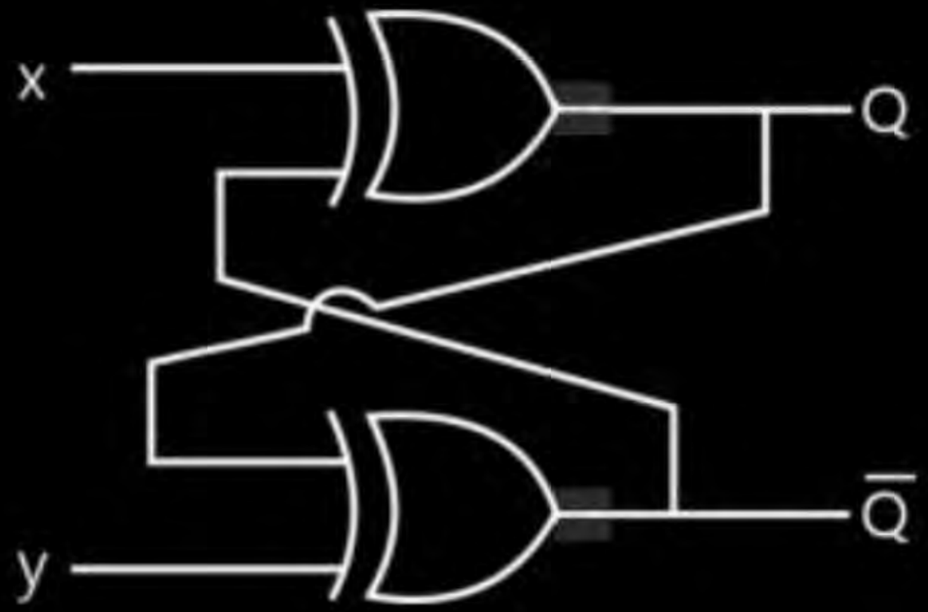
$\bar{Q}$ ⊙ 1 = $\bar{Q}$

Q ⊙ $\bar{Q}$ = 0

Q ⊙ 0 = $\bar{Q}$

$\bar{Q}$ ⊙ 0 = Q

LATCHES



X	Y	Q	$\bar{Q}$
0	0	$\bar{Q}$	Q (Toggle)
0	1	$\bar{Q}$	$\bar{Q}$ (Invalid)
1	0	Q	Q [Invalid]
1	1	Q	$\bar{Q}$ (HOLD)

$Q \oplus Q = 0$

$\bar{Q} \oplus \bar{Q} = 0$

$Q \oplus 0 = Q$

$\bar{Q} \oplus 0 = \bar{Q}$

$Q \oplus \bar{Q} = 1$

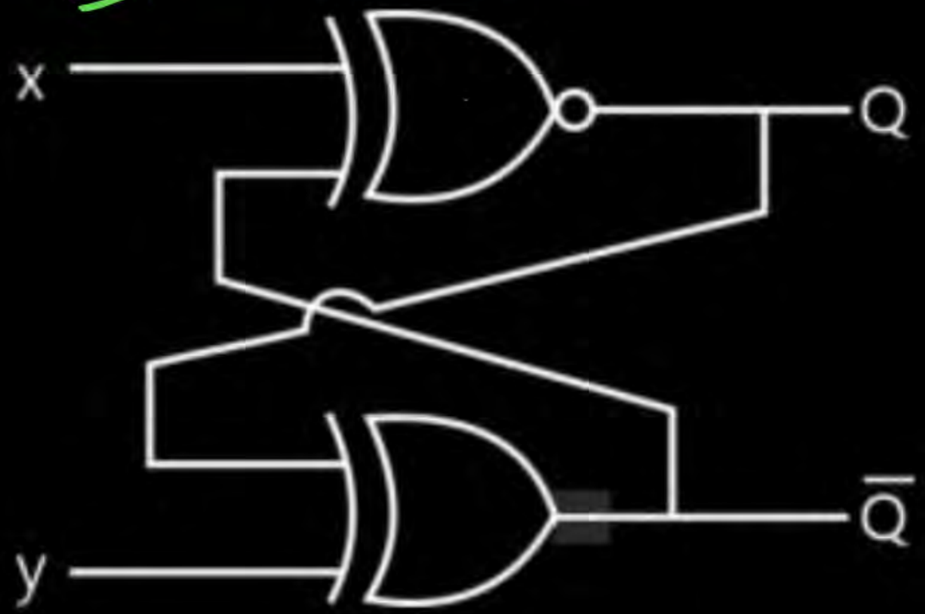
$\bar{Q} \oplus Q = 1$

$Q \oplus 1 = \bar{Q}$

$\bar{Q} \oplus 1 = Q$

LATCHES

HW



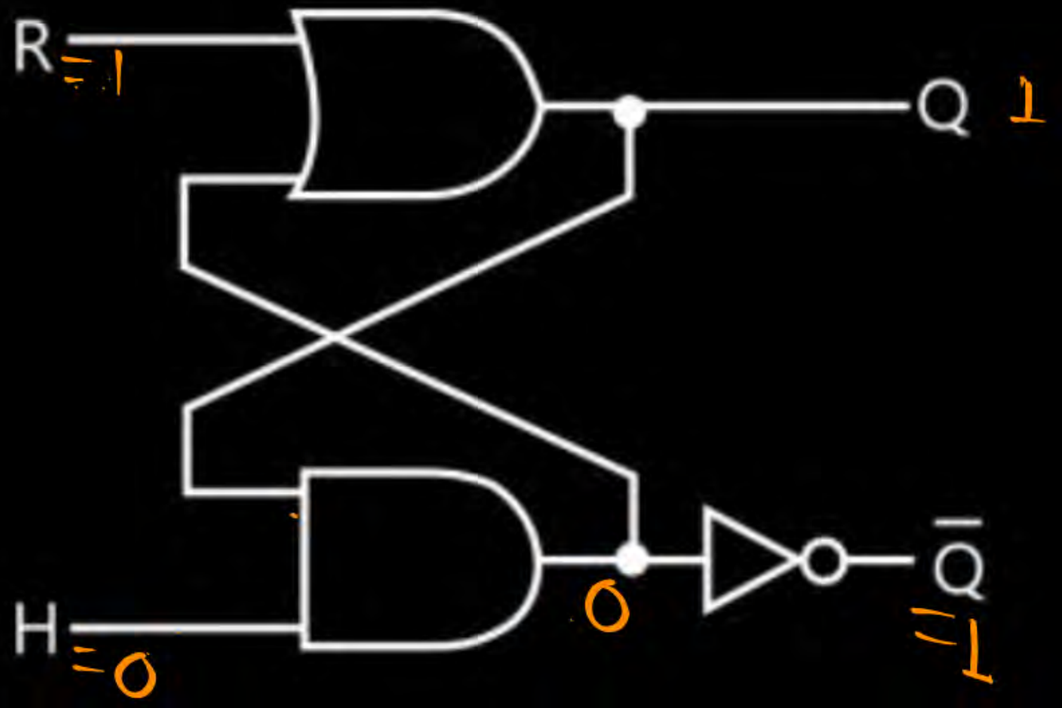
X	Y	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

LATCHES

Q.1

R	H	Q	$\bar{Q}$
0	0	0	1
0	1	Q	$\bar{Q}$
1	0	1	1 X.
1	1	1	0

Consider a latch circuit shown in figure below. Which of the following set of input is invalid for circuit?



A. R = 0, H = 0 ✗

B. R = 0, H = 1 ✗

C. R = 1, H = 1 ✗

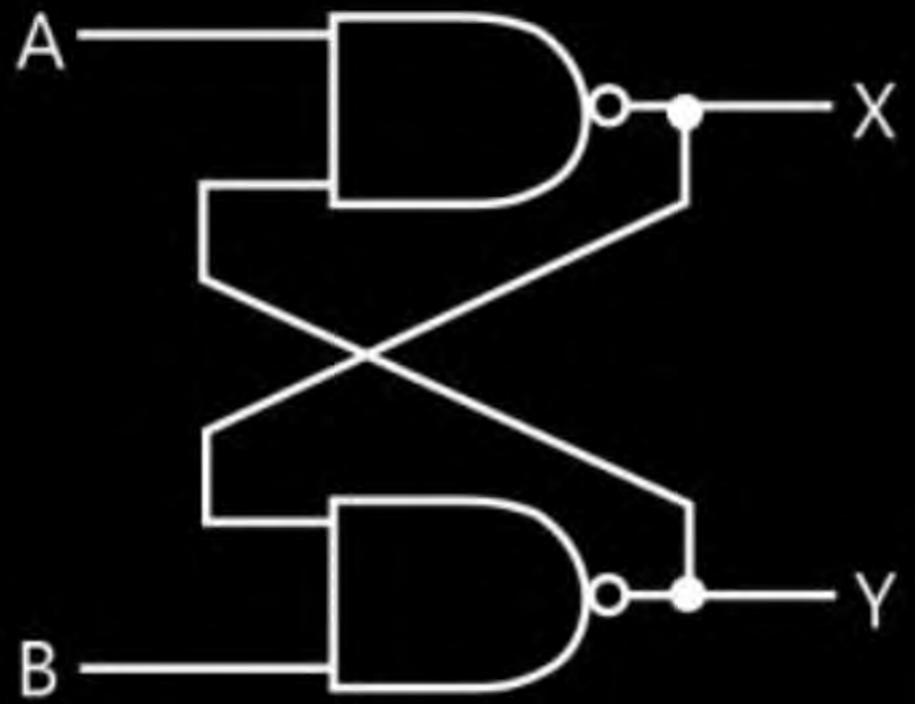
D. R = 1, H = 0

LATCHES

Q.2

HLO.

In the circuit shown below, initially A = 1 and B = 1. The input B is now replaced by a sequence 101010 ..... the outputs X and Y will be



(A) Fixed at 0 and 1, respectively

(B) Fixed at 1 and 0, respectively

(C) X = 1010..... while Y = 1010....

(D) X = 1010 ..... while Y = 0101 .....

Q.

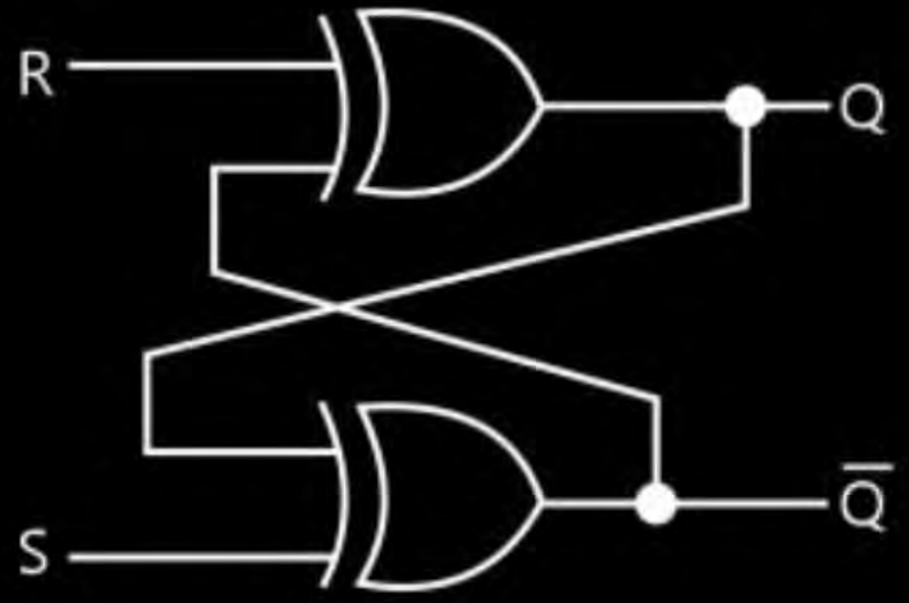
Which of the following will be correct for the given sequential circuit?

A. The circuit would hold the previous state for S=0, R=0

B. The circuit would hold the previous state for S=0, R=1

C. The circuit would hold the previous state for S=1, R=1

D. The circuit would never be able to hold the previous state under any condition




THANK YOU GW
SOLDIERS !