A SiC-Based High-Efficiency Isolated Onboard PEV Charger With Ultrawide DC-Link Voltage Range

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***Abstract*—In *LLC*-based onboard battery charging architectures used in plug-in electric vehicles (PEV), the dc link voltage can be actively regulated to follow the battery pack voltage so that the *LLC* converter can operate in proximity of resonant frequency and achieve high efficiencies over the wide range of battery pack voltage. However, conventional boost-type power factor correction (PFC) converters are unable to provide ultrawide dc link voltages since their output voltages should always be larger than their input voltages. This paper proposes a Silicon Carbide (SiC)-based onboard PEV charger using single-ended primary-inductor converter (SEPIC) PFC converter followed by an isolated *LLC* resonant converter. With the proposed charger architecture, the SEPIC PFC converter is able to provide an ultrawide range for dc link voltage, and consequently enhance the efficiency of the *LLC* stage by ensuring operation in proximity of resonant frequency. A 1-kW SiC-based prototype is designed to validate the proposed idea. The experimental result shows that the SEPIC PFC converter achieves unity power factor, 2.72% total harmonic distortion, and 95.3% peak conversion efficiency. The *LLC* converter achieves 97.1% peak efficiency and always demonstrates a very high efficiency across the ultrawide dc-link voltage range. The overall efficiency of the charger is 88.5% to 93.5% from 20% of the rated load to full load.**

***Index Terms*—Battery charger, *LLC* resonant converter, plug-in electric vehicle (PEV) charger, power factor correction (PFC), silicon carbide (SiC), single-ended primary-inductor converter (SEPIC).**

I. Introduction

TWO-STAGE isolated ac/dc converters have been widely used in onboard battery charging architectures for plug-in electric vehicles (PEVs) [1]. The two-stage ac/dc converters are typically composed of a power factor correction (PFC) converter followed by an isolated dc/dc converter. Boost-type topologies are commonly utilized as the PFC stage converters due to their simple circuit configurations, continuous input current, and low total harmonic distortion (THD) [2]. In order to be compatible with the universal grid voltage (85–265 V, 47–70 Hz), the output voltage of the PFC stage, referred to as dc link voltage, is typically regulated at 390 V [3]–[5]. In the isolated dc/dc stage, the *LLC* resonant converters are usually employed due to their attractive features such as soft switching, galvanic isolation, and short-circuit protection [6]–[8]. The output voltage of the *LLC* converter is regulated by pulse frequency modulation, with the resonant frequency as the optimal operation frequency associated with the highest efficiency [9]. The overall structure of a conventional two-stage PEV battery charger architecture using a boost-type PFC and a full-bridge *LLC* converter is shown in Fig. 1 [1].

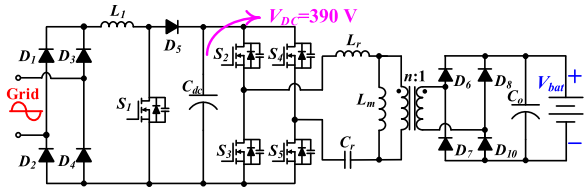

Fig. 1. Conventional two-stage isolated charger using a boost PFC and a full-bridge *LLC* converter.

Even though the peak efficiency of the conventional chargers with boost-type PFC converters might be over 93%, they have lower efficiencies at medium and particularly light loads. The operation frequency of the *LLC* converter moves away from the resonant frequency when the battery pack voltage is lower than its rated voltage at a low state of charge. Consequently, the circulating losses and switching losses increases, which deteriorate the efficiency [5], [10].

Thus, a PFC converter capable of providing a wide regulated dc link voltage, such as a single-ended primary inductor converter (SEPIC) PFC converter, can improve the overall efficiency of the systems to a great extent. The SEPIC PFC converter enables the dc link voltage to follow the battery pack voltage with the *LLC* converter operating in proximity of resonant frequency with a unity gain. Hence, the *LLC* converter can maintain high efficiency over the entire range of battery pack voltage, and the overall efficiency can be improved significantly especially when the battery pack voltage is much lower than the rated voltage [11], [12]. The proposed two-stage isolated charger based on SEPIC PFC converter and *LLC* resonant converter is shown in Fig. 2.

Although the silicon devices applied in the two-stage onboard PEV chargers can support high frequency operation, the performance would degrade significantly when the junction temperature is high [13]. This limits the power density and the operation frequency of the chargers. In [14], a two-stage high-frequency 3.3-kW onboard battery charger is presented. However, the power density is limited by the thermal limitations in silicon

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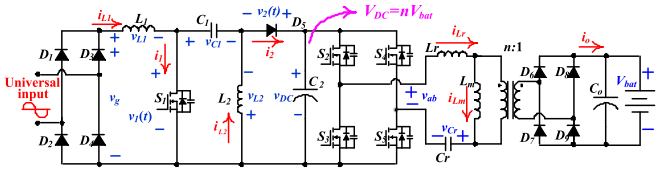

Fig. 2. Proposed two-stage isolated charger based on SEPIC PFC converter and *LLC* resonant converter.

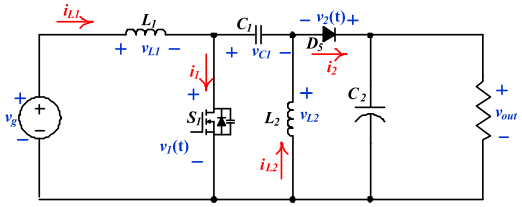

Fig. 3. Schematic of SEPIC converter.

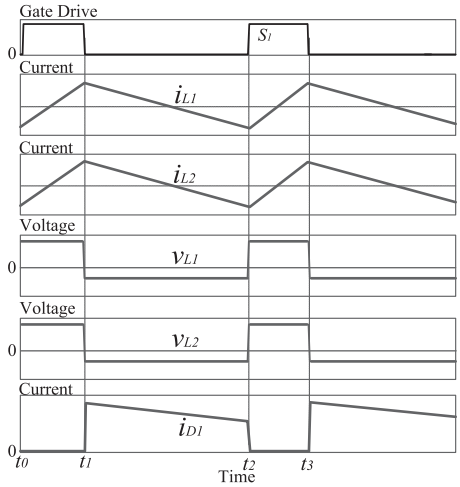

Fig. 4. Switching waveforms of a SEPIC converter over one switching period.

switches and diodes. Thus, wide bandgap silicon carbide (SiC) devices are used to improve the performance [15]–[17].

The contribution of this work lies in following aspects.

1) A unique onboard charger architecture is adapted to optimize efficiency of the charger over the wide output voltage ranges.
2) Detailed modeling, design considerations, and dynamic analyses of utilizing SEPIC topology in high-voltage high-power PFC application are presented.
3) An *LLC* topology with integrated magnetic transformer and small L_m/L_r is designed and implemented.
4) An all SiC-based converter prototype, with reduced semiconductor losses and higher conversion efficiency is designed and tested.

This paper is organized as follows. The design of the SEPIC PFC converter is presented in Section II. The design of the dc/dc resonant converter is elaborated in Section III. The circuit modeling and control strategy are analyzed in Section IV. The simulation results and experimental results of a 1-kW prototype are demonstrated in Section V for validation of the analyses. Finally, Section VI concludes the paper.

II. Design of SEPIC PFC Converter

A. Theory of Operation

In continuous conduction mode (CCM), there are two operation modes in a switching period. The schematic is demonstrated in Fig. 3. The typical waveforms are shown in Fig. 4. In the steady state, the average voltages across the inductors, $<v_{L1}>$ and $<v_{L2}>$, in one switching period are equal to zero.

Therefore, the steady-state voltage of capacitor C_1 is equal to the input voltage. If C_1 is large enough, assuming small ripple approximation, the voltage of capacitor C_1 can be expressed as

$$v_{C1} = v_g. \tag{1}$$

In a SEPIC PFC converter, the voltage gain could be either larger than unity or smaller than unity. This means, in rectifier application, the rectified output voltage does not necessarily need to be greater than the amplitude of the grid voltage. Therefore, the SEPIC topology brings the benefit of ultrawide dc-link voltage range in the active rectifier applications.

Neglecting the voltage ripple at the output capacitor, the output voltage v_o can be considered as a constant equal to V_o. Thus, the corresponding duty cycle can be calculated as

$$d(t) = \frac{V_o}{V_M\,|\sin\omega t| + V_o} \tag{2}$$

where V_M is the amplitude of grid voltage, and ω is the angular frequency, which is typically 120 π rad/s in the U.S.

Equation (2) describes how the duty cycle of SEPIC converter would vary in the steady state in the ac/dc PFC applications. The varying range of duty cycle is

$$\frac{V_o}{V_M + V_o} \le d(t) \le 1. \tag{3}$$

B. Design of Main Components

1) Inductors L_1 and L_2: In the PEV onboard battery charging applications, the power level of the front-end ac/dc PFC converter is usually high. At the same power level, the CCM is preferred to the discontinuous conduction mode (DCM) because the current stresses of components in CCM are much smaller than DCM.

Assuming that the SEPIC converter operates in the boundary conduction condition (BCM), T_s is the switching period and D is the duty cycle. During the time interval (0, DT_s], the switch is ON, and the inductor current increases at the rate of $v_g/L_{1,b}$ where $L_{1,b}$ is the boundary value of the input inductor L_1. The inductor current ripple can be calculated as

$$\Delta i_{L_1} = \frac{v_g}{L_{1,b}} DT_s. \tag{4}$$

The BCM happens when the current ripple is equal to twice the average input current. Thus,

$$\Delta i_{L_1} = \frac{v_g}{L_{1,b}} DT_s = 2i_{\text{in}}. \tag{5}$$

Hence,

$$L_{1,b} = \frac{v_g}{2i_{\text{in}}} DT_s. \tag{6}$$

Assuming unity power factor, the ratio of input voltage and input current could be expressed by an effective resistor, R_e

$$R_e = \frac{v_g}{i_{\text{in}}} = \frac{V_{\text{rms}}^2}{P_{\text{in}}} \tag{7}$$

where V_{rms} is the root mean square value of the grid voltage and P_{in} is the input power.

Thus, the CCM condition for input current can be expressed as

$$L_1 > \max\left\{\frac{R_e}{2} DT_s\right\} = \frac{V_{\text{rms}}^2}{P_{\text{in}}} \frac{T_s}{2}. \tag{8}$$

According to (8), the smaller the switching period T_s is, the more easily the converter can enter into CCM. The larger the minimum input power $P_{\text{in,min}}$ is, the more easily the converter can operate in CCM.

Similarly, the BCM for inductor L_2 can be derived. The CCM condition for inductor current i_{L_2} can be calculated as

$$L_2 > \max\left\{\frac{R_L}{2} D'T_s\right\} = \frac{R_{L,\max}}{2} \frac{V_M}{V_M + V_o} T_s. \tag{9}$$

According to (9), the smaller the switching period T_s is, the more easily the converter can enter into CCM. The smaller the maximum value of load resistance, $R_{L,\max}$, is, the easier the converter can enter into CCM. Based on calculation, the inductances of L_2 and L_2 are both calculated as 550 μH.

2) SEPIC Capacitor C_1: For the SEPIC capacitor C_1, according to (1), the average voltage on C_1 is equal to the input voltage. The capacitor C_1 needs to keep a constant voltage (CV) in a switching period and to follow the variation of the input voltage [18]. Thus, for the selection of the capacitance C_1, both the grid frequency f_g, and the switching frequency f_s need to be considered. On the one hand, the resonant frequency of the SEPIC capacitor C_1 and the inductors have to be much larger than the grid frequency to avoid input current oscillation. On the other hand, this resonant frequency has to be much lower than the switching frequency to reduce the voltage ripple of the SEPIC capacitor. The resonant frequency of the SEPIC capacitor C_1 and the inductors L_1 and L_2 is defined as

$$f_r = \frac{1}{2\pi} \sqrt{\frac{1}{C_1(L_1 + L_2)}}. \tag{10}$$

The relations of this resonant frequency to the grid frequency and the switching frequency can be expressed as

$$f_g < f_r < f_s. \tag{11}$$

In this work, the switching frequency of the PFC stage f_{s_1} is set as 100 kHz, and f_r is set as 1.5 kHz. The inductances of L_1 and L_2 are both 550 μH. Thus, the SEPIC capacitor C_1 can be selected as 10 μF.

3) DC link Capacitor and Voltage Ripple: With regard to the output capacitor, the switching frequency voltage ripple is negligible as the dc link capacitance is typically very large.

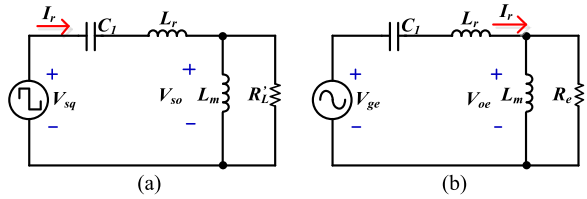

Fig. 5. Models of full-bridge *LLC* resonant converter: (a) nonlinear nonsinusoidal model and (b) linear sinusoidal model.

Twice the line frequency voltage ripple is more critical since it directly impacts the performance of the isolated dc/dc stage. The low-frequency voltage ripple on the output capacitor can be derived as [19]

$$\Delta v_o = \frac{P_{\text{in}} T_{\text{line}}}{\pi C_2 V_o} \tag{12}$$

where T_{line} is the period of the grid voltage.

According to (12), the maximum voltage ripple happens when the input power reaches its peak point. In order to reduce the low-frequency voltage ripple, a large value of output capacitor is preferred. However, this would make the electrolytic capacitor bank bulky. The tradeoff between capacitor size and output voltage ripple must be taken into consideration when designing the converter. Based on the calculation, the dc link capacitance is selected as 2 mF.

4) SiC Power Devices: The voltage stress on the diode of the SEPIC PFC converter is the sum of the peak input voltage and the dc link voltage. The C4D20120D Schottky diode from CREE Inc is chosen due to its high-repetitive peak reverse voltage of 1200 V, which is high enough to handle the voltage stress on the diode of the SEPIC PFC converter. This SiC power diode has a better performance than the comparable Si power diode due to its negligible reverse recovery current, especially at frequencies over 100 kHz. Thus, the switching loss of the SEPIC PFC converter can be reduced significantly [16]. The MOSFETs are CMF10120 from CREE Inc, which inherently have lower switching and conduction losses.

III. Design of *LLC* Resonant Converter

A. Theory of Operation and Transfer Function

1) Equivalent Model of Circuit: The schematic of a full-bridge *LLC* resonant converter is shown in Fig. 2. The switches S_2 and S_5 turn ON and OFF simultaneously, while switches S_3 and S_4 turn ON and OFF simultaneously with 180° phase shift. Hence, the input voltage of the *LLC* converter is a square waveform, it can be modeled as a square voltage source *Vsq* as shown in Fig. 5(a), where all the passive components are included and *RL'* is the load resistance seen from the primary side of the transformer. The SEPIC PFC converter in the proposed battery charger enables the dc link voltage to follow the battery voltage ranging from 200 to 420 V during charging. For the *LLC* converter, the output voltage is regulated to be the same as the input voltage all the time. Thus, the turn ratio of the *LLC* converter is designed as 1. The equivalent load resistance *Re* is

expressed as [20]

$$R_e = \frac{v_{1,\mathrm{RMS}}}{i_{1,\mathrm{RMS}}} = \frac{\frac{2\sqrt{2}}{\pi}V_o}{\frac{\pi}{2\sqrt{2}}I_o} = \frac{8V_o}{\pi^2 I_o} = \frac{8}{\pi^2}R_L. \quad (13)$$

Thus, the linear sinusoidal model can be obtained as shown in Fig. 5(b).

2) Transfer Function: Based on the linear equivalent circuit, the voltage gain transfer function can be derived as

$$M(s) = \frac{V_{\mathrm{oe}}}{V_{\mathrm{ge}}} = \left| \frac{(j\omega L_m)\|R_e}{(j\omega L_m)\,\|R_e + j\omega L_r + \frac{1}{j\omega C_r}} \right| \quad (14)$$

where *j* is equal to $\sqrt{-1}$.

Here, the primary resonant frequency *fr* is

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}. \quad (15)$$

The voltage gain transfer function can be rearranged as

$$M(s) = \left| \frac{L_n \cdot f_n^2}{[(L_n+1)\cdot f_n^2 - 1] + j[(f_n^2-1)\cdot f_n \cdot Q \cdot L_n]} \right| \quad (16)$$

where *fn*, equal to f_{s2}/*fr*, is the normalized frequency of the *LLC* converter operation frequency *fs2*, the quality factor *Q* is defined as $\sqrt{L_r/C_r}/R_e$, and the inductance ratio L_n is defined as L_m/L_r.

B. Design of Main Components

1) Inductance Ratio: In contrast to telecommunication applications, where *LLC* topology needs to have a large inductance ratio (L_m/L_r) to satisfy hold-up time requirement, in the onboard charging applications, hold-up time is no longer a constraint. Therefore, an *LLC* converter with larger L_r can be designed to reduce current stress on the circuit components. In a conventional onboard charger topology, the large L_r is usually realized through an additional inductor in series with the transformer. Integrating L_r into the transformer can eliminate a magnetic component and reduce the weight and cost of the converter. Integration of L_r into the transformer is a challenging design constraint, which is explained in the following section and achieved in this work.

2) Integrated Transformer: In this work, the resonant inductor and the magnetizing inductor are integrated into a single transformer. Ferroxcube ETD59 ferrite magnetic core is used to develop the transformer. The core material is 3C90. The sandwich winding technique is utilized to reduce the leakage inductance on the secondary side of the transformer. The primary turns are winded both in the middle layer of the sandwich and in the bottom portion of the window area. Therefore, the winding in the bottom portion of the winding area contributes to the leakage inductance in the primary side. By adjusting the ratio between the top portion and bottom portion, desired primary leakage inductance can be obtained.

The magnetizing inductance can be adjusted by changing the air gap between the two pieces of magnetic cores. The flux variation can be calculated using

$$\Delta B = \frac{E_i T_n}{N A_e} \quad (17)$$

where *N* is the number of primary turns, A_e is the core cross-sectional area, E_i is the voltage applied to the core, and T_n is the maximum time the voltage is applied. In order to limit conduction loss in the resonant tank, the magnetizing inductance cannot be small. The inductance ratio is selected to be 3.4 in this work. The magnetizing inductance is designed as 107.6 μH, and hence the resonant inductance is chosen to be 31.7 μH.

3) Resonant Capacitor: The primary resonant frequency of the *LLC* converter is designed as 196 kHz. Thus, the resonant capacitor, based on (15), is selected as 20 nF.

4) SiC Power Devices: The dc/dc converter provides isolation and required voltage gain between the source and load. The CMF10120 from CREE Inc., is used as the power MOSFETs of full-bridge topology, and the power diodes are SCS220AGC from ROHM Company. Using SiC power switches, the operation frequency can be increased. Thus, the size of the resonant converter can be reduced, and the power density can be improved.

Based on the design considerations discussed in Sections II and III, the designed parameters of both the SEPIC PFC converter and the dc/dc resonant converter are summarized in Table I.

The components chosen with their part number are listed in Table II. The operation frequency of *LLC* converter is set slightly higher than the resonant frequency to ensure the zero voltage switching (ZVS) operation at different loads. The cur-

TABLE I
DESIGNED PARAMETERS OF THE TWO-STAGE PEV CHARGER

Quantity	Symbol	Parameter
Input voltage	V_{in}	85–265 V, 50–60 Hz
Output voltage	V_{out}	100–420 V
Input inductor	L_1	550 μH
Output inductor	L_2	550 μH
SEPIC capacitor	C_1	10 μF
DC link capacitor	C_2	2 mF
PFC Operation frequency	f_{s1}	100 kHz
Magnetizing inductor	L_m	107.6 μH
Resonant inductor	L_r	31.7 μH
Resonant capacitor	C_r	20 nF
LLC resonant frequency	f_r	196 kHz
LLC operation frequency	f_{s2}	200 kHz

TABLE II
COMPONENTS CHOSEN WITH THE PART NUMBERS

Component	Part number
SEPIC switch	CMF10120
SEPIC diode	C4D20120D
SEPIC capacitor	B32924F3335K
DC link capacitor	ECE-T2WP471FA
LLC switch	CMF10120
LLC diode	SCS220AGC
Resonant capacitor	B32922C3224M

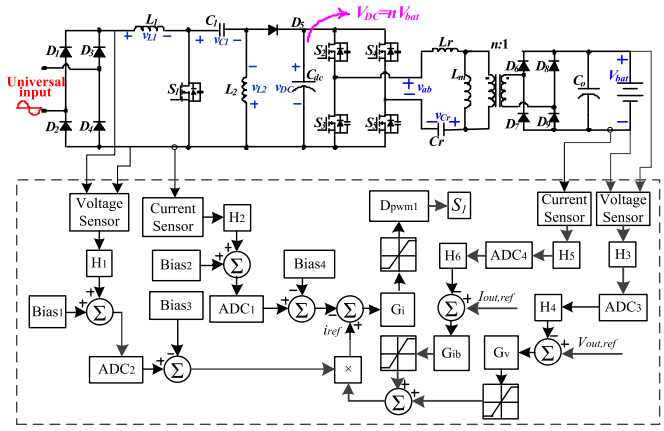

Fig. 6. Digital control strategy of the two-stage battery charger.

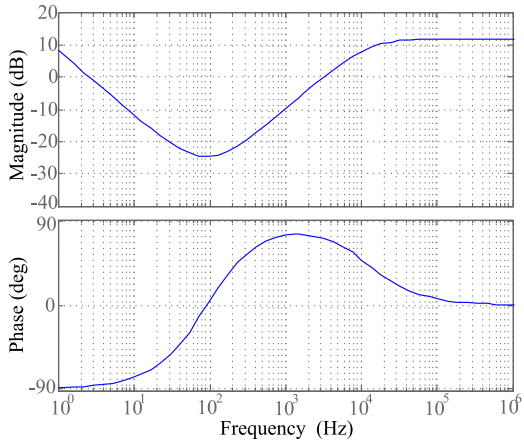

Fig. 7. Bode plot of voltage loop compensator.

rents flowing through these diodes at commutation are close to zero though the diodes at the secondary side do not work in pure zero current switching (ZCS). Moreover, the Schottky SiC diodes with the negligible reverse recovery charge are utilized at the secondary side. Thus, the switching loss is very small and negligible.

IV. Circuit Modeling and Control Strategy

A. Small-Signal Modeling and Transfer Function

In this work, the dc/dc converter serves as a voltage follower, where the output voltage follows the dc link voltage with a small voltage drop mainly caused by conduction losses. Thus, the whole dc/dc part can be modeled as a resistor. Since the operation frequency of dc/dc converter is in proximity of resonant frequency and the conduction loss in the resonant tank is very small, this resistor is negligible compared with the equivalent load resistor. Therefore, the modeling part is mainly focused on the SEPIC PFC converter. Using the state space averaging [21], the transfer functions of duty cycle to output voltage *Gvd* and duty cycle to input current *Gid* can be obtained as

$$G_{\rm vd} = \frac{\left(\frac{L_1+L_2}{L_1L_2}\right)\frac{V_g}{s} - \frac{V_o}{D'R}}{C_2 s + \frac{D}{R} + \left(\frac{L_1+L_2}{L_1L_2}\right)\frac{D'^2}{s}} \tag{18}$$

$$G_{\rm id} = \frac{V_o}{L_1 D s}. \tag{19}$$

B. Control Strategy

The schematic of control strategy is shown in Fig. 6. The output voltage and output current are regulated according to the charging profile of the battery pack. The output current control is active in constant current (CC) charging mode until the battery voltage reaches the nominal voltage when the battery charger enters the CV charging mode and the output voltage control is active. The voltage sensors and current sensors are applied in the circuit. For the ac input current and ac input voltage, the dc biases need to be added so that the DSP can sample such ac signals. In the digital control, these dc biases are removed before the sampled ac signals enter the control loops. Since the gain of the *LLC* converter is always close to unity, the dc link voltage is regulated by regulating the output voltage of the battery charger.

1) Design of Outer Voltage Loop: In the voltage control loop, a voltage sensor is used to measure the output voltage signal and transduce it into an isolated scaled-down voltage signal. The sensed voltage is compared to the reference value $v_{\rm ref}$ to generate an error signal. This error signal is compensated by the voltage loop compensator *Gv*. Output of the voltage loop compensator is multiplied by an ac signal in phase with the input voltage to generate the mixed current reference signal $i_{\rm ref}$.

The voltage loop compensator needs to ensure enough phase-margin and provide enough attenuation at low frequency to limit the low-frequency voltage ripples. Thus, the voltage loop compensator is designed as a proportional integral derivative controller with the transfer function expressed as

$$G_v = G_{\rm vo}\frac{\left(1+\frac{s}{\omega_z}\right)\left(1+\frac{\omega_{L1}}{s}\right)}{\left(1+\frac{s}{\omega_p}\right)}. \tag{20}$$

The bandwidth of the outer voltage loop is designed as 1.5 kHz with phase margin of 52° at crossover frequency. Thus, the f_z, f_p, and f_{LI} are calculated as 82 Hz, 12.2 kHz, and 100 Hz, respectively. The *Gvo* is calculated as 0.026. The bode plot of voltage loop compensator *Gv* is shown in Fig. 7.

Using this voltage compensator, the low-bandwidth outer loop meets design requirements. The bode-plot of the outer loop gain with voltage compensator is shown in Fig. 8. At the crossover frequency (zero dB), the phase margin is close to 90° (over 45°). The phase margin is enough for stability of the system. At 67 Hz, a sharp phase drop happens. The overall close-loop phase delay drops to −170°, which does not affect the stability of the system, since as pointed out the stability is determined by the phase margin at the crossover frequency (zero dB). The system operates stably as demonstrated by both the simulations and experiments.

2) Design of Inner Current Loop: A current sensor is used to transduce the input inductor current signal into a voltage signal. A low-pass filter is utilized to attenuate

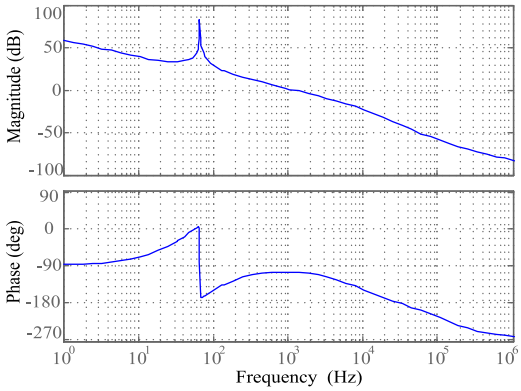

Fig. 8. Bode plot of the outer loop gain with voltage compensator.

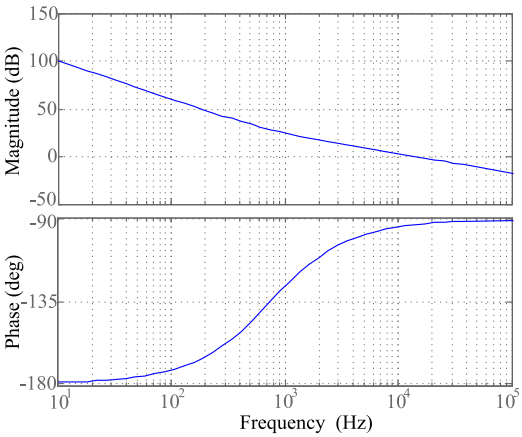

Fig. 9. Bode plot of the inner loop gain with current compensator.

the high-frequency switching harmonics. The sensed average inductor current is compared to its reference value $i_{\rm ref}$ to generate an error signal. This error signal is compensated by the current loop compensator *Gi* and fed to the pulse-width modulator $(1/V_M)$. The current loop compensator is designed to ensure sufficient phase margin of the current control loop. A PI compensator is designed for *Gi*. It is expressed as

$$G_i = G_{\rm io}\left(1+\frac{\omega_{L2}}{s}\right). \tag{21}$$

The bandwidth of the inner current loop is designed as 15 kHz. Thus, *Gio* is calculated as 1.2, and the $f_{\rm L2}$ is calculated as 1.5 kHz. By using this current compensator, the wide-bandwidth inner loop meets the design requirements. The bode-plot of the outer loop gain with voltage compensator is shown in Fig. 9. For the inner current loop, according to Fig. 9 at the crossover frequency, the phase margin is about 85°, which ensures stable operation, as it is over 45°. The phase delay at low-frequency region does not directly affect the phase margin of the system. The noise with frequency less than 120 Hz is negligible in the circuit, and the phase delay for the 120 Hz harmonics is larger than 15°, which does not affect the stability of the system. Since, the design requirements of the output current control are similar to the design requirements of the output voltage control, the design of compensator $G_{\rm ib}$ is similar to that of the compensator $G_{\rm v}$.

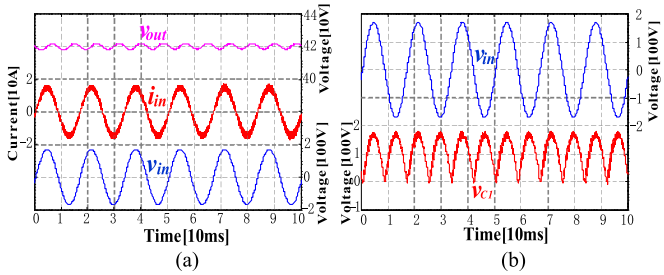

Fig. 10. Simulation results of the input current, output voltage ripple, input voltage, and SEPIC capacitor voltage with $V_{\rm out} = 420$ V.

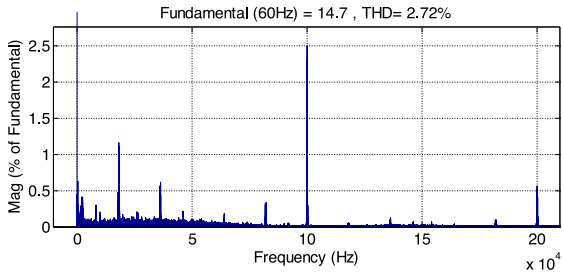

Fig. 11. Fast Fourier transform analysis of the input current at rated power with $V_{\rm out} = 420$ V.

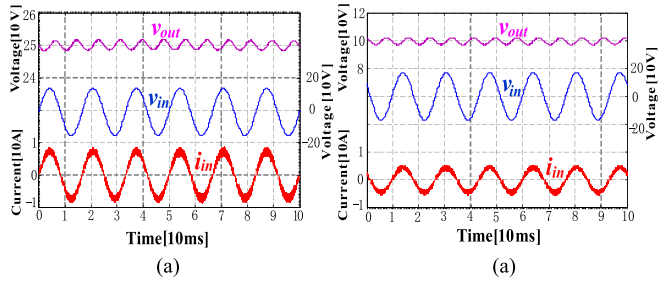

Fig. 12. Simulation results of the input current and output voltage at (a) $V_{\rm out} = 250$ V and (b) $V_{\rm out} = 100$ V.

V. Simulation Results and Experimental Results

A. Simulation Results

1) SEPIC PFC Stage: In order to verify the design, simulations are performed with listed parameters in Table I. In the simulation, MOSFETs and diodes are assumed as ideal devices. Two digital PI compensators are built to stabilize the current loop and the voltage loop. Fig. 10 demonstrates the operation of the converter at the rated power (1 kW). The input voltage is 120 V, and the output voltage is 420 V. According to Fig. 10(a), the input current follows the input voltage with 0.9996 power factor. The electrical stresses on different components can be determined based on the simulation result at the rated power. As shown in Fig. 10(b), $v_{\rm C1}$ is roughly equal to the absolute value of $v_{\rm in}$, which is in agreement with (1). Fig. 11 presents the simulated harmonics distortion from the input current. According to Fig. 11, the THD is 2.72%.

Fig. 12(a) shows the simulated waveforms of input current and output voltage at the beginning of CC charging mode, where the output voltage is 250 V, and the output power is 600 W. The power factor is 0.999, and the THD is 4.03%. Fig. 12(b) shows

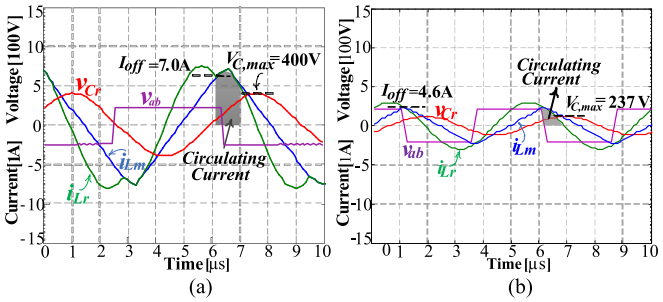

Fig. 13. *LLC* converter performance comparison at 1 kW: (a) conventional control strategy; and (b) proposed control strategy.

the simulated waveforms of input current and output voltage at the precharge stage. The output voltage is 100 V, and the input voltage is 120 V. The power factor is 0.999, and the THD is 6.79%. It should be noted that if the output power is sufficiently low, according to (9), the converter might operate in DCM.

2) LLC DC/DC Stage: With regards to the secondary stage dc/dc conversion, a comprehensive comparison is made between the proposed control strategy with a variable dc link voltage and the conventional frequency-modulation control strategy with a fixed dc link voltage [14]. A 1-kW *LLC* converter compatible with 100–420-V battery pack voltages is designed to test these two control strategies. The theoretical analyses and design considerations of this *LLC* converter are discussed in Section III. For the proposed control strategy, the operation frequency of the *LLC* converter is set as constant 200 kHz, and the dc link voltage follows the battery pack voltage. For the conventional control strategy, the dc link voltage is fixed at 390 V, and the operation frequency of the *LLC* converter is tuned by a voltage close loop depending on the battery pack voltage.

Fig. 13 demonstrates operation of the *LLC* converter at 1 kW ($V_{\rm bat} = 420$ V, $I_{\rm bat} = 2.38$ A) for both the proposed and conventional control strategies. In comparison to the conventional approach, the proposed approach reduces the turning-off current from 7.0 to 4.6 A. In addition, the circulating current and the current stress on the rectifier diode are largely reduced. The voltage stress on C_r is also reduced significantly from 400 to 237 V by applying the proposed control strategy.

B. Experimental Results

Based on the parameters in Table I, a prototype with rated power of 1 kW is designed and built to verify the proposed concepts. Fig. 14(a) shows the picture of the ac/dc PFC converter prototype. The system is controlled by a TMS320F28335 DSP controller from Texas Instruments, Inc. The switching frequency of the SEPIC PFC converter is set at 100 kHz. The gate driver ICs for the SiC MOSFETs are NCP 5181 from ON Semiconductor.

Fig. 14(b) shows the picture of the 1-kW dc/dc *LLC* converter prototype, which is compatible with 100–420 V battery pack voltages. Only one magnetic component is used in this converter. Both the resonant inductor L_r and the magnetizing inductor L_m are integrated into one single transformer. Film capacitors are utilized as the output filter capacitor. The measured resonant frequency f_r between L_r and C_r is equal to 196 kHz.

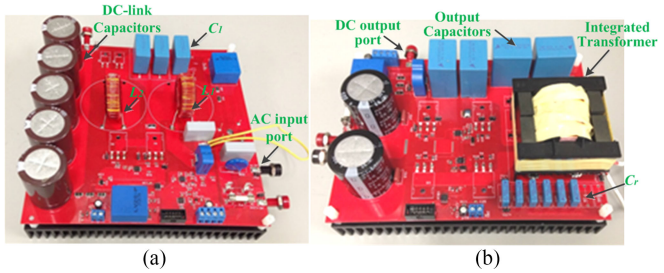

Fig. 14. Designed charger prototype. (a) AC/DC SEPIC PFC converter and (b) full-bridge *LLC* converter.

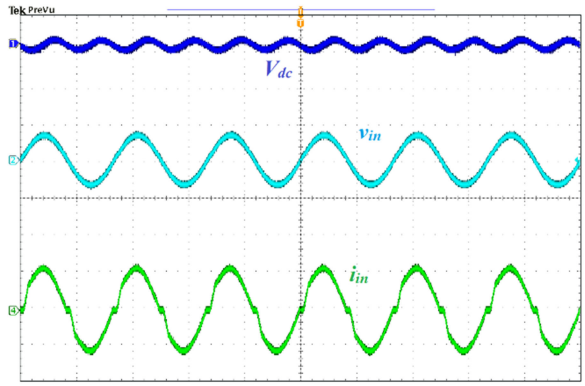

Fig. 15. Experimental results of the output voltage, input voltage, and the input current ($V_{\rm in} = 120$ V, $V_{\rm dc} = 420$ V). From top to bottom: $V_{\rm dc}$ (20 V/ div, ac coupling), $v_{\rm in}$ (250 V/ div), $i_{\rm in}$ (10 A/ div), time (10 ms/div).

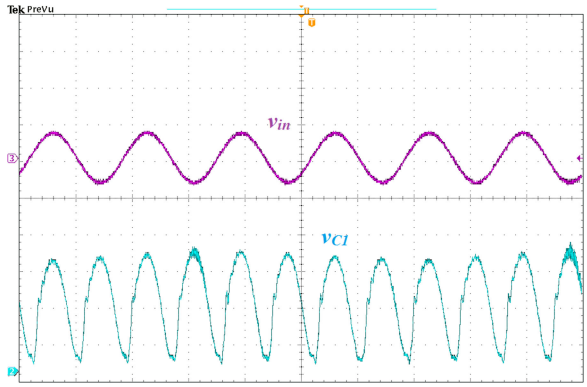

Fig. 16. Experimental results of the input voltage, and the SEPIC capacitor voltage. ($V_{\rm in} = 120$ V, $V_{\rm dc} = 420$ V). From top to bottom: $v_{\rm in}$ (250 V/div), $v_{\rm C1}$ (50 V/div), time (10 ms/div).

Figs. 15–17 demonstrate the experimental results of the converter operating at 980 W in CV charging mode. Fig. 15 shows the waveforms of grid input voltage and ac input current. The dc link voltage is regulated at 420 V, which is higher than the peak grid input voltage. As seen in Fig. 15, the input current follows the input voltage with no phase difference. The power factor is recorded as 0.993, while the conversion efficiency is measured as 95.3%. The waveform of the dc link voltage is demonstrated in Channel 1. The frequency of the dc-link voltage ripple is twice the grid frequency. The amplitude of the voltage ripple on the dc link voltage is well suppressed to be around 8 V.

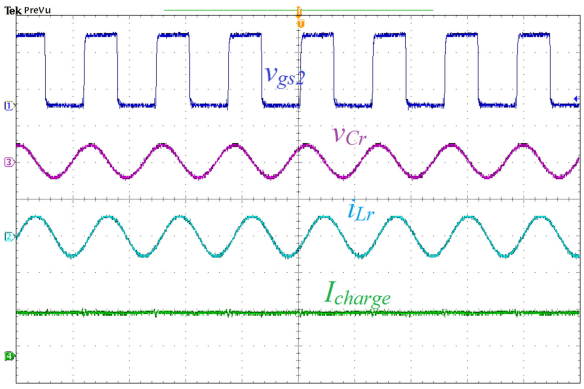

Fig. 17. Experimental results of the *LLC* charger ($V_{\rm bat} = 420$ V, $I_{\rm charge} = 2.36$ A). From top to bottom: $v_{\rm gs2}$ (10 V/div), $v_{\rm Cr}$ (500 V/div), $i_{\rm Lr}$ (10 A/div), $I_{\rm charge}$ (2 A/div), time (4 μs/div).

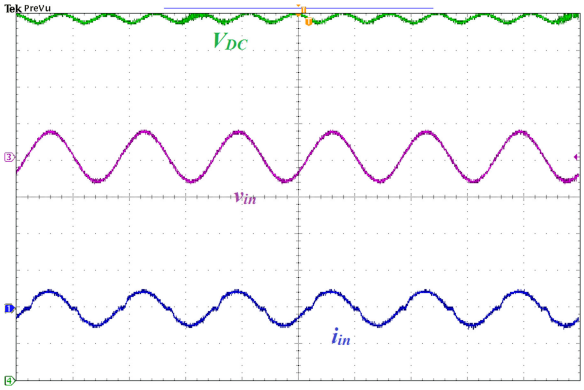

Fig. 18. Experimental results of the output voltage, input voltage, and the input current ($V_{\rm in} = 120$ V, $V_{\rm dc} = 100$ V). From top to bottom: $V_{\rm dc}$ (10 V/div), $v_{\rm in}$ (250 V/div), $i_{\rm in}$ (10 A/ div), time (10 ms/div).

Fig. 16 shows the experimental waveforms of input voltage and SEPIC capacitor C_1 voltage. It can be seen in the screenshot that SEPIC capacitor voltage is roughly equal to the absolute value of the input voltage. This agrees with the simulation results [see Fig. 10(b)].

Fig. 17 shows the waveforms of *LLC* converter at output voltage of 420 V in CV charging mode, and the charging current of 2.36 A. Due to the use of the proposed variable dc link control strategy, the circuit is still operating at the resonant frequency. The output voltage of the dc/dc converter follows the dc link voltage with the gain close to unity.

Figs. 18 and 19 demonstrate the experimental results of the converter operating in CC charging mode. Fig. 18 shows the operation of SEPIC converter with 120-V 60-Hz grid voltage and 100-V dc-link voltage, which is smaller than the peak grid input voltage. The power factor in this case is measured to be 0.983. The experimental waveforms agree with the simulated results. Fig. 19 shows the waveforms of *LLC* converter during constant charging with a CC of 3.6 A with the output voltage of 100 V.

In order to make a fair comparison with the state of the art, another 1-kW battery charger topology using a boost PFC stage and the same *LLC* topology is designed and controlled using a conventional fixed dc-link (390 V) control strategy.

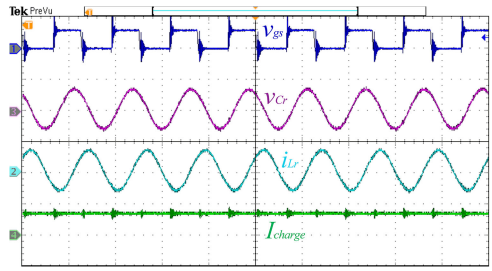

Fig. 19. Experimental results of the *LLC* charger ($V_{\rm bat} = 100$ V, $I_{\rm charge} = 3.6$ A). From top to bottom: $v_{\rm gs2}$ (25 V/div), $v_{\rm Cr}$ (250 V/div), $i_{\rm Lr}$ (20 A/div), $I_{\rm charge}$ (5 A/div), time (4 μs/div).

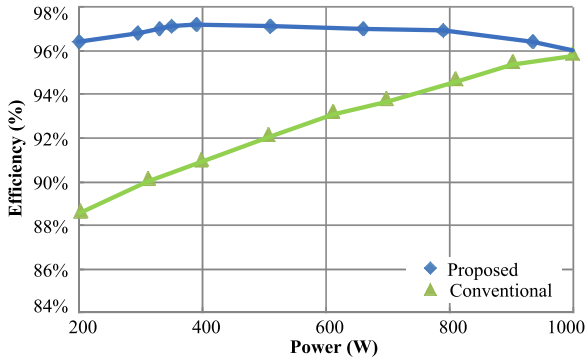

Fig. 20. Efficiency comparisons of the *LLC* resonant converter using conventional fixed input and proposed regulated input voltage topologies.

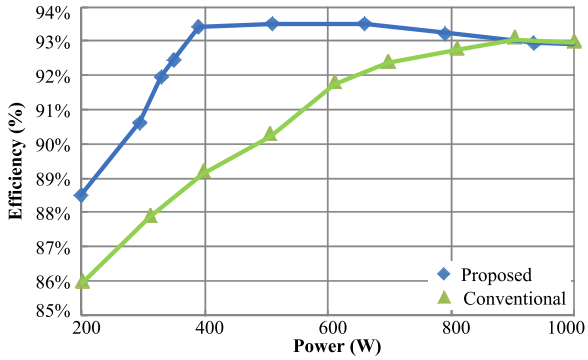

Fig. 21. Overall efficiency of a conventional boost stage charger with a fixed dc link voltage and the proposed SEPIC stage battery charger with a regulated dc-link voltage.

The measured efficiency results for both charger topologies are shown in Figs. 20 and 21. In Fig. 20, the experimentally measured efficiency curve of the *LLC* converter in the proposed topology with a variable dc link voltage is captured and plotted against the efficiency curve of the *LLC* converter in the conventional topology having boost PFC stage converter with a fixed dc link voltage.

Fig. 20 shows that the *LLC* converter with the proposed control strategy maintains higher efficiency around 97% at power levels from 200 to 1 kW compared to the *LLC* converter with the conventional control strategy, especially at light and medium loads. The efficiency curve for a conventional frequency-control *LLC* converter is measured with fixed input voltage and variable output voltage. The switching frequency is modulated to

TABLE III
EFFICIENCY COMPARISON OF PFC STAGE AND *LLC* STAGE

Load (W)	PFC stage efficiency (%)		*LLC* stage efficiency (%)		Overall system efficiency (%)	
	Conv. PFC	Prop. PFC	Conv. *LLC* ($V_{dc} - V_{out}$)	Prop. *LLC* ($V_{dc} - V_{out}$)	Conv. charger	Prop. charger
1000	97.1	96.2	95.8 (390–420 V)	96.6 (420–420 V)	93.0	93.0
900	97.8	96.6	95.2 (390–380 V)	96.3 (380–380 V)	93.1	93.1
600	98.3	96.4	93.0 (390–250 V)	97.0 (250–250 V)	91.5	93.5
400	98.0	96.2	91.0 (390–420 V)	97.1 (420–420 V)	89.2	93.4

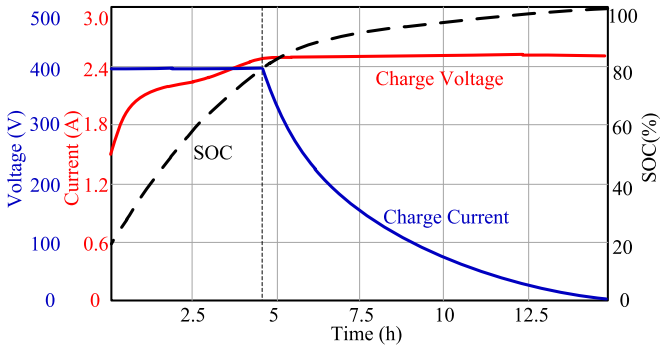

Fig. 22. Charging profile for a 4.8-kWh battery using 1-kW onboard battery charger.

regulate the battery voltage during charging. When the battery voltage is below the rated voltage, the switching frequency moves away from the resonant frequency, to reach the required voltage gain, resulting in a lower efficiency.

The overall efficiency curves of both the proposed and the conventional two-stage onboard chargers are shown in Fig. 21. Even though the peak overall efficiency of the proposed battery charger is 93.5%, it is interesting to note that using the proposed charger topology and the variable dc link control strategy the efficiency is improved over a wider range of output powers, i.e., from 88.5% to 93.5% corresponding to 20% of the rated load to full load.

In fact, the efficiency of SEPIC PFC stage might be slightly lower than the conventional boost PFC stage with the same output voltage at the same power level due to the higher voltage stress of the output diode and more passive components. However, by using the proposed control strategy, the efficiency of the *LLC* stage can be significantly improved as shown in Fig. 20. Due to the large improvement of the *LLC* stage efficiency, the overall efficiency of the proposed two-stage charger would be higher than the conventional one considering the efficiencies of both the PFC and *LLC* stages.

The conventional boost PFC with the fixed dc-link voltage control strategy is compared with the SEPIC PFC with adjustable dc link voltage at different loading conditions, as shown in Table III. The power levels and the output voltages are determined according to the charging profile of a 4.8-kWh Li-ion battery pack using the 1-kW two-stage onboard battery charger, as shown in Fig. 22 [12]. Since the capacity of the battery pack of a Chevrolet Volt is 16 kWh, here the capacity of the battery pack

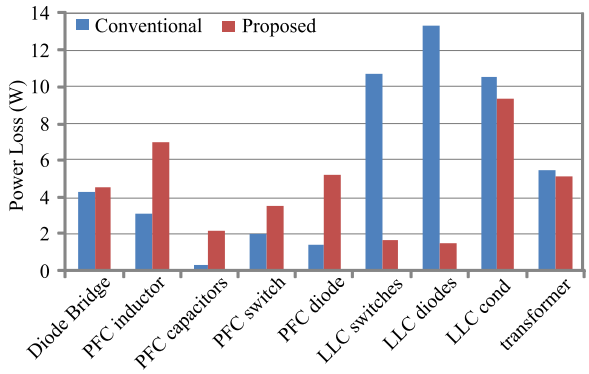

Fig. 23. Loss-breakdowns of the proposed and the conventional chargers at 600 W.

is proportionally scaled down along with the charger. Therefore, the charging profile of a 4.8-kWh battery pack is utilized in the experiments.

For the conventional charger, the constant dc link voltage is designed at 390 V in the middle of battery voltage range so that the *LLC* converter can operate in a limited frequency range for a wide output voltage range [3]–[5]. The dc link voltage and the output voltage are listed for *LLC* converters at each power level. In the case of the SEPIC PFC stage, the dc link voltage of the proposed two-stage charger can be regulated to follow the battery voltage during charging. Thus, the *LLC* converter can always operate in proximity of the resonate frequency. Hence, the efficiency of the *LLC* stage can be significantly improved as shown in Fig. 20. Due to the large improvement of the *LLC* stage efficiency, the overall efficiency of the proposed two-stage charger would be higher than the conventional one considering the efficiencies of the both PFC and *LLC* stages.

In addition, the proposed and conventional chargers are compared in terms of power losses. Fig. 23 shows the loss-breakdowns of PFC stages and *LLC* stages at 600 W.

In Fig. 23, the "*LLC* switches" indicate the turn-off switching loss of *LLC* switches, and the "*LLC* diodes" indicate the turn-on switching loss of the *LLC* converter's body diodes. The "*LLC* cond" includes the conduction losses of the resonant capacitor, *LLC* switches, and *LLC* diodes. The "transformer" includes the power losses of magnetizing inductor and the resonant inductor since the resonant inductor is integrated with the magnetizing inductor.

For the conventional charger operating at 600 W, the switching frequency of *LLC* converter is much higher than its primary resonant frequency since the dc link voltage is regulated at constant 390 V which is higher than the output voltage of 250 V. Thus, *LLC* switches turn ON at hard switching, and the body diodes of *LLC* switches turn OFF at hard switching as well. The power loss resulting from the *LLC* switches is much higher than that of *LLC* switches in the proposed charger.

VI. CONCLUSION

In this paper, an onboard PEV battery charger based on a SEPIC PFC converter and an *LLC* topology is proposed. The SEPIC PFC stage converter enables the dc link voltage to

follow the battery pack voltage with *LLC* converter operating in proximity of resonant frequency to optimize the conversion efficiency of the charger. The proposed charger architecture demonstrates attracting features such as:

1) compatibility with universal grid inputs;
2) ability to charge the fully depleted battery packs;
3) simplified control algorithm;
4) taking advantage of SiC MOSFETs to enhance the charger efficiency.

Both the small-signal modeling of SEPIC topology and the control loop analysis are carried out. Design considerations to ensure CCM operation and to limit the current and voltage ripples are discussed in detail. A novel-integrated magnetic solution for *LLC* topology with large primary leakage inductance is proposed, designed, and verified. A 1-kW charger prototype, which includes both the ac/dc and the isolated dc/dc converters, is designed to validate the proof of concept. Experimental results demonstrate that the designed charger is able to maintain a wide dc-link voltage range (100 V–420 V) while keeping the *LLC* converter operating at its maximum efficiency point. The SEPIC PFC converter achieves unity power factor, 2.72% THD, and 95.3% peak conversion efficiency. The *LLC* converter demonstrates 96.5% efficiency at full load condition (rated power) and 93.8% efficiency at light load condition (10% of rated power). The peak overall efficiency is 93.5% with the peak efficiency of *LLC* resonant converter as 97.1%. At 20% of the full load, the efficiency of *LLC* converter is 96.4%, and the overall efficiency of the charger is 88.5%.

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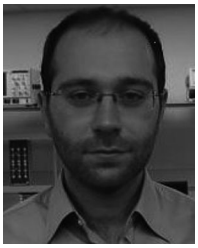

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