1MHz High Efficiency LLC Resonant Converters with Synchronous Rectifier

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***Abstract*- This paper proposes a novel synchronous rectifier driving scheme for resonant converters. An LLC resonant converter with proposed synchronous rectification is designed and analyzed. It is a high efficiency, high power density solution for future frond end converters. Hold up time extension capability is achieved for designed LLC resonant converter without sacrificing the efficiency for nominal condition. 1kW, 1MHz LLC resonant converter with proposed SR is built to demonstrate its advantages (size and efficiency) over the diode rectification and PWM converter. Overall 95.1% efficiency and 96W/in^3 power density are achieved.**

I. INTRODUCTION

Performance per watt requirements are driving higher energy efficiency metrics in server and telecom equipment designs for both idle and active power states. Hence there is a large incentive to increase the overall efficiency of power delivery systems. Two commonly used power delivery architectures are shown in Figure 1. It is obvious that the 400V/48V or 400V/12V DC/DC converter is the key to determine the whole power delivery system efficiency.

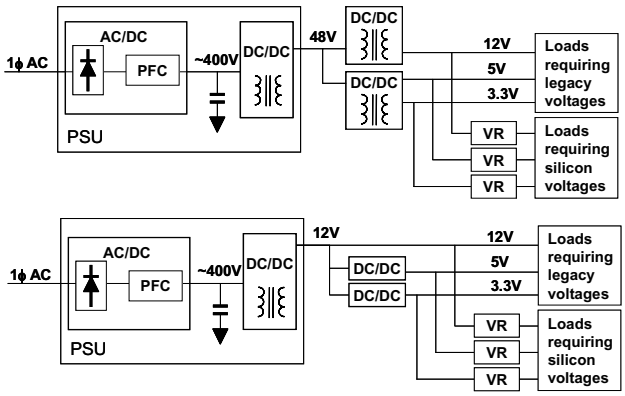

Figure 1. Typical power delivery architectures within servers.

Meanwhile, with the development of power conversion technology, power density becomes another challenge for DC/DC converters [1]-[3]. Although increasing switching frequency can dramatically reduce the passive component size, its effectiveness is limited by the converter efficiency and thermal management design. To overcome these issues, LLC resonant converters with synchronous rectifiers (SR) are proposed in this paper. The synchronous rectifiers with novel driving schemes for resonant converters can considerably reduce both body diode conduction loss and reverse recovery loss. The analysis shows that the LLC resonant converter with SR can achieve very high efficiency at 1MHz frequency.

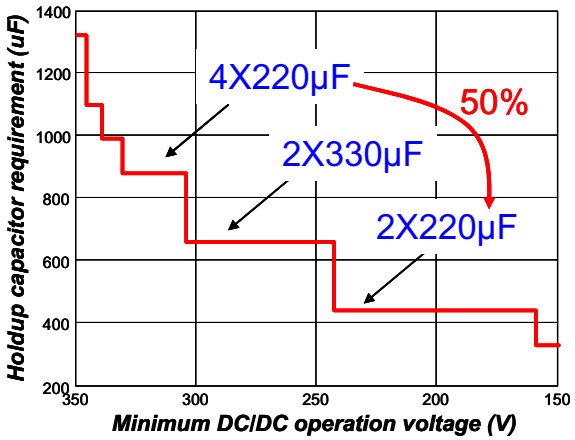

Figure 2. Holdup time capacitor requirement for DC/DC stage with different minimum input voltage.

On the other hand, to meet the holdup time requirement, bulky capacitors have to be used to provide the energy during holdup time, which is affected by DC/DC stage operation input voltage range. The relationship between holdup time capacitor requirement and minimum DC/DC stage input voltage for 1kW front-end converter is shown in Figure 2. Apparently, wide operation range DC/DC stage can reduce the holdup time capacitance. Therefore, the size and cost of the bulky capacitors are reduced. Higher system power density is obtained. With variable frequency control, the voltage gain of LLC resonant converter can be changed. During the hold up time, the operation frequency is far below the series resonant frequency. Thus, high voltage gain is achieved. While, at the nominal condition, the LLC resonant converter operates very close to the resonant frequency. The LLC resonant tank parameters can be optimized to achieve very low conduction loss and switching loss. The detail design procedure is provided in section III. As a result, hold up time extension capability is accomplished without sacrificing the nominal efficiency. The LLC resonant converter is considered as one of the most desirable topology for this application.

Finally, a 1MHz 1kW 400V-48V LLC resonant converter with SR is built to demonstrate the design. The over 95.1% efficiency is achieved for 20% ~ 100% load conditions. The experimental results verify the analysis and reveal that LLC resonant converter with SR is very promising for high-efficiency high-power density applications.

II. Driving Schemes of Synchronous Rectifiers for Resonant Converters

While diodes have been used in the past in power converter designs, power MOSFETs have much lower forward voltage drop than, for example, Schottky diodes, synchronous rectification, where a transistor is controlled to conduct at approximately the periods that a diode would conduct, has become a design of choice for such applications. However, for a synchronous rectifier (SR) to exhibit an advantage over a Schottky diode, very precise control over the switching control waveform is required in order to obtain advantageously reduced switching losses. Unlike PWM switching converters which have also been used in such applications, the turn-on times of switches on the primary side of the power converter circuit and the turn-on times of switches in the SR on the secondary side of the circuit are not exactly in phase for resonant converters and thus cannot use the same driving signal for control of conduction times. Otherwise, the SR would conduct circulating energy, namely a reverse current from the load to the source; thus causing much increased RMS currents and causing efficiency to deteriorate dramatically [4]. Therefore, some different driving arrangement for the SR is required.

For some types of resonant converters such as parallel resonant converters and series-parallel resonant converters, the transformer winding voltage may be used to drive the SR [5]. However, for other types of synchronous rectifiers such as a series resonant converter and a LLC resonant converter illustrated in Figure 3 and Figure 4, respectively, the polarity of the voltage on the secondary winding can change only after the SR is turned off. In other words, when the SR is on, the voltage on the secondary winding of a transformer or autotransformer is clamped to the output voltage and thus cannot change polarity before the SR is turned off and, as a result, the voltage on the secondary winding cannot be used to control the SR (e.g. which must be controlled prior to the change in polarity on the transformer secondary). To solve this problem, it has been proposed to utilize the leakage inductance of the transformer to reshape the terminal voltage of the transformer secondary in order to derive a signal to drive the SR [6]. However, due to addition voltage stress caused by such an arrangement, such a solution is only suitable for power converter structures having a very low voltage output, usually limited to a very few volts. Further, such an arrangement is strongly dependent of di/dt effects. It has also been proposed to use transformer secondary currents for SR control drive signals: when the body diode of the SR conducts, the SR is turned on and when the current become zero or becomes negative, the SR is turned off. However, this proposed SR control scheme suffers from the obvious drawbacks that a current transformer is awkward to fabricate and leads to increased size and cost while its insertion inductance may compromise high frequency performance such as high voltage stress and higher switching losses.

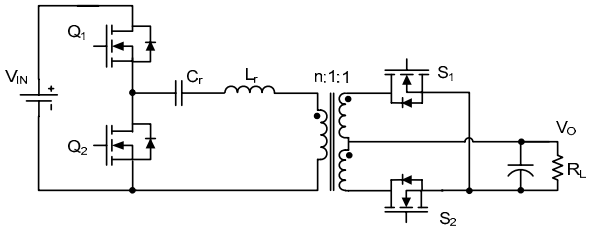

Figure 3. Series resonant converter with SR.

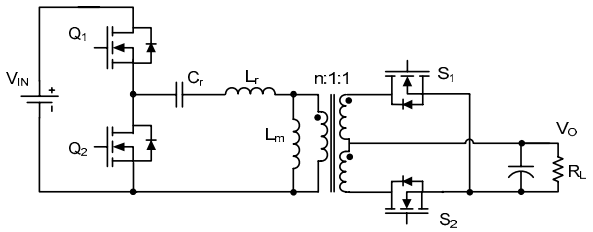

Figure 4. LLC resonant converter with SR.

A possible driving method is to sense the drain to source voltage of the SR. The sensed Vds of SR is processed by control circuits to determine the level of the current. The SR can be switched in close proximity of the zero current transition. With advanced IC technology and proper noise immunity layout, precise voltage sensing range is reached around millivolt without problem. However, the accuracy of this driving scheme is highly affected by the package of the SR. Due to the inevitable package inductance, the sensed terminal drain to source voltage of SR is actually the sum of MOSFET resistive voltage drop and package inductive voltage drop. In Figure 5, it is clearly shown that the sensed Vd's of SR terminal is far deviated from the real Vds of MOSFET. The SR drive signal is much shorter than the expected value.

$$\text{SR duty cycle: } D_{SR} = \frac{T_{on\_SR}}{T_S / 2}. \tag{1}$$

$$D_{SR} = \frac{\pi - a\tan\left(2\pi f_s \frac{L_{SR}}{R_{ds\_on}}\right) - a\sin\left(\frac{-V_{th1}}{I_o \cdot \frac{\pi}{2} \cdot R_{ds\_on} \cdot \left|1 + j \cdot 2\pi f_s \frac{L_{SR}}{R_{ds\_on}}\right|}\right)}{\pi}. \tag{2}$$

The duty cycle of SR is defined in (1) and is calculated in (2). The D_{SR} is determined by SR package inductance L_{SR}, SR R_{ds_on}, switching frequency f_s, turn off threshold voltage V_{th1} and load current I_o.

The DirectFet is considered the device with the least package inductance. Only 0.5nH inductance is observed for this compact package [9]. For the tested 12V output prototype, IRF6635 DirectFet is chosen. The R_{ds_on} is 1.3mΩ. The actual duty cycle vs. switching frequency & load current for different package inductance is plotted in Figure 6 and Figure 7 respectively. The higher the switching frequency, the worse it becomes. Much higher package inductance exists in packages other than DirectFet. The operation condition is even worse.

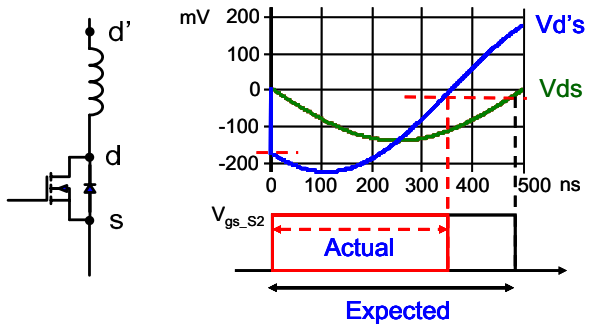

Figure 5. Sensing voltage deviation due to SR package inductance.

In order to overcome the issue of L_{SR}, a novel phase compensation driving scheme is proposed in this paper. A block diagram of the proposed circuit is shown in Figure 8. The main sections are the V_{ds} phase compensation network, signal processing and gate driver stages for the SR. The input signal to the proposed driving circuit is voltage waveform across the physical terminal of power MOSFET SR. Based on the analysis mentioned above, such voltage waveform is actually $V_{d's}$ and can not be directly used to drive the SR. An active phase compensation network is used to provide the true resistive voltage of V_{ds}. Thus, the generated voltage reflects exactly the conduction period of SR. The phase compensated V_{ds}, as the output signal of the compensation network, is then transferred into the next stage. The post signal processing block consists of a set of window comparators which converters the input signal into control pulses. The driving circuit utilizes these control pulses to drive SR ultimately. Discrete transistors or developed IC chips can implement such functions.

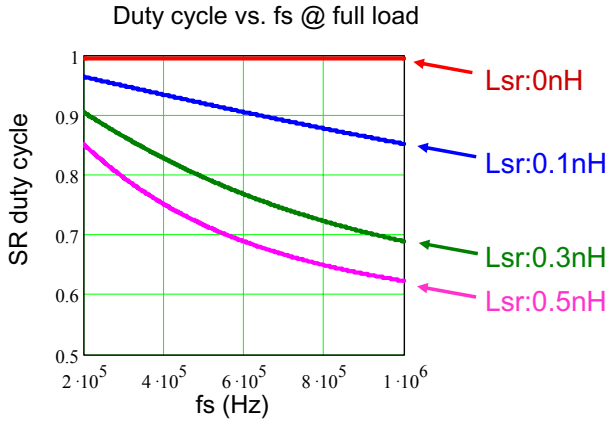

Figure 6. SR duty cycle vs. fs for different L_{SR}.

The detail schematic of active phase compensation network is illustrated in Figure 9. Rcs and Ccs are passive network to generate compensated voltage. Sa and Sb are small signal active switches to reset the passive phase compensation network for each cycle. The gate signals for Sa, Sb and main SR are plotted in Figure 10. During t0~t1, the SR is turned off, Sa is also turned off. Vcs represent the voltage of SR. Thus compensation network remains off. The equivalent circuit is shown in Figure 11. At t1, the voltage of SR becomes negative and the SR is turned on immediately. Sa is turned on at this moment either. Small period t1~t2 guarantees the full turn-on of SR and also eliminates adverse effect of oscillation. The compensation network is in reset mode. During t2~t3, Sb is turned off. Passive compensation network provides the resistive voltage drops on SR. The equivalent circuit is drawn in Figure 12. At t3, the current of SR is close to zero. The SR is turned off. Then the SR can achieve zero current and zero voltage turn off. Similarly, short period t3~t4 is set to avoid the adverse effect of turn off ringing.

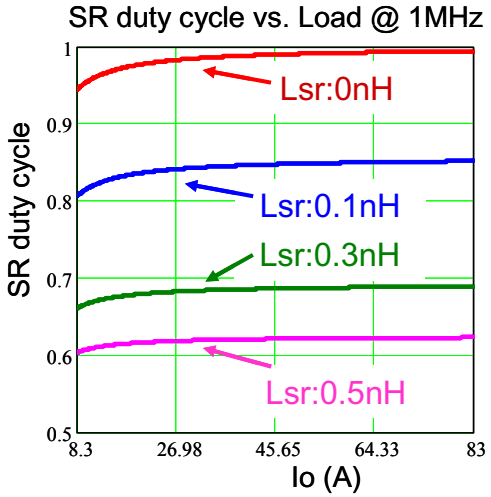

Figure 7. SR duty cycle vs. load for different L_{SR}.

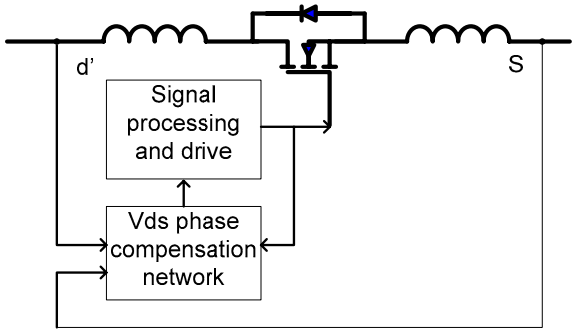

Figure 8. Simplified functional diagram for proposed SR driving scheme.

To precisely capture the resistive voltage drop on SR, the phase compensation network should be properly designed. Assuming the current goes through SR is iLsr(s), the compensated voltage can be expressed as follows:

$$Vcs(s) = \frac{Isr(s) \cdot Rds \cdot (1 + s \cdot Lsr / Rds)}{1 + s \cdot Rcs \cdot Ccs} \quad (3)$$

If $Rcs \cdot Ccs = \frac{Lsr}{Rds}$ (4) and

$$V_{cs}(t1\_) = V_{Rds\_on}(t1\_) \quad (5),$$

then $V_{cs}(s) = Isr(s) \cdot Rds = V_{Rds\_on}(s)$ (6)

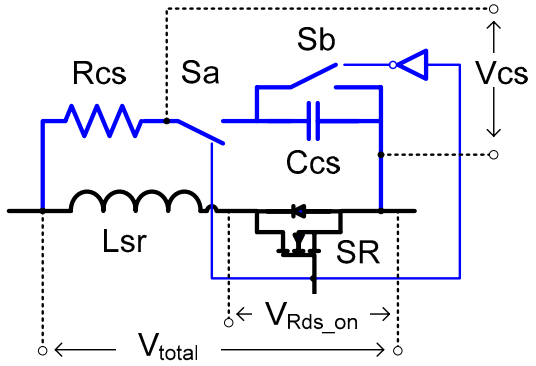

Figure 9. Schematic of Vds phase compensation network.

The passive compensation network is designed to satisfy (3), (4) and (6). The active switches are set to satisfy (5). As a result, the compensation network can precisely represent the voltage of the power MOSFET on resistance. The simulation result is shown in Figure 13. The SR is modeled as an ideal switch in series with R_{ds_on} and L_{SR}. The V_{total} is the terminal voltage Vd's. The V_{Rds_on} is the actual resistive voltage of SR Vds. The Vcs is the compensated voltage for SR driving scheme. It can be seen that Vcs follows V_{Rds_on} very well. Theoretically, they are identical in phase and amplitude. The experimental result will be analyzed in Section IV. It should be noted that the proposed SR drive method can be extended to other resonant converters and PWM converters.

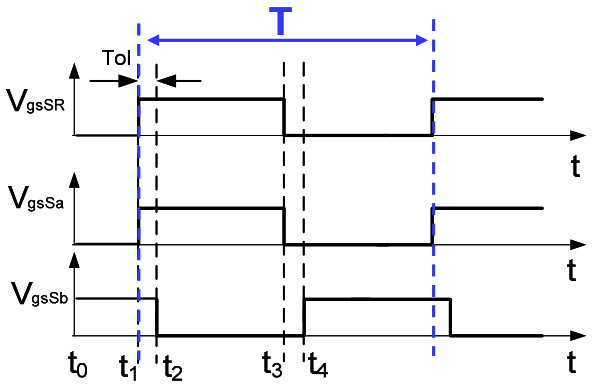

Figure 10. . Gate signal for Sa, Sb and main SR.

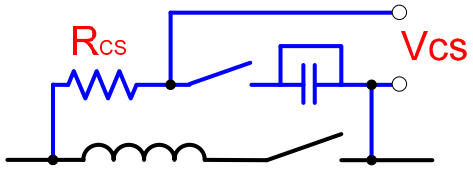

Figure 11. Equivalent circuit during SR is off.

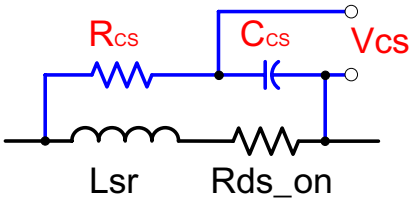

Figure 12. Equivalent circuit during SR is on.

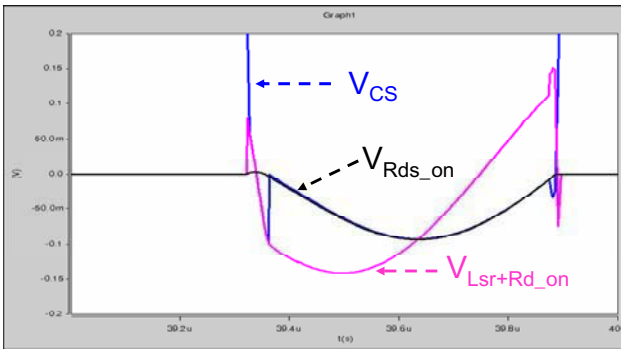

Figure 13. Simulation result for V_{Rds_on}, V_{total} and V_{cs} represented in Figure 9.

III. Design and Analysis of LLC Resonant Converter with SR

The DC gain characteristic of the LLC resonant converter is depicted in Figure 14. The resonant ridge is the boundary line of zero voltage switching (ZVS) and zero current switching (ZCS) regions. Due to utilization of MOSFET as primary side switches, ZVS is preferred.

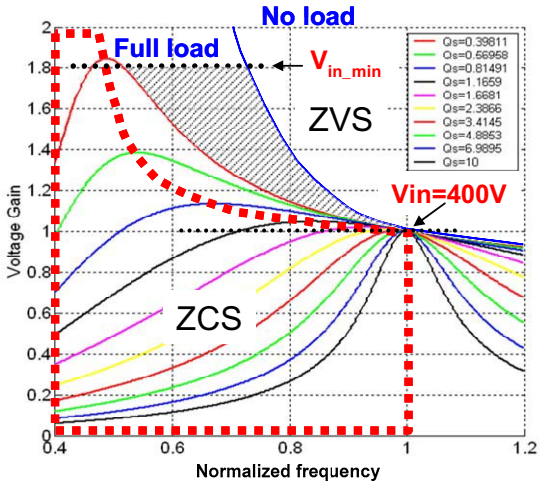

Figure 14. The DC gain characteristic of the LLC resonant converter.

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{7}$$

$$Q = \frac{\sqrt{L_r / C_r}}{n^2 R} \tag{8}$$

$$L_n = \frac{L_m}{L_r} \tag{9}$$

$$iL_{m\_pk} = \frac{nV_o}{L_m \frac{1}{4 f_{s0}}} \tag{10}$$

$$\frac{iL_{m\_pk}}{2} \geq \frac{V_{bus} C_{jun\_eq}}{t_{dead}} \tag{11}$$

$$L_m \leq \frac{t_{dead}}{16 f_0 C_{jun\_eq}} \tag{12}$$

$$L_n Q = \frac{L_m}{L_r} \frac{\sqrt{\frac{L_r}{C_r}}}{n^2 R_L} = \frac{L_m}{n^2 R_L \sqrt{L_r C_r}} = \frac{2\pi f_0 L_m}{n^2 R_L} \tag{13}$$

$$V_{in\_min} = \sqrt{V_{in\_nom}^2 - \frac{2 P_o T_{holdup}}{C_{holdup} \eta_{avg}}} \tag{14}$$

$$M_{max} = \frac{nV_o}{2V_{in\_min}} \tag{15}$$

The resonant frequency, quality factor and inductance ratio are defined in (7), (8) and (9) respectively. When switching frequency is less than or equals the resonant frequency, the primary side turn off current is determined by the magnetizing current. The LLC resonant converter is preferable to operate at resonant frequency. The LLC resonant converter can achieve lowest circulating energy at the resonant frequency. Also, the turn off current of primary side achieves the lowest value. Therefore, the highest efficiency is accomplished at the resonant frequency. When switching frequency is higher than the resonant frequency, the turn off current is much higher than the magnetizing current. Consequently, much larger switching loss deteriorates the converter efficiency. To avoid high switching loss, the switching frequency is designed not beyond the resonant frequency. The operation region is also shown in Figure 14. During the nominal condition, the LLC resonant converter operates close to the resonant frequency to achieve highest efficiency. During the hold up time, the switching frequency is reduced to provide the high voltage gain. The operation region is illustrated in the shaded area.

The magnetizing current helps to achieve ZVS from zero loads to full load range. On the other hand, too large magnetizing current increases the circulating energy of the resonant tank. The magnetizing inductance is designed to guarantee the ZVS without increasing too much circulating energy. Based on the basic operation analysis of LLC resonant converter, the ZVS condition is ensured by the peak magnetizing current. In the defined operation region, the minimum peak magnetizing current exists at the resonant frequency. It can be calculated in (10). To ensure ZVS operation for the whole operation range, such minimum peak magnetizing current should be able to charge and discharge total equivalent device junction capacitors C_{jun_eq} within dead time t_{dead}. Therefore, the equation (11) is a must. Combining (10) and (11), the minimum magnetizing inductance is given in (12). Achieving ZVS can eliminate turn on loss. On the other hand, turn off loss should be minimized to improve the efficiency. For LLC circuit, smaller turn off current is desirable to reduce turn off loss. The larger the Lm, the less the switching loss. Therefore, the optimal Lm should be designed to exactly satisfy the ZVS requirement.

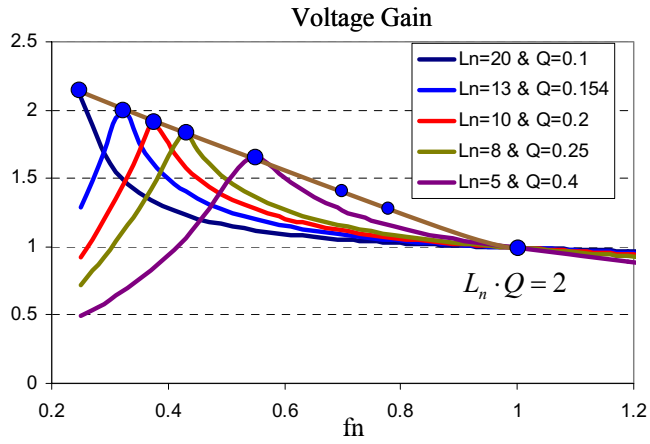

Figure 15. The peak voltage gain curve for constant $L_n \cdot Q$.

Following simple algebra, substitution of (7) and (8) into (9) yields (13). R_L represents the full load resistance. Since f_0 and n are constant values, the product of L_n and Q is also a constant value for the designed L_m. To obtain the resonant tank parameters, L_n and Q values should be determined. The hold up time voltage gain requirement becomes another constraint to finalize the design. A series of voltage gain curves is plotted in Figure 15. For each voltage gain curve, the product of L_n and Q remains constant. Namely, based on (13), the magnetizing inductance is a fixed value. Once the peak point of each curve is connected, a peak voltage gain curve is created. Such peak voltage gain curve is uniquely defined by the specific value of L_n•Q. If L_n•Q is continuous changed, the peak voltage gain surface can be illustrated in Figure 16.

Based on the hold up time requirement, the LLC resonant converter has to provide the power to the load as the input voltage drops to V_{in_min}, which is provided in (14). The nominal input voltage V_{in_nom} is assumed as 390V (PFC output voltage ripple is considered). The output power P_o is 1kW. Hold up time T_{holdup} is 20ms. Hold up capacitance C_{hodup} is 2x220μF. The average efficiency η_{avg} during the hold up time is conservatively assumed as 90%. The hold up time maximum voltage gain M_{max}=1.77 can be calculated from (15).

In order to leave some margin, M_{max}=1.87 is adopted for the design. Mapped into the voltage gain plot, M_{max} becomes a horizontal plane, which is depicted in Figure 17. There is a borderline of M_{max} horizontal plane and the LLC peak voltage gain surface. This boundary line or Curve B represents all the possible combinations of L_n and Q, which can achieve specified M_{max}.

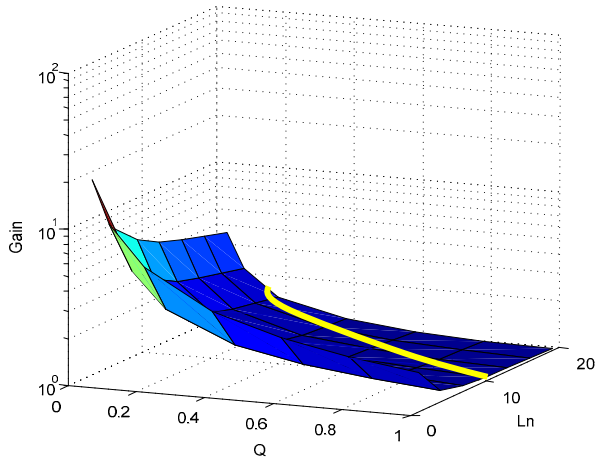

Figure 16. The peak voltage gain surface for different $Ln \cdot Q$.

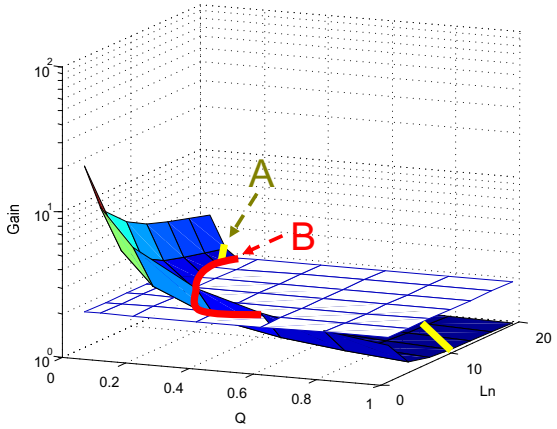

Figure 17. The hold up time maximum voltage gain plane.

According to aforementioned discussion, there is another peak voltage gain curve or Curve A, which is determined by constant L_n•Q or designed magnetizing inductance. There is one and only one intersection point between Curve A and Curve B. Such intersection point, which is shown in Figure 18, reveals the design point. Namely, L_n and Q can be obtained. Therefore, based on (8) and (9), the remaining resonant tank parameters L_r and C_r can be determined.

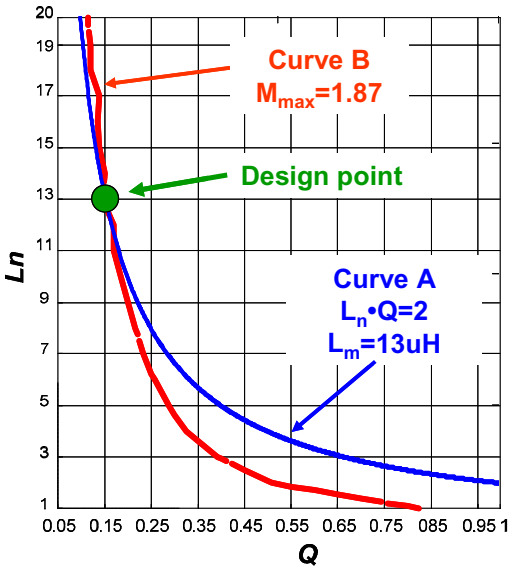

Figure 18. The intersection point between Curve A and Curve B reveals the design point.

IV. Experimental Results

A 1MHz 1kW 400V-48V prototype, shown in Figure 19, is built to verify the proposed driving scheme and design for LLC resonant converters with SR. Following the design procedure discussed in section III, the L_m is chosen as 13µH. The resonant inductor Lr is 1µH and the resonant capacitor is chosen as 25nF. The transformer turns ratio is 4. With careful design, the resonant inductor is integrated with the transformer. As a result, there is only one magnetic component in the prototype. The 96W/in^3 power density is achieved.

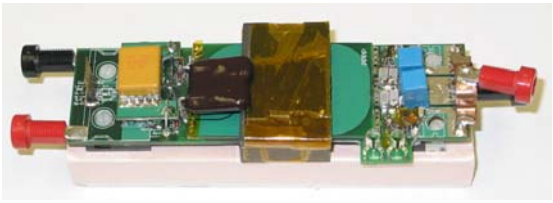

Figure 19. 1MHz 1kW 400V-48V LLC resonant converter with SR.

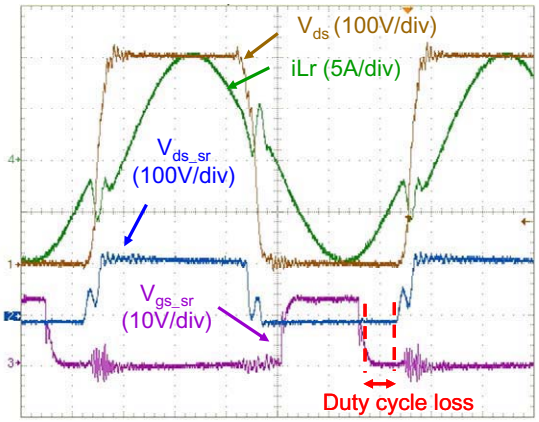

Figure 20. Waveforms of SR without compensation network.

The waveforms of SR for LLC resonant converter without compensation network are shown in Figure 20. The SR duty cycle loss is obvious and matches the analytical result derived in section II. With proposed SR driving method, the SR duty cycle loss is minimized. The waveform is shown in Figure 21.

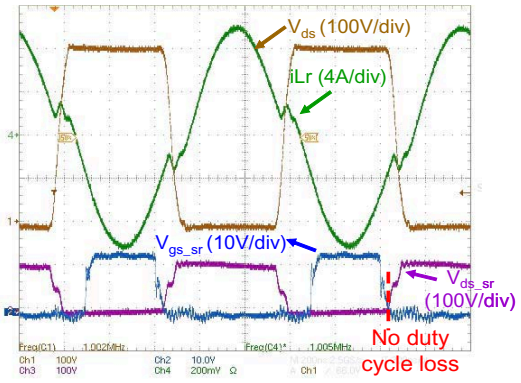

Figure 21. Waveforms of SR with proposed driving scheme.

Another 1MHz 1kW 400V-48V LLC converter with Schottky diode rectifiers is also built for comparison. The waveforms are shown in Figure 22. For LLC converter with SR, the body diode conduction time is almost reduced to zero. Therefore, the reverse recovery issues are minimized. With great improvement both on conduction loss and switching loss, the over 95.1% efficiency can be achieved for 20%~100% load range. The efficiency curves for different prototypes are drawn in Figure 23. The efficiency of popular asymmetrical half bridge PWM DC/DC converter (200kHz, 1kW) is also plotted. It is clear that LLC resonant converter can achieve much higher efficiency than PWM counterpart.

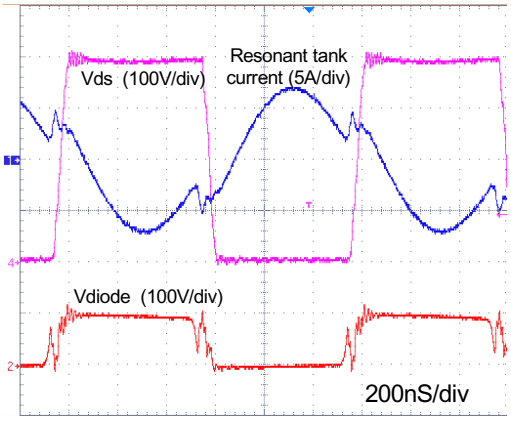

Figure 22. Waveforms of LLC resonant converter with Schottky diode rectifiers.

V. Conclusion

This paper describes 1MHz highly efficient, high power density LLC resonant converters. A novel SR driving scheme is proposed for resonant converters. The LLC resonant converter is designed to achieve high efficiency at the nominal condition. During hold up time, the LLC resonant converter can operate until the input voltage drop to very low value. Thus, the high voltage gain of LLC resonant converter is designed to reduce the hold up capacitor. Size and cost can be saved for the whole system.

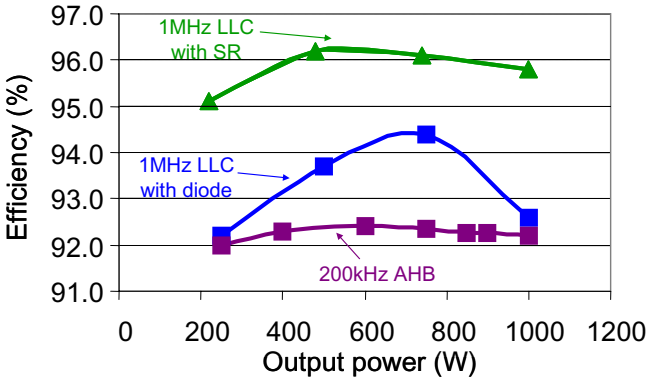

Figure 23. Efficiency comparison for different DC/DC converters.

A 1MHz, 1kW LLC resonant converter with SR is built to verify the theoretical analysis and optimal design. The experimental results show that the proposed LLC resonant converter with SR can achieve low stresses, high efficiency and high power density.

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