Assignment 3

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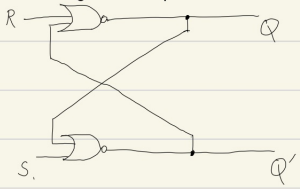
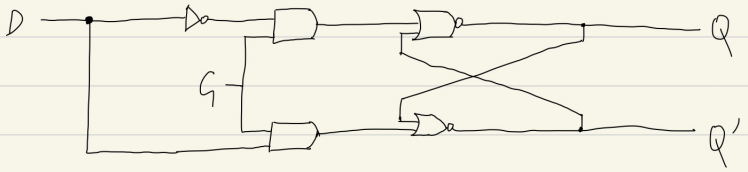
1 Q1

1.

(a). We use NOR gates for the SR latch part, we have:



We use 2 AND gates and an invert for the other, we have:

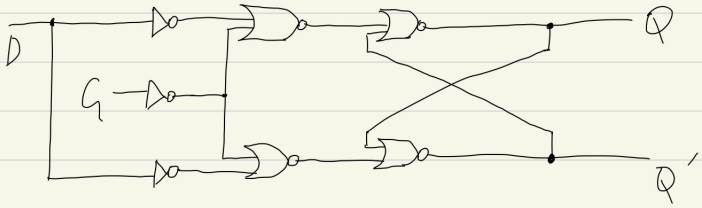


According to the circuit, we find its truth table is:

Present		Next.
D_t	Q_t	Q_{t+1}
0	0	0
0	1	0
1	0	1
1	1	1

This truth table is the same as the one in class, Hence we have verified the circuit operation.

(b) We use NOR gates and inverters to generate the D latch, the circuit is based on the last one:



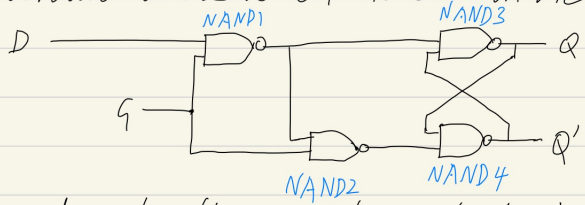
According to the circuit, we find its truth table is:

Present		Next.
D_t	Q_t	Q_{t+1}
0	0	0
0	1	0
1	0	1
1	1	1

This truth table is the same as the one in class, Hence we have verified the circuit operation.

2.

(c). We use four NAND gates to generate the D-latch. The circuit is based on the one in the class.



According to the circuit, we find its truth table is:

Present		Next.
D_t	Q_t	Q_{t+1}
0	0	0
0	1	0
1	0	1
1	1	1

This truth table is the same as the one in class. Hence we have verified the circuit operation.

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2 Q2

2.

(a) According to the meaning of the question, we can get the characteristic table:

P	N	Q
0	0	0
0	1	Q
1	0	Q'
1	1	1

(b). First, we have the truth table of P, N, Q_t, Q_{t+1}

P	N	Q_t	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

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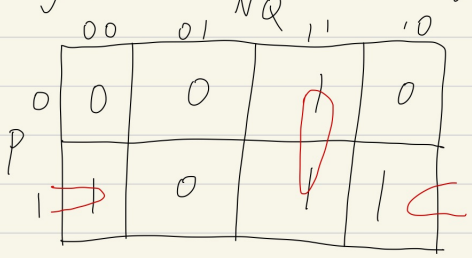
According to the truth table, we get the k-map.



we have $Q_{t+1} = P \cdot Q_t' + NQ_t$

cc). According to the meaning of the question, we can get the excitation table:

Q_t	Q_{t+1}	P	N
0	0	0	x
0	1	1	X
1	0	x	0
1	1	x	1

5.

(d). According to (b), we know the characteristic equation of PN flip-flop is $Q_{t+1} = PQ'_t + NQ_t$

The truth table of D flip-flop:

D	Q_{t+1}
0	0
0	1

Hence the characteristic equation of D flip-flop is $Q_{t+1} = D$.

In order to convert PN flip-flop to D flop-flop, we let $P = N = D$.

Then $Q_{t+1} = PQ'_t + NQ_t = DQ'_t + DQ_t = D(Q'_t + Q_t) = D$.

In this case, PN flip-flop and D flip-flop have the same characteristic equation.

Hence PN flip-flop can be converted to a D flip-flop.

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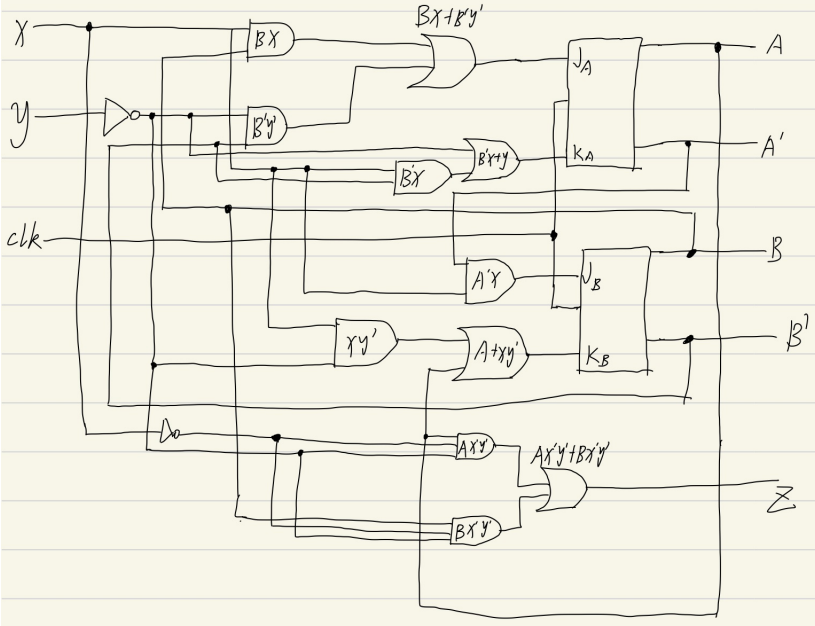
3 Q3

3.(a).

We know that $J_A = Bx + B'y'$, $K_A = B'x + y$, $J_B = A'x$, $K_B = A + xy$, and the logic diagram of the circuit has two JK flip-flop



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(b) According to the logic diagram of the circuit, we find the state table:

x	y	A_t	B_t	A_{t+1}	B_{t+1}	z	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	0	1	1	0	0	1
0	0	1	1	1	0	1	0	0	0	1
0	1	0	0	0	0	0	0	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	0	0	0	1	0	1
0	1	1	1	0	0	0	0	1	0	1
1	0	0	0	1	1	0	1	1	1	1
1	0	0	1	1	0	0	1	0	1	1
1	0	1	0	0	0	0	1	1	0	1
1	0	1	1	1	0	0	1	0	0	1
1	1	0	0	0	1	0	0	1	1	0
1	1	0	1	1	1	0	1	1	1	0
1	1	1	0	0	0	0	0	1	0	1
1	1	1	1	0	0	0	1	1	0	1

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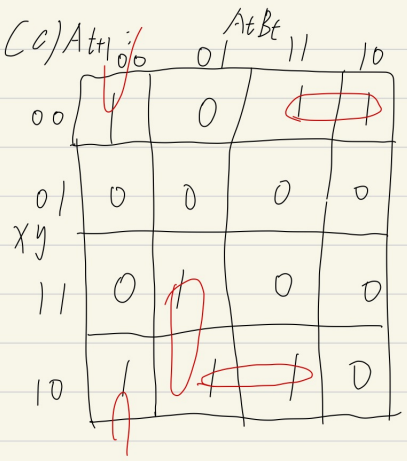
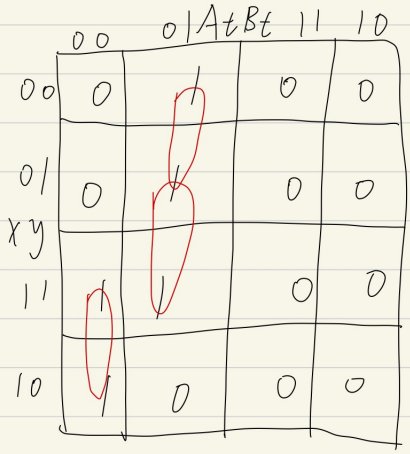
(c) A_{t+1} :



$A_{t+1} = xA_t'B_t + xy'B_t' + x'y'A_t + yA_tB_t$

$= A'Bx + B'xy + Ax'y + ABy'$



$B_{t+1} = xA_t'B_t' + x'A_t'B_t + yA_t'B_t$

$= A'B'x + A'Bx' + A'By$

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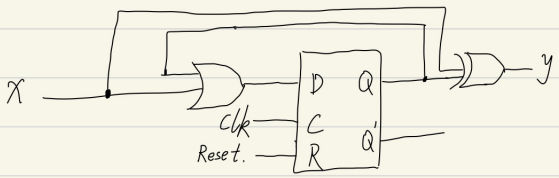
4 Q4

4.

According to the meaning of the question, we have the following truth table:

x(input)	Q_t	Q_{t+1}	y(output)
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	0

we next use D flip-flop to generate the circuit:



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