CS 207 Digital Logic - Spring 2020
Lab 14

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May 20, 2020

Objective

1. Use your Verilog knowledge to finish the mini-project.

Lab Exercise Submission

1. You should name all source code as instructed. Mis-named files will not be recognized.
2. You should submit all source code files with an extension "`.v`".
3. You should submit all source code directly into the sakai system below. **Do not compress them into one folder.**

   `https://sakai.sustech.edu.cn/portal/site/ebf68254-68c5-4cfe-9d42-b26758f854ee`
4. Lab exercises should be submitted before the deadline, typically one week after the lab session. No late submission policy applies to lab exercises.

1 Mini-project

Design and verify a 32-bit unsigned divider. The module should takes 32-bit length inputs A and B, calculate A/B, output a 32-bit length quotient Q and a 32-bit length remainder R. The module should also have necessary I/O pins, including `CLK` and `reset` which resets the calculation on low voltage (`0`). The calculation is performed on the positive edge of `CLK`. You **cannot** use

- `assign Q = A / B;`, or
- `assign R = A % B;`.

The module should follow the design below:

divide.v

```
module divide(Q, R, A, B, CLK, reset);
// Module Code
endmodule
```

and save in file `divide.v`.

Assignment

Save the source code in **`divide.v`**. Upload this file to Sakai under **Assignments → Lab Exercise 14**.