CS 207 Digital Logic - Spring 2020
Lab 8

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Objective

1. Follow up combinational circuit design.

Lab Exercise Submission

1. You should name all source code as instructed. Mis-named files will not be recognized.
2. You should submit all source code files with an extension "`.v`".
3. You should submit all source code directly into the sakai system below. **Do not compress them into one folder.**

   `https://sakai.sustech.edu.cn/portal/site/ebf68254-68c5-4cfe-9d42-b26758f854ee`
4. Lab exercises should be submitted before the deadline, typically one week after the lab session. No late submission policy applies to lab exercises.

1 Exercise

1.1 Exercise 1

Implement a three-way voter with A, B, C inputs and F output **using gate-level design**. The voter outputs `1` when at least two inputs are `1`, otherwise the output is `0`. The module should follow the design below:

voter.v

```
module voter(F, A, B, C);
// Module Code
endmodule
```

and save in file `voter.v`.

> **Assignment**
> Save the source code in **`voter.v`**. Upload this file to Sakai under **Assignments → Lab Exercise 8**.

1.2 Exercise 2

Implement a one-bit comparator with A, B inputs and a 3-bit F output **using gate-level design**. When $A < B$, the first bit of F, i.e., `F[0]`, is `1`, and the other two bits are `0`. When $A = B$, the second bit is one and others zeros. When $A > B$, the third bit is one and others zeros. The module should follow the design below:

comparator_1.v

```
module comparator_1(F, A, B);
// Module Code
endmodule
```

and save in file `comparator_1.v`.

> **Assignment**
> Save the source code in **`comparator_1.v`**. Upload this file to Sakai under **Assignments → Lab Exercise 8**.

1.3 Exercise 3

Implement an eight-bit comparator with 8-bit A, B inputs and a 3-bit F output. When $A < B$, the first bit of F, i.e., `F[0]`, is `1`, and the other two bits are `0`. When $A = B$, the second bit is one and others zeros. When $A > B$, the third bit is one and others zeros. The module should follow the design below:

comparator_8.v

```
module comparator_8(F, A, B);
// Module Code
endmodule
```

and save in file `comparator_8.v`.

Assignment

Save the source code in `comparator_1.v`. Upload this file to Sakai under **Assignments → Lab Exercise 8**.

1.4 Exercise 4

Implement the following function with a 4-bit input x and a 4-bit output y:

$$y = \begin{cases} x & 0 \leq x < 5 \\ 5 & 5 \leq x \leq 10 \\ 15 - x & 10 < x \leq 15 \end{cases} .$$

The module should follow the design below:

`sfunction.v`

```
module sfunction(Y, X);
// Module Code
endmodule
```

and save in file `sfunction.v`.

Assignment

Save the source code in `sfunction.v`. Upload this file to Sakai under **Assignments → Lab Exercise 8**.

Assignment

When you finished Lab Exercise 8, there should be four `.v` files in the Sakai system: `voter.v`, `comparator_1.v`, `comparator_8.v`, and `sfunction.v`.