# CS 207 Digital Logic - Spring 2020
# Assignment 2

Deadline: Friday, Apr 10

Write down your answer to the questions on a new sheet with **detailed** procedures.
Drawing the circuit only will lead to zero point.

1. (0.5 points) Design a four-bit 2's complementer with only OR and XOR gates.
2. (0.5 points) Design a combinational circuit with three inputs, $x$, $y$, and $z$, and three outputs, $A$, $B$, and $C$. When the binary input is $0$, $1$, $2$, or $3$, the binary output is one greater than the input. When the binary input is $4$, $5$, $6$, or $7$, the binary output is two less than the input.
3. (0.5 points) A majority circuit is a combinational circuit whose output is equal to $1$ if the input variables have more $1$'s than $0$'s. The output is $0$ otherwise. Design a 3-input majority circuit by finding the circuit's truth table, Boolean equation, and a logic diagram.
4. (0.5 points) An 8-to-1 MUX has inputs $A$, $B$, and $C$ connected to selection lines $S_2$, $S_1$, and $S_0$ respectively. The data inputs $I_0$ to $I_7$ are connected as $I_1 = I_2 = I_7 = 0$, $I_3 = I_5 = 1$, $I_0 = I_4 = D$, and $I_6 = D'$. Determine the Boolean expression of the MUX output.
5. (1.0 points) Implement the Boolean function $F(A, B, C, D) = \sum(1, 3, 4, 11, 12, 13, 15)$ using
   (a) decoder and external gates, and
   (b) 8-to-1 MUX and external gates.