CS 207 Digital Logic - Spring 2020
Assignment 3

Deadline: Friday, Apr 24

Write down your answer to the questions on a new sheet with **detailed** procedures.
Drawing the circuit only will lead to zero point.

1. (0.9 points) The D latch is constructed with four NAND gates and an inverter in the class. Consider the following three other ways for obtaining a D latch. In each case, draw the logic diagram and verify the circuit operation.
   (a) Use NOR gates for the SR latch part and AND gates for the other two. An inverter may be needed.
   (b) Use NOR gates for all four gates. Inverters may be needed.
   (c) Use four NAND gates only (without an inverter).

2. (0.8 points) A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.
   (a) Tabulate the characteristic table.
   (b) Derive the characteristic equation.
   (c) Tabulate the excitation table.
   (d) Show how the PN flip-flop can be converted to a D flip-flop.

3. (0.7 points) A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are $J_A = Bx + B'y'$, $K_A = B'x + y$, $J_B = A'x$, $K_B = A + xy'$, $z = Ax'y' + Bx'y'$.
   (a) Draw the logic diagram of the circuit.
   (b) Tabulate the state table.
   (c) Derive the state equations for A and B.

4. (0.6 points) Design a one-input, one-output serial 2's complementer. The circuit accepts a string of bits from the input, and outputs 0's until the first 1 is received. After that, the 2's complement of the input is generated at the output. The circuit can be reset asynchronously to reset the operation.