CS 207 Digital Logic - Spring 2020
Assignment 5

Deadline: Friday, May 22

Write down your answer to the questions on a new sheet with **detailed** procedures. Drawing the circuit only will lead to zero point.

1. (1.0 points) Design a synchronous counter that has the following sequence: `0010`, `0110`, `1000`, `1001`, `1100`, `1101`, and repeat. From the undesired states the counter must always go to `0010` on the next clock pulse.

2. (1.0 points) Show that a BCD ripple counter can be constructed using a four-bit binary ripple counter with asynchronous clear and NAND gates that detects the occurrence of count `1010`.

3. (1.0 points) Design a timing circuit that provides an output signal that stays on for exactly twelve clock cycles. A start signal sends the output to the `1` state, and after twelve clock cycles the signal returns to the `0` state.