DIGITAL DESIGN

Faculty Of Computers And Information Technology

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Chapter 4

Discussion

Chapter 5

Question 1

The *D* latch is constructed with four NAND gates and an inverter. Consider the following three other ways for obtaining a *D* latch. In each case, draw the logic diagram and verify the circuit operation.

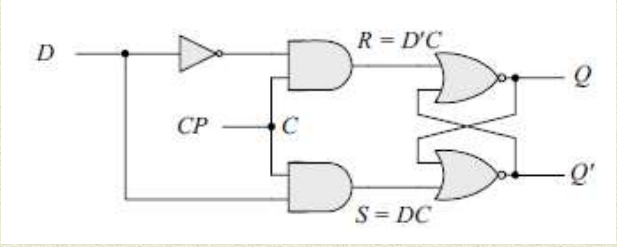
(a) Use NOR gates for the *SR* latch part and AND gates for the other two. An inverter may be needed.

(b) Use NOR gates for all four gates. Inverters may be needed.

(c) Use four NAND gates only (without an inverter). This can be done by connecting the output of the upper gate

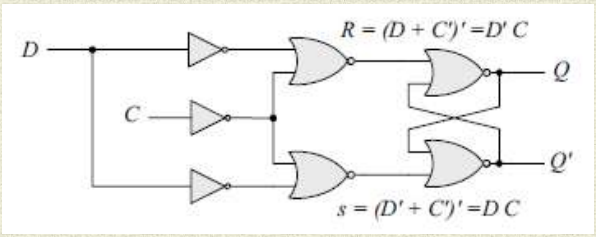
Solution of Question 1

(a) Use NOR gates for the *SR* latch part and AND gates for the other two. An inverter may be needed.



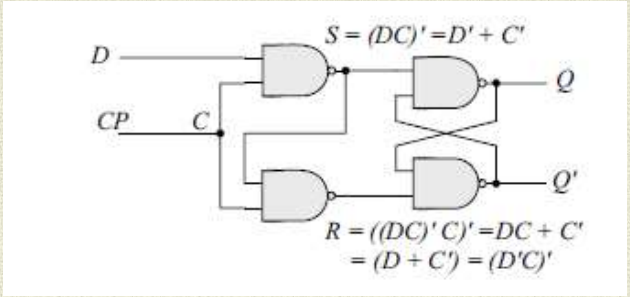
Solution of Question 1

(b) Use NOR gates for all four gates. Inverters may be needed.



Solution of Question 1

(c) Use four NAND gates only (without an inverter). This can be done by connecting the output of the upper gate



Question 2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A *PN* flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs *P* and *N* are 00, 01, 10, and 11, respectively.

(a) Tabulate the characteristic table.
(b) Derive the characteristic equation.
(c) Tabulate the excitation table.
(d) Show how the *PN* flip-flop can be converted to a *D* flip-flop.

Solution of Question 2


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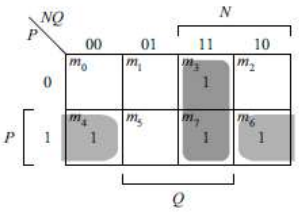
(a)

P	*N*	Q(t + 1)
0	0	0
0	1	*Q(t)*
1	0	*Q'(t)*
1	1	1

(b)

P	*N*	*Q(t)*	*Q(t + 1)*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



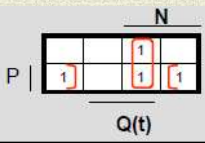
$Q(t+1) = PQ' + NQ$

(c)

Q(t)	*Q(t+1)*	*P*	*N*
0	0	0	x
0	1	1	x
1	0	x	0
1	1	x	1

Connect P and N together

Q(t+1)= PQ'+NQ



Question 3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A sequential circuit has two *JK* flip-flops *A* and *B*, two inputs *x* and *y*, and one output *z* .
The flip-flop input equations and circuit output equation are

$$J_A = Bx + B'y' \qquad K_A = B'xy'$$
$$J_B = A'x \qquad K_B = A + xy'$$
$$z = Ax'y' + Bx'y'$$

(a) Draw the logic diagram of the circuit.
(b) Tabulate the state table.
(c) Derive the state equations for *A* and *B* .

Solution of Question 3


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(a) $J_A = Bx + B'y'$ $\quad J_B = A'x$
$K_A = B'xy'$ $\quad K_B = A + xy'$ $\quad z = Axy + Bx'y'$

Solution of Question 3

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(b)

Present State AB	Inputs xy	Next State AB	Output z	FF Inputs $J_A K_A$	FF Inputs $J_B K_B$
00	00	10	0	10	00
00	01	00	0	00	00
00	10	11	0	11	11
00	11	01	0	00	10
01	00	01	1	00	00
01	01	01	0	00	00
01	10	10	0	10	11
01	11	11	0	10	10
10	00	10	0	10	01
10	01	10	0	00	01
10	10	00	0	11	01
10	11	10	1	00	01
11	00	10	1	00	01
11	01	10	0	00	01
11	10	10	0	10	01
11	11	10	1	10	01

Solution of Question 3

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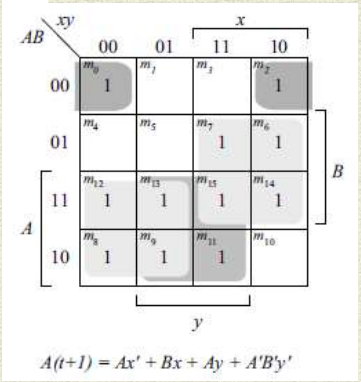
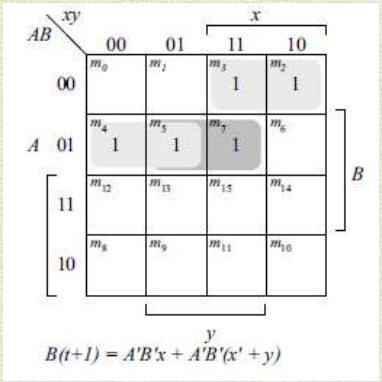
(c)



$A(t+1) = Ax' + Bx + Ay + A'B'y'$



$B(t+1) = A'B'x + A'B'(x' + y)$