CS 207 Digital Logic - Spring 2020
Lab 15

James Yu

May 27, 2020

Objective

1. Use your Verilog knowledge to finish the mini-project.

Lab Exercise Submission

1. You should name all source code as instructed. Mis-named files will not be recognized.
2. You should submit all source code files with an extension "`.v`".
3. You should submit all source code directly into the sakai system below. **Do not compress them into one folder.**

   `https://sakai.sustech.edu.cn/portal/site/ebf68254-68c5-4cfe-9d42-b26758f854ee`
4. Lab exercises should be submitted before the deadline, typically one week after the lab session. No late submission policy applies to lab exercises.

1 Mini-project

Design and verify a traffic light controller for a railway level crossing (`https://en.wikipedia.org/wiki/Level_crossing`). By default, rail light is red (`100`) and road light is green (`001`). A 1-bit sensor input C receives `1` when a train is approaching, then the road light turns yellow (`010`) from the next time step for three time steps, then turns red and rail light turns green. After the train, C receives `0`, rail light turns yellow for three time steps, then turns red and road light turns green. Output the simulation log in the following format, with changes deemed necessary:

```
TIME =   0, reset = 1, sensor = 0, road = 1, rail = 4
TIME = 100, reset = 1, sensor = 1, road = 1, rail = 4
```

```
TIME = 101, reset = 1, sensor = 1, road = 2, rail = 4
TIME = 104, reset = 1, sensor = 1, road = 4, rail = 1
TIME = 150, reset = 1, sensor = 0, road = 4, rail = 1
TIME = 151, reset = 1, sensor = 0, road = 4, rail = 2
TIME = 154, reset = 1, sensor = 0, road = 1, rail = 4
TIME = 200, reset = 1, sensor = 1, road = 1, rail = 4
TIME = 201, reset = 1, sensor = 1, road = 2, rail = 4
TIME = 204, reset = 1, sensor = 1, road = 4, rail = 1
TIME = 250, reset = 1, sensor = 0, road = 4, rail = 1
TIME = 251, reset = 1, sensor = 0, road = 4, rail = 2
TIME = 253, reset = 1, sensor = 1, road = 4, rail = 2
TIME = 254, reset = 1, sensor = 1, road = 4, rail = 1
TIME = 300, reset = 1, sensor = 0, road = 4, rail = 1
TIME = 301, reset = 1, sensor = 0, road = 4, rail = 2
TIME = 304, reset = 1, sensor = 0, road = 1, rail = 4
```

The module should follow the design below:

divide.v

```
1 module traffic(road, rail, C, reset);
2 // Module Code
3 endmodule
```

and save in file `traffic.v`.

Assignment

Save the source code in **`traffic.v`**. Upload this file to Sakai under **Assignments → Lab Exercise 15**.