电子与电气工程系
Department of Electrical and Electronic Engineering

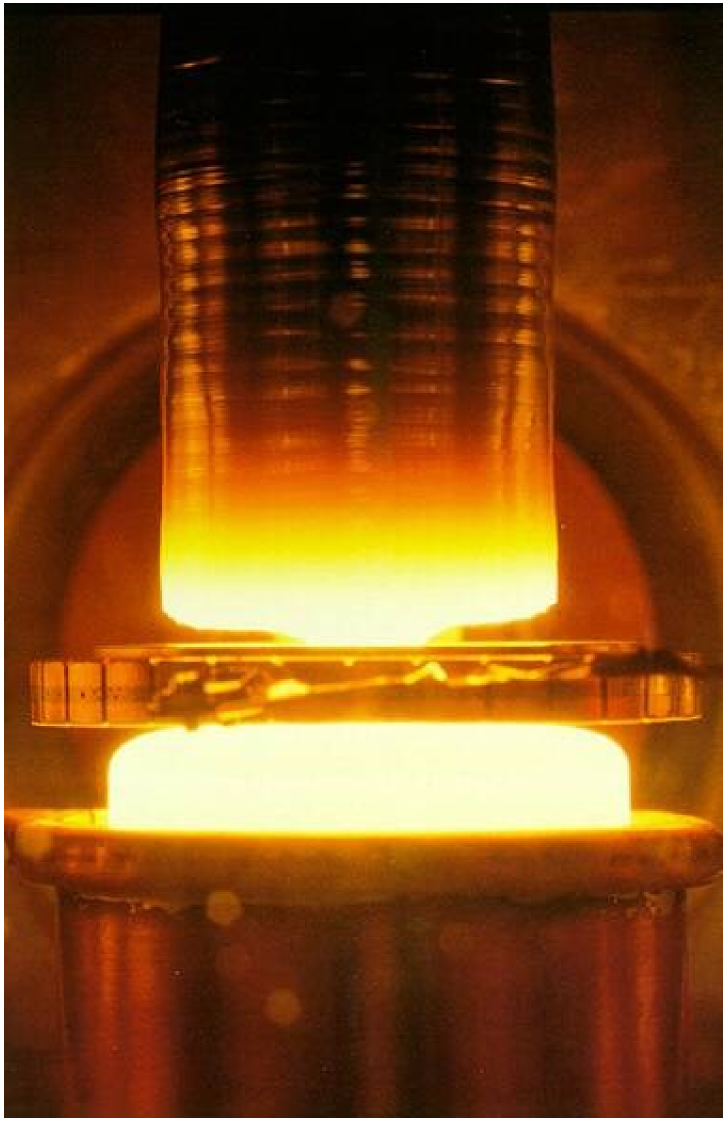
Wafer

Lecturer: Mengyuan Hua

Summary

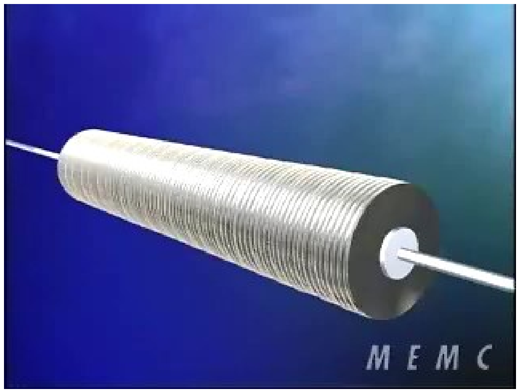
- Wafer shaping
- Crystal defects
- Material properties

Silicon Ingot

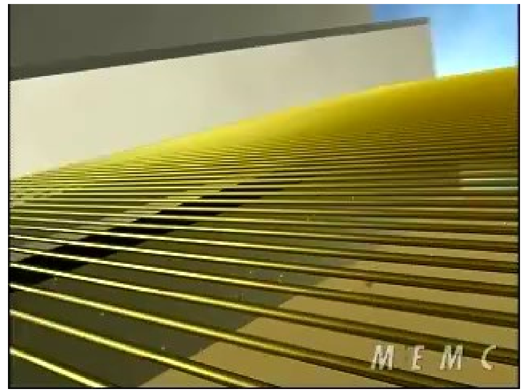


From Ingots to Wafers

Many processing steps are needed to convert ingots into wafers for VLSI fabrication

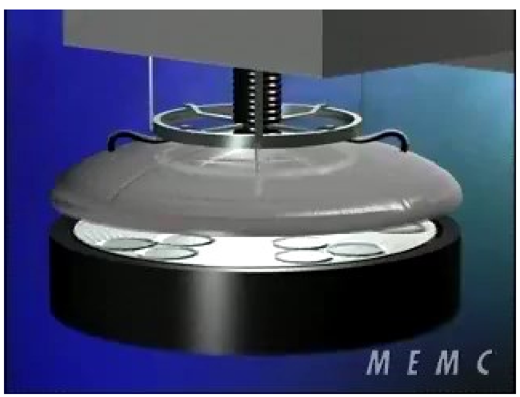


- Shaping ingot

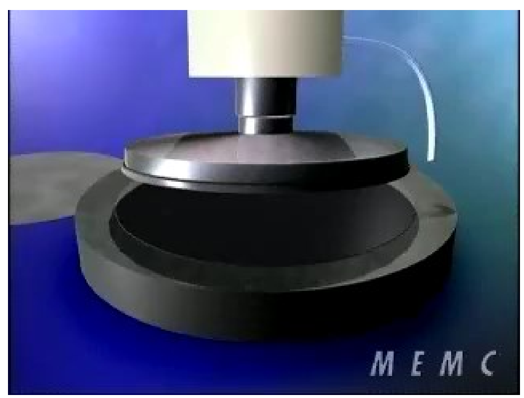


- Saw into wafers

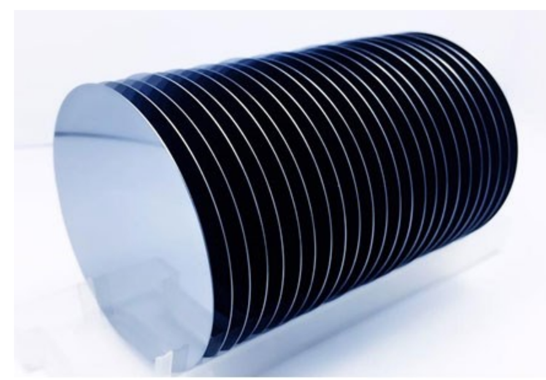
- Edge smoothing



- Flatness



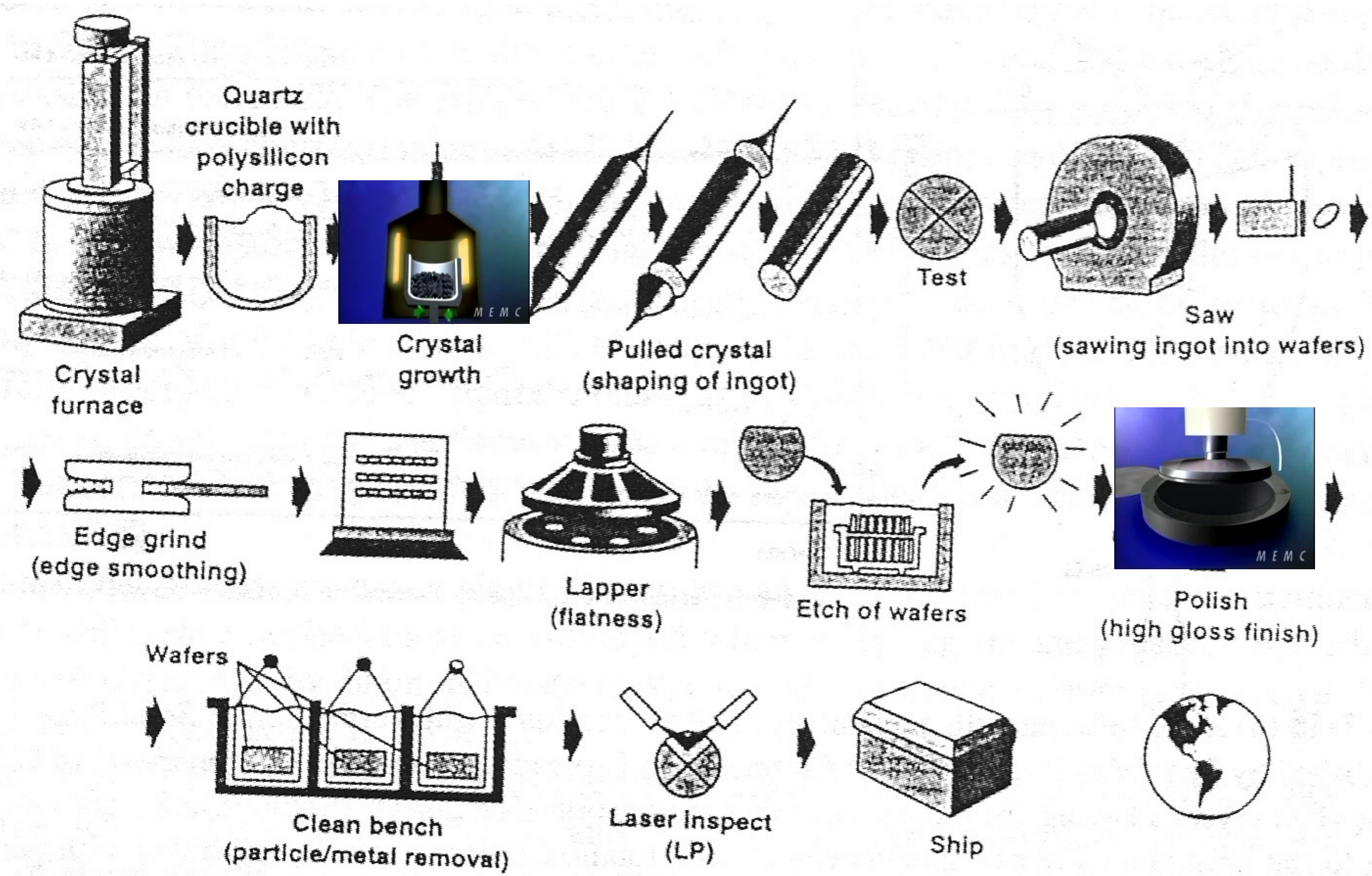
- Polish



- Clean and Inspect

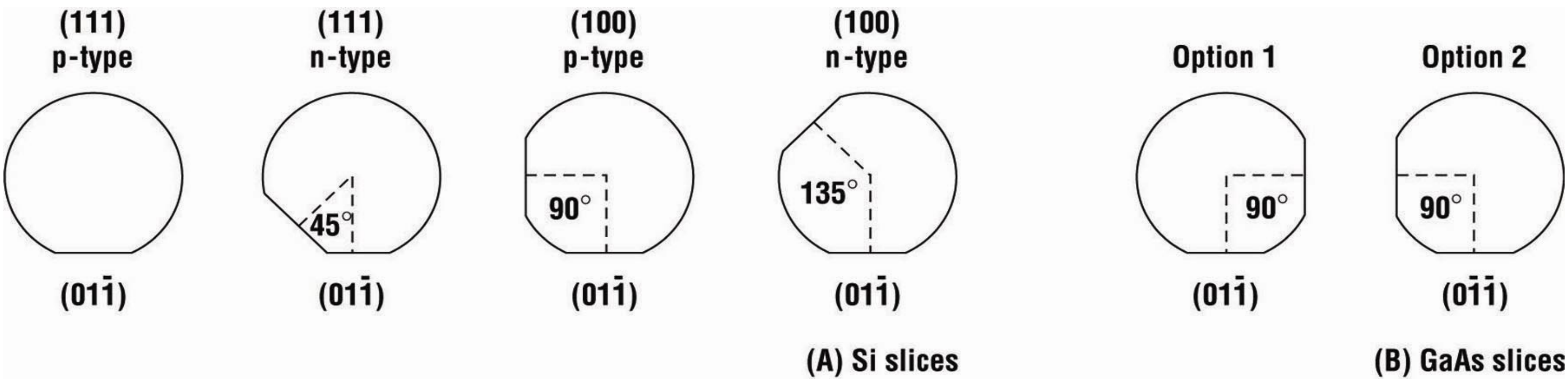
Wafer Shaping

Many processing steps are needed to convert ingots into wafers for integrated circuit fabrication

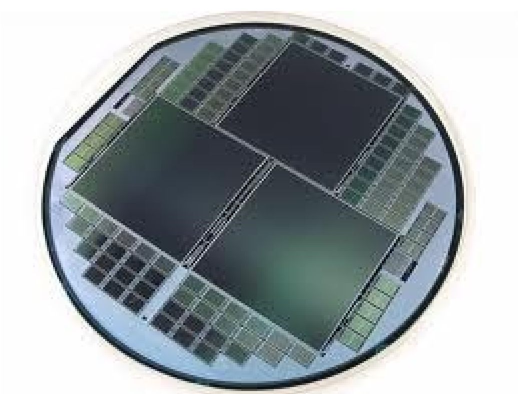


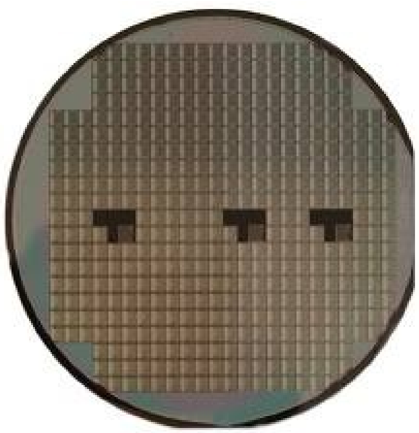
Identifying Flats

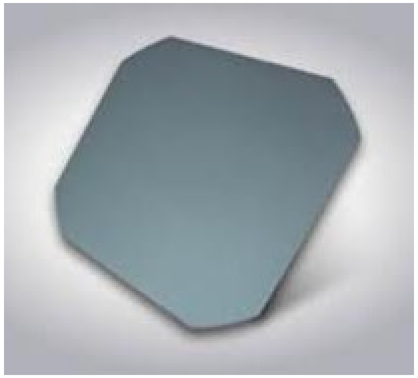
Wafers are marked for doping type and crystal orientation



Standard flat orientations for different semiconductor wafers

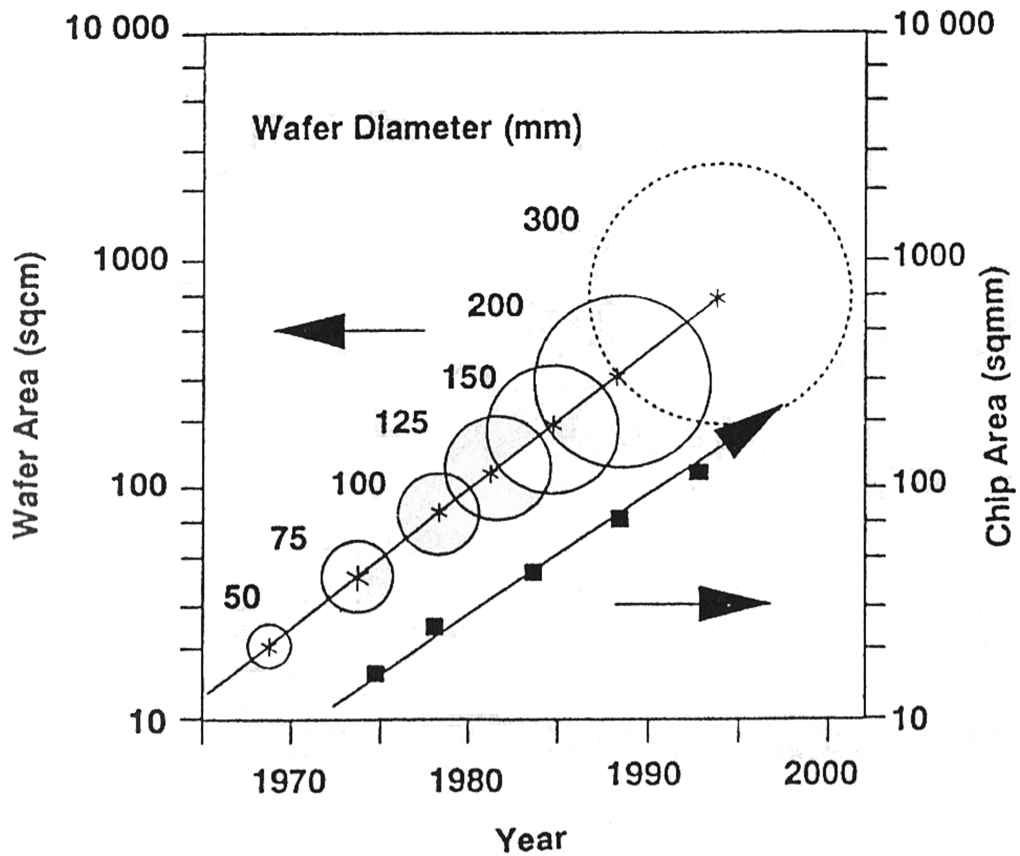






Solar cell

Trend in Wafer Sizes



Diameter	Area (Sq. Inches)
2 Inch	3.1
3 Inch	7.1
100mm	12.6
125mm	19.6
150mm	28.3
200mm	50.2
300mm	109.5

Diameter Increase	Percentage Area Increase
2” → 3”	125%
3” → 100 mm	78%
100 mm → 125 mm	56%
125 mm → 150 mm	44%
150 mm → 200 mm	78%
200 mm → 300 mm	125%

40% cost reduction for every new generation of wafer size

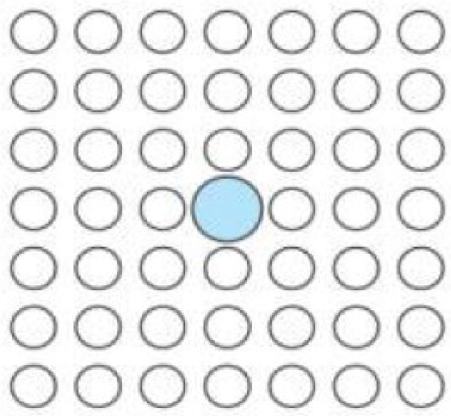
State of the art Silicon wafers

Diameter	[mm]	150 / 200 / 300	± 0.20
Thickness	[µm]	625 / 700 / 775	± 10
Bow	[µm]	10	
Global flatness	[µm]	3	
Microroughness	[nm RMS]	0.2	
Cleanliness	[partices/cm^2]	< 0.03	
Oxygen concentration	[ppma]	15-19 or (< 22)	± 3%
Carbon concentration	[ppma]	< 3	
Bulk metal contamination	[ppba]	< 0.001	
Grown in dislocations	[1/cm^2]	< 0.1	
Cost	[$/cm^2]	0.2	

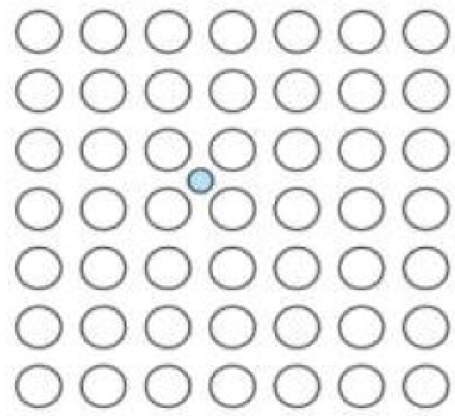
Summary

- Wafer shaping
- Crystal defects
- Material properties

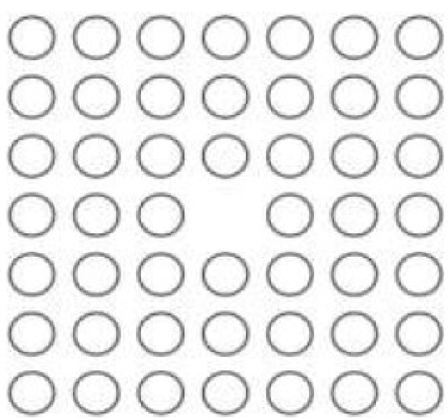
Crystal Defects: Point Defects



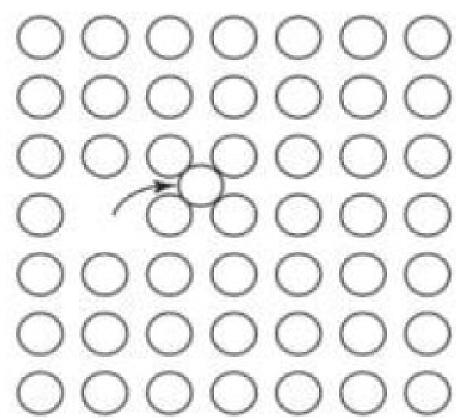
Substitutional impurity



Interstitial impurity

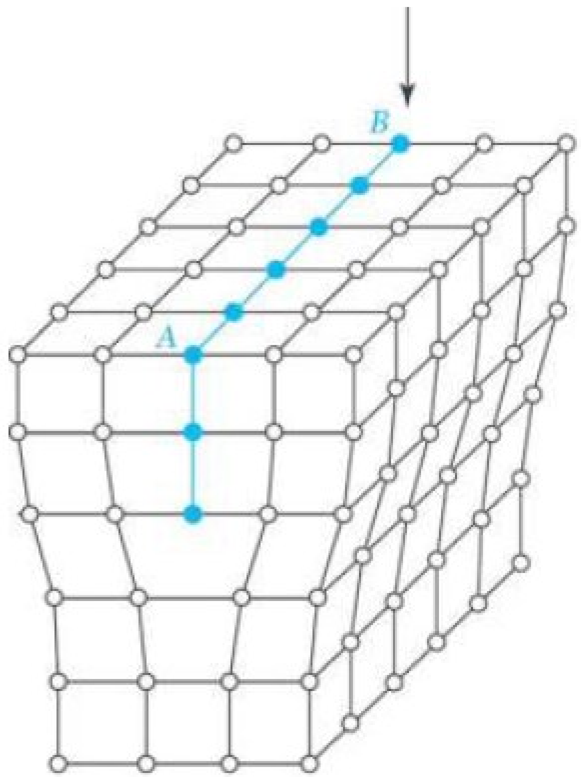


Lattice vacancy

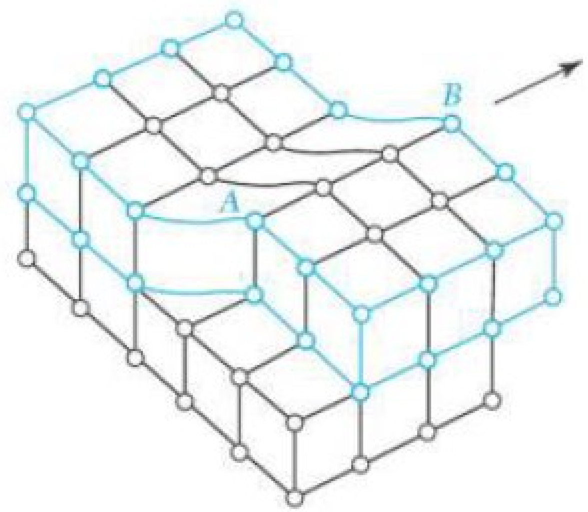


Frenkel-type defect

Crystal Defects: Line Defects



Edge dislocation

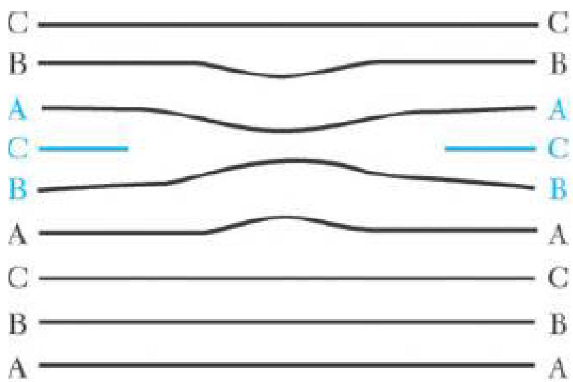


Screw dislocation

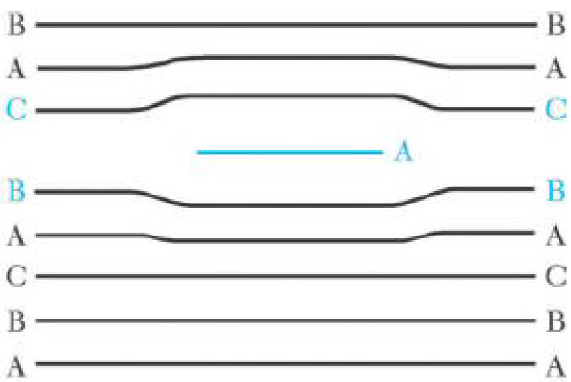
Crystal Defects

Area defect – 2-D

- Extend in two directions through crystal
- Example: stacking fault at polycrystalline grain boundaries



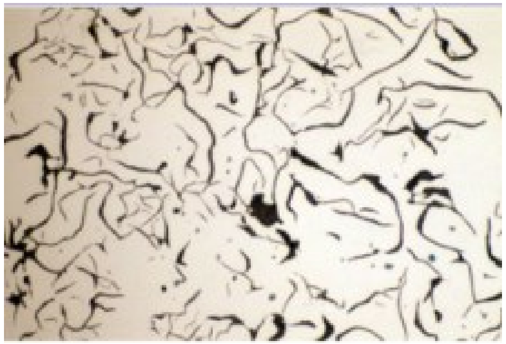
***(a)* Intrinsic stacking fault.**



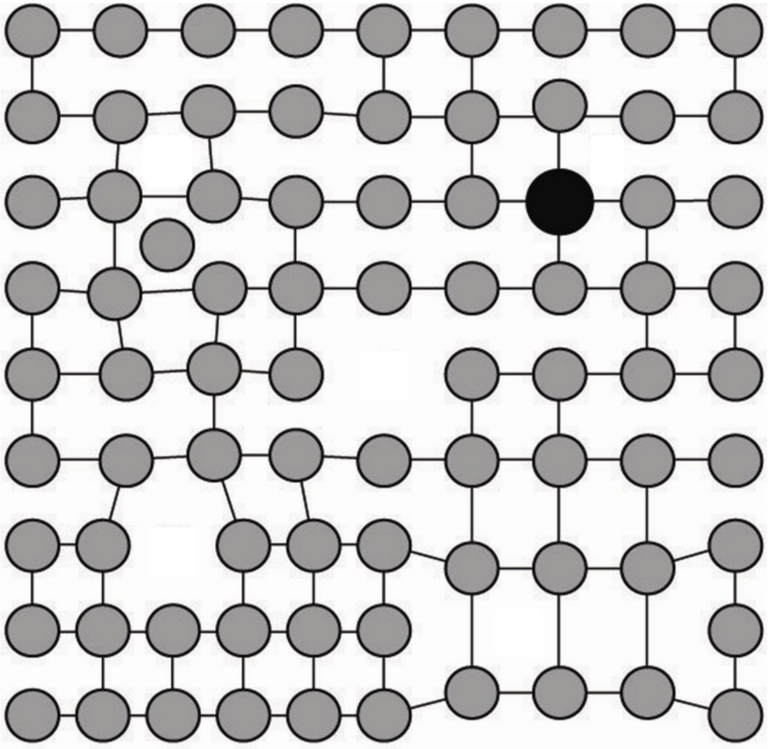
(*b*) Extrinsic stacking fault

Volume defect -3-D

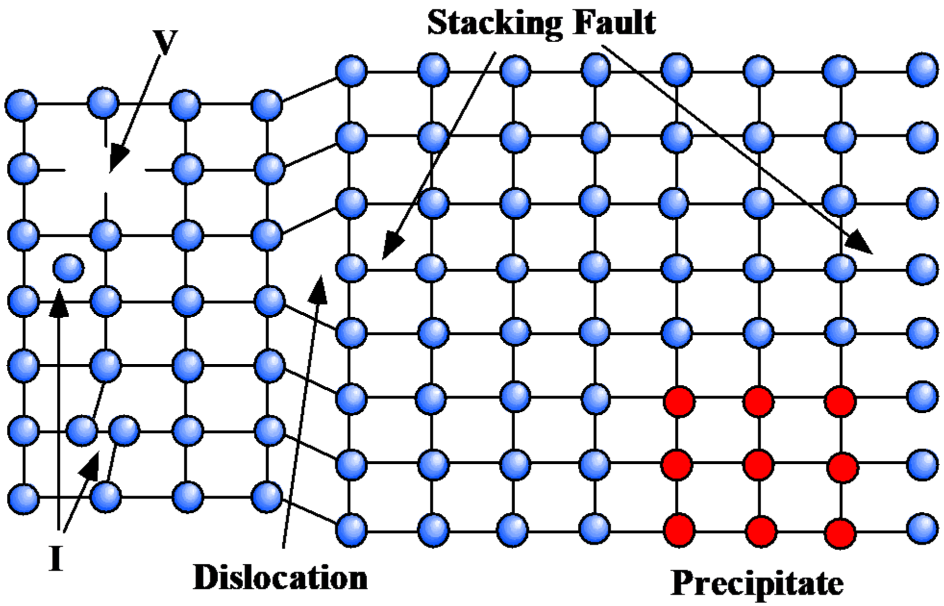
- Irregular structure in all three dimensions
- Example: impurity precipitate



How many defects in Crystal Structures?



Simple 0- and 1-D semiconductor defects include: (A) vacancies, (B) self-interstitials, (C) substitutional impurities, (D) edge dislocations, and (E) dislocation loops.



Illustrations for vacancies (V), interstitials (I), dislocation, stacking fault and precipitate

Defect Concentrations

- At any temperature other than 0 K, there exists thermal energy which can create vacancy and self-interstitial defects
- Vacancy and self-interstitial defects always exist, thus we call them **intrinsic defects**

Vacancy concentration is described by an Arrhenius equation:

$$N_v^o = N_o e^{-E_a/kT}$$

N_o: the number density of atoms in crystal lattice (e.g., for Si, it is 5.02×10^{22} cm^{-3})

E_a: the activation energy associated with the formation of a vacancy (2.6 eV for Si)

K: the Boltzmann's constant (8.617×10^{-5} eV/K)

Example

Find the vacancy concentration of silicon crystal at room temperature and at 1000^{o}C.

Solution: At room temperature, $kT = 8.617\times10^{-5}\times 298 = 0.0257$ eV = 25.7 meV

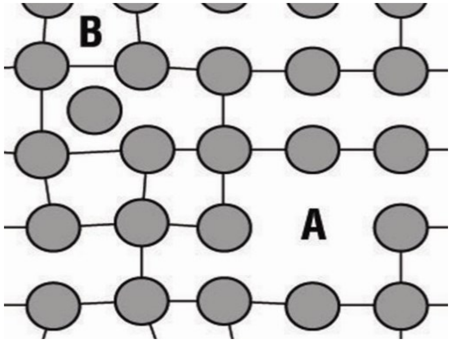
So, $N_v^o = 5.02\times10^{22}\times e^{-2.6/0.0257} = 5.81\times10^{-22}$ cm^{-3} = 0

At 1000^{o}C, $kT = 8.617\times10^{-5}\times 1273 = 0.1097$ eV, so $N_v^o = 5.02\times10^{22}\times e^{-2.6/0.1097}$ $= 2.55\times10^{12}$ cm^{-3}

How pure Si we need?

Defect Concentrations

The defect sites can be charged when silicon is doped



- Doping introduces extra electrons and holes into the silicon crystal
- At vacancy defect, silicon bonds are not saturated. Electrons can be captured to make the vacancy negatively charged or removed to make the vacancy defect positively charged

The concentration of charged vacancies at equilibrium is described by:

$$N_{v-}^{o} = N_{v}^{o} \frac{n}{n_i} e^{(E_i - E_v^{-})/kT} \qquad N_{v+}^{o} = N_{v}^{o} \frac{p}{n_i} e^{(E_v^{+} - E_i)/kT}$$

$N_v{}^o$: the total number density of vacancy defects

$E_v{}^-$, $E_v{}^+$: the energy levels associated with the negatively and positively charged vacancies

n_i: the intrinsic carrier concentration at temperature T

Outline

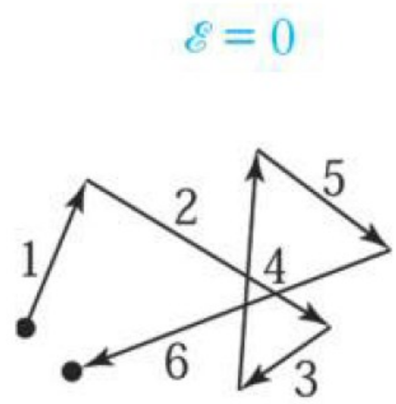
- Wafer shaping
- Crystal defects
- Material properties

Material Properties

Property[a]	Characteristics: Czochralski	Characteristics: Float zone	Requirements for ULSI
Resistivity (phosphorus) *n*-type (ohm-cm)	1–50	1–300 and up	5-50 and up
Resistivity (antimony) *n*-type (ohm-cm)	0.005–10	—	0.001–0.02
Resistivity (boron) *p*-type (ohm-cm)	0.005–50	1–300	5–50 and up
Resistivity gradient (four-point probe) (%)	5–10	20	< 1
Minority carrier lifetime (μs)	30–300	50–500	300–1000
Oxygen (ppma)	5–25	Not detected	Uniform and controlled
Carbon (ppma)	1–5	0.1–1	< 0.1
Dislocation (before processing) (per cm^2)	≤ 500	≤ 500	≤ 1
Diameter (mm)	Up to 200	Up to 100	Up to 300
Slice bow (μm)	≤ 25	≤ 25	< 5
Slice taper (μm)	≤ 15	≤ 15	< 5
Surface flatness (μm)	≤ 5	≤ 5	< 1
Heavy-metal impurities (ppba)	≤ 1	≤ 0.01	< 0.001

[a] ppma, parts per million atoms; ppba, parts per billion atoms.

Resistivity: mobility



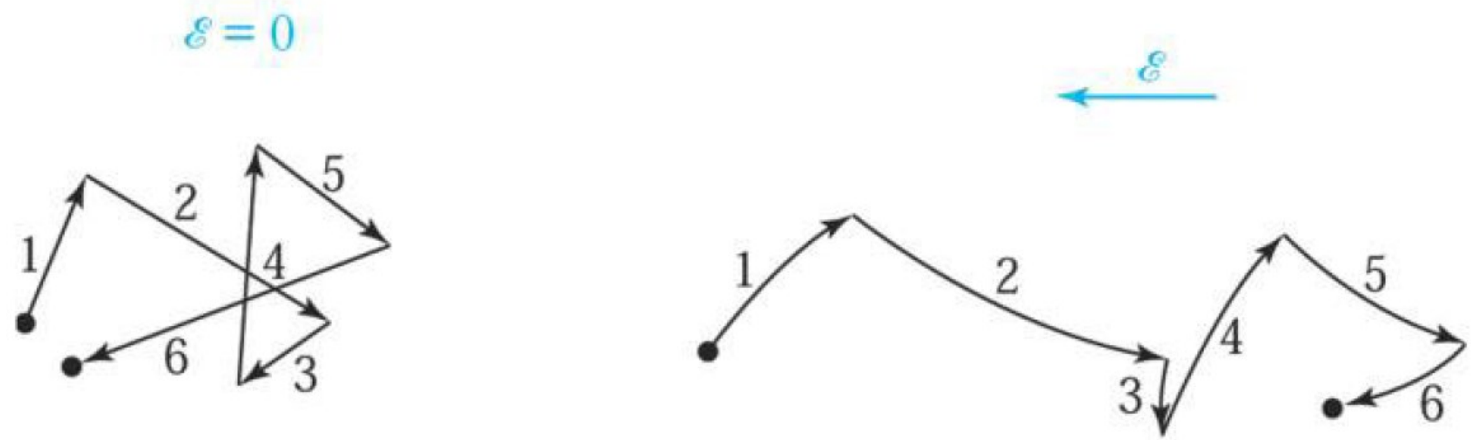
Schematic path of an electron in a semiconductor. (*a*) Random thermal motion. (*b*) Combined motion due to random thermal motion and an applied electric field.

$$\frac{1}{2} m_n \upsilon_{th}^2 = \frac{3}{2} kT$$

thermal velocity = 10^7 cm/s

400 times of the fastest airplane!

Resistivity : mobility



Schematic path of an electron in a semiconductor. (*a*) Random thermal motion. (*b*) Combined motion due to random thermal motion and an applied electric field.

E-field

Mass of carrier

$$q\mathscr{E}\tau_c = m_n \upsilon_n$$

Mean free time

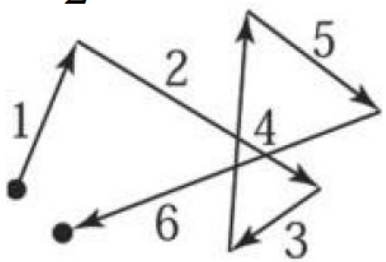
Drift velocity

$$\upsilon_n = \boxed{\left(\frac{q\tau_c}{m_n}\right)}\mathscr{E}$$

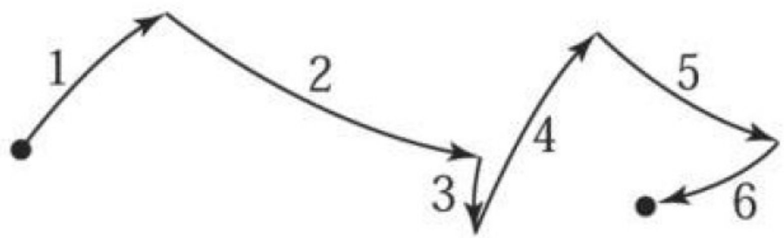
Mobility μ

Resistivity : mobility

$$\frac{1}{2}m_n\upsilon_{th}^2 = \frac{3}{2}kT \qquad \mathscr{E}=0$$



$$q\mathscr{E}\tau_c = m_n\upsilon_n \qquad \xleftarrow{\mathscr{E}}$$



Calculate the mean free time of an electron having a mobility of 1000 cm^2/V-s at 300 K and E= 1MV/cm; also calculate the mean free path. Assume m_n = 0.26 m_0 in these calculations.

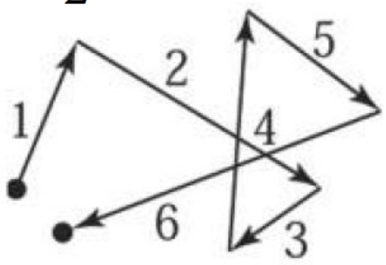
$$q\mathscr{E}\tau_c = m_n\upsilon_n$$

$$\mu_n \equiv \frac{q\tau_c}{m_n}$$

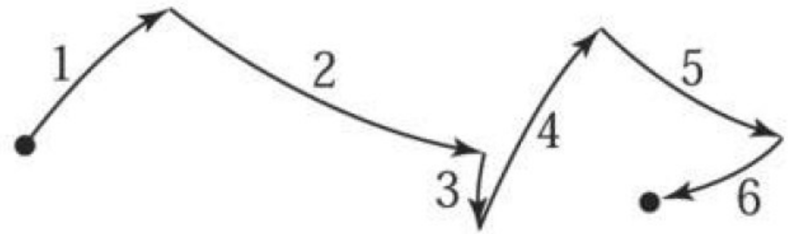
Thermal velocity? Or drift velocity? Or both?

Resistivity : mobility

$$\frac{1}{2}m_n\upsilon_{th}^2 = \frac{3}{2}kT \qquad \mathscr{E}=0$$



$$q\mathscr{E}\tau_c = m_n\upsilon_n \qquad \xleftarrow{\mathscr{E}}$$



Calculate the mean free time of an electron having a mobility of 1000 cm^2/V-s at 300 K and E= 1MV/cm; also calculate the mean free path. Assume m_n = 0.26 m_0 in these calculations.

Thermal velocity? Or drift velocity? Or both?

The thermal velocity is 2.28×10^7 cm/s for $m_n = 0.26\,m_0$ from Eq. (1).

The mean free path is given by

$$l = \upsilon_{th}\tau_c = (3kT/m_n)^{1/2}\tau_c = (2.28\times10^7\ \text{cm/s})(1.48\times10^{-13}\ \text{s}) = 3.37\times10^{-6}\ \text{cm} = 33.7\ \text{nm}.$$

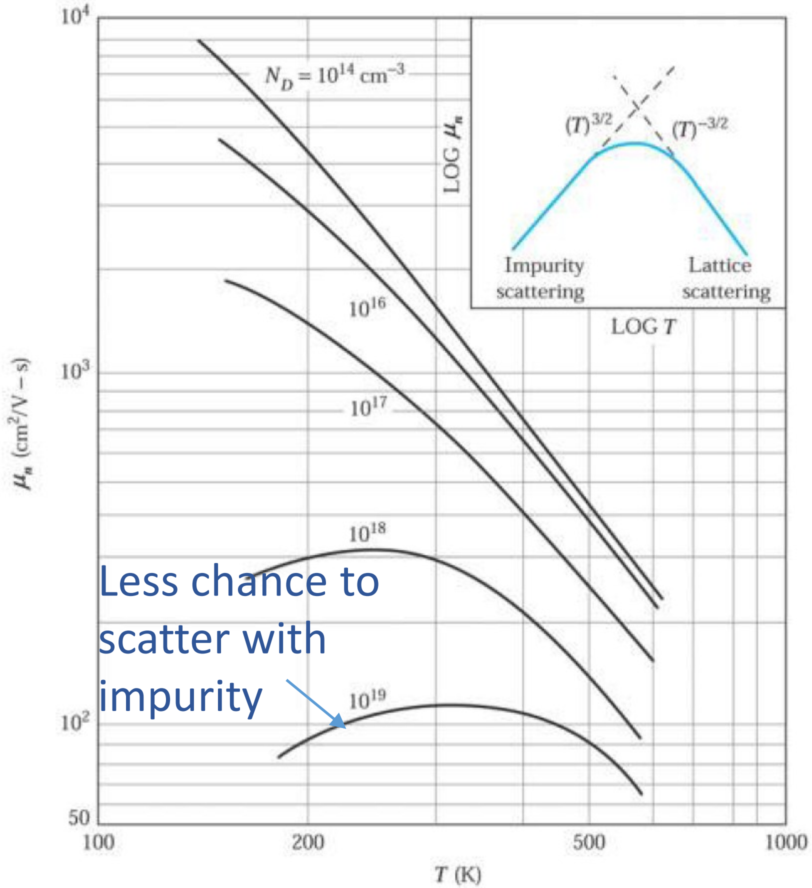
Resistivity : mobility

$$\mu_n \equiv \frac{q\tau_c}{m_n}$$

$$\frac{1}{\tau_c} = \frac{1}{\tau_{c,\ lattice}} + \frac{1}{\tau_{c,\ impurity}}$$

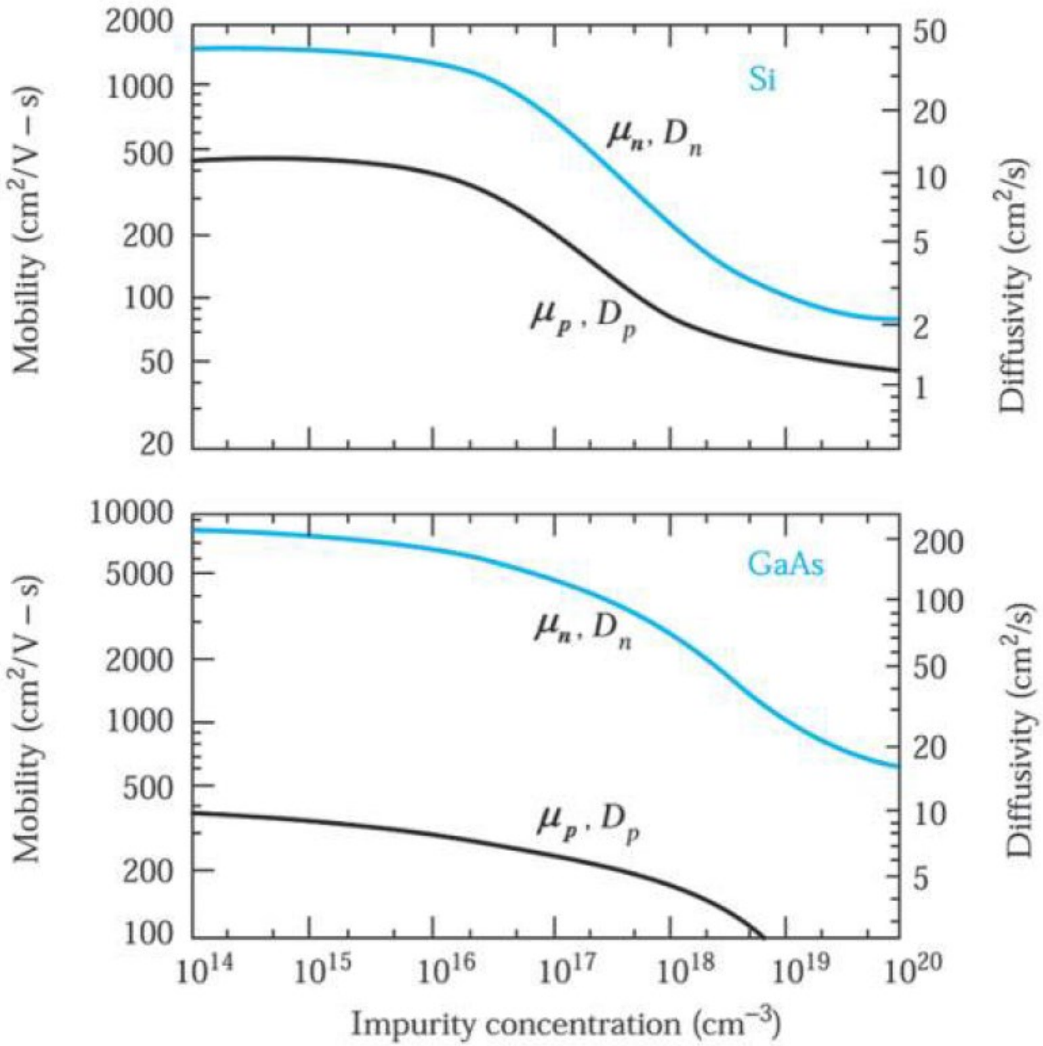
$$\frac{1}{\mu} = \frac{1}{\mu_L} + \frac{1}{\mu_I}$$

$$\upsilon_n = \mu_n \mathscr{E}$$

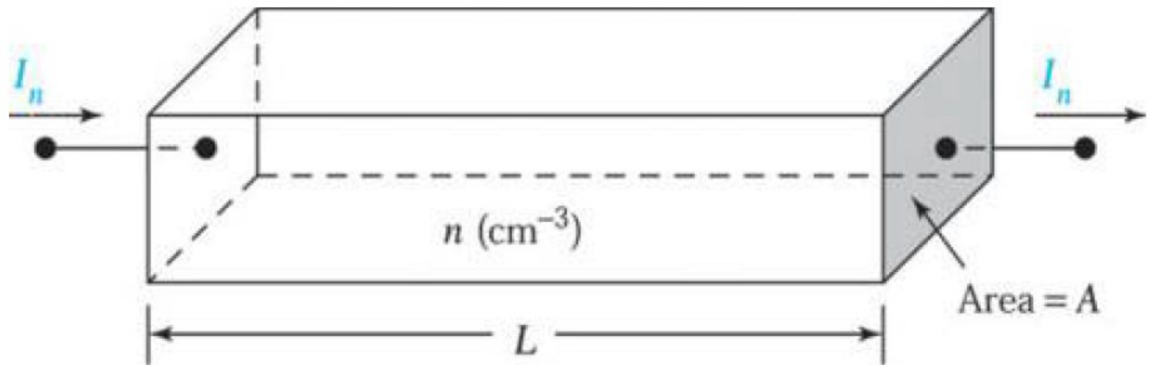


Less chance to scatter with impurity

Resistivity: Mobility



Resistivity

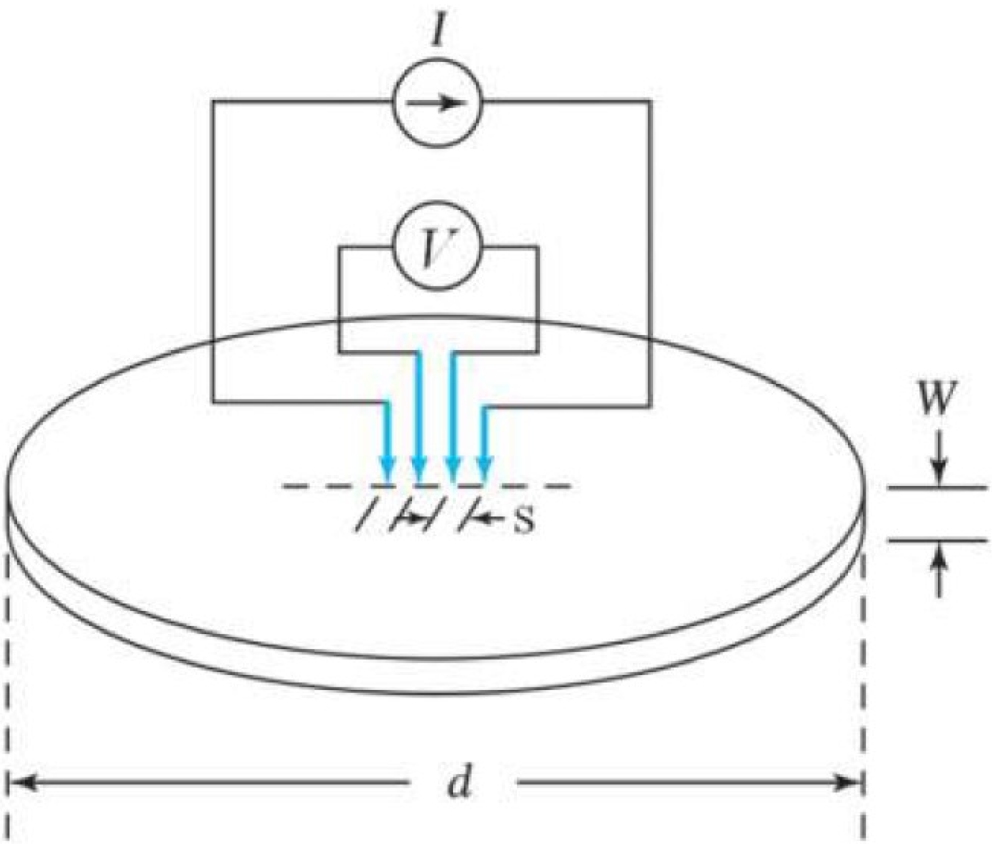


$$J_n = \frac{I_n}{A} = \sum_{i=1}^{n}(q\upsilon_i) = qn\upsilon_n = \boxed{qn\mu_n}\mathcal{E}$$

Resistivity $\rho = \dfrac{1}{qn\mu_n}$ **Conductivity**

Resistance can be measured with four-point probe method

Four-point probe method



$$\rho = \frac{V}{I} \cdot W \cdot CF \quad \Omega\text{-cm}$$

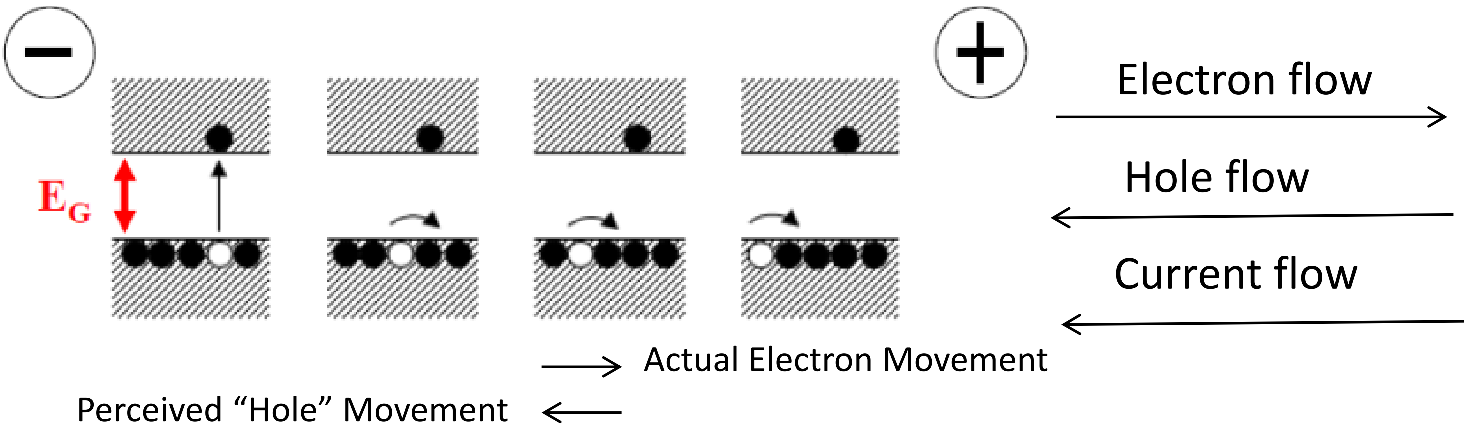
Material Properties

Property[a]	Characteristics: Czochralski	Characteristics: Float zone	Requirements for ULSI
Resistivity (phosphorus) *n*-type (ohm-cm)	1–50	1–300 and up	5-50 and up
Resistivity (antimony) *n*-type (ohm-cm)	0.005–10	—	0.001–0.02
Resistivity (boron) *p*-type (ohm-cm)	0.005–50	1–300	5–50 and up
Resistivity gradient (four-point probe) (%)	5–10	20	< 1
Minority carrier lifetime (μs)	30–300	50–500	300–1000
Oxygen (ppma)	5–25	Not detected	Uniform and controlled
Carbon (ppma)	1–5	0.1–1	< 0.1
Dislocation (before processing) (per cm^2)	≤ 500	≤ 500	≤ 1
Diameter (mm)	Up to 200	Up to 100	Up to 300
Slice bow (μm)	≤ 25	≤ 25	< 5
Slice taper (μm)	≤ 15	≤ 15	< 5
Surface flatness (μm)	≤ 5	≤ 5	< 1
Heavy-metal impurities (ppba)	≤ 1	≤ 0.01	< 0.001

[a] ppma, parts per million atoms; ppba, parts per billion atoms.

Electrons and holes in Semiconductors

- In pure (also called intrinsic) Si, free electrons and holes appear in PAIRS



- The "hole" is an abstraction; it has no substance and does not actually move itself, but movement of electrons in the opposite direction is perceived as the hole moving.
- In an ideal(intrinsic) semiconductor crystal, $n_i=p_i$
- Hole mobility is usually lower than electron mobility.

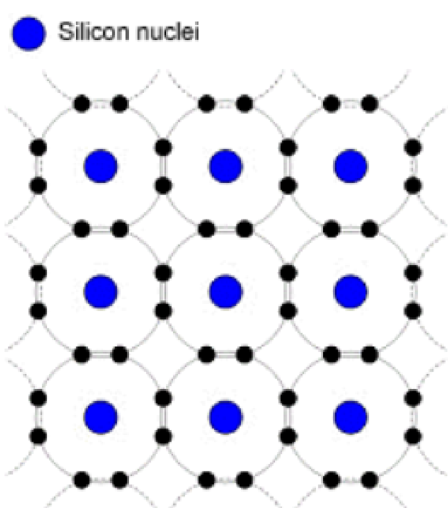
Due to very low intrinsic electron and hole concentration, intrinsic Si exhibits very low conductivity at room temperature.

Extrinsic semiconductors

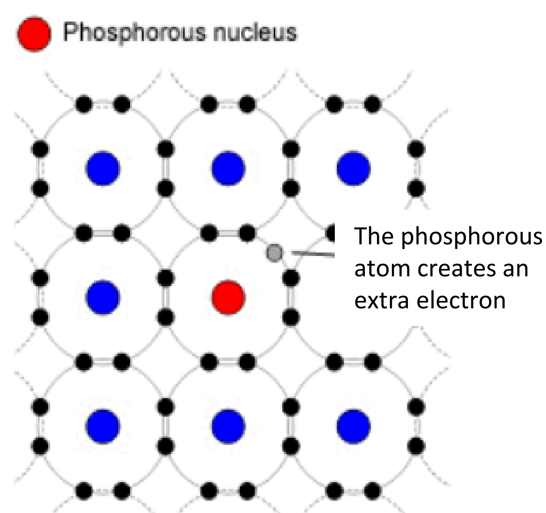
The conduction in a semiconductor can be changed via doping. Doping is the introduction of foreign atoms such as B, As, P in Si.

- **Doping with donors:** gives an n-type material. "n" means negative, that is free electrons n_n > free holes p_n.
- **Doping with acceptors:** gives a p-type material. "p" means positive, that is free holes p_p > free electrons n_p.

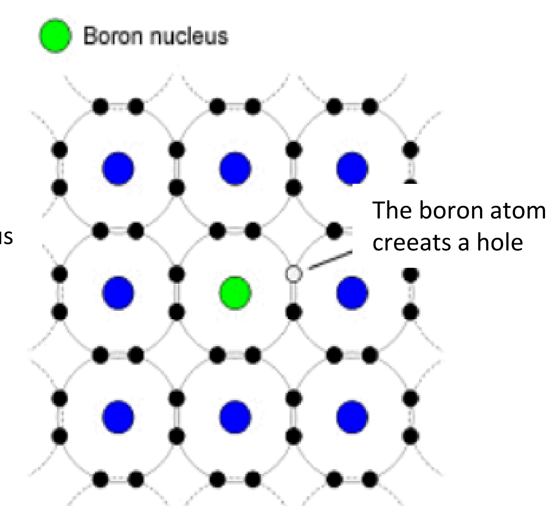
Pure silicon



N-type silicon



P-type silicon



Recombination Lifetime

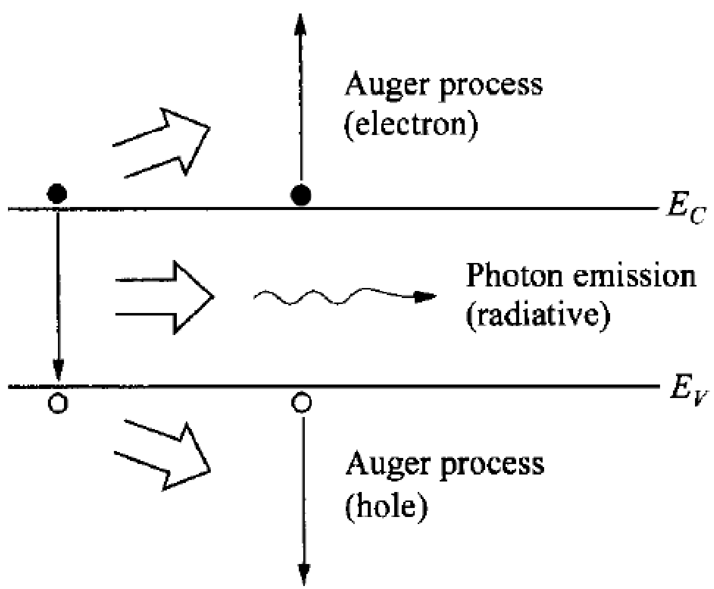
During recombination, the energy of the carriers is dissipated by several mechanisms:

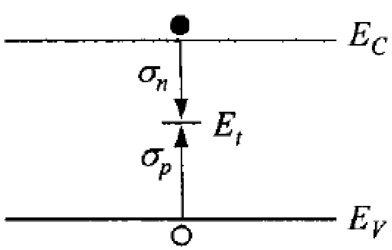
Band-to-band

- Emission of a photon (referred to as radiative recombination);
- Transmission of the energy to a third particle, which can be either an electron or a hole (referred to as Auger recombination).

Deep trap center

- Distribution of the energy into the lattice in the form of phonons (referred to as Shockley-Read-Hall (SRH) or multi-phonon recombination);





Non-radiative recombination

Shockley–Read–Hall Recombination

- In a semiconductor such as Si with an indirect band gap structure, the probability for direct transitions from the conduction band to the valence band is small. Consequently, the radiative recombination lifetime for silicon is on the order of 1 s.
- In comparison, the density of recombination centers is sufficiently high, even in high purity silicon used to fabricate power devices, so as to reduce the lifetime associated with recombination via the deep levels to less than 100 μs.

- SHR lifetime is given by

$$\tau_{SRH} = \frac{\tau_p(n_o + n_1 + \Delta n) + \tau_n(p_o + p_1 + \Delta p)}{p_o + n_o + \Delta n}$$

$$n_1 = n_i \exp\left(\frac{E_T - E_i}{kT}\right); p_1 = n_i \exp\left(-\frac{E_T - E_i}{kT}\right)$$

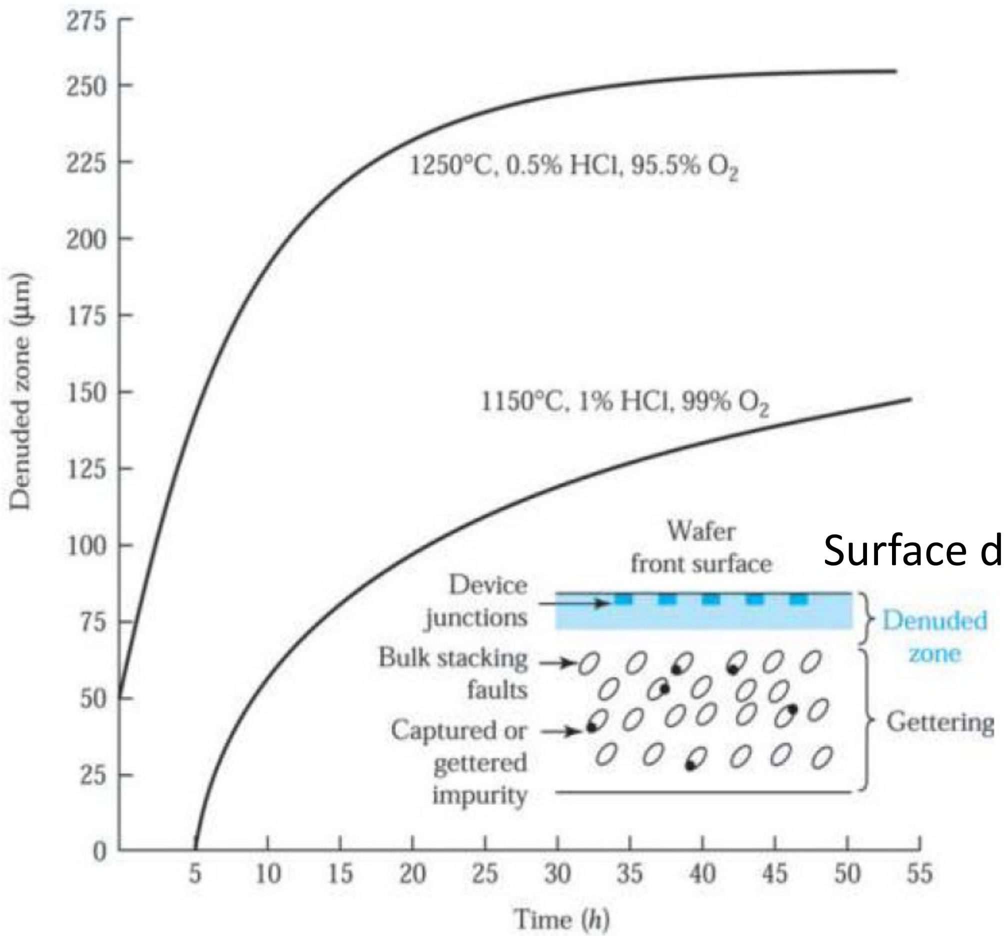
$$\tau_p = \frac{1}{\sigma_p v_{th} N_T}; \tau_n = \frac{1}{\sigma_n v_{th} N_T}$$

Material Properties

Property[a]	Characteristics: Czochralski	Float zone	Requirements for ULSI
Resistivity (phosphorus) *n*-type (ohm-cm)	1–50	1–300 and up	5-50 and up
Resistivity (antimony) *n*-type (ohm-cm)	0.005–10	—	0.001–0.02
Resistivity (boron) *p*-type (ohm-cm)	0.005–50	1–300	5–50 and up
Resistivity gradient (four-point probe) (%)	5–10	20	< 1
Minority carrier lifetime (μs)	30–300	50–500	300–1000
Oxygen (ppma)	5–25	Not detected	Uniform and controlled
Carbon (ppma)	1–5	0.1–1	< 0.1
Dislocation (before processing) (per cm^2)	≤ 500	≤ 500	≤ 1
Diameter (mm)	Up to 200	Up to 100	Up to 300
Slice bow (μm)	≤ 25	≤ 25	< 5
Slice taper (μm)	≤ 15	≤ 15	< 5
Surface flatness (μm)	≤ 5	≤ 5	< 1
Heavy-metal impurities (ppba)	≤ 1	≤ 0.01	< 0.001

[a] ppma, parts per million atoms; ppba, parts per billion atoms.

Gettering Effects



Surface diffusion

吸杂

Denuded zone width for two sets of processing conditions. Inset shows a schematic of the denuded zone and gettering sites in a wafer cross section.