电子与电气工程系
Department of Electrical and Electronic Engineering

Chemical Vapor Deposition

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IV. Non-traditional methods

New methods

- **Atomic Layer Deposition (ALD)**
- **Magnetron sputtering**
- **PLD**
- **MBE**
- **Biotemplating thin film deposition**
- **Supercritical fluid deposition technology**
- **Electrochemical deposition and self-limiting growth**
- **Liquid deposition and interface engineering**
- **Gas-liquid interface deposition technology**
- **Laser induced thin film deposition**
- **3D printing**

Application area:

- **Two-dimensional materials**
- **Topological insulators**
- **Nanoelectronics**
- **Quantum computing**

V. Beyond CMOS

- Self-Assembly Techniques for Nanofabrication
- Fabrication of 2D material electronic devices
- Advanced packaging techniques

- Roadmap of photonic Integrated circuits
- Roadmap of memory devices
- Roadmap of carbon-based Electronics and ICs
- Roadmap of CMOS Logic ICs
- Roadmap of quantum devices

- ICs in electric vehicle
- ICs in 5G/6G communication

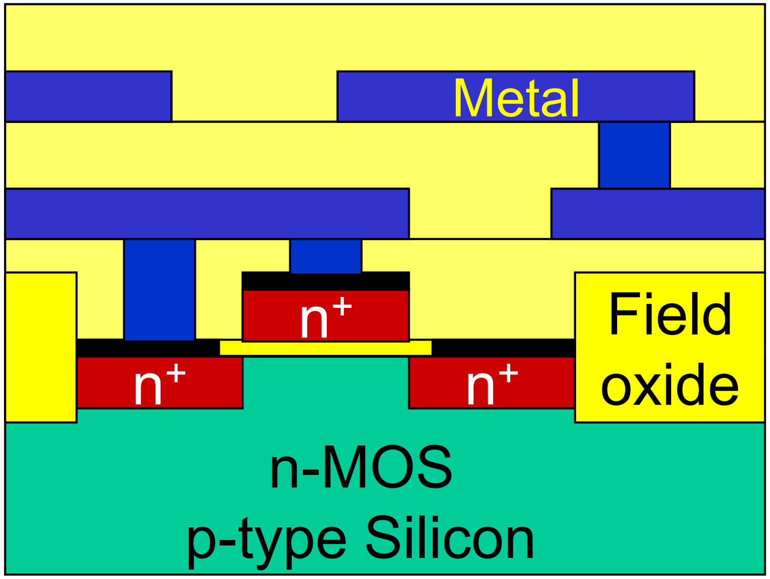
- SOI epi-wafer
- 3D integration

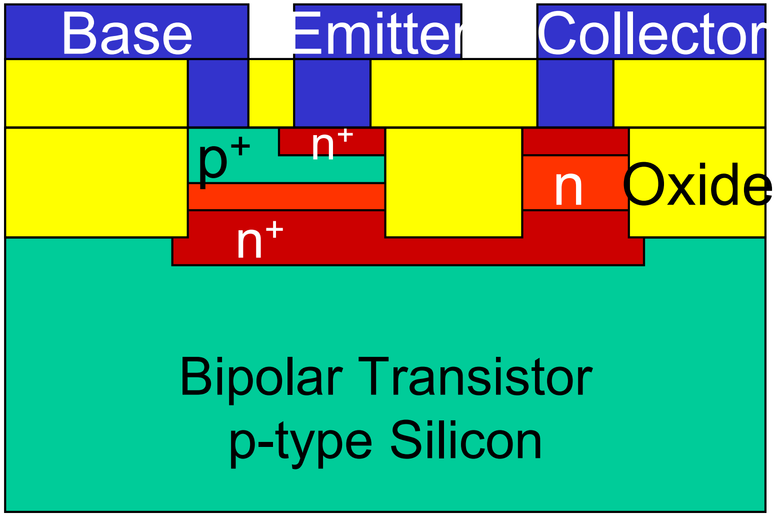
Outline

- Applications
- Materials
  - Semiconductors
  - Insulators
  - Conductors
- Methods
  - CVD – Chemical Vapour Deposition
    - APCVD, LPCVD, PECVD, HDPCVD, VPE
  - PVD – Physical Vapour Deposition
    - Evaporation, Sputtering
  - Spin-on
  - Electrochemical Deposition

Applications

- Epitaxial layers
  - Buried doped layers
  - Heterostructures
- Poly-silicon Gates
- Interlayer Dielectrics
- Interconnects – Metals
- Contacts
- Masking materials
- Structural materials
- Sacrificial layers





Thin Film Deposition Methods

Chemical Vapour Deposition - CVD

- Vapour phase epitaxy - VPE
- Atmospheric pressure – APCVD
- Low pressure CVD – LPCVD
- Plasma enhanced CVD – PECVD
- High density plasma CVD - HDPCVD

- Semiconductors
- Dielectrics
- Metals

Liquid Phase Epitaxy – LPE

- Semiconductors III-V

Physical Vapour deposition - PVD

- Vacuum Evaporation
- Molecular Beam Epitaxy – MBE
- Sputtering – Reactive sputtering
- Semiconductors III-V
- Metals

Electrochemical deposition

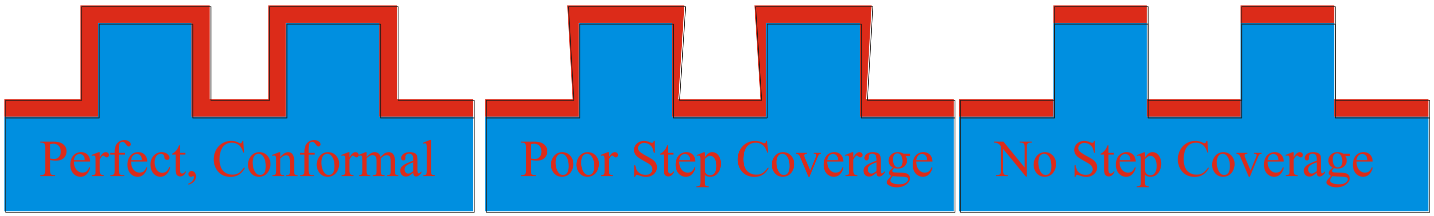
- Electroplating, Electroless plating
- Metals

Spin-on deposition

- Dielectrics (Doped glasses)

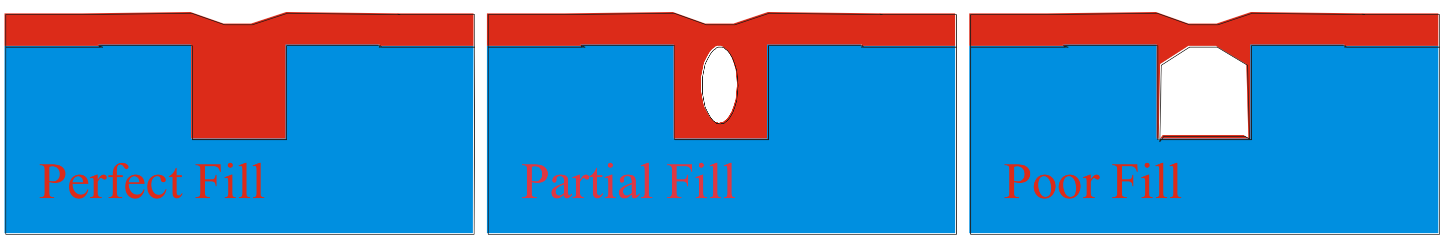
Important Issues

Step Coverage



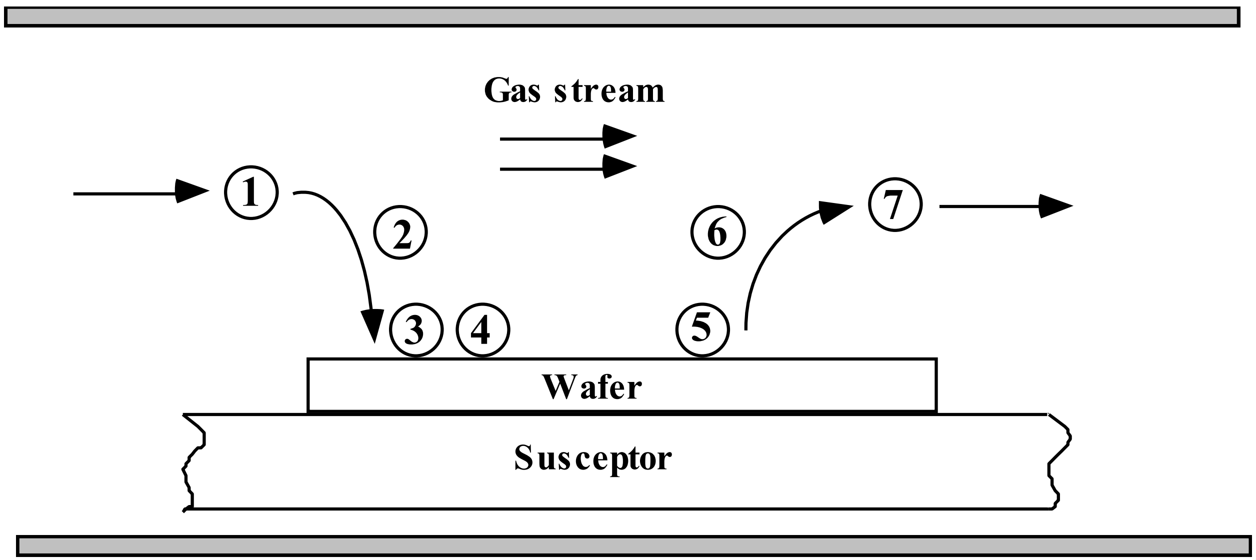
(LPCVD PECVD PVD-evaporation)

Trench Filling



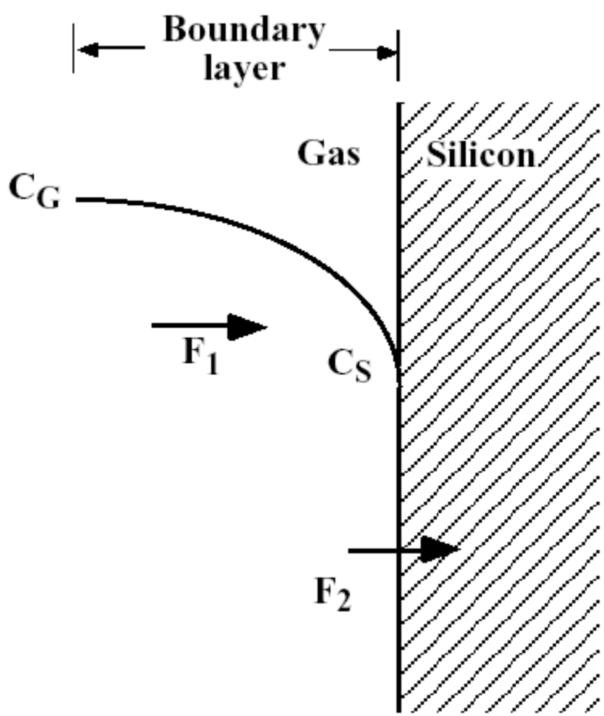
Additionally: Growth temperature. Uniformity < 5%. Adhesion. Morphology, stoichiometry & density. Pinhole density < 1/cm^2. Stress – built-in and thermal mismatch.

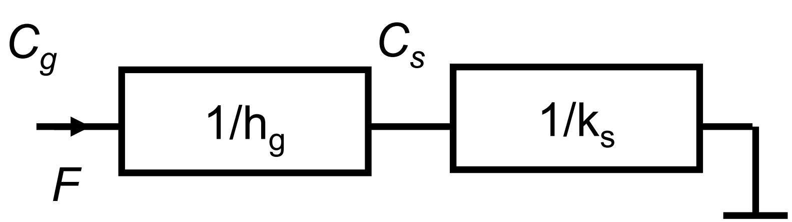
Chemical Vapor Deposition process



1. Transport of reactants to the deposition region.
2. Transport of reactants from the main gas stream through the boundary layer to the wafer surface.
3. Adsorption of reactants on the wafer surface.
4. Surface reactions.
5. Desorption of byproducts.
6. Transport of byproducts through boundary layer.
7. Transport of byproducts away from the deposition region.

CVD Kinetics





N: Incorporated molecules per volume

Mass Transfer Flux: $F_1 = h_g\left(C_g - C_s\right)$

1. Order Chemical Reaction Flux: $F_2 = k_s C_s$

Steady State Flux: $F_1 = F_2 = F = C_g \dfrac{h_g k_s}{h_g + k_s}$

Surface Concentration: $C_s = \dfrac{C_g}{1 + k_s / h_g}$

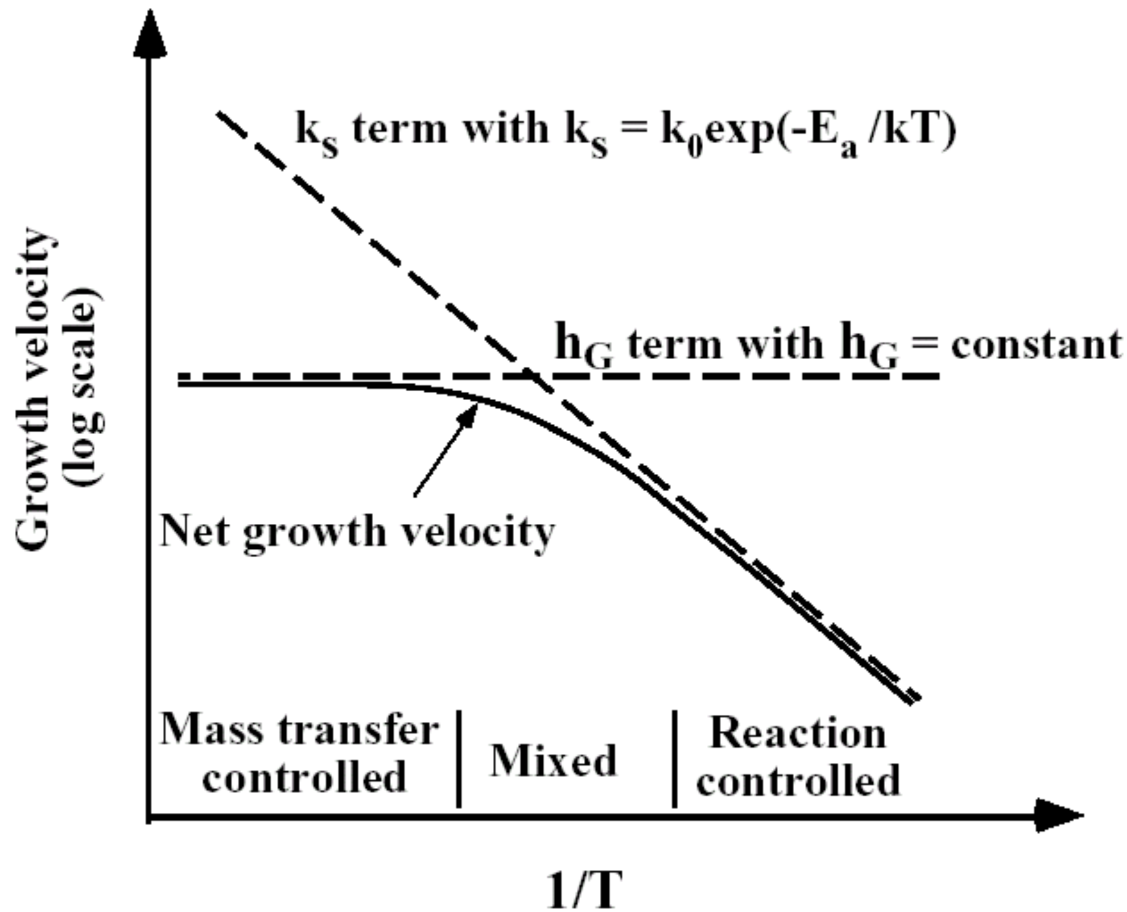
Growth Rate: $R = \dfrac{F}{N} = \dfrac{h_g k_s}{h_g + k_s}\dfrac{C_g}{N} = \dfrac{h_g k_s}{h_g + k_s}\dfrac{C_T}{N} Y$

Source Gas Mole Fraction: $Y = \dfrac{C_g}{C_T}$

Mass Transfer Control $\left(h_g << k_s\right)$: $R \cong h_g \dfrac{C_T}{N} Y$

Surface Reaction Control $\left(h_g >> k_s\right)$: $R \cong k_s \dfrac{C_T}{N} Y$

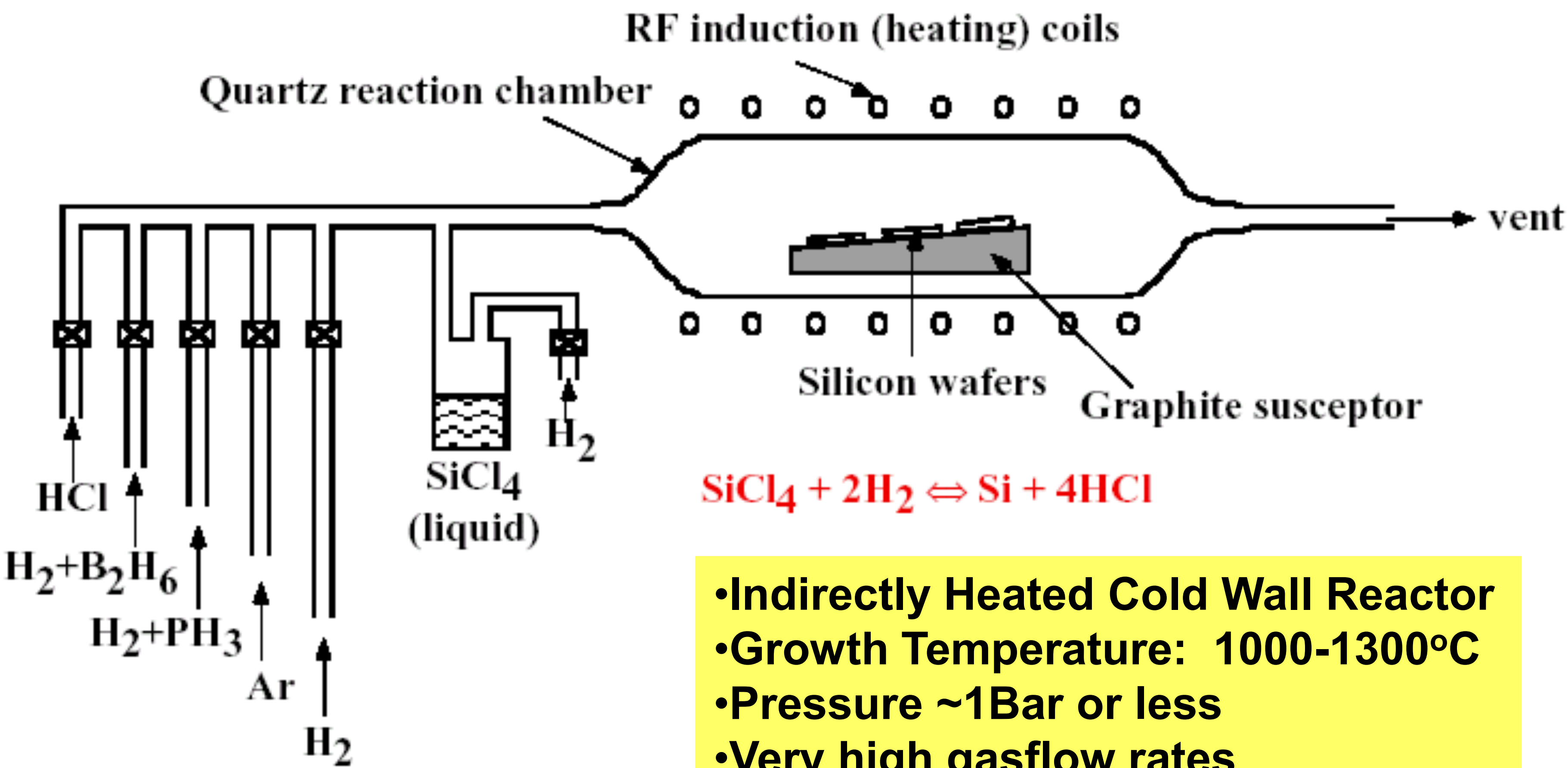
Growth Rate: Temperature Dependence



Surface reaction constant: strong temperature dependence

Mass transfer coefficient: strong geometry & pressure dependence

APCVD - Vapour Phase Epitaxy (VPE)



$SiCl_4 + 2H_2 \Leftrightarrow Si + 4HCl$

Other Si-Sources:
Silane: SiH_4
Chlorosilane: SiH_xCl_y

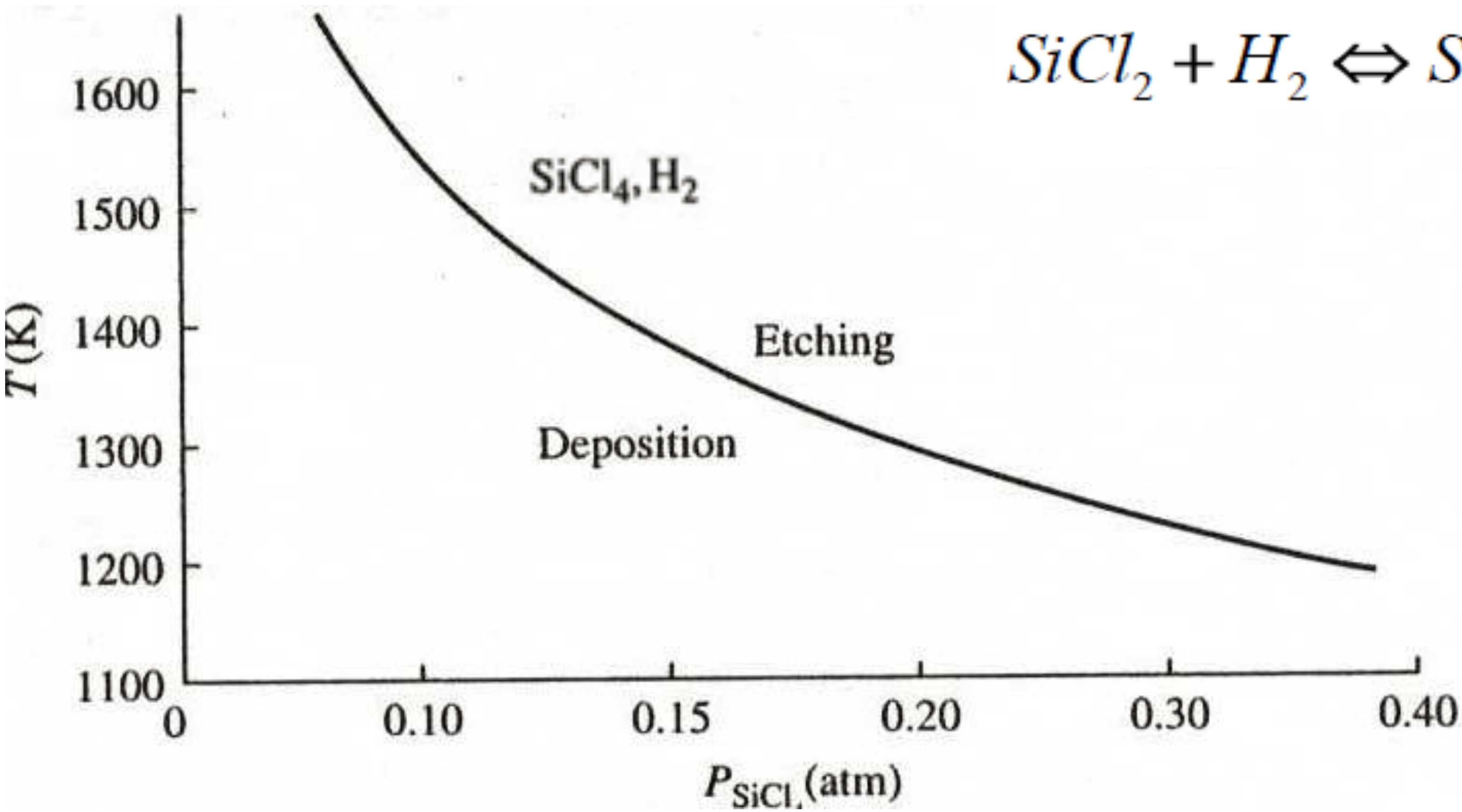
- **Indirectly Heated Cold Wall Reactor**
- **Growth Temperature: 1000-1300°C**
- **Pressure ~1Bar or less**
- **Very high gasflow rates**
- **Low Si-compound Molar Fraction**
- **Quite Low Wafer Throughput**
- **HCl used for pre-epi etch/clean**

Chemical reactions

$$SiH_4 \Rightarrow Si + 2H_2$$

$$SiCl_4 + H_2 \Leftrightarrow SiHCl_3 + HCl$$

$$SiHCl_3 + H_2 \Leftrightarrow SiH_2Cl_2 + HCl$$



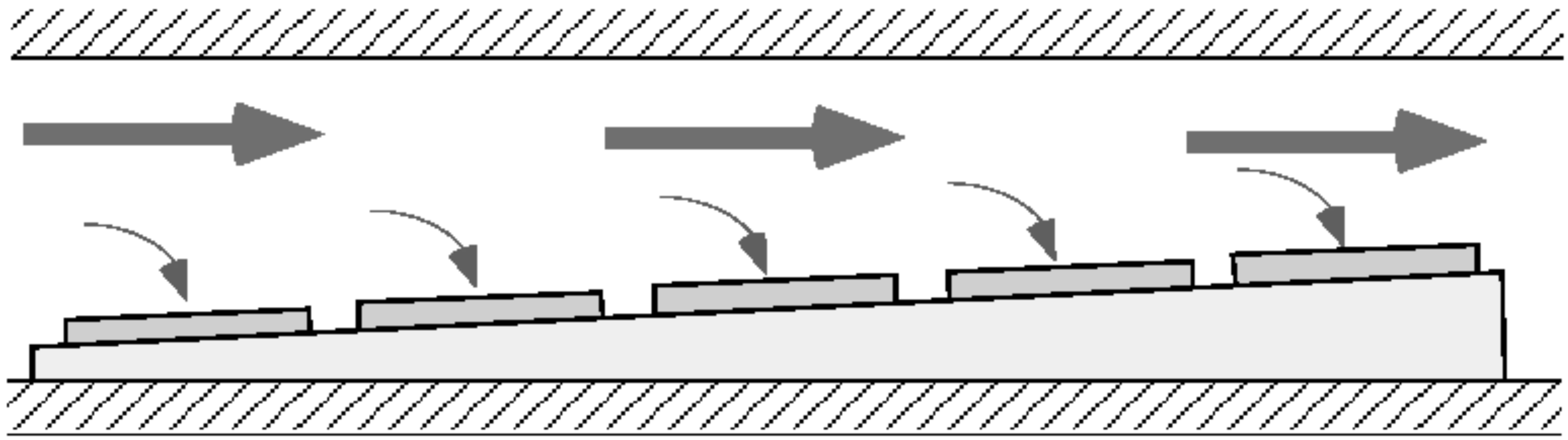
$$SiHCl_3 \Leftrightarrow SiCl_2 + HCl$$

$$SiH_2Cl_2 \Leftrightarrow SiCl_2 + H_2$$

$$SiH_2Cl_2 \Leftrightarrow Si + 2HCl$$

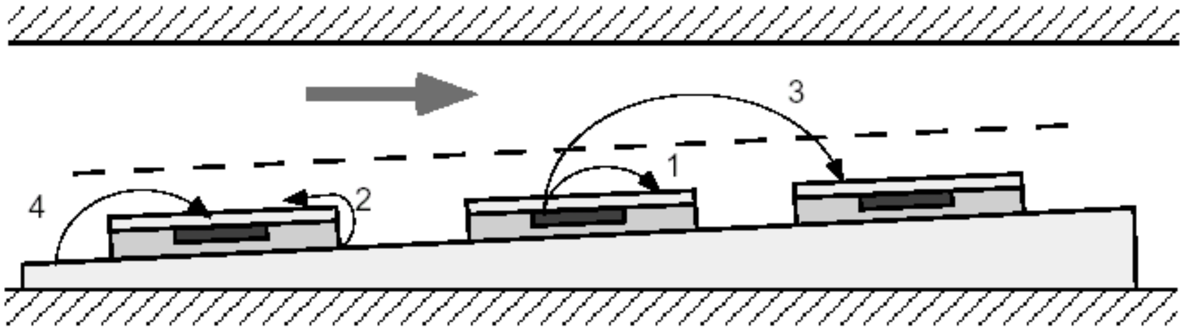
$$SiCl_2 + H_2 \Leftrightarrow Si + HCl$$

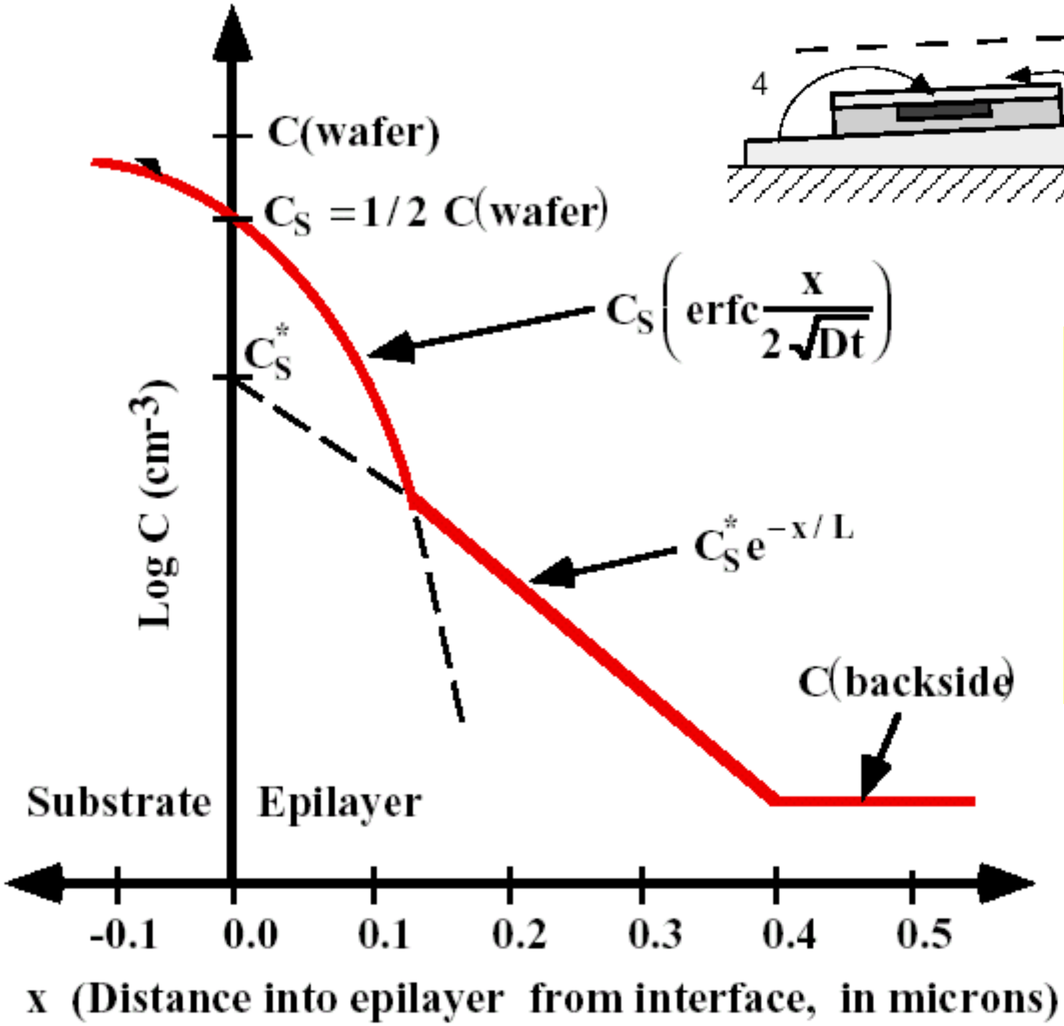
Gas Depletion Compensation



The growth consumes source gas molecules ⇒
Concentration & rate drops with increasing x
Tilting the susceptor decreases boundary layer thickness with x⇒
Rate increases with x
A specific tilt just balances the gas depletion

VPE Auto-doping



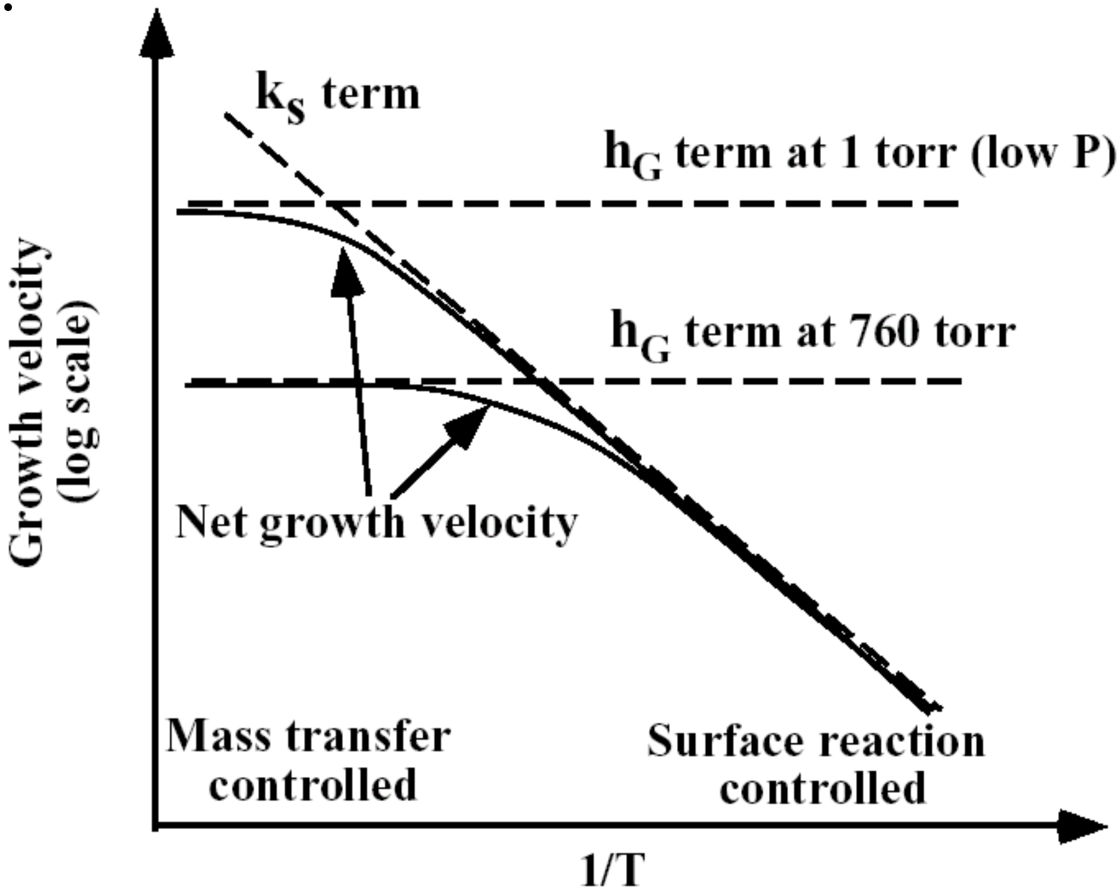


Outdiffusion from substrate:
Erfc-profile (Step-profile)

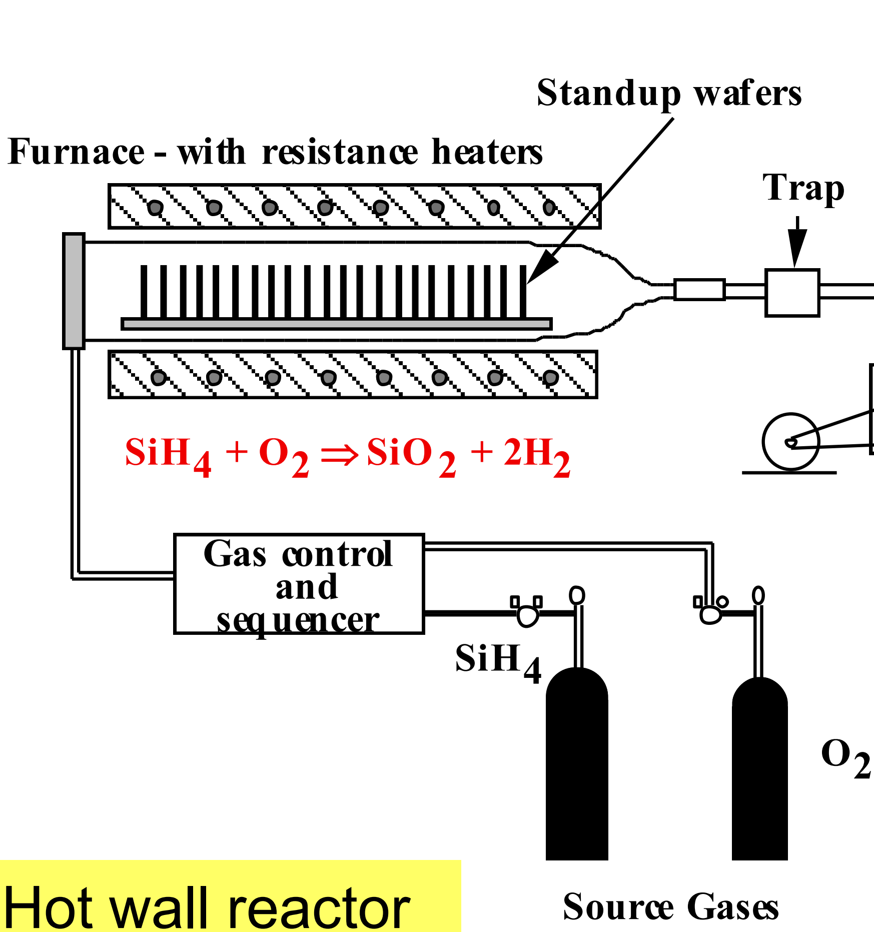
Homogenous exponential profile
Related to pre-epi etch

APCVD - Limitation

- Atmospheric pressure systems have major drawbacks:
    - At high T, a horizontal configuration must be used (few wafers at a time).
    - At low T, the deposition rate goes down and throughput is again low.



LPCVD - Low Pressure CVD



- The solution is to operate at low pressure. In the mass transfer limited regime,

$$h_G = \frac{D_G}{\delta_S} \quad \text{But} \quad D_G \propto \frac{1}{P_{total}}$$

- D_G will go up 760 times at 1 torr, while increases δs by about 7 times. Thus h_G will increase by about 100 times.
- Transport of reactants from gas phase to surface through boundary layer is no longer rate limiting.
- Process is more T sensitive, but can use resistance heated, hot-walled system for good control of temperature and can stack wafers.

Hot wall reactor
High productivity
P~0.01-1Torr
T~400-900^{o}C

LPCVD – Chemical reaction

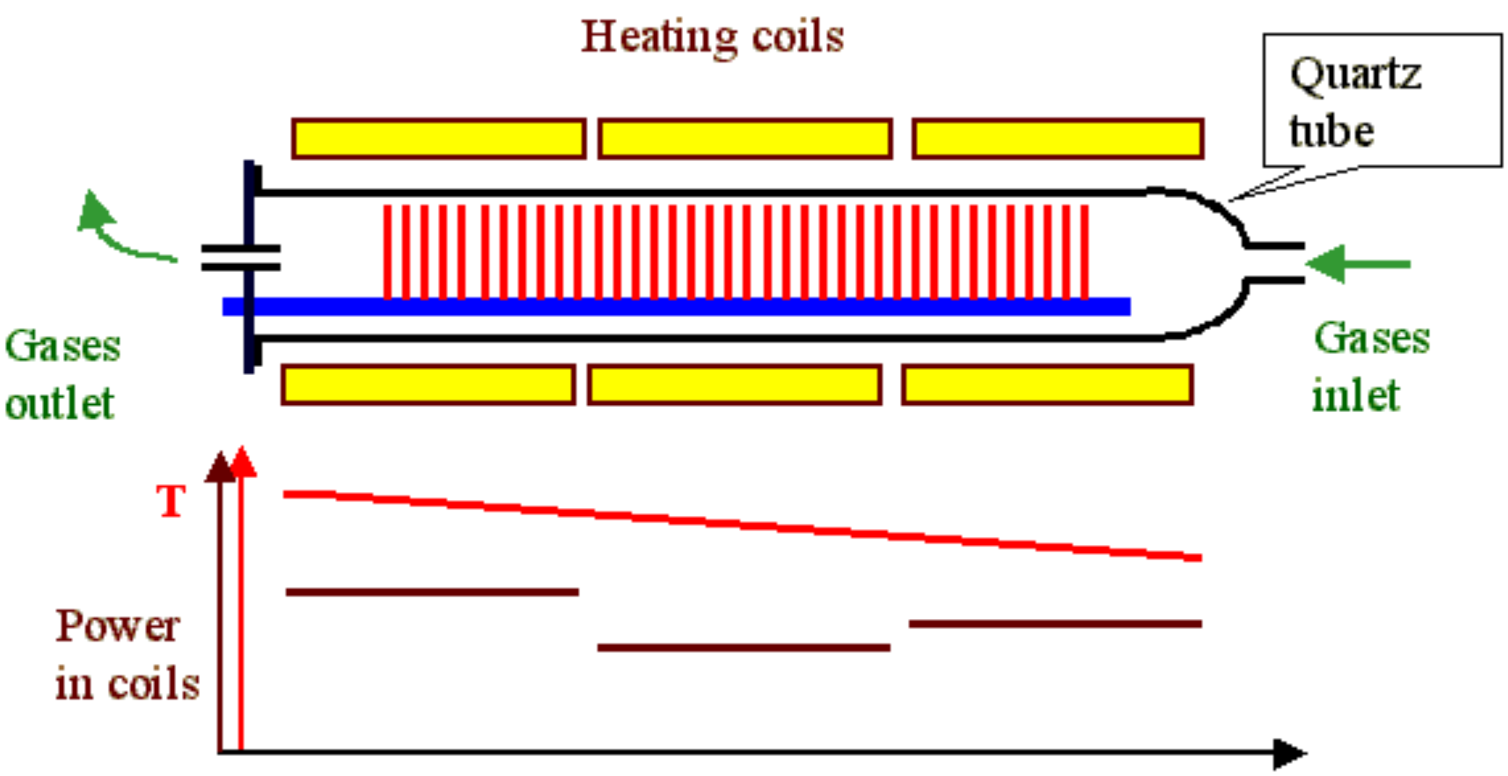
$$SiH_4 \rightarrow Si(amorphous) + 2H_2 \quad (600\text{-}650\ ℃)$$

Pressure: 1 torr;
T<575 ℃, amorphous Si;
T>600 ℃, column structure;
Amorphous Si starts to crystallize above 600 ℃;
Column structure grain grows with thermal annealing;

Advantages:

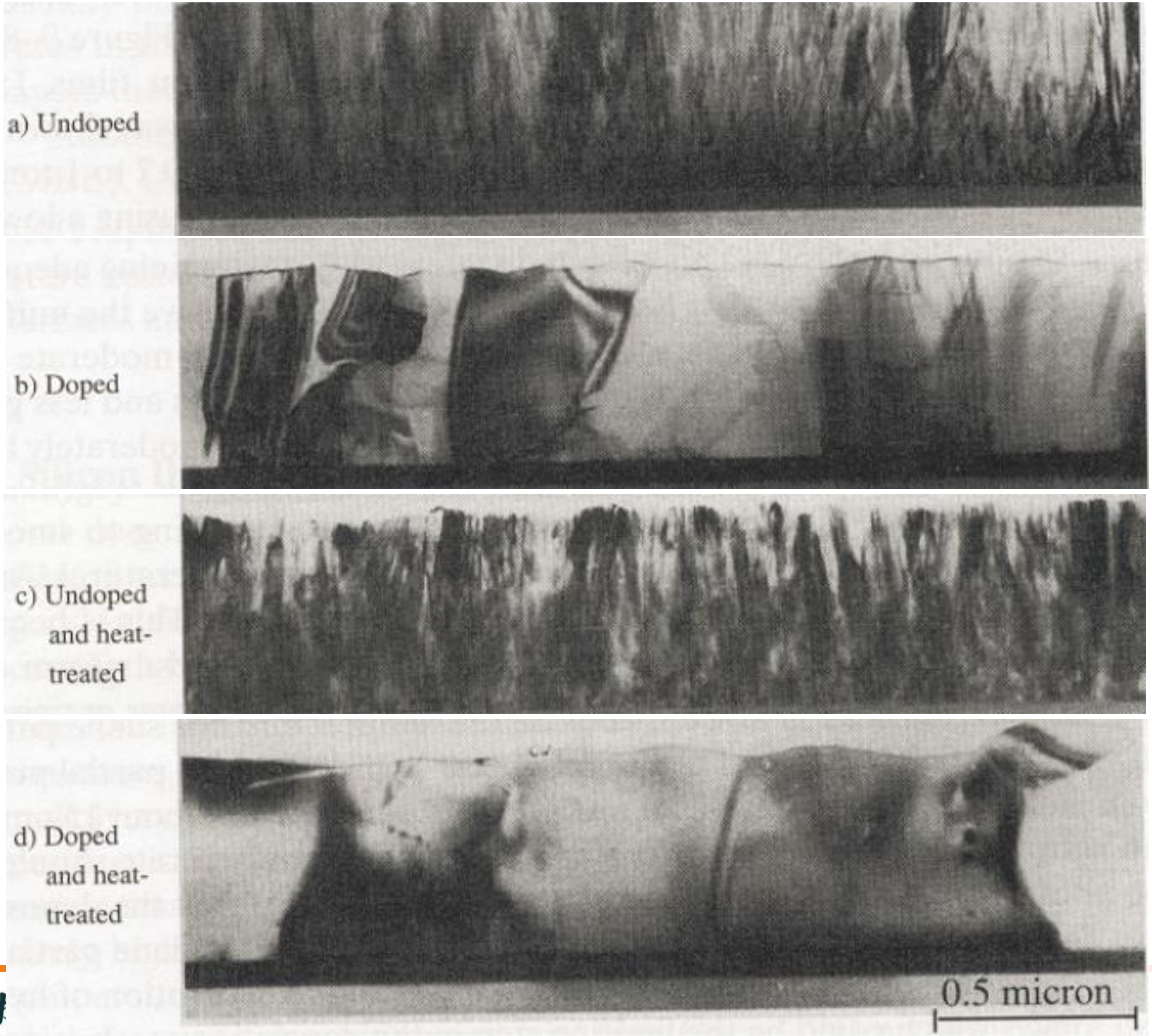
- ✓100~200 wafers; high throughput;
- ✓Good thickness uniformity;
- ✓Well controlled composition;
- ✓Good step coverage;
- ✓Relatively low temperature;
- ✓High deposition rate

Temperature compensation of Gas-depletion



Growth consumes source material ⇒
Growth rate drops with distance from inlet
Compensate by increasing T with distance.

TEM image of LPCVD PolySi at 625 ºC



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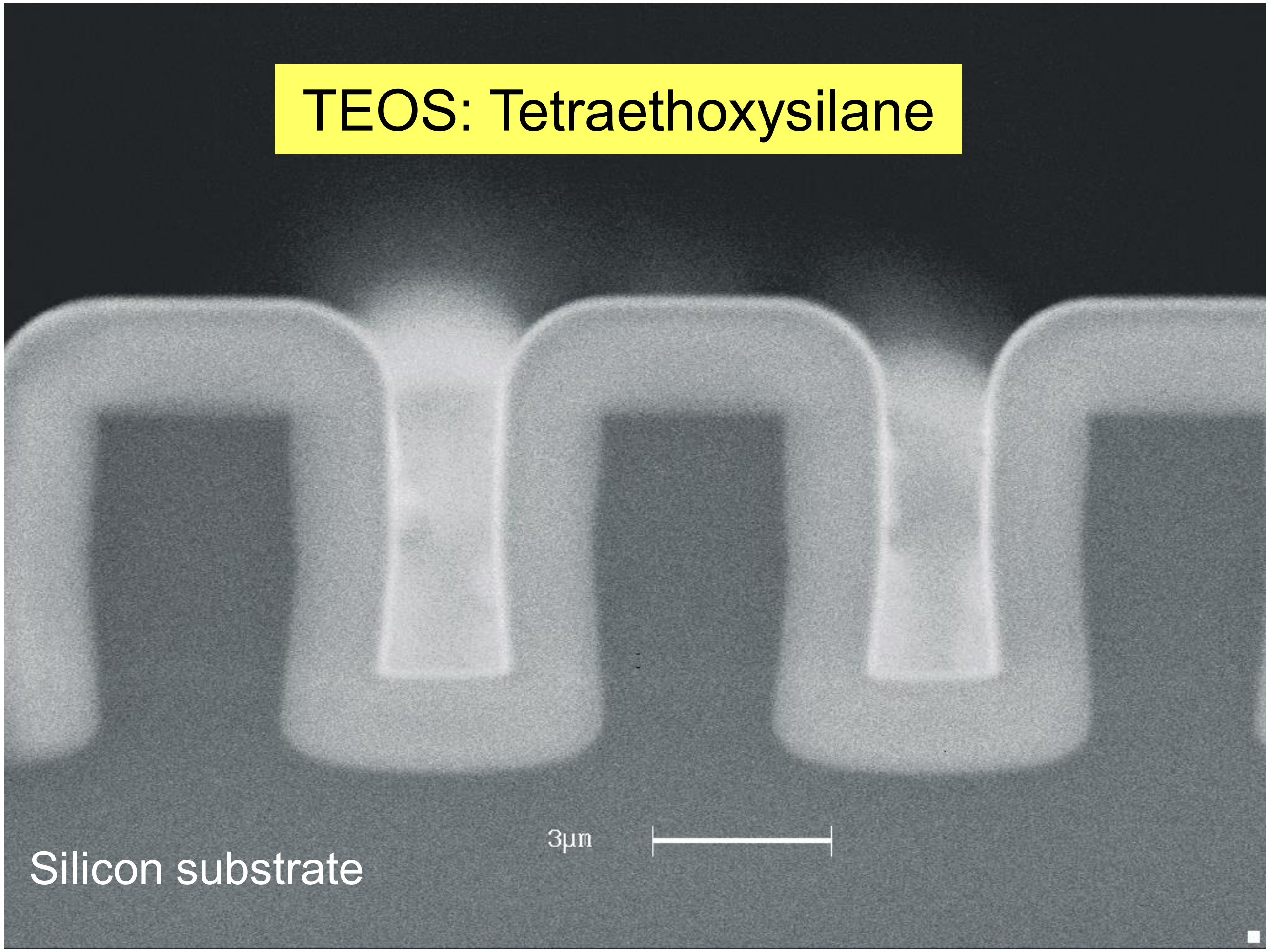
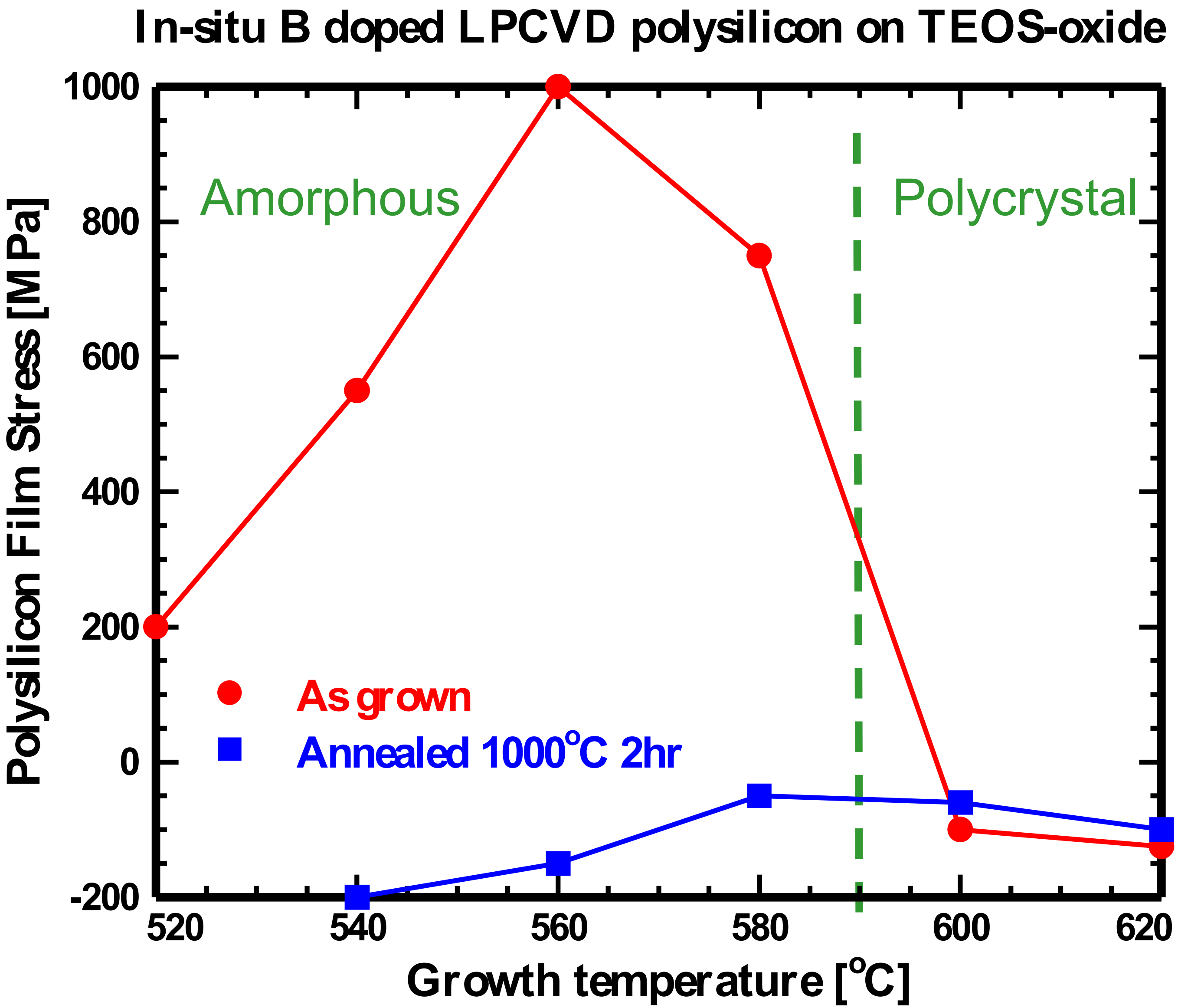
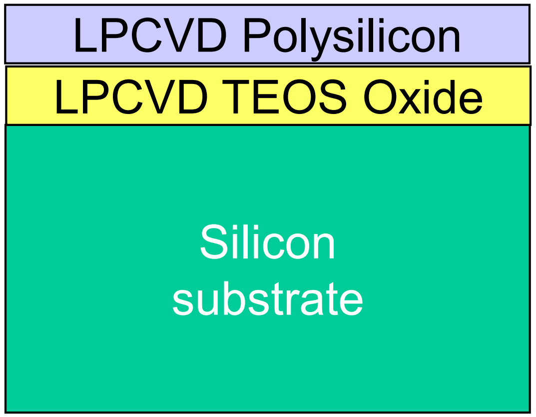
LPCVD TEOS Oxide $Si(OC_2H_5)_4$



Good Step Coverage & Trench Filling – Almost Conformal
Due to high mobility of TEOS on the surface

Stress in Boron Doped LPCVD Polysilicon





Net reaction

$SiH_4 + xB_2H_6 \Rightarrow$

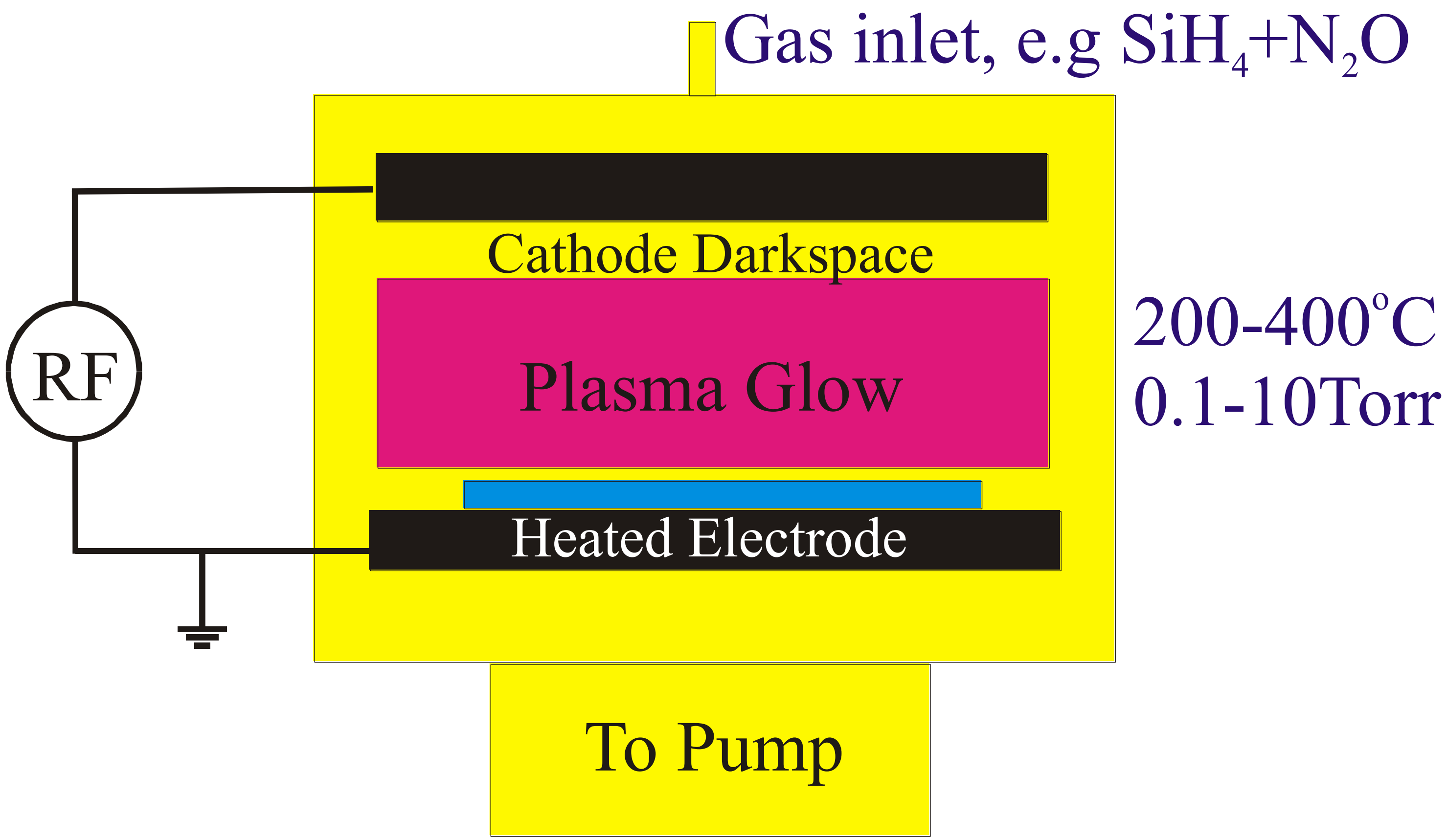
$Si(2xB) + (2+3x)H_2$

Problems in APCVD – LPCVD @ low T

Low temperature deposition impractical:

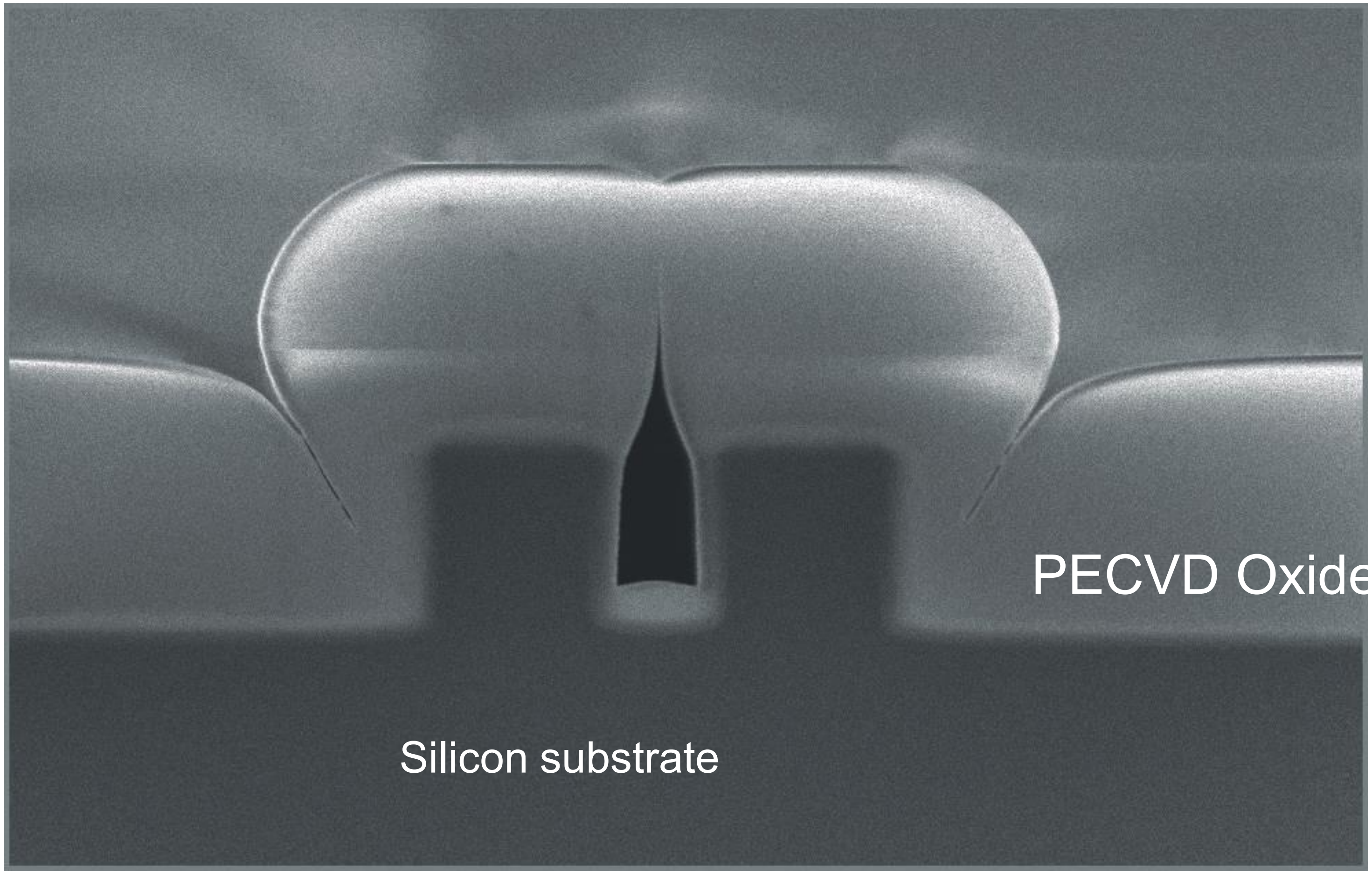
- Very low rates at low temperature
  - ~exp($-E_a/kT$)
- Low film quality
  - Porous due to low surface diffusivity
  - Poor step coverage/ trench filling
    - High sticking coefficient
    - Low surface diffusivity
- Solution: PECVD – Plasma Enhanced CVD

Plasma Enhanced CVD – PECVD



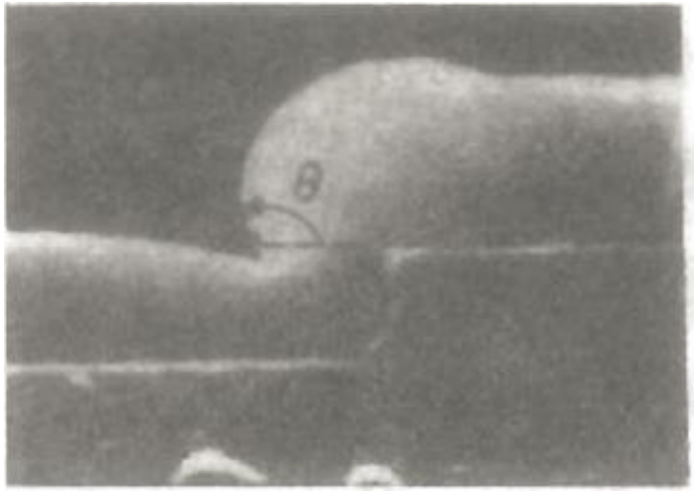
<u>The gas discharge creates:</u>
Reactive, Energetic Molecular Fragments – Increases surfacereaction constant k_s
Energetic Ions – Ion bombardment densify the film
<u>Result:</u> High deposition rates & dense films at low temperatures.

PECVD Oxide Film SiH_4+N_2O at 300°C

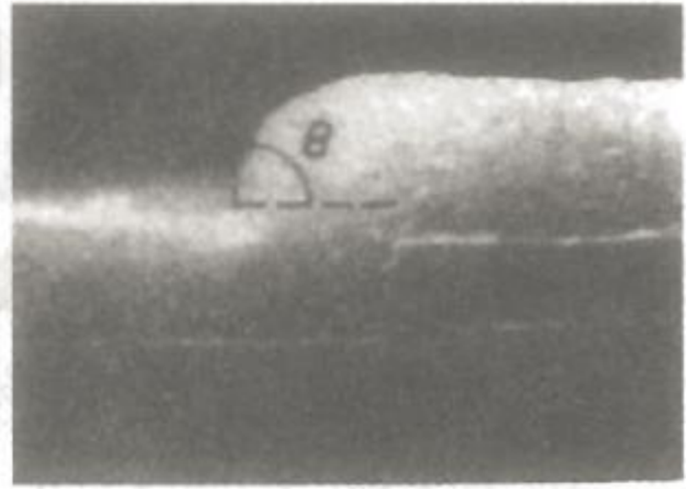


Poor trench filling, voids & cracks due to low surface mobility
Step coverage and trench filling is a general PECVD problem.

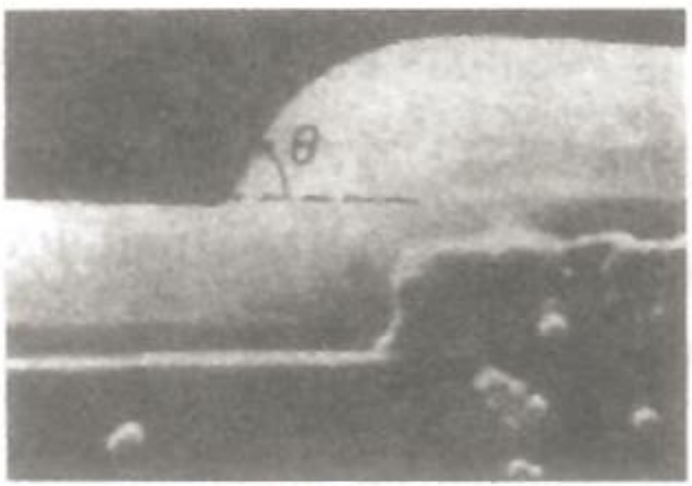
PSG/BPSG reflow for Oxide



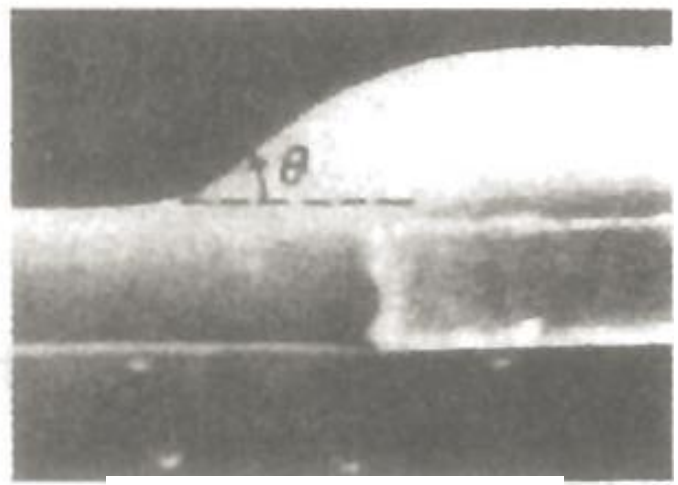
without P



with 2.2%P

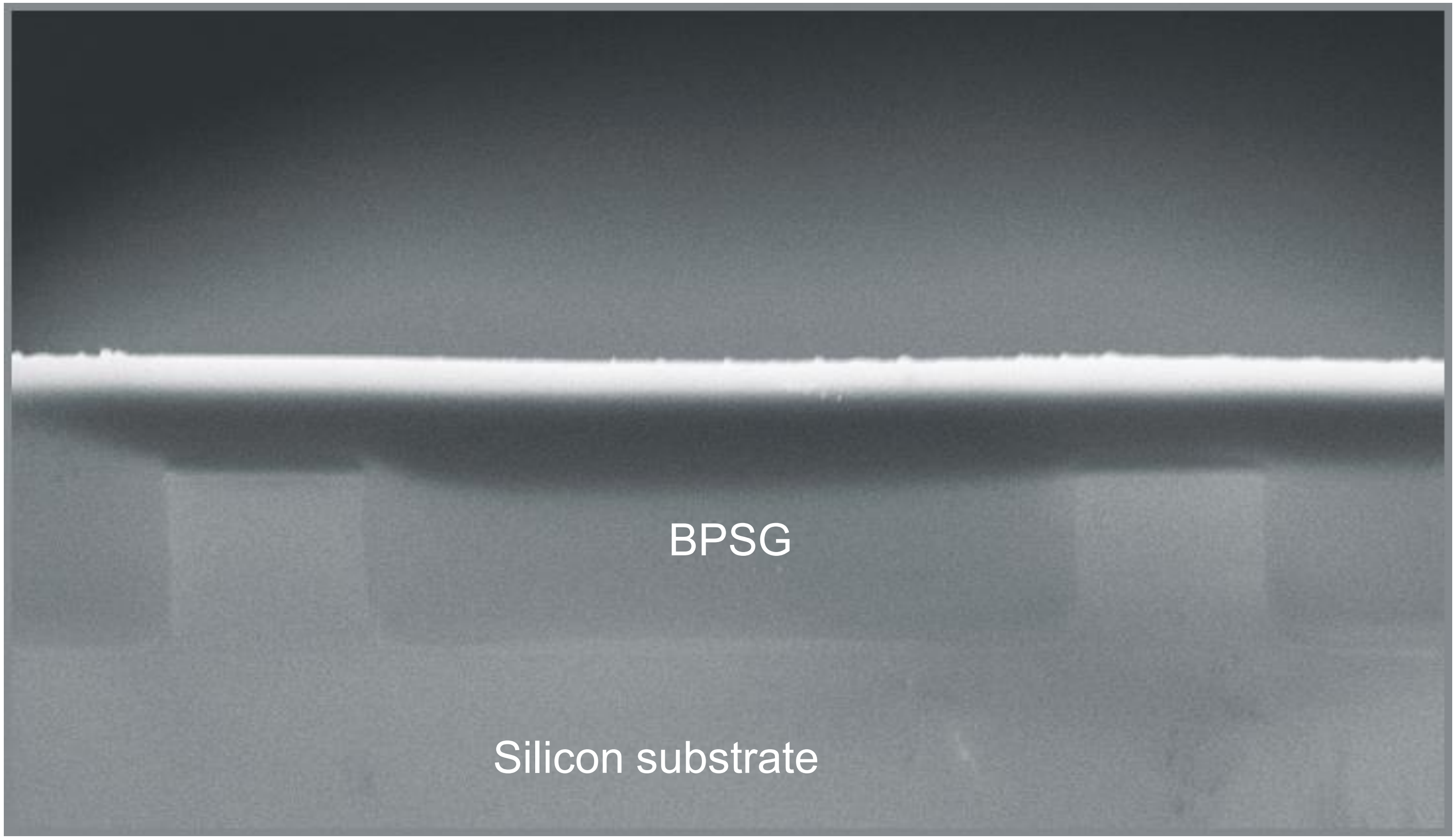


with 4.6%P



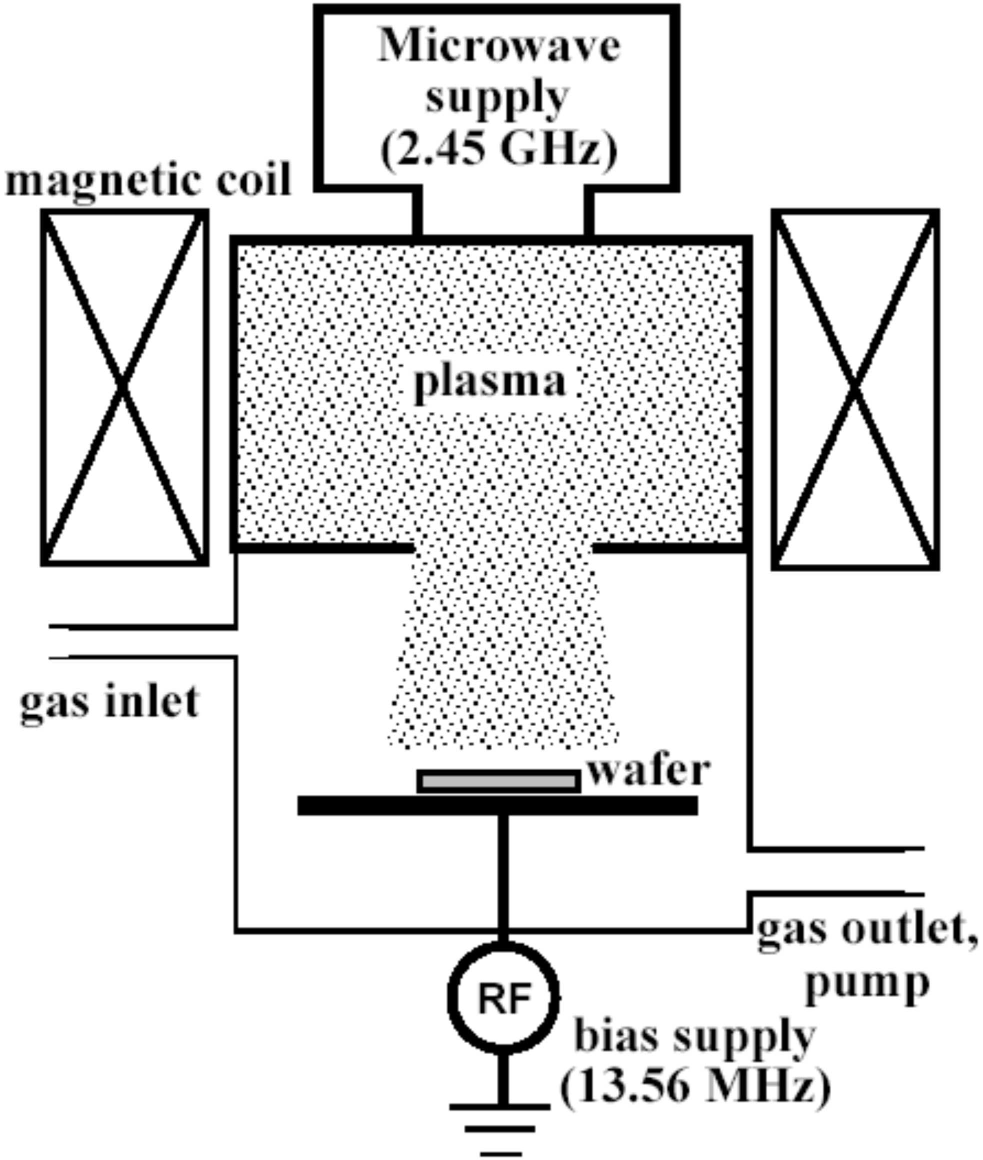
with 7.6%P

Annealed PECVD BPSG



SEM cross-section of PECVD BPSG Oxide on structured silicon.
Planarized surface after anneal due to viscous flow and surface tension.
BPSG: Boron Phosphorous Silica Glass

High Density Plasma CVD



Remote high density plasma source

•High deposition rate possible

Independent substrate bias

•Controlled simultaneous deposition & sputter-etching

  •Planarization

  •Controlled ionflux-induced densification & stress control