

Electronic Materials and Devices

5 Semiconductor

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5.9 Field-effect transistors (FETs)

FET uses the electric field effect to control the output current

场效应晶体管，简称称场效应管，是利用电场效应来控制输出回路电流的一种半导体器件

Compare FET with BJT:

BJT (Bipolar junction transistor) 双极型晶体管:

- ☐ **Current-controlled device 电流控制型器件**
- ☐ **Input resistance is small**
- ☐ **Both electrons and holes are involved in conduction**

FET 场效应晶体管:

- High input resistance: $10^7 \sim 10^{15} \Omega$**
- Only one type of carriers (electrons or holes) is involved in conduction**
- Small size, light, low-power consumption, long life span**
- Low noise, high stability, simple fabrication process**
- Widely used in large-scale integration circuits**

FET 场效应晶体管：

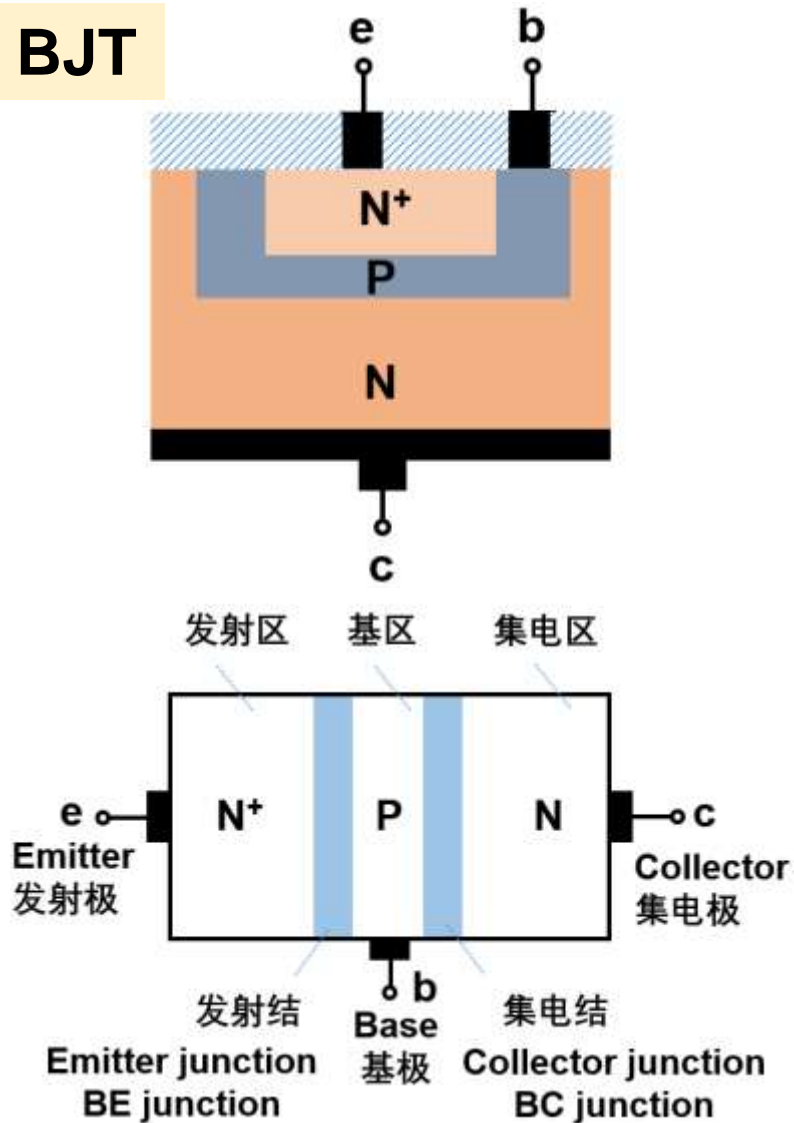
**1. JFET (Junction Field Effect Transistor)
结型场效应管**

**2. IGFET (Insulated Gate Field Effect Transistor)
绝缘栅型场效应管**

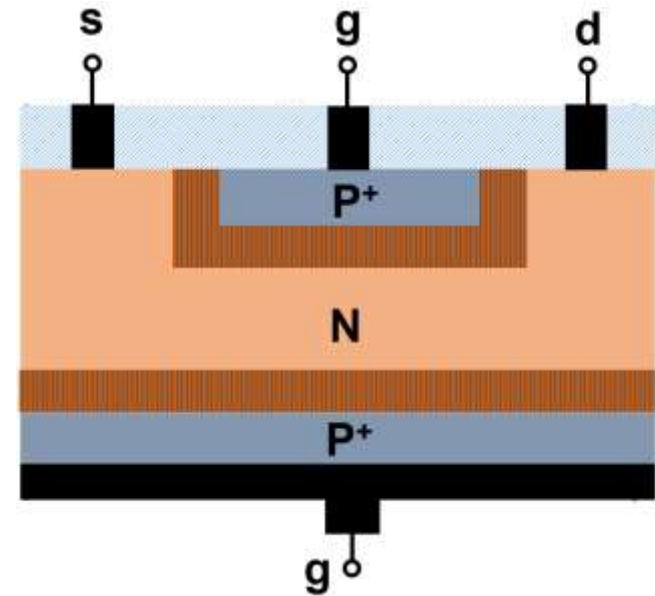
MOSFET (Metal-oxide-semiconductor FET)

Junction Field Effect Transistor (JFET)

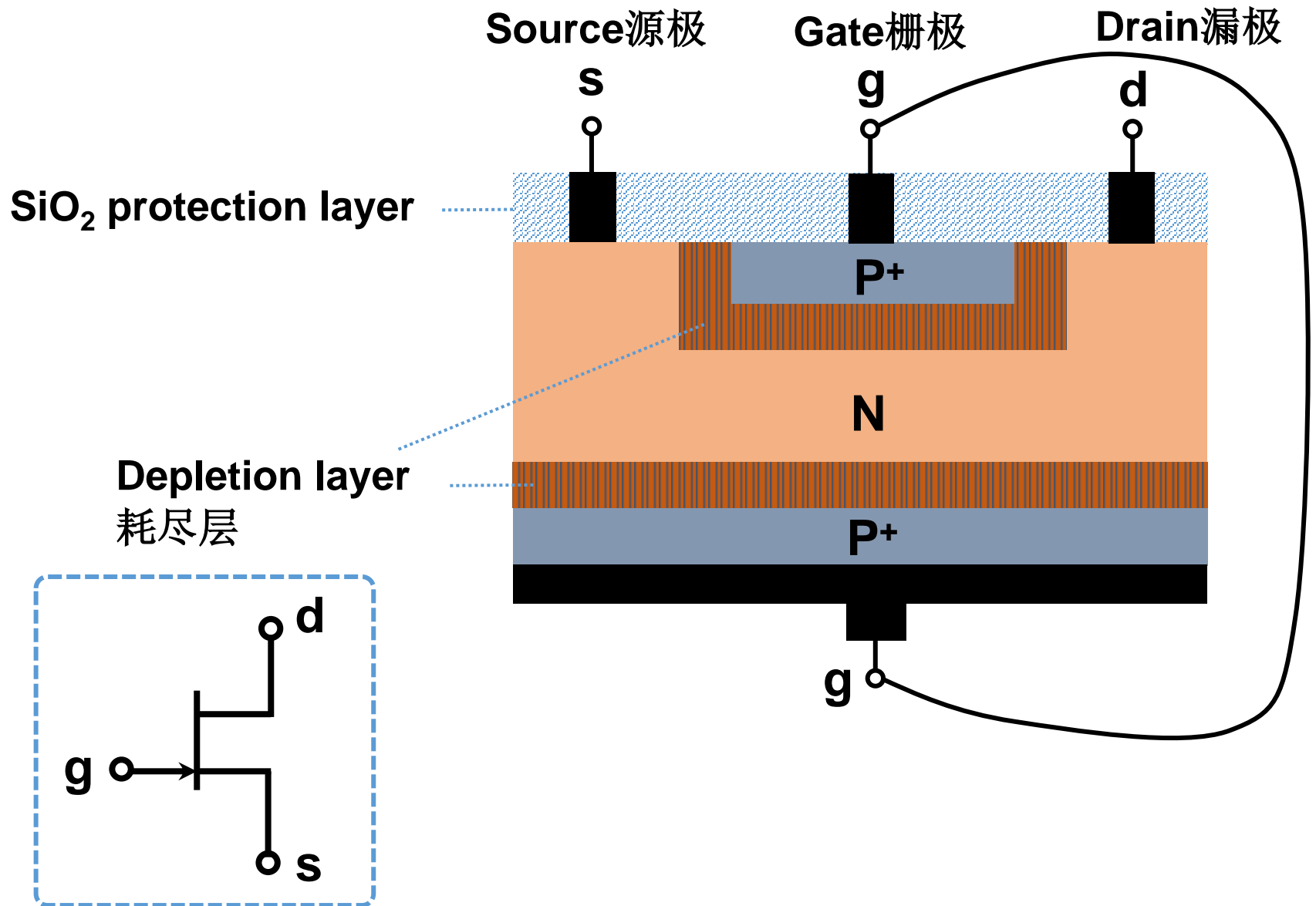
BJT



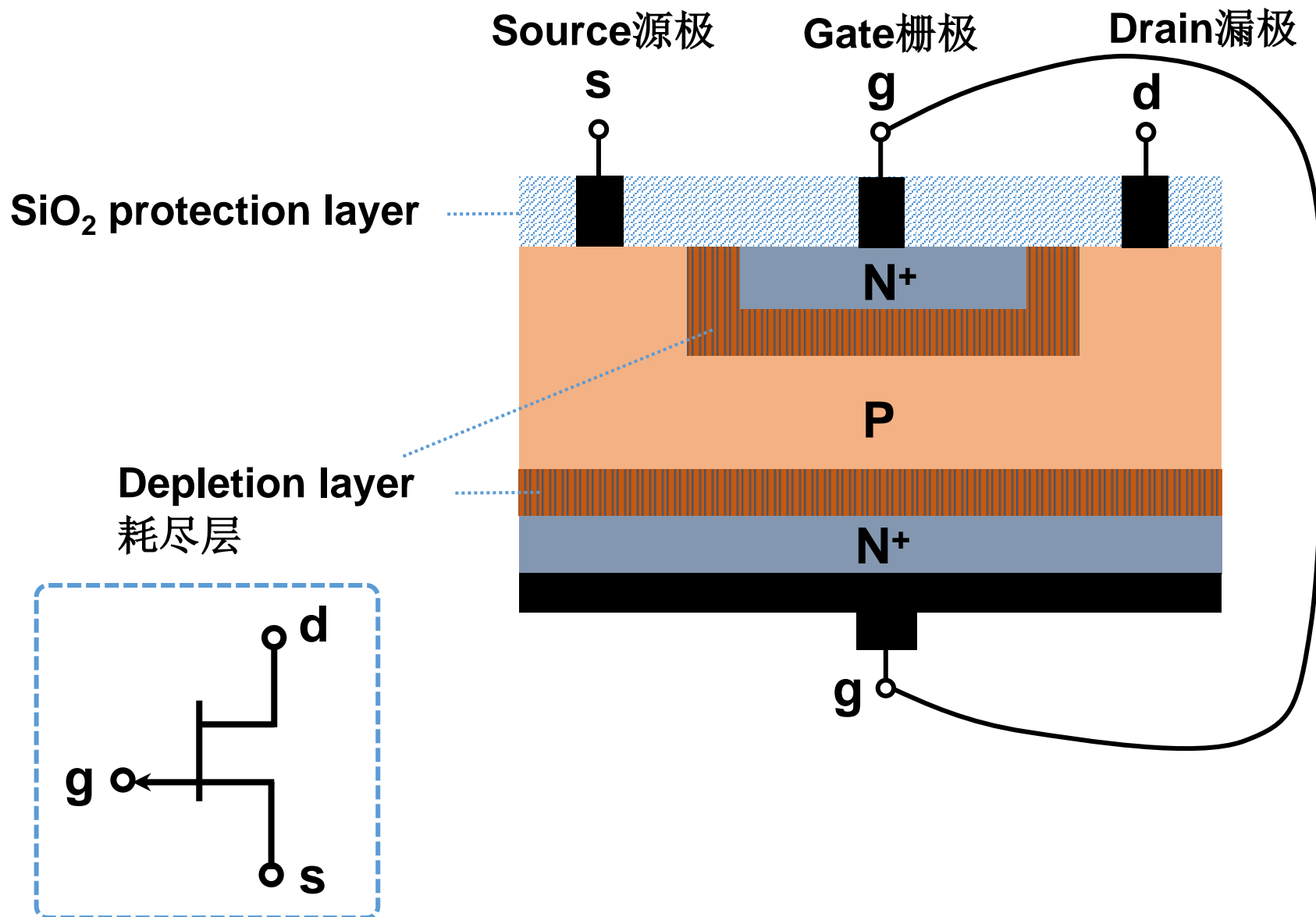
JFET



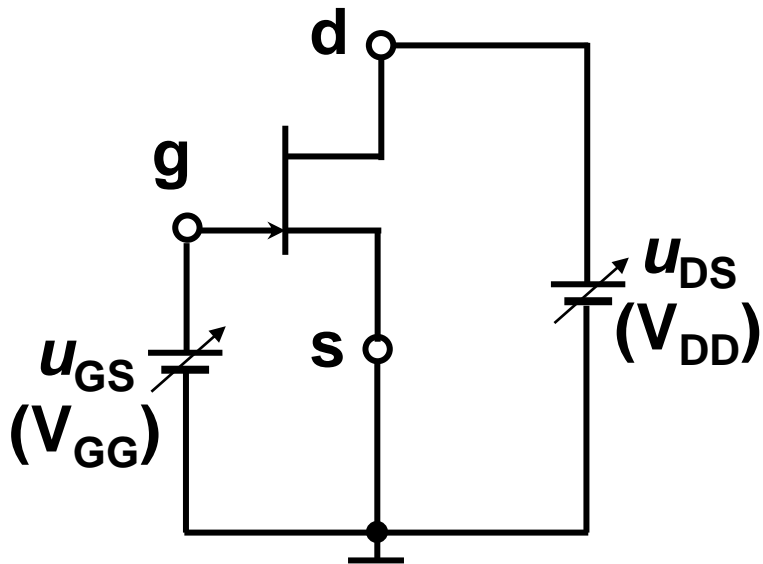
N-type JFET



P-type JFET

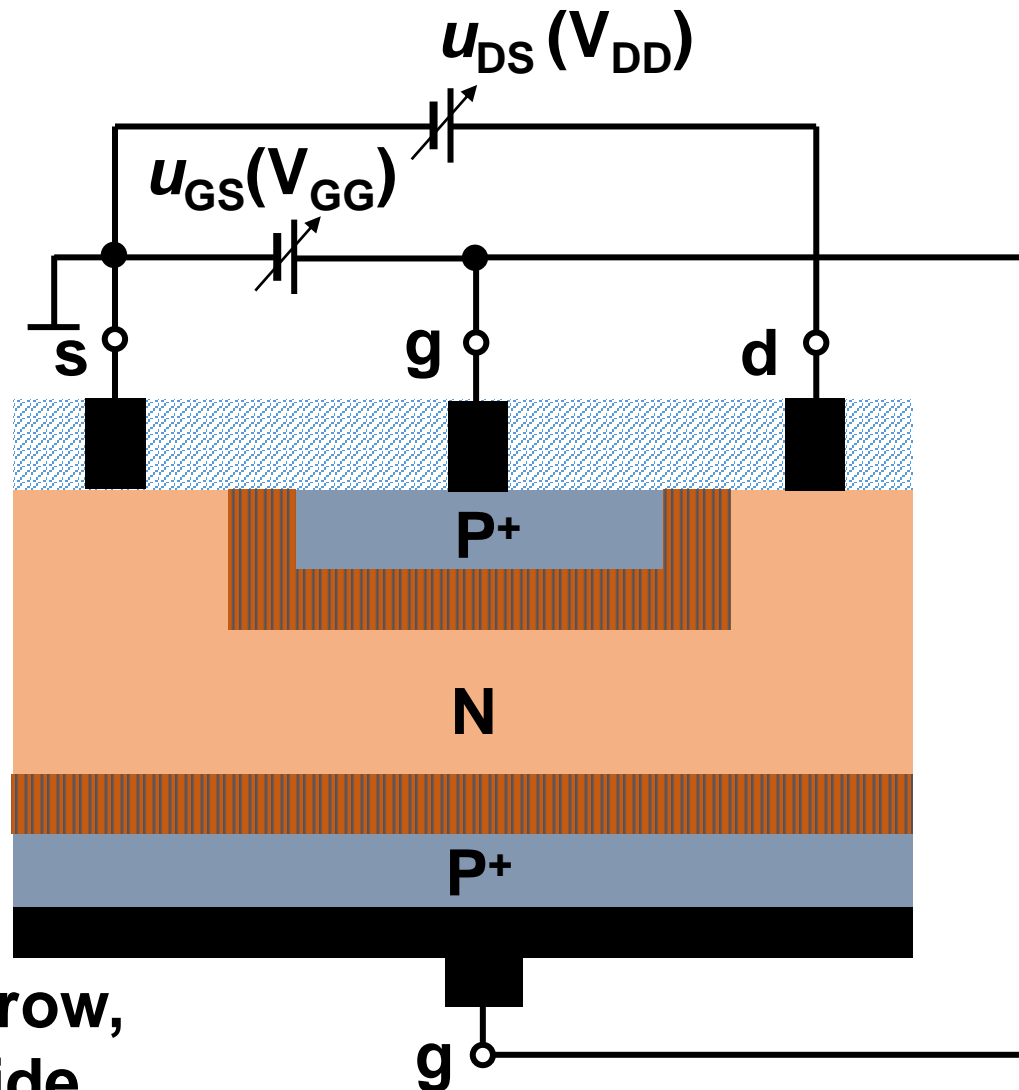


Electrical connection of N-type JFET



When $u_{GS}=u_{DS}=0$:

Depletion region is narrow,
conduction channel is wide



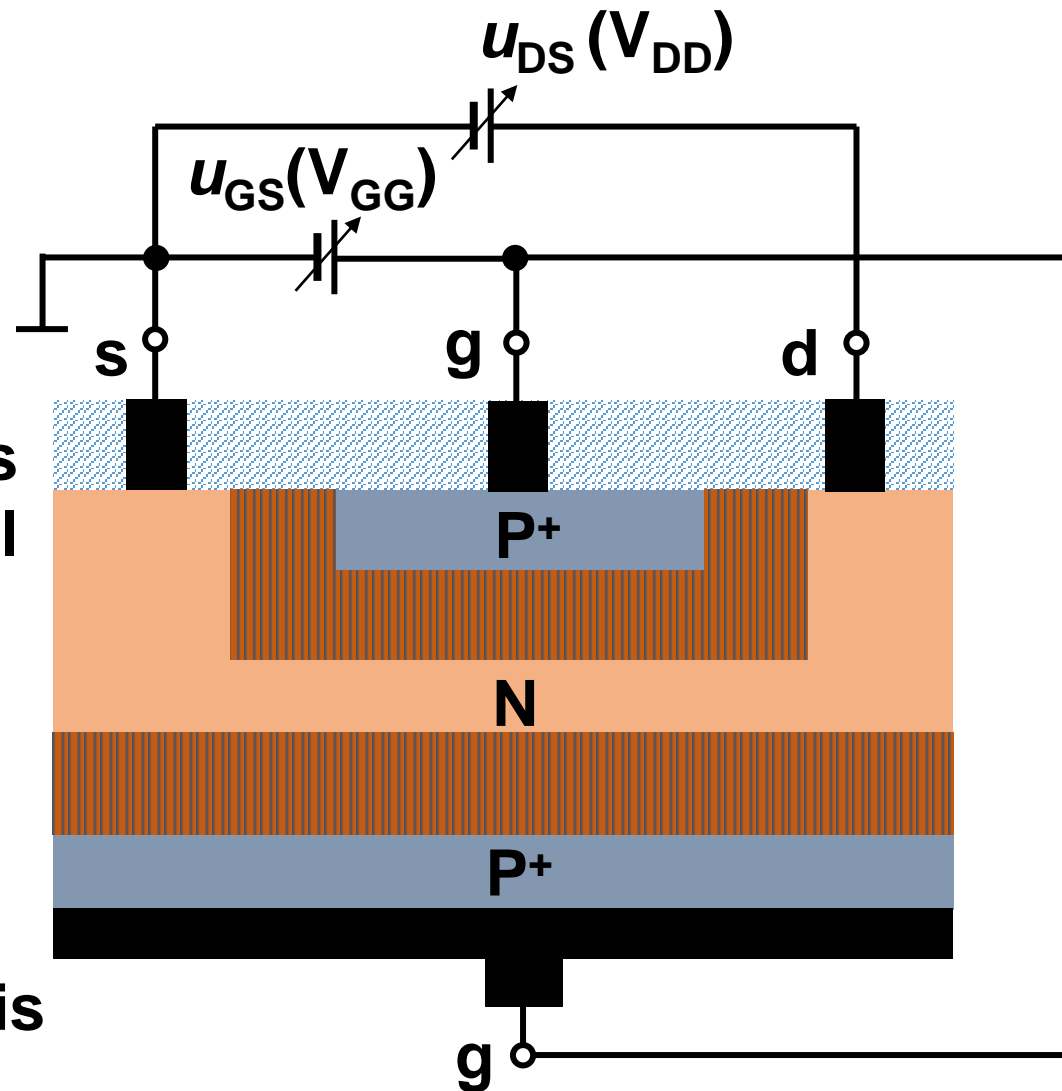
1) $u_{DS}=0$

When $U_{GS(off)} < u_{GS} < 0$:

Depletion region becomes wider, conduction channel becomes narrower

The resistance $R_{DS} \uparrow$

Current between g and s is very small: equal to the reverse saturation current!



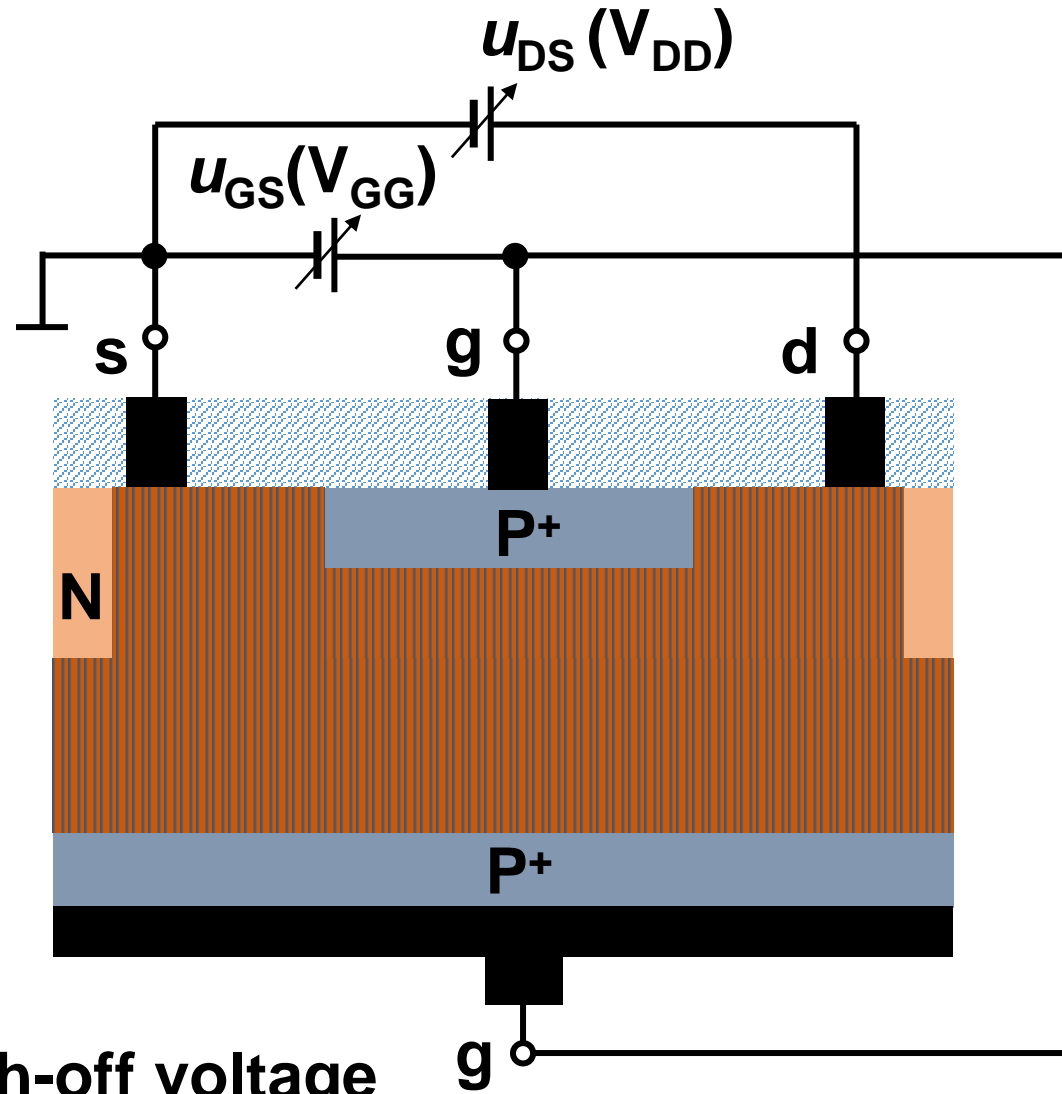
1) $u_{DS}=0$

When $u_{GS} < U_{GS(off)}$:

Depletion regions are connected, conduction channel disappears

The resistance R_{DS} is extremely large

$U_{GS(off)}$ is called gate pinch-off voltage
夹断电压



2) $u_{GS}=0$

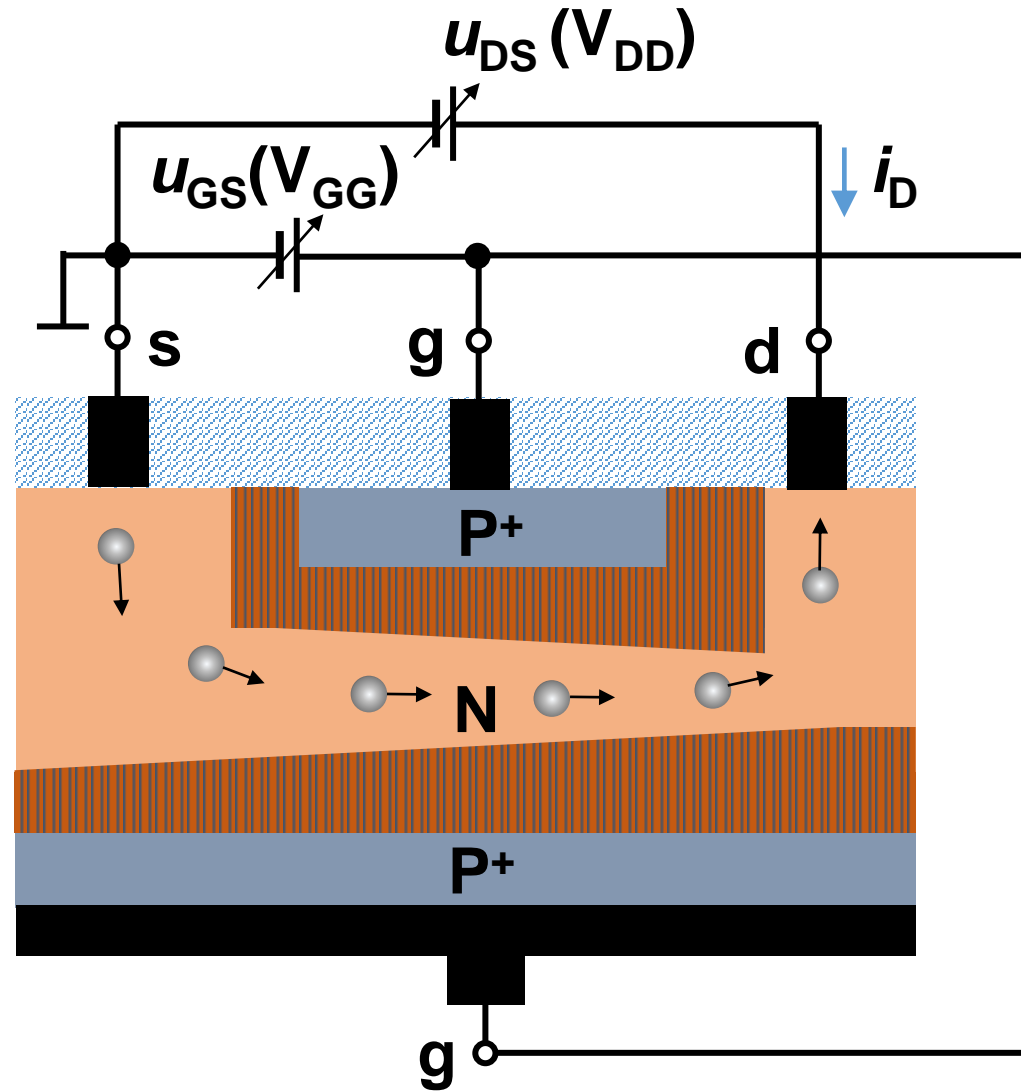
When $0 < u_{DS} < |U_{GS(off)}|$:

The drain current $i_D \neq 0$

$u_{DS} \uparrow, i_D \uparrow$

The reverse voltage on PN is position-dependent

Conduction channel becomes wedge-shaped

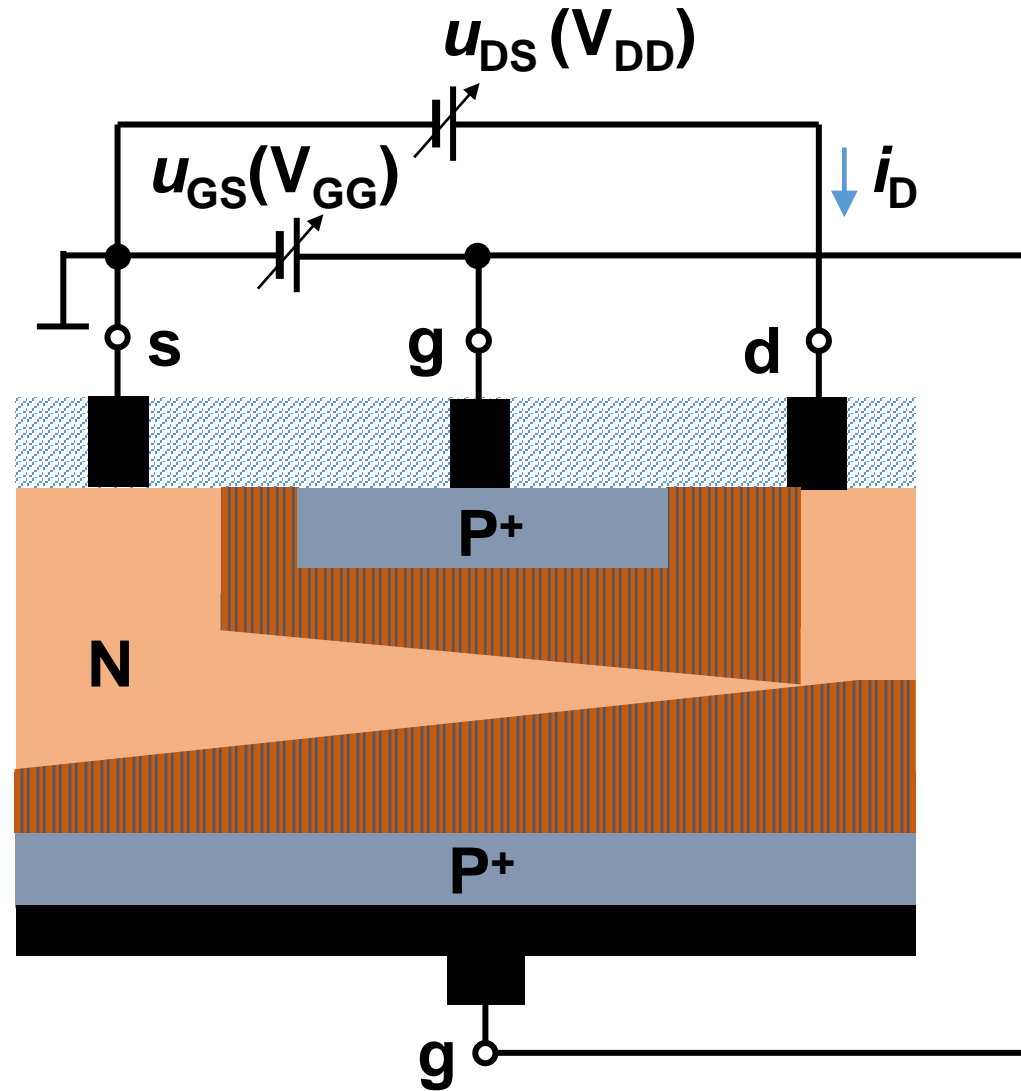


2) $u_{GS}=0$

When $u_{DS}=|U_{GS(off)}|$:

i_D reaches the maximum value

Pinch-off region is a point
点夹断(预夹断)



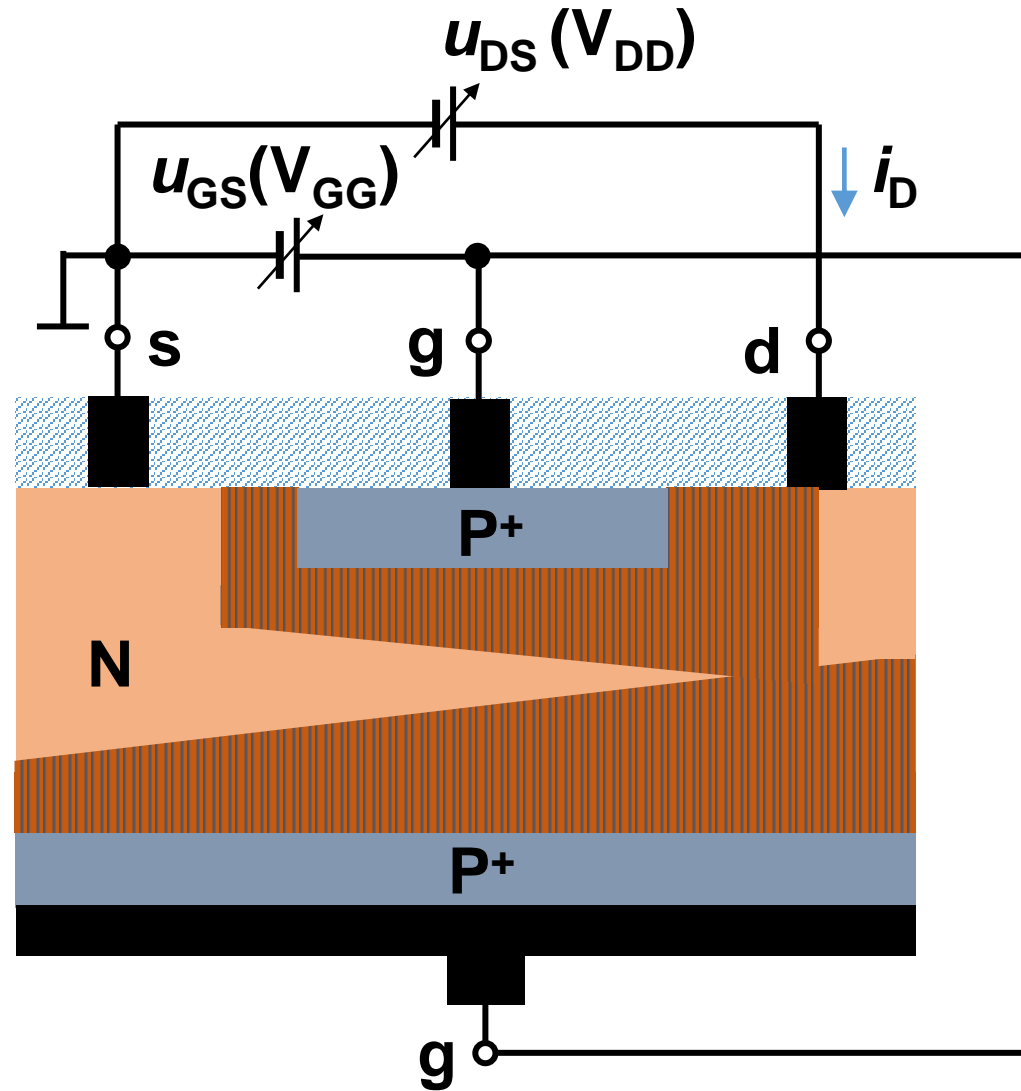
2) $u_{GS}=0$

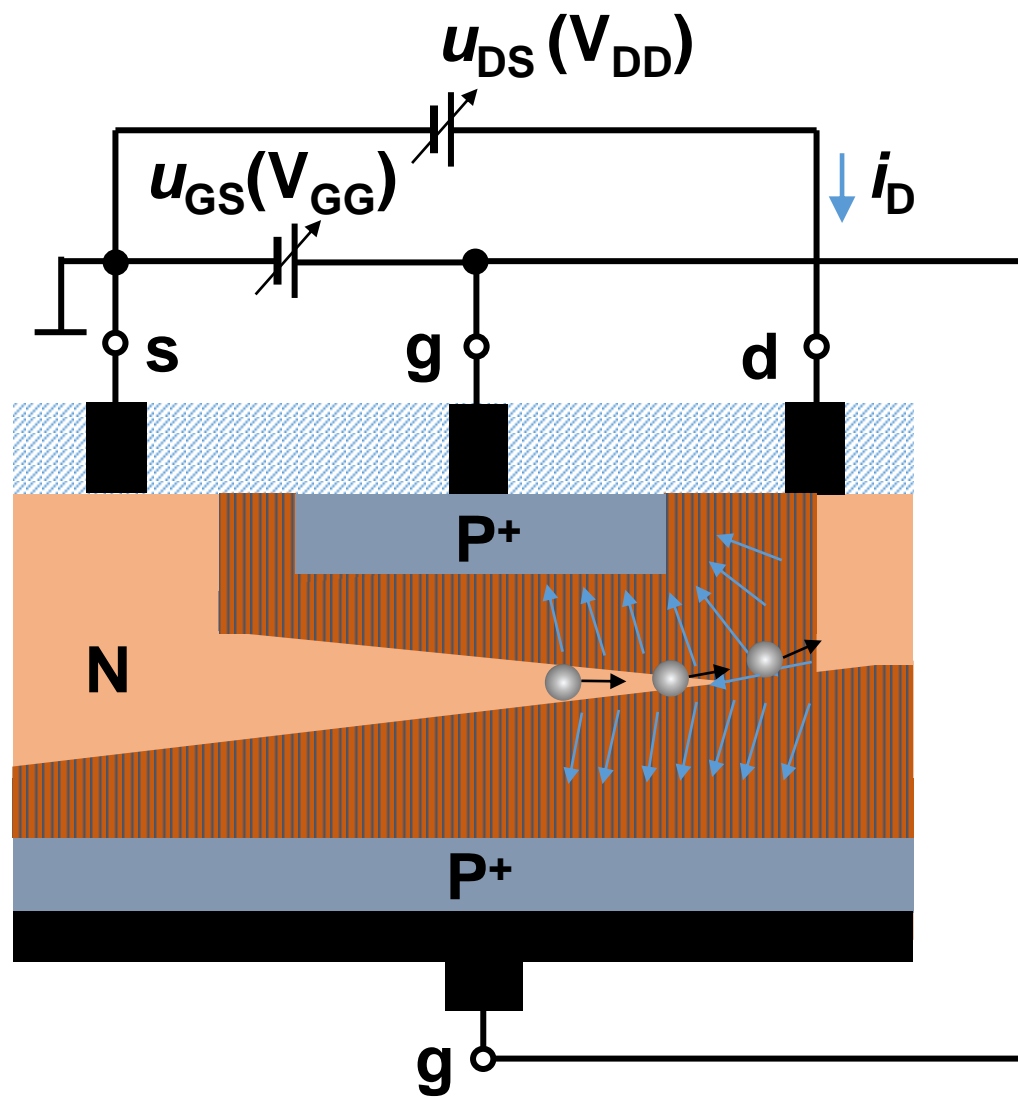
When $u_{DS} > |U_{GS(off)}|$:

i_D reaches the maximum value and does not increase with u_{DS}

Pinch-off region becomes wider and longer
夹断区延长

Q: Why there is still current when DS channel is pinched off?





$$3) u_{GS} < 0, u_{DS} > 0$$

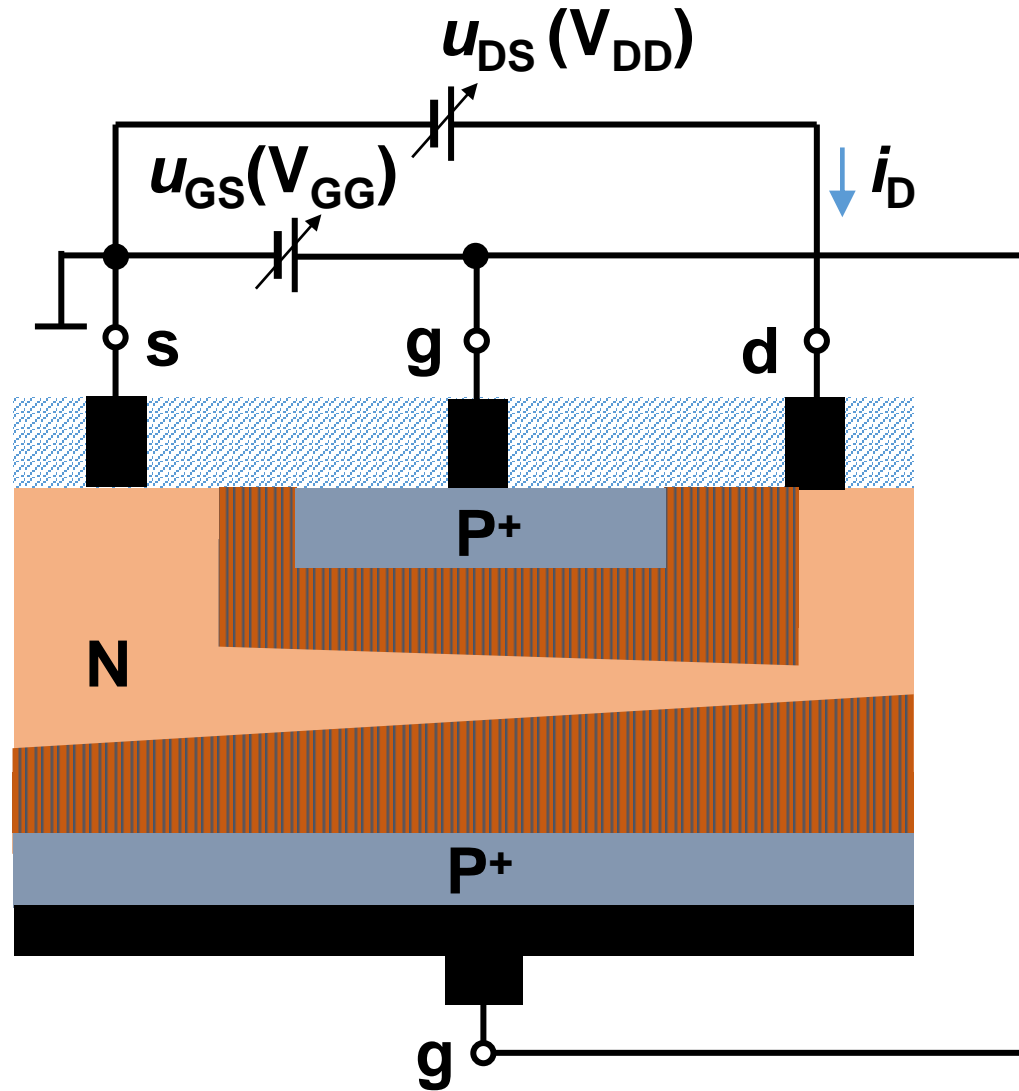
u_{DS} and u_{GS} will modify the channel shape together

When $u_{DS} = |U_{GS(off)}| + u_{GS}$

or $u_{DG} = |U_{GS(off)}|$

or $u_{GD} = U_{GS(th)}$

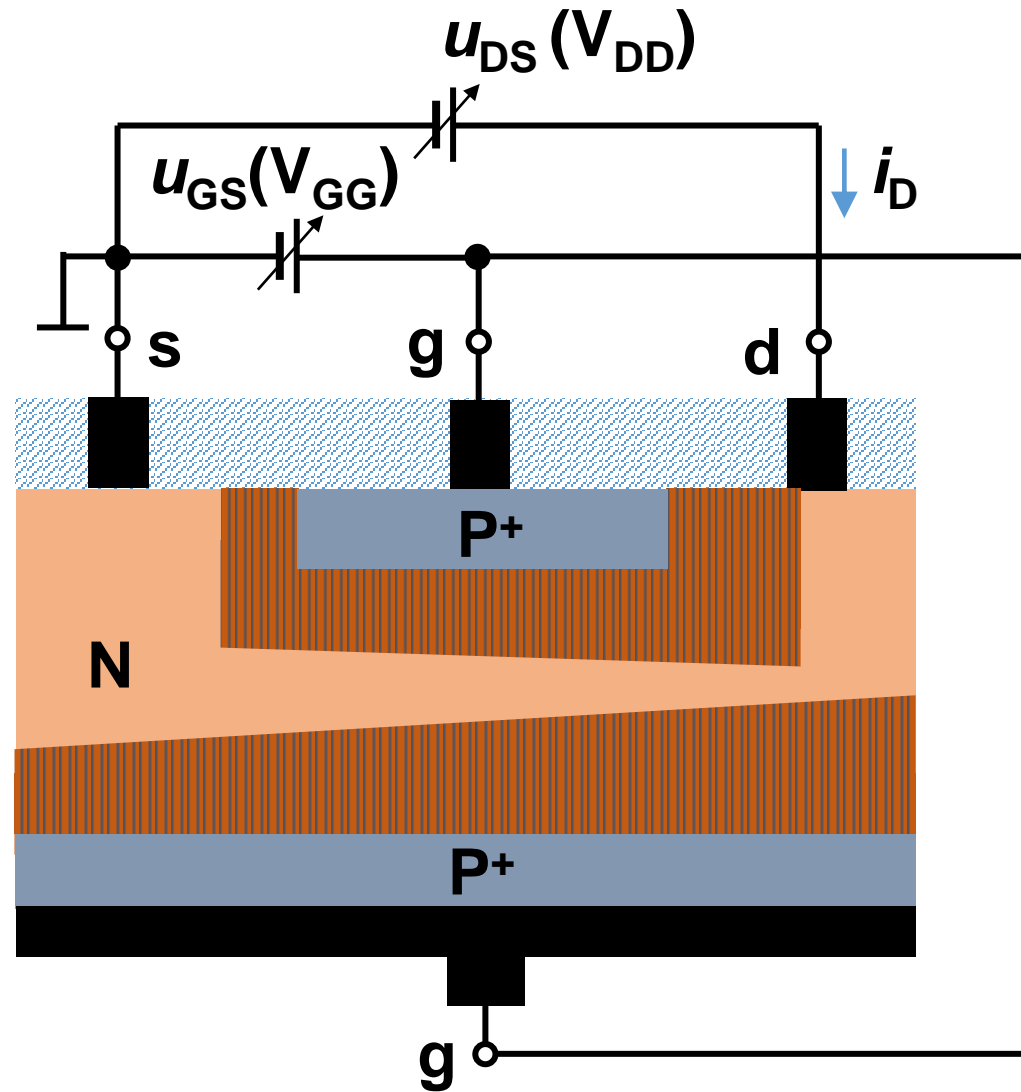
The channel begins to pinch off



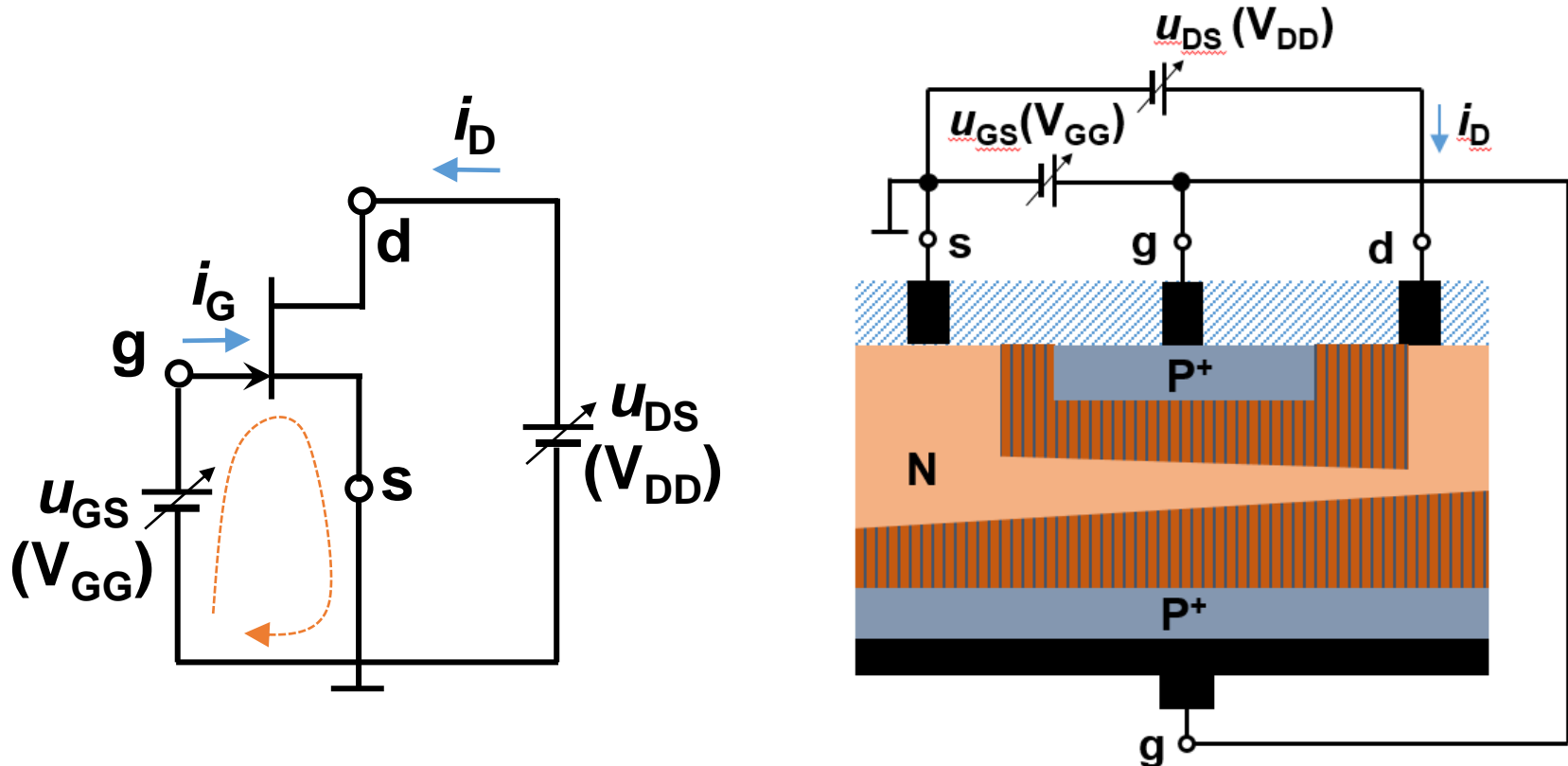
Important notes:

$u_{GS} > 0$ and $u_{DS} < 0$
are not allowed in N-
type JFET

Because depletion region
will come thin, and leakage
current between gate and
drain is very large.



JFET: I-V characteristics



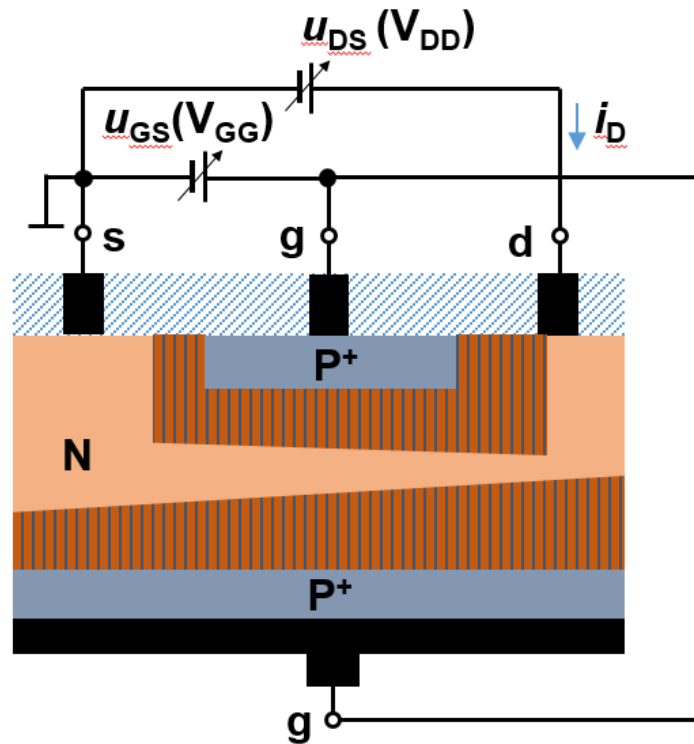
Input circuit: $i_G \approx 0$

Extremely high input resistance

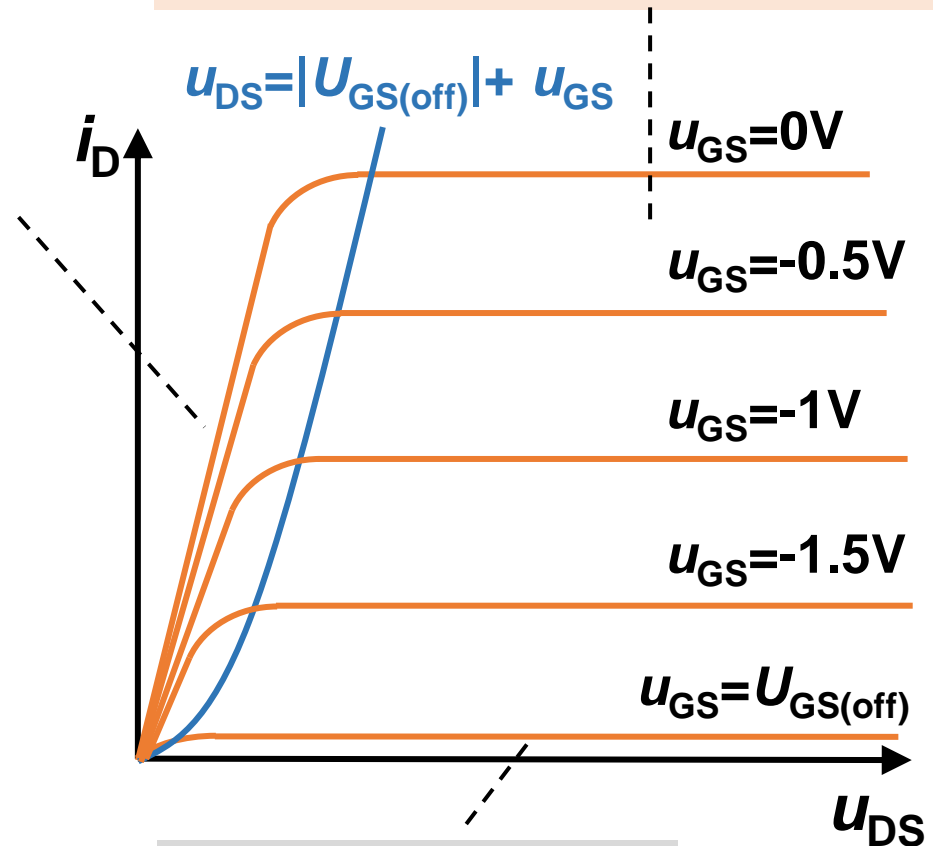
Output I-V curve

$$i_D = f(u_{DS})|_{u_{GS}=\text{constant}}$$

Variable resistor region
可变电阻区



Constant current region
恒流区



Cut-off region
夹断/截止区

Variable resistor region 可变电阻区

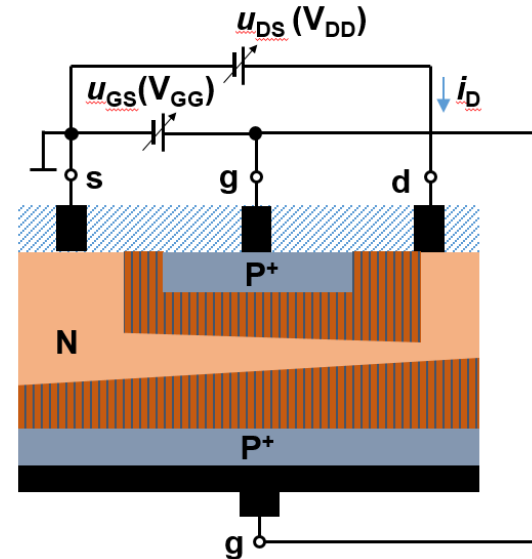
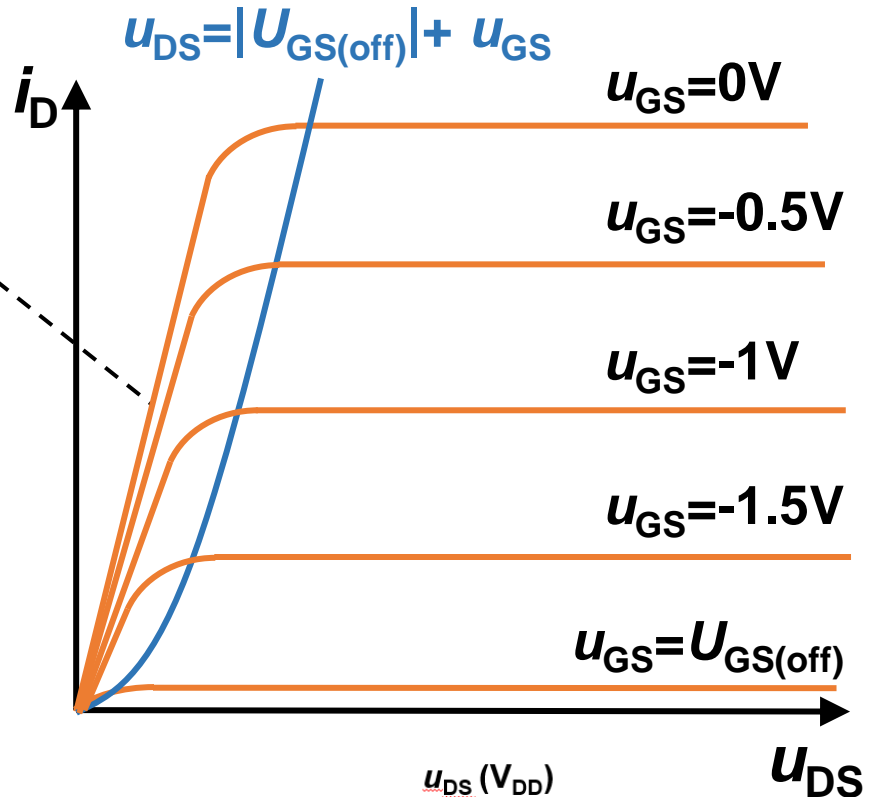
- u_{DS} is small, the channel does not pinch off

$$u_{DS} < |U_{GS(off)}| + u_{GS}$$

$$|u_{GS}| < |U_{GS(off)}|$$

- FET behaves like a resistance-tunable resistor

Tunable by u_{GS}



Constant current region

恒流区

- u_{DS} is large, channel pinches off 沟道预夹断

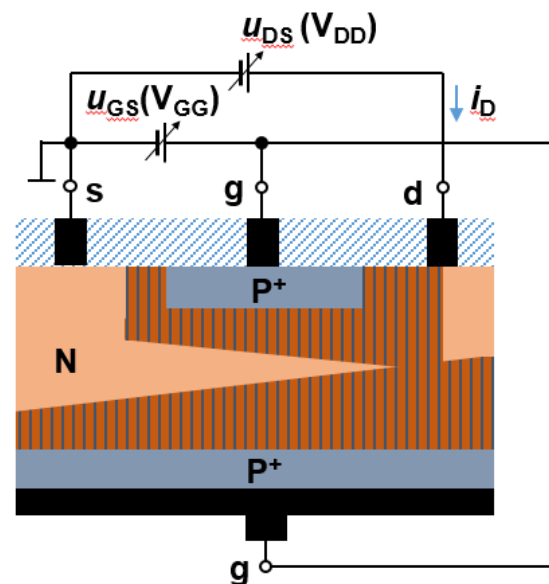
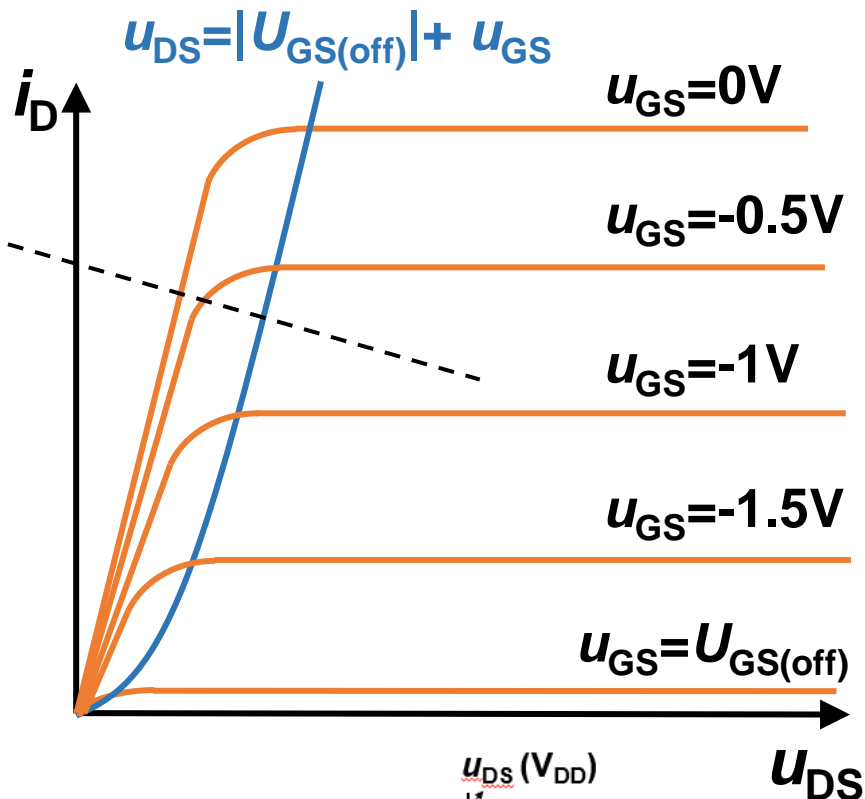
$$u_{DS} \geq |U_{GS(off)}| + u_{GS}$$

$$|u_{GS}| < |U_{GS(off)}|$$

- i_D is almost constant, only depends on u_{GS}

- Also can be called as amplification region

也称作放大区

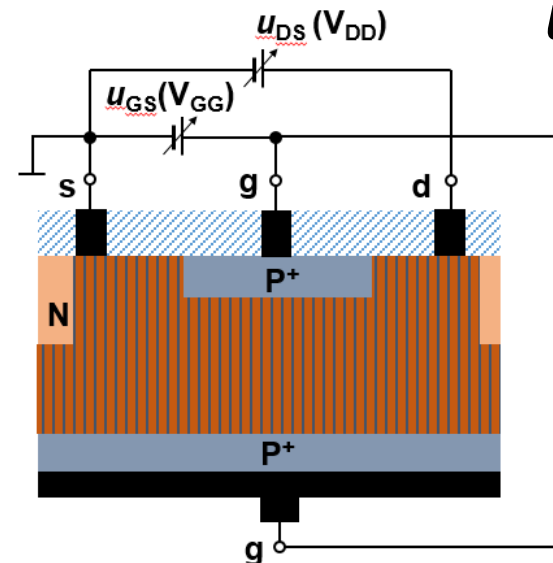
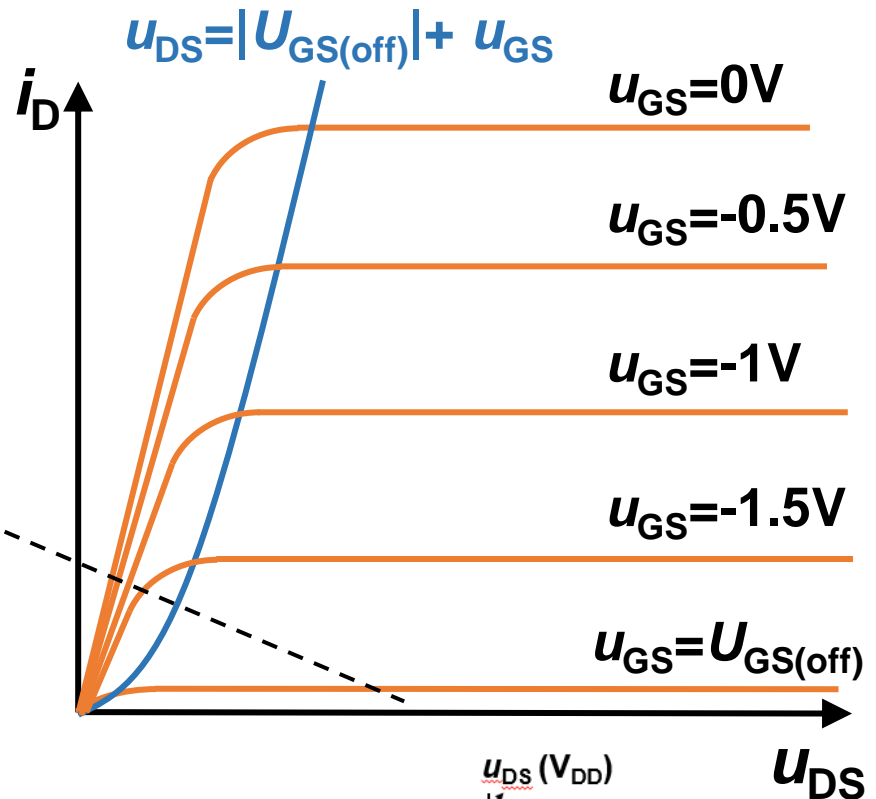


Cut-off region
夹断/截止区

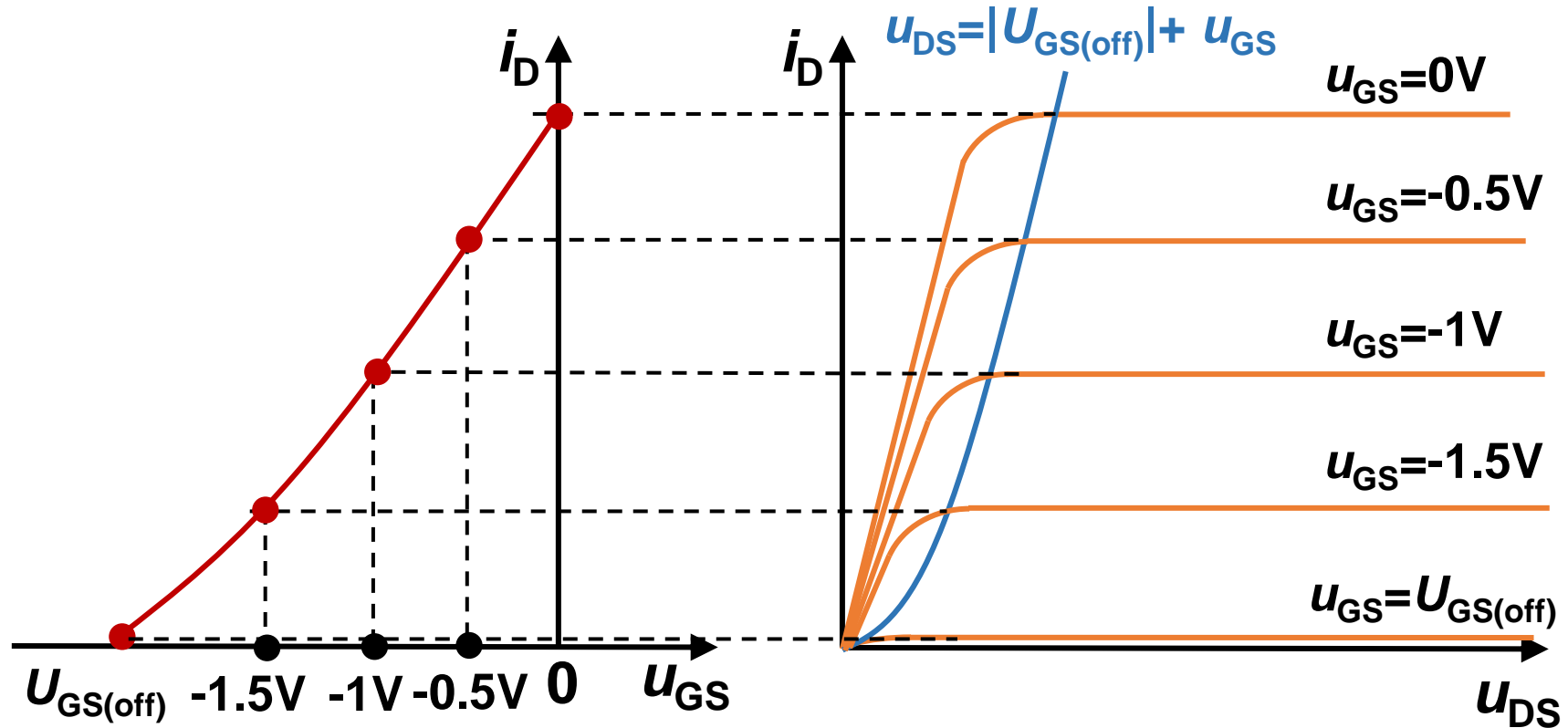
□ Channel fully pinches off

$$|u_{GS}| > |U_{GS(off)}|$$

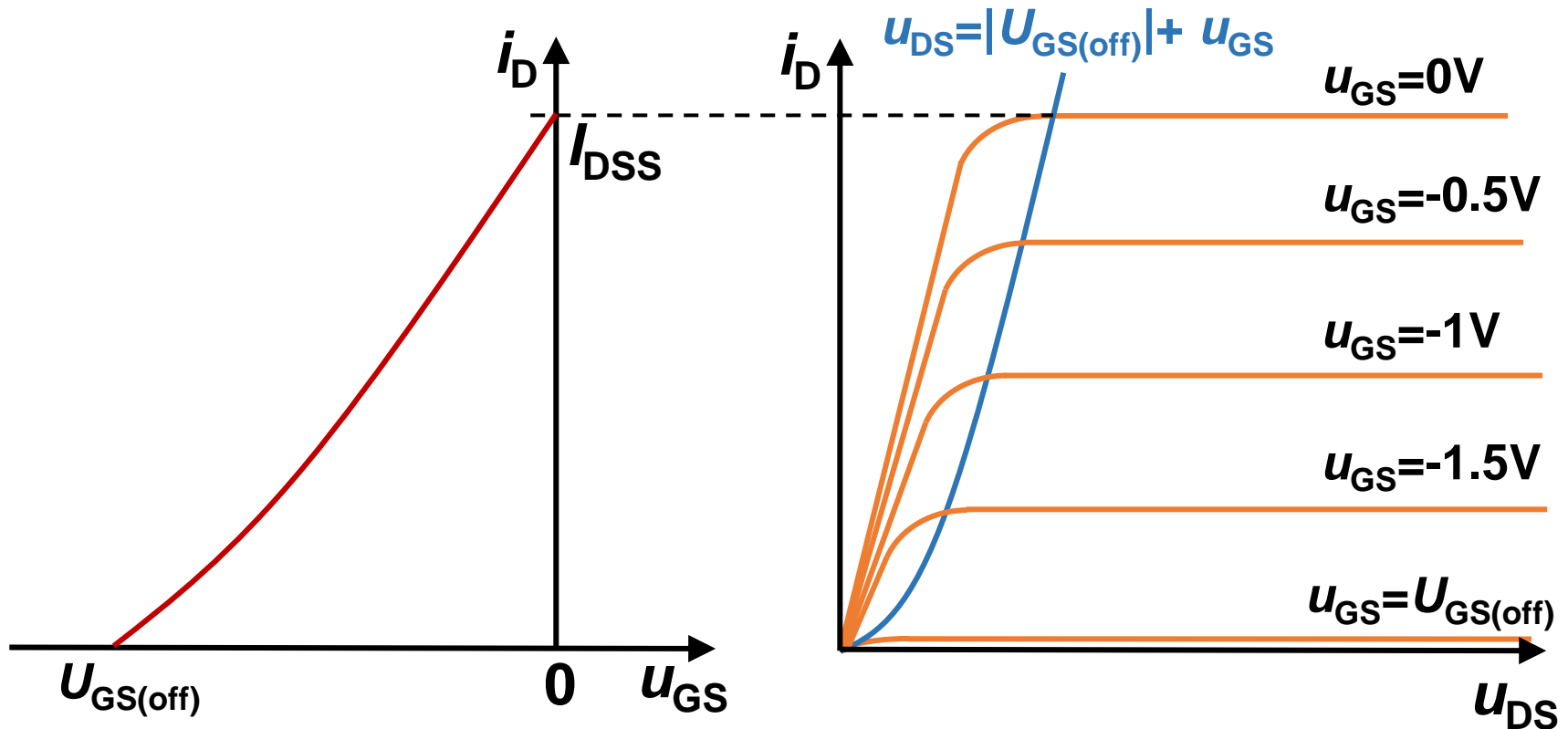
$$\square i_D \approx 0$$



Transfer curve 转移特性曲线 $i_D = f(u_{GS})|_{u_{DS}=\text{constant}}$



- In constant-current region, the transfer curves are independent of u_{DS}
- In variable resistor region, the transfer curves depend on u_{DS}

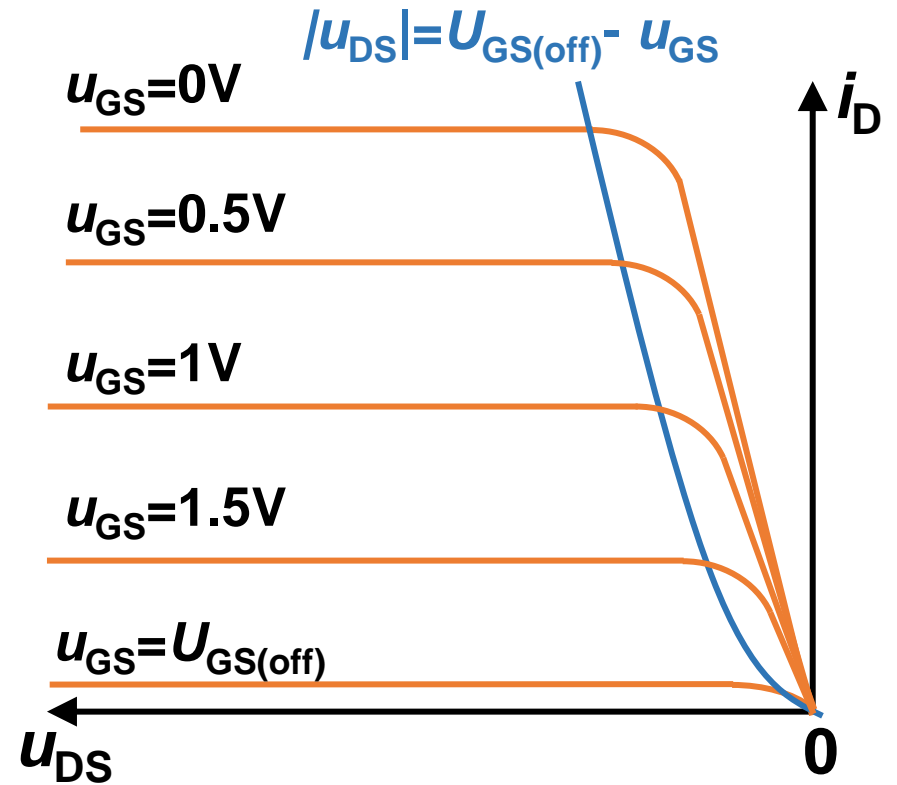
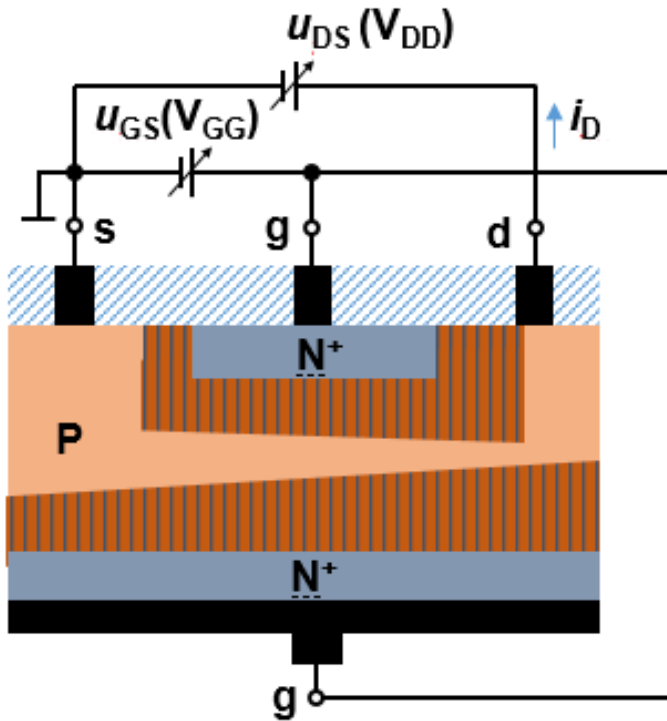


At constant-current region:

$$i_D = I_{DSS} \left(1 - \frac{u_{GS}}{U_{GS(off)}} \right)^2 \quad (U_{GS(off)} < u_{GS} < 0)$$

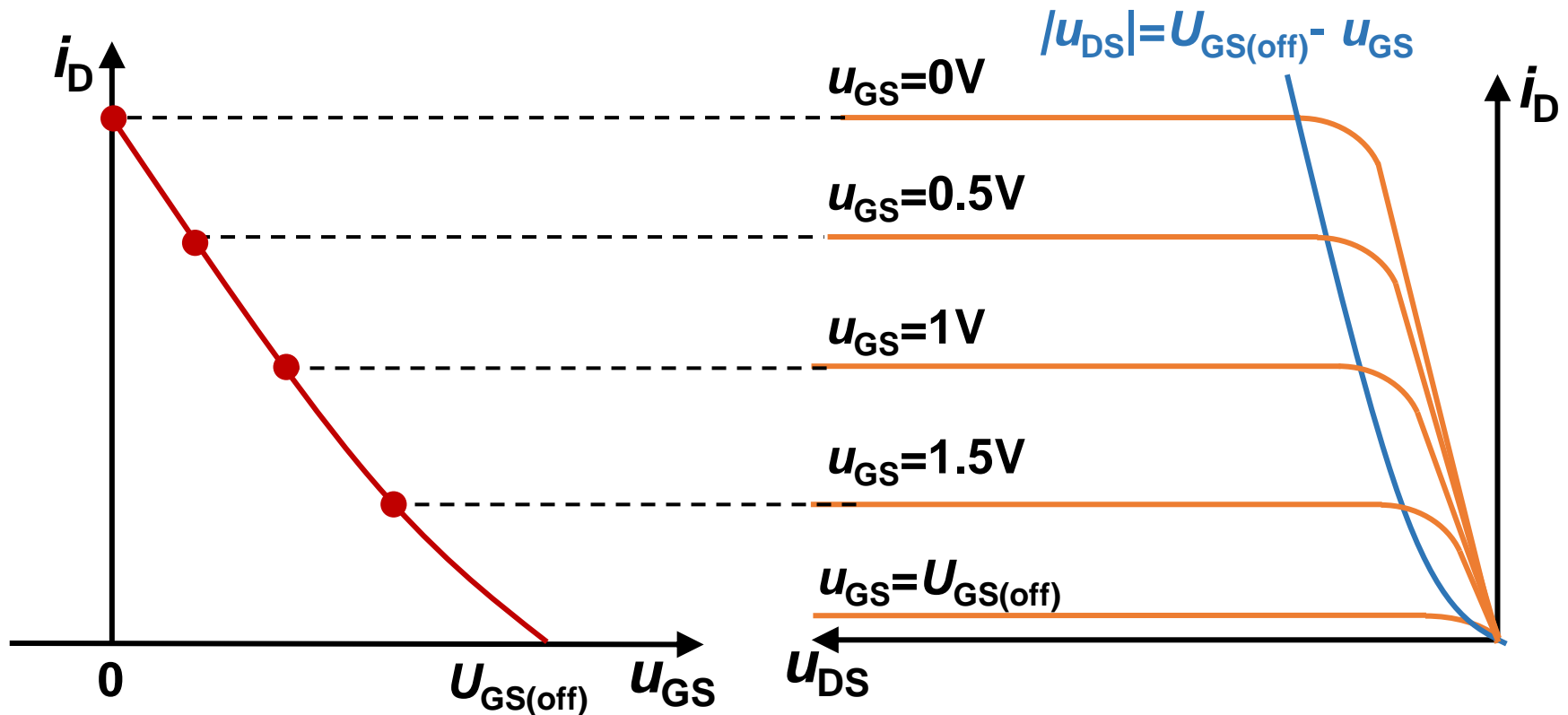
I_{DSS} is the drain current at $u_{GS}=0$, $u_{DS} > |U_{GS(off)}|$

For P-type JFET



For P-type JFET

Transfer curve 转移特性曲线 $i_D = f(u_{GS})|_{u_{DS}=\text{constant}}$



JFET: Key parameters

□ DC parameters 直流参数

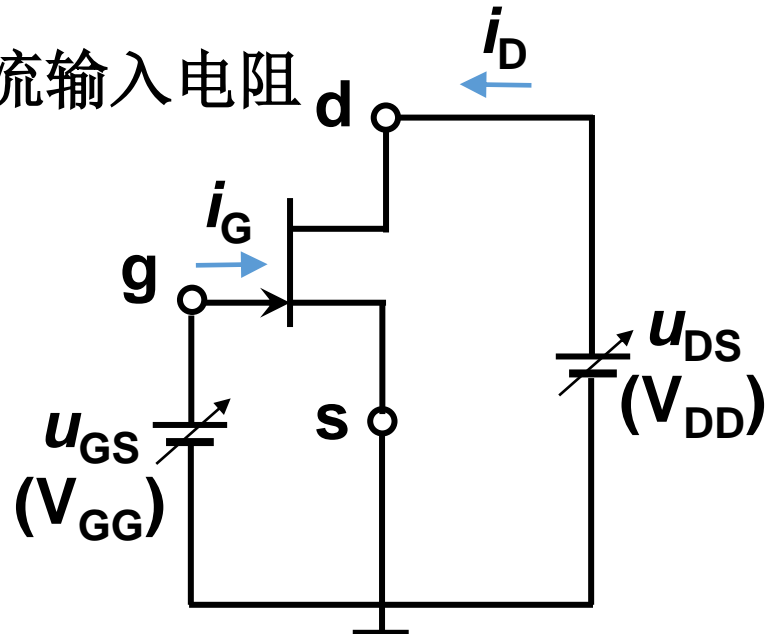
□ 1) Pinch-off voltage $U_{GS(off)}$ 夹断电压

□ 2) Drain saturation current I_{DSS} 漏极饱和电流

I_{DSS} : The drain current at $u_{GS}=0$, $u_{DS}>|U_{GS(off)}|$

□ 3) DC Input resistance R_{GS} 直流输入电阻

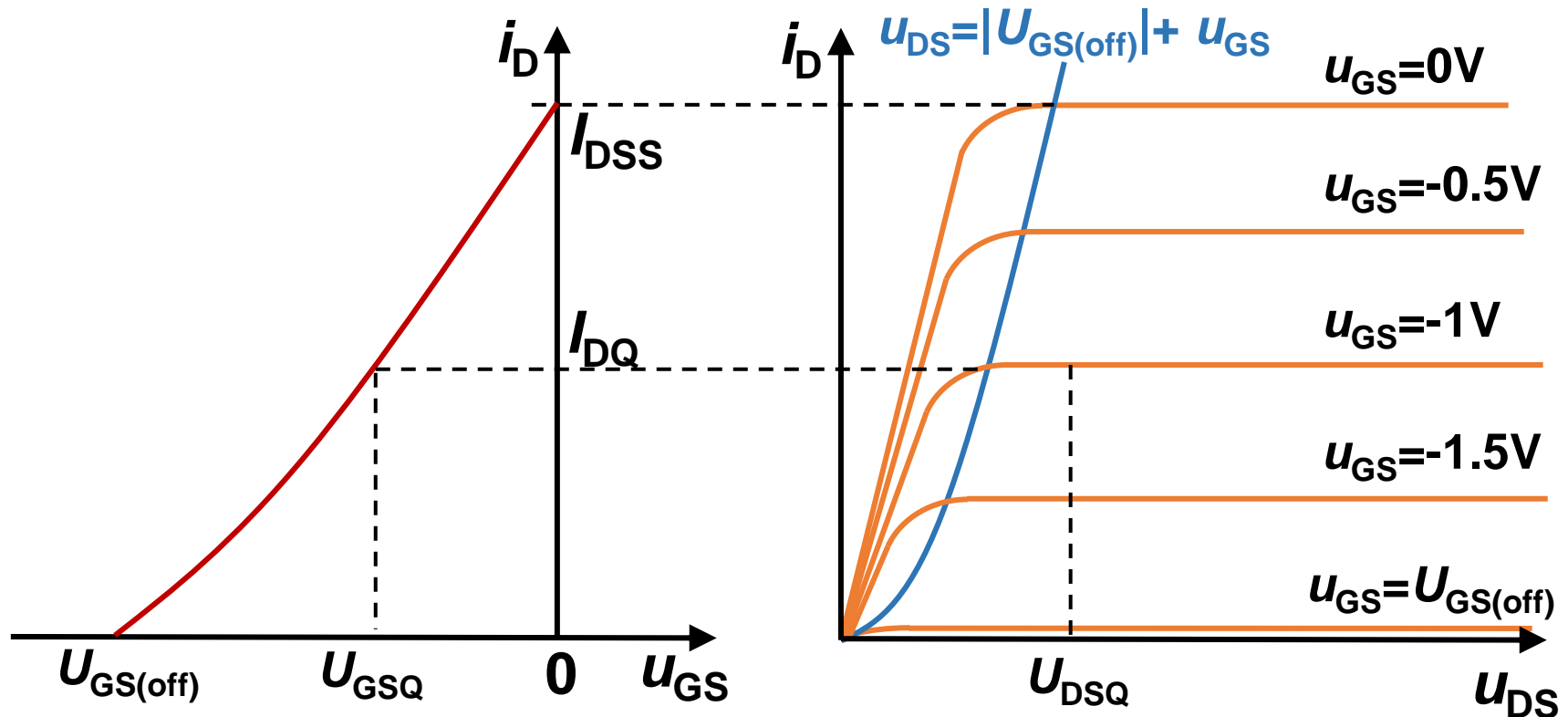
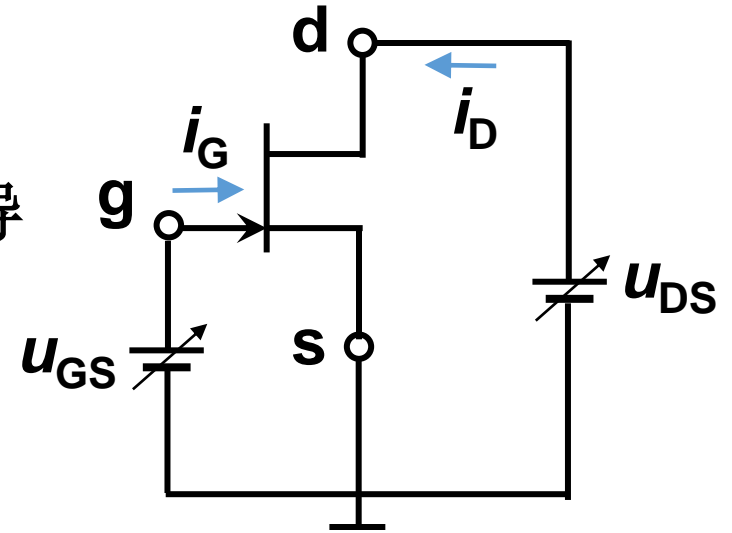
$$R_{GS} = \frac{U_{GS}}{I_G} \bigg|_{u_{DS}=0, U_{GS}=\text{constant}}$$



□ AC parameters 交流参数

□ 1) Transconductance g_m 互导/跨导

$$g_m = \left. \frac{di_D}{du_{GS}} \right|_{u_{DSQ}, u_{GSQ}, I_{DQ}}$$



□ AC parameters 交流参数

□ 1) Transconductance g_m 互导/跨导

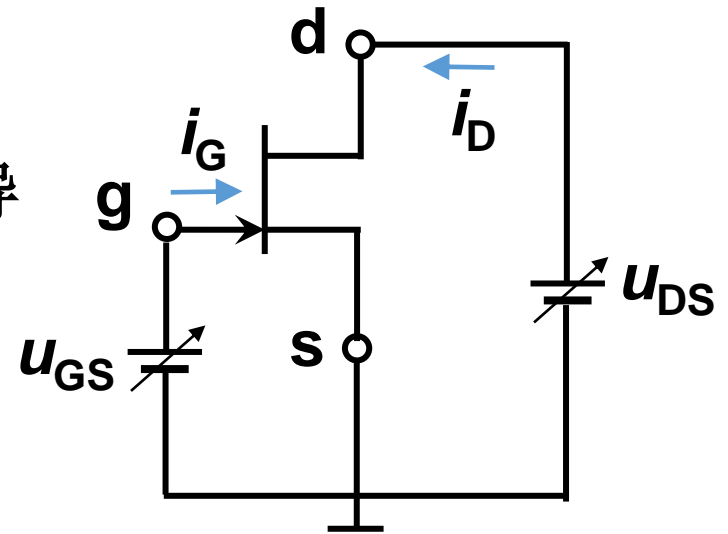
$$g_m = \left. \frac{di_D}{du_{GS}} \right|_{u_{DSQ}, u_{GSQ}, I_{DQ}}$$

At constant-current region:

$$i_D = I_{DSS} \left(1 - \frac{u_{GS}}{U_{GS(off)}} \right)^2$$

$$g_m = -\frac{2}{U_{GS(off)}} \sqrt{I_{DSS} I_{DQ}}$$

Larger I_{DQ} , larger g_m



2) There exists capacitance between drain, source and gate: C_{gs} , C_{gd} , C_{ds}

In high frequency circuits, we need to consider C_{gs} , C_{gd} , C_{ds}

Q1: As shown in the figure, FET has $U_{GS(off)} = -5V$;
Ask: In the three situations listed below, FET
works in which region?

1) $u_{GS} = -8V, u_{DS} = 4V$

2) $u_{GS} = -3V, u_{DS} = 4V$

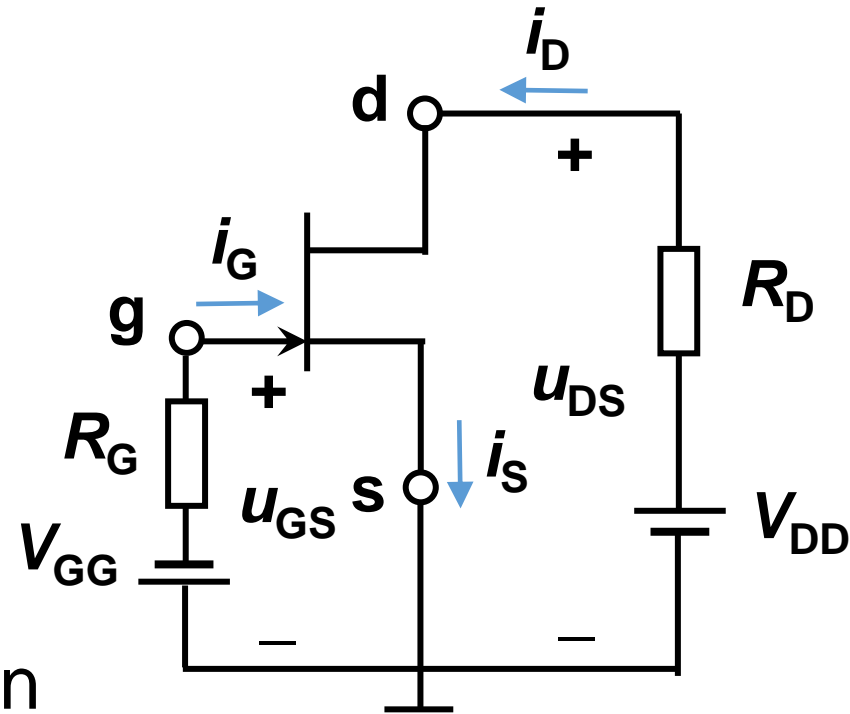
3) $u_{GS} = -3V, u_{DS} = 1V$

Answer:

1) $u_{GS} < U_{GS(off)}$, in cut-off region

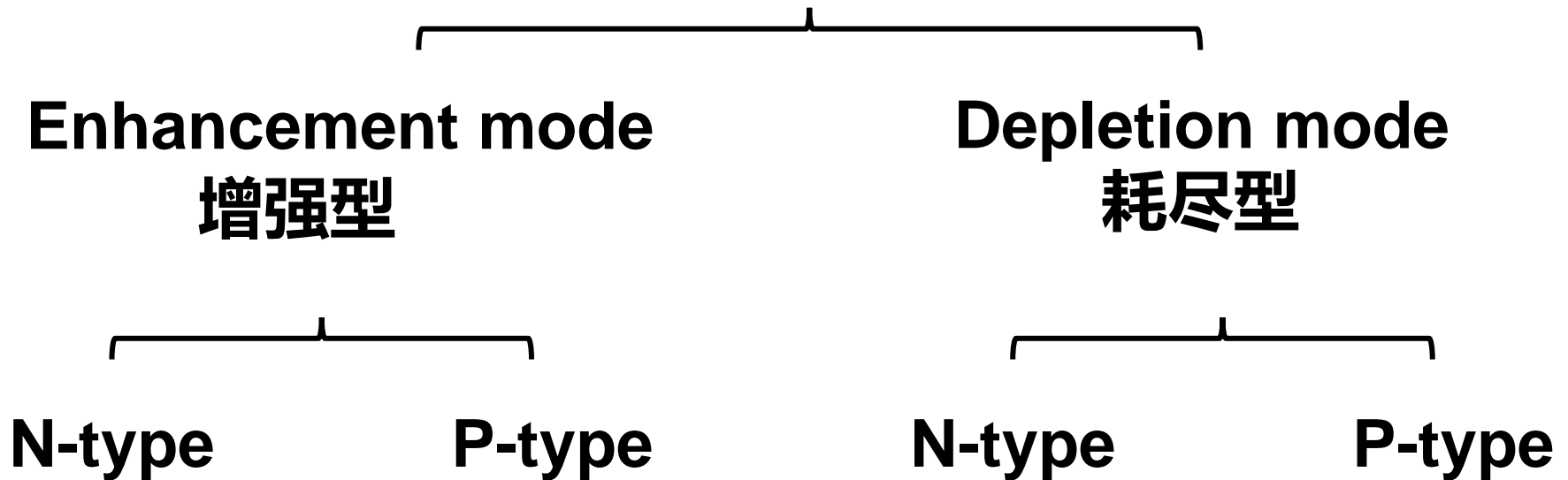
2) $u_{DS} > |U_{GS(off)}| + u_{GS}$, in constant-current region

3) $u_{DS} < |U_{GS(off)}| + u_{GS}$, in variable resistor region

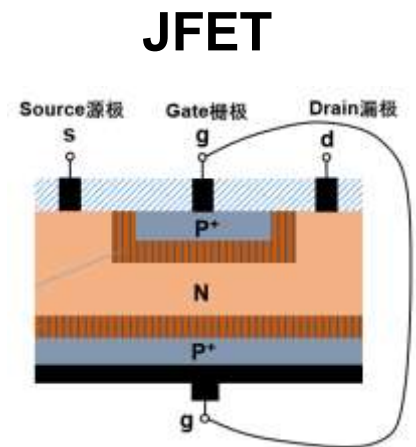
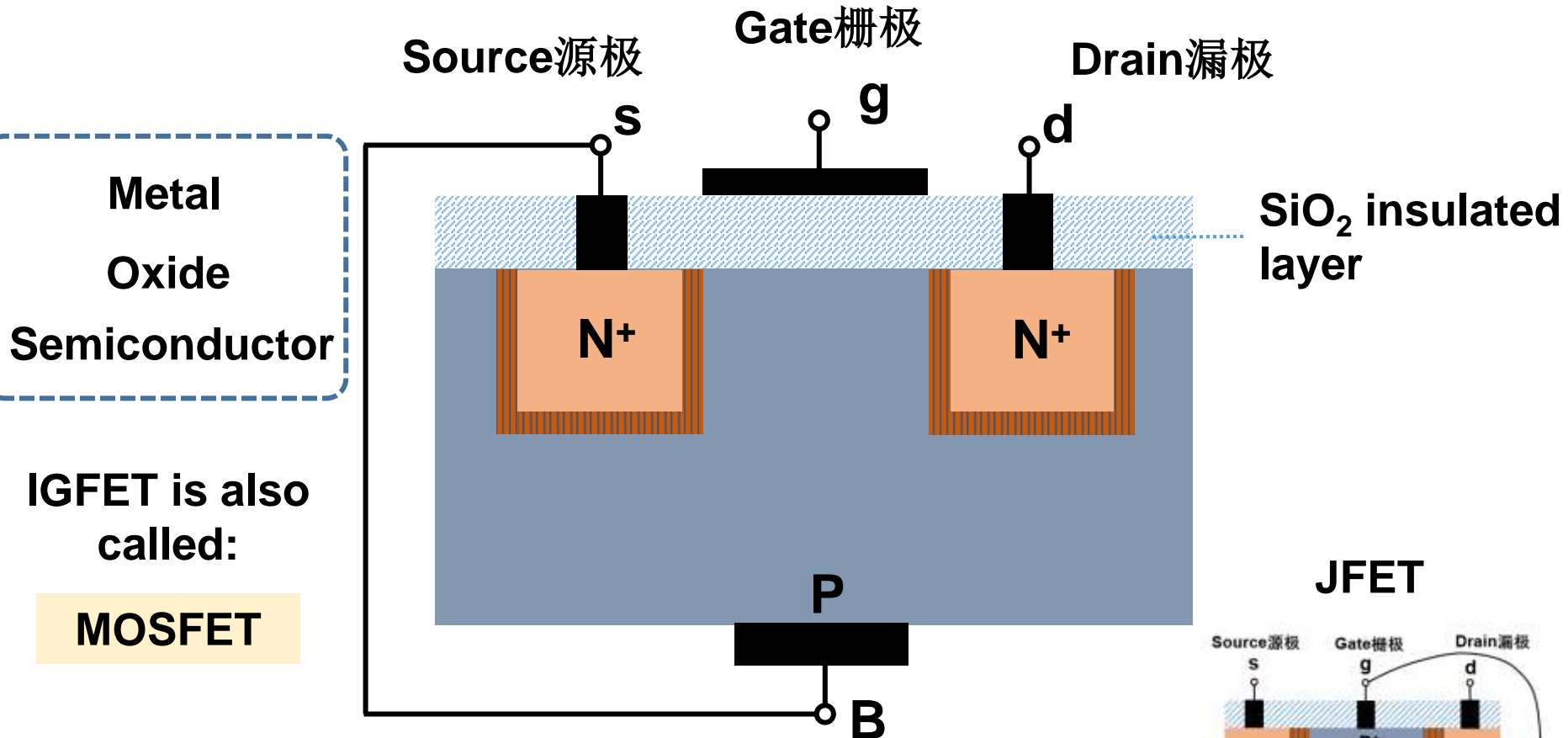


IGFET

IGFET (Insulated Gate Field Effect Transistor)
绝缘栅型场效应管



Enhanced N-type IGFET

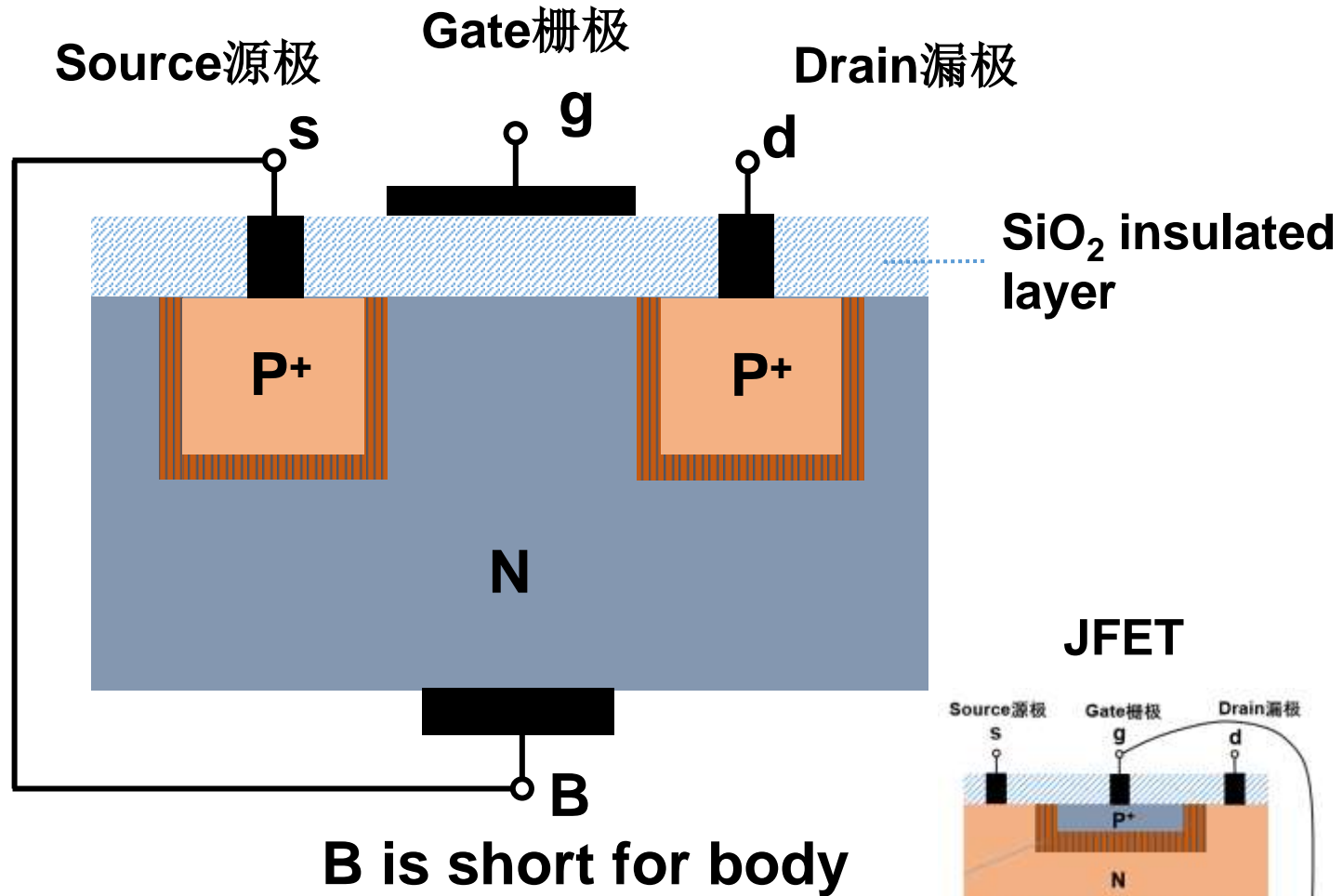


Enhanced P-type IGFET

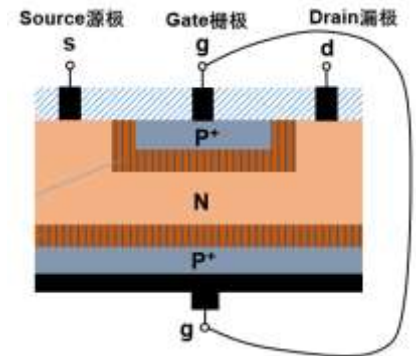
Metal
Oxide
Semiconductor

IGFET is also
called:

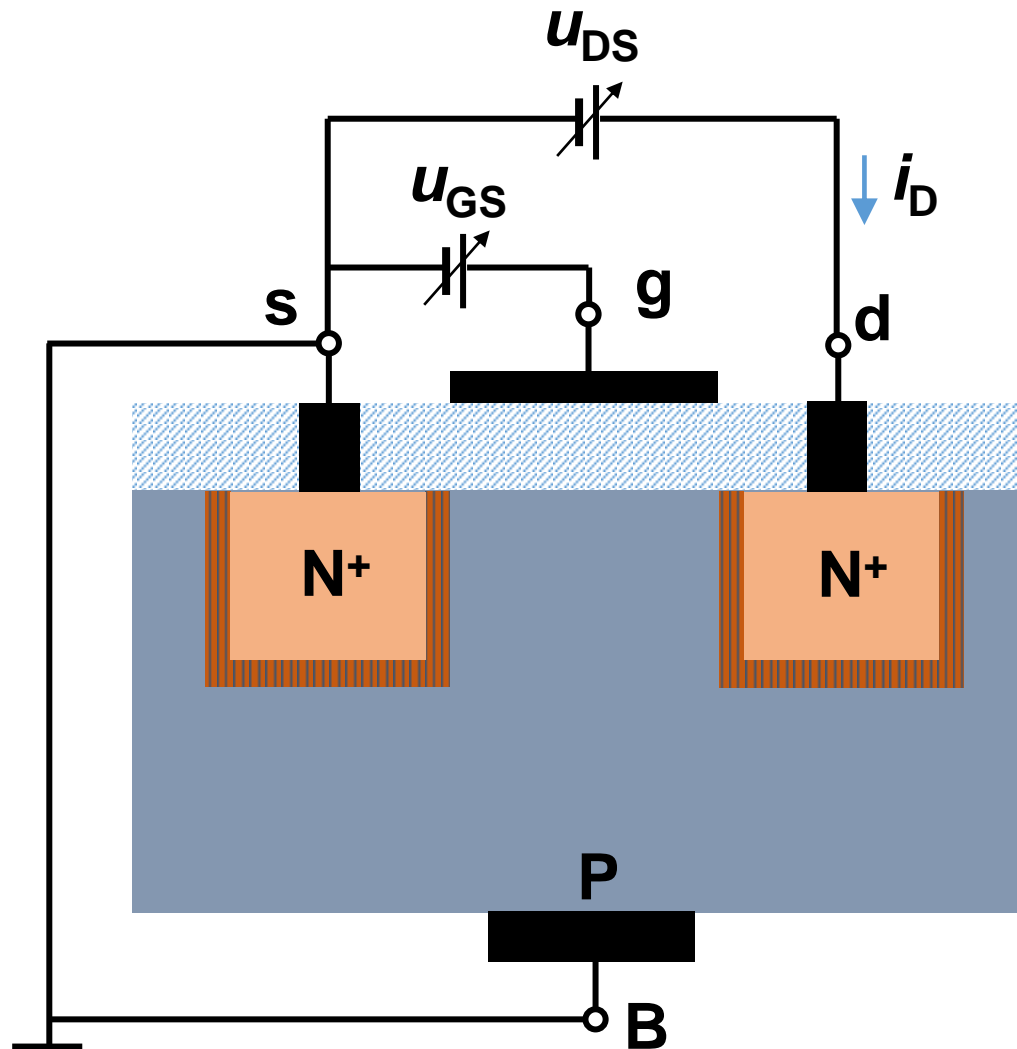
MOSFET



JFET



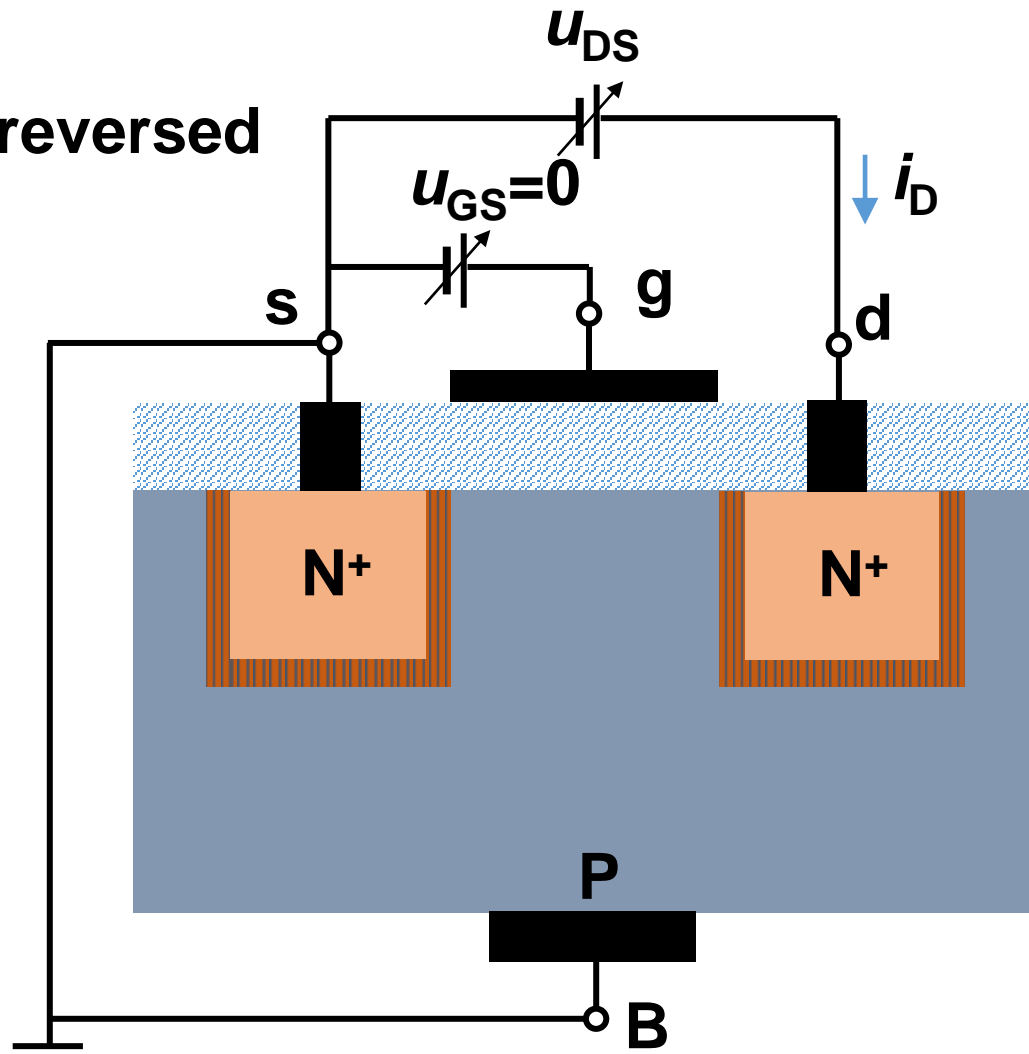
Working principle:



1) $u_{GS} = 0, u_{DS} \neq 0$:

One PN junction is reversed

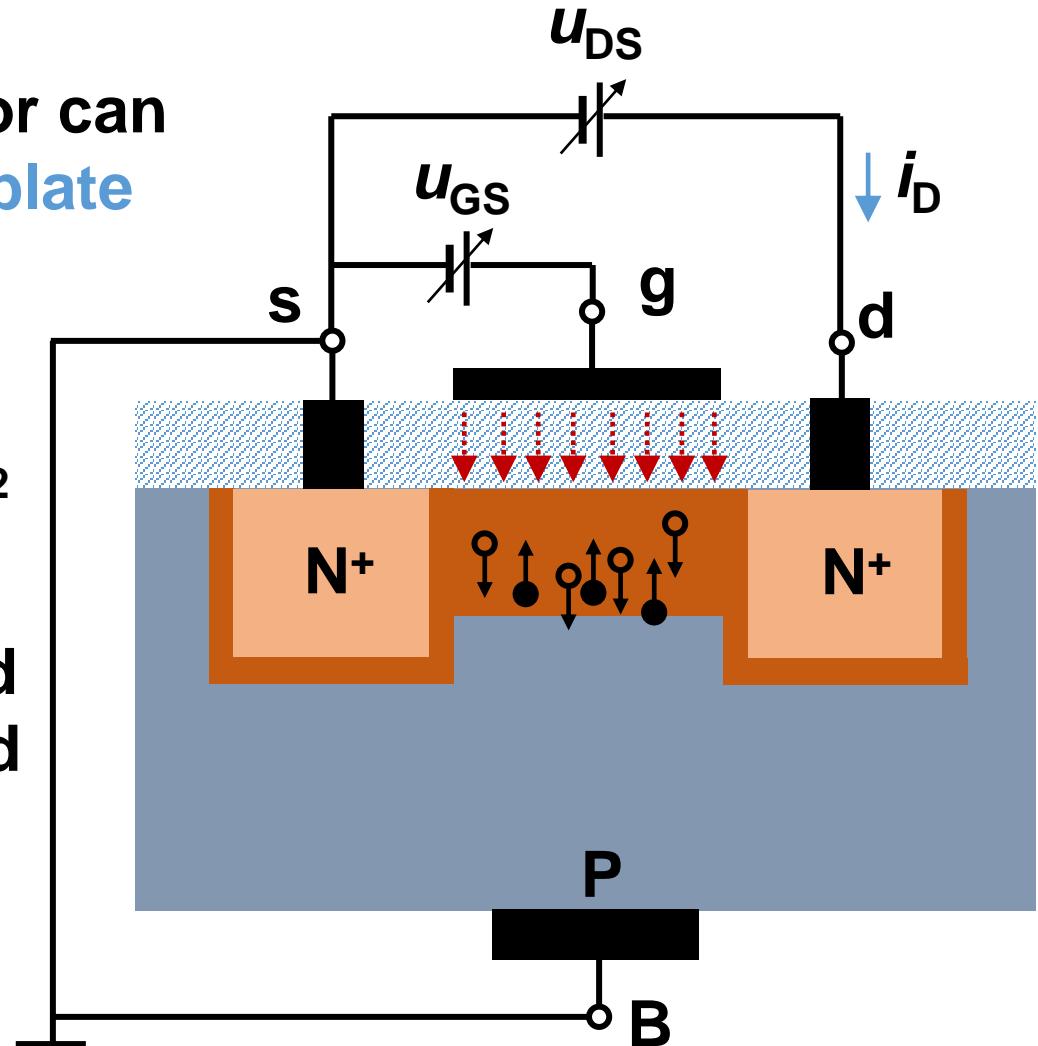
$$i_D = 0$$



2) $u_{GS} > 0, u_{DS} = 0$:

Gate-SiO₂-Semiconductor can be treated as a **parallel-plate capacitor** 平行板电容器

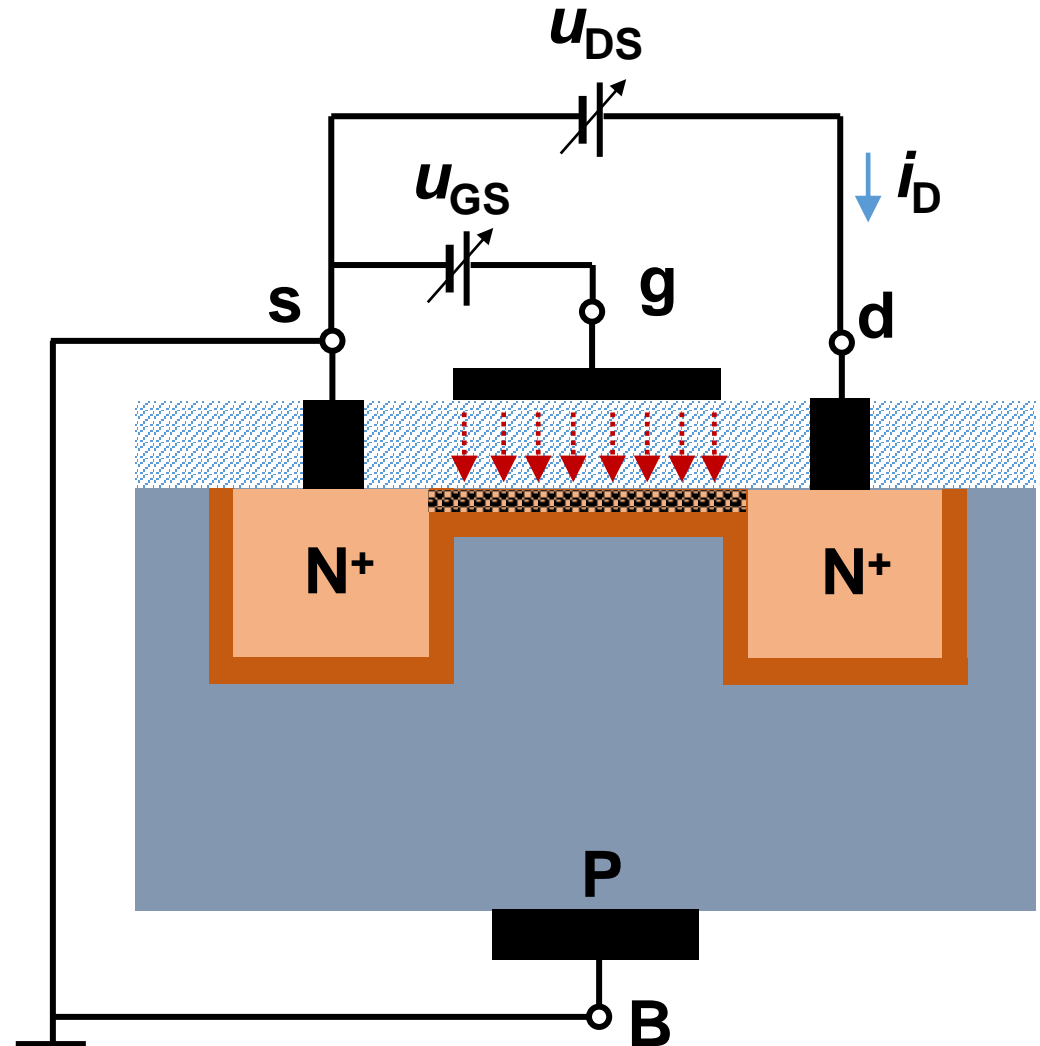
- When $u_{GS} > 0$, electric field is induced in SiO₂ layer
- Electrons are attracted and holes are repulsed to SiO₂ surface



When $u_{GS} = U_{GS(th)} > 0$

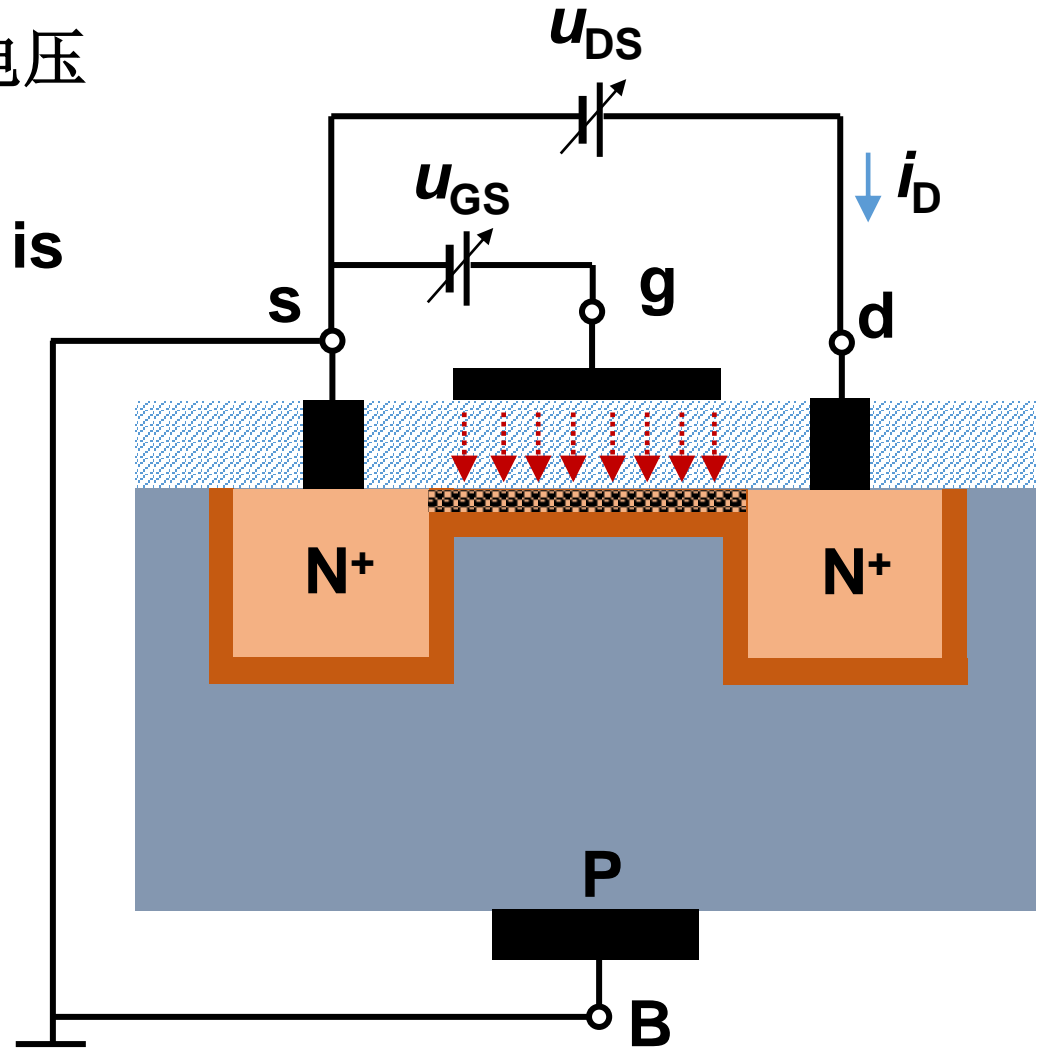
□ A thin conducting layer of electron gas, is formed near SiO_2 surface

□ We call this layer the inversion layer (反型层),



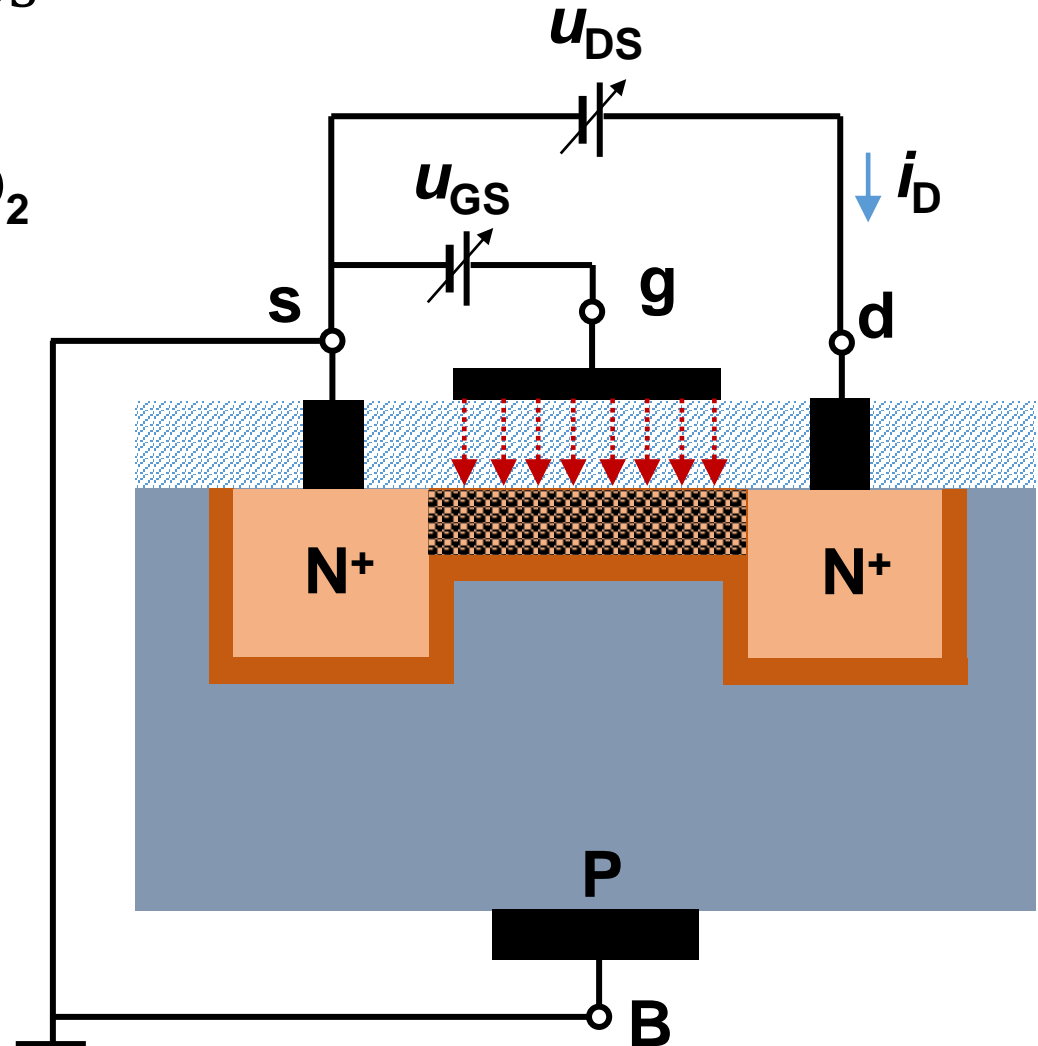
$U_{GS(th)}$ is called the
threshold voltage 开启电压

Enhanced N-type IGFET is
also called NMOSFET



When $u_{GS} > U_{GS(th)}$, $u_{DS} = 0$

- The electric field in SiO_2 is larger
- $u_{GS} \uparrow$, the electron density near SiO_2 is higher
- The current between g and s is even much smaller than that in JFET.



3) $u_{GS} > U_{GS(th)}$, $u_{DS} > 0$

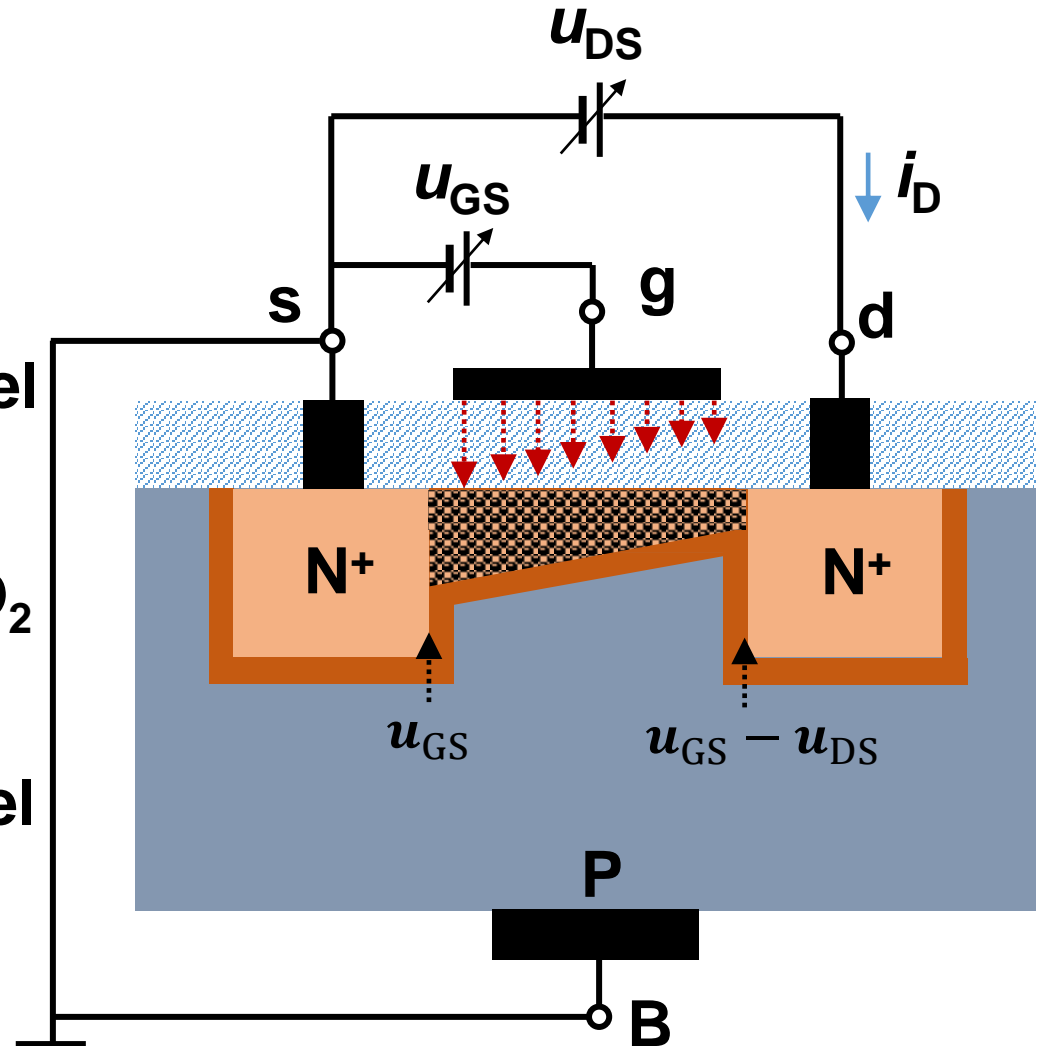
□ $i_D > 0$

□ $u_{DS} \uparrow, i_D \uparrow$

□ The potential of channel near drain is smaller

□ The electric field in SiO_2 near drain is smaller

□ The conducting channel is wedge-shaped 楔形

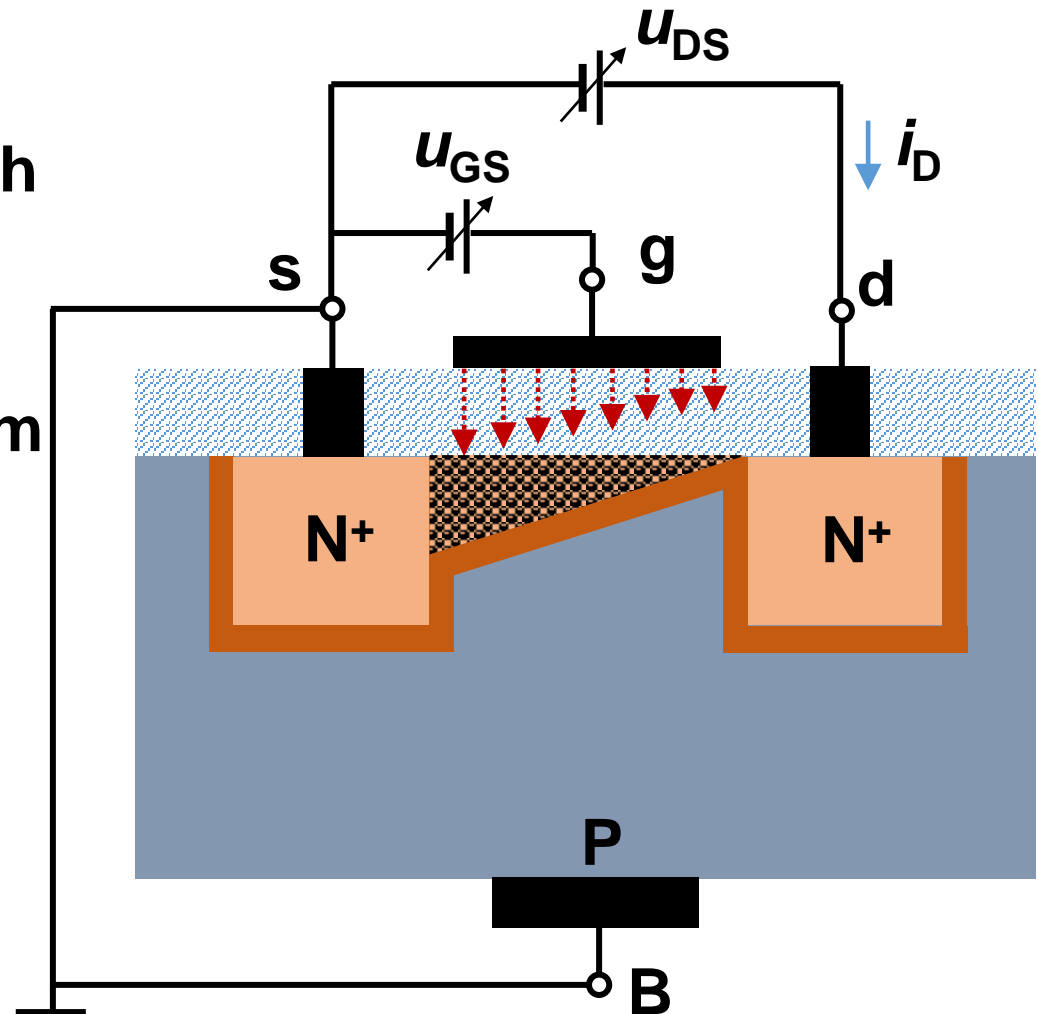


When $u_{DS} = u_{GS} - U_{GS(th)}$ or $[u_{GD} = U_{GS(th)}]$

□ Channel begins to pinch off 沟道预夹断

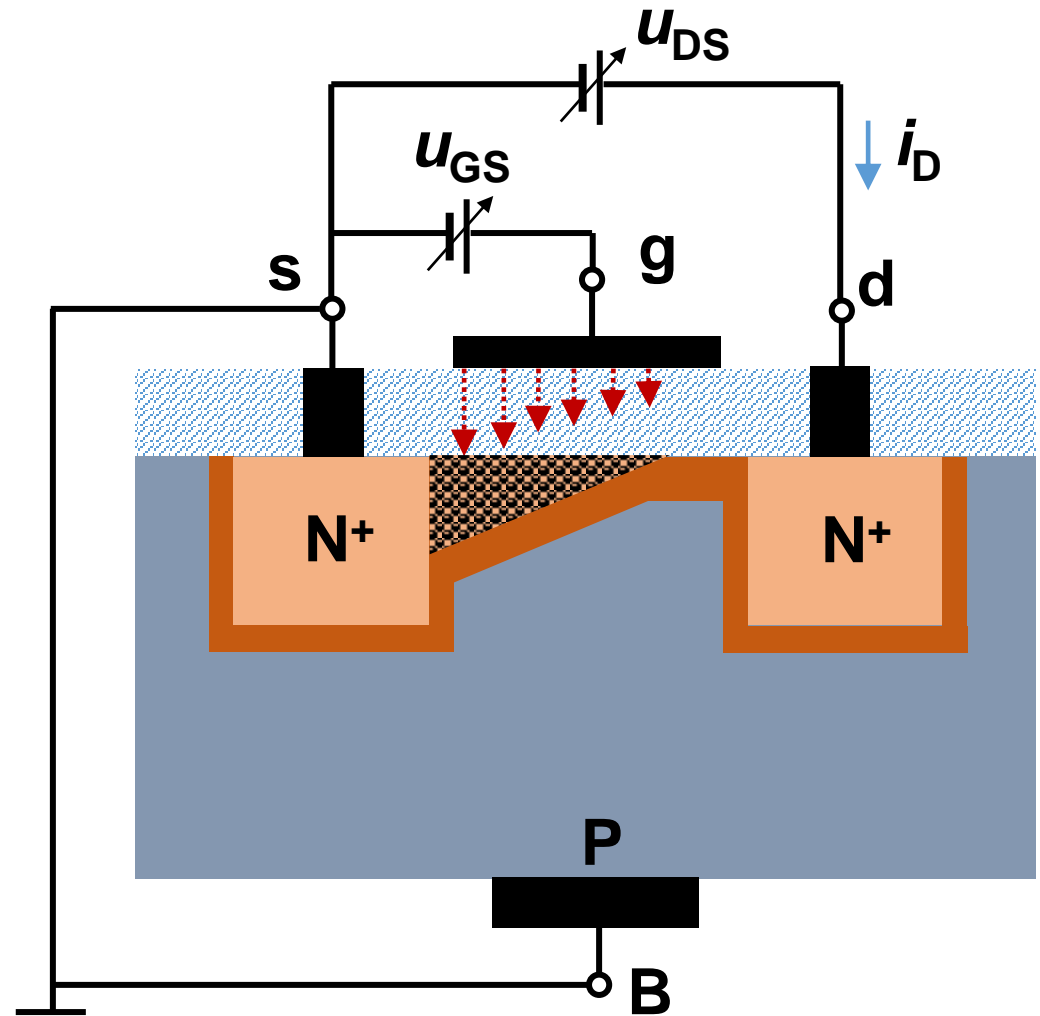
□ i_D reaches the maximum value

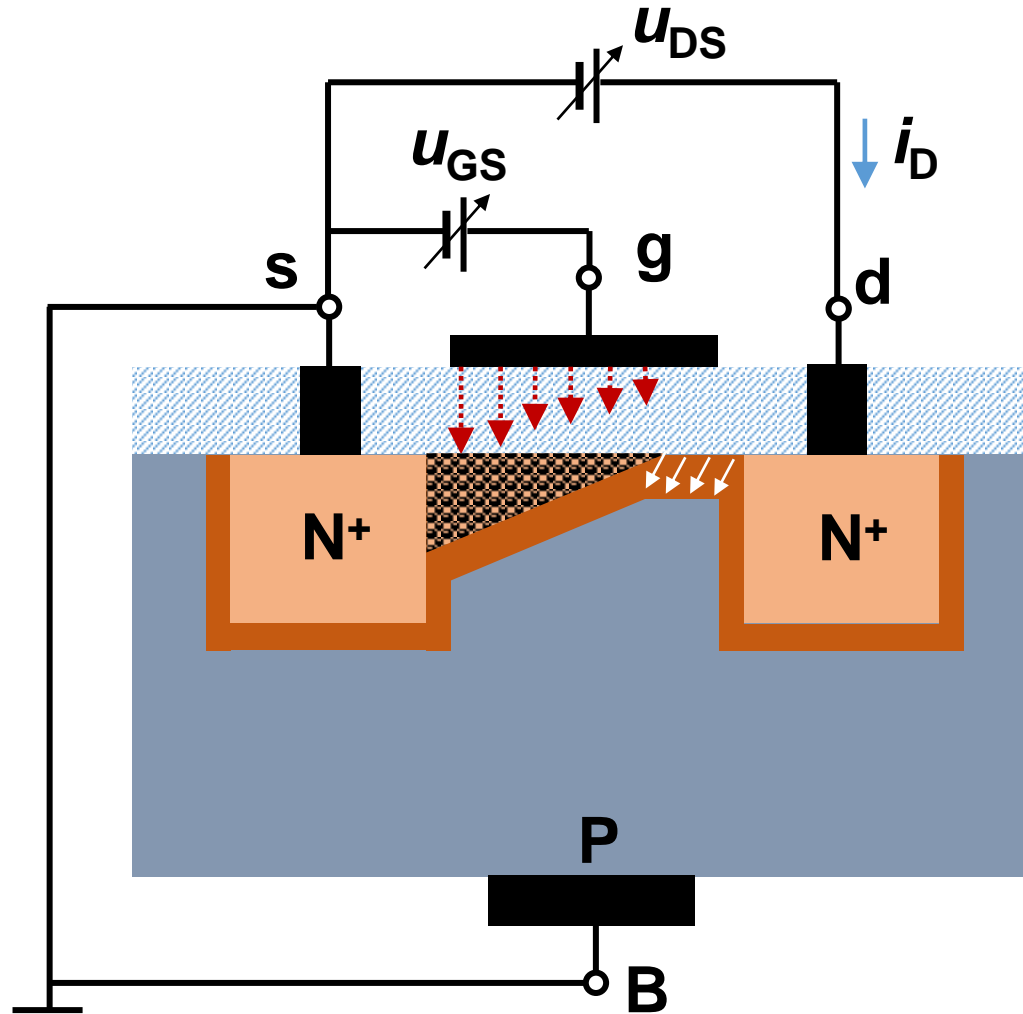
□ NMOS begins to enter the constant current region



When $u_{DS} > u_{GS} - U_{GS(th)}$

- The pinch-off region extends 夹断区延长
- i_D is almost a constant
- NMOS is in constant current region





Electron can pass through the pinch off region.

For enhanced PMOS

- To induce hole inversion layer in N-type Si:

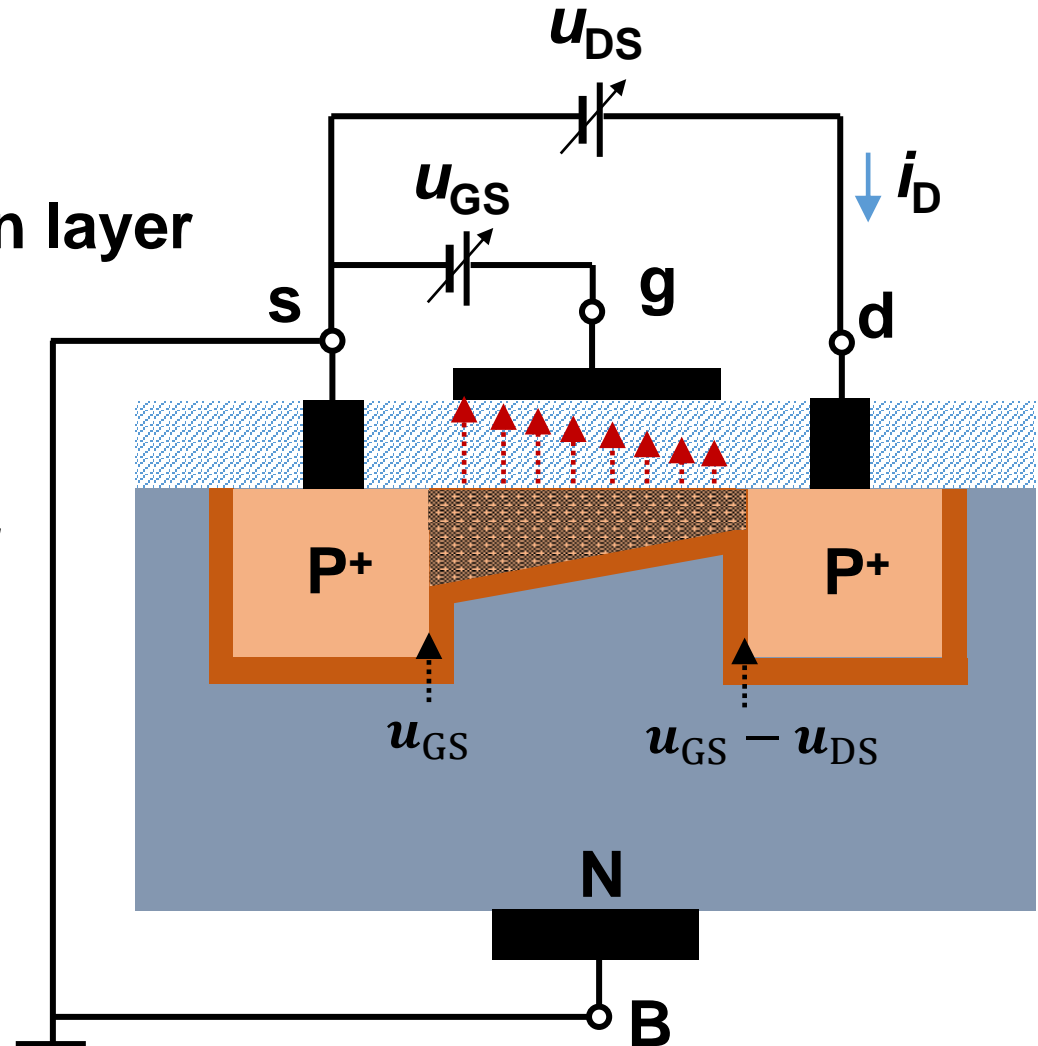
$$U_{GS(th)} < 0$$

- To let channel pinch off

$$u_{DS} < 0$$

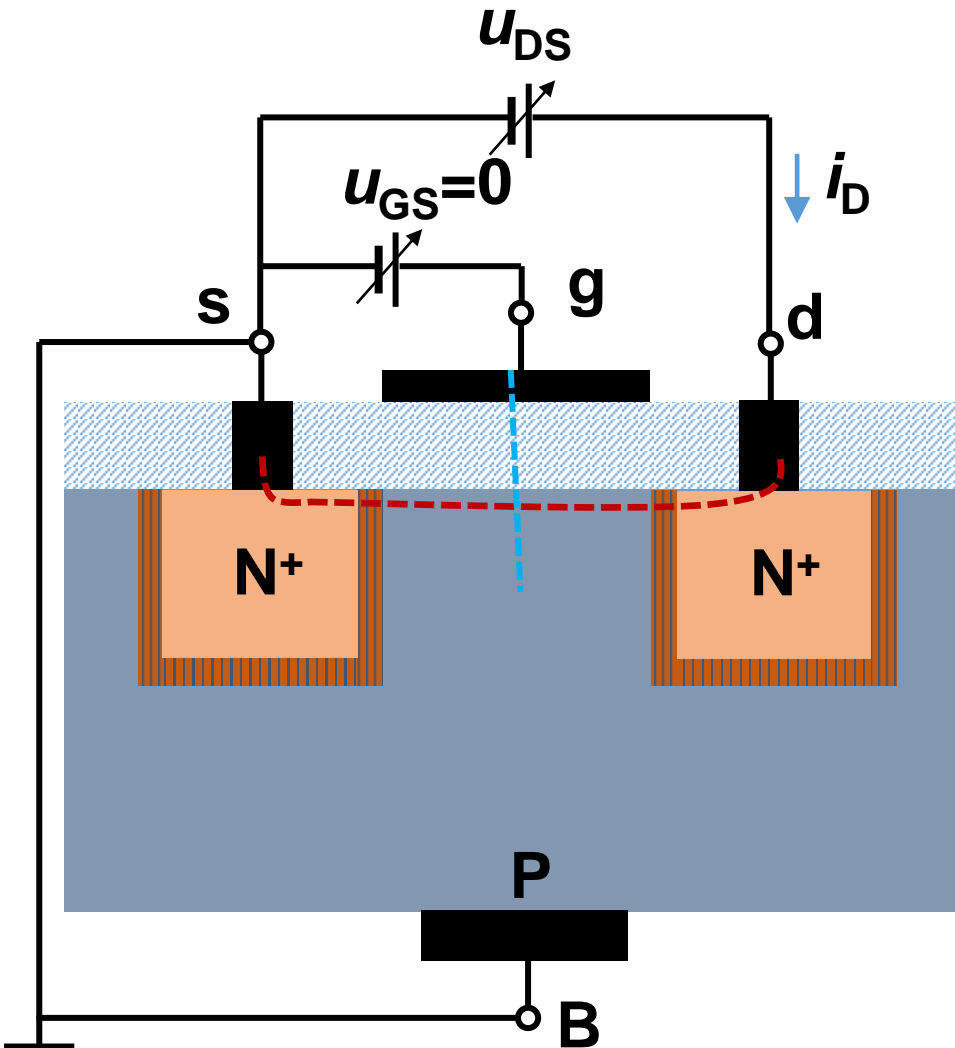
$$u_{DS} = u_{GS} - U_{GS(th)}$$

or $[u_{GD} = U_{GS(th)}]$

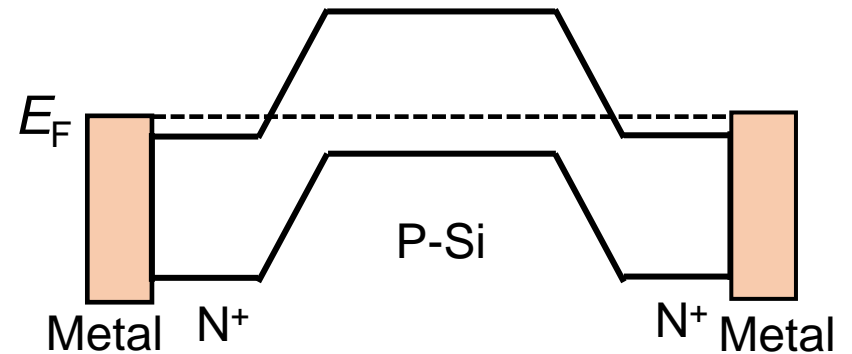


Band diagram of MOSFETs

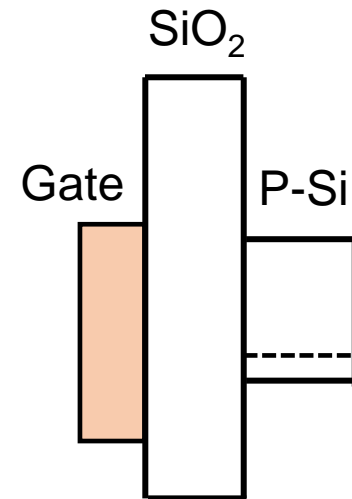
1) $u_{GS} = 0, u_{DS} = 0$:



Band diagram along red line

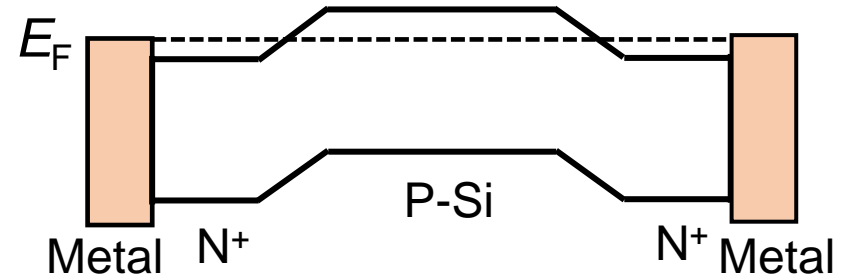
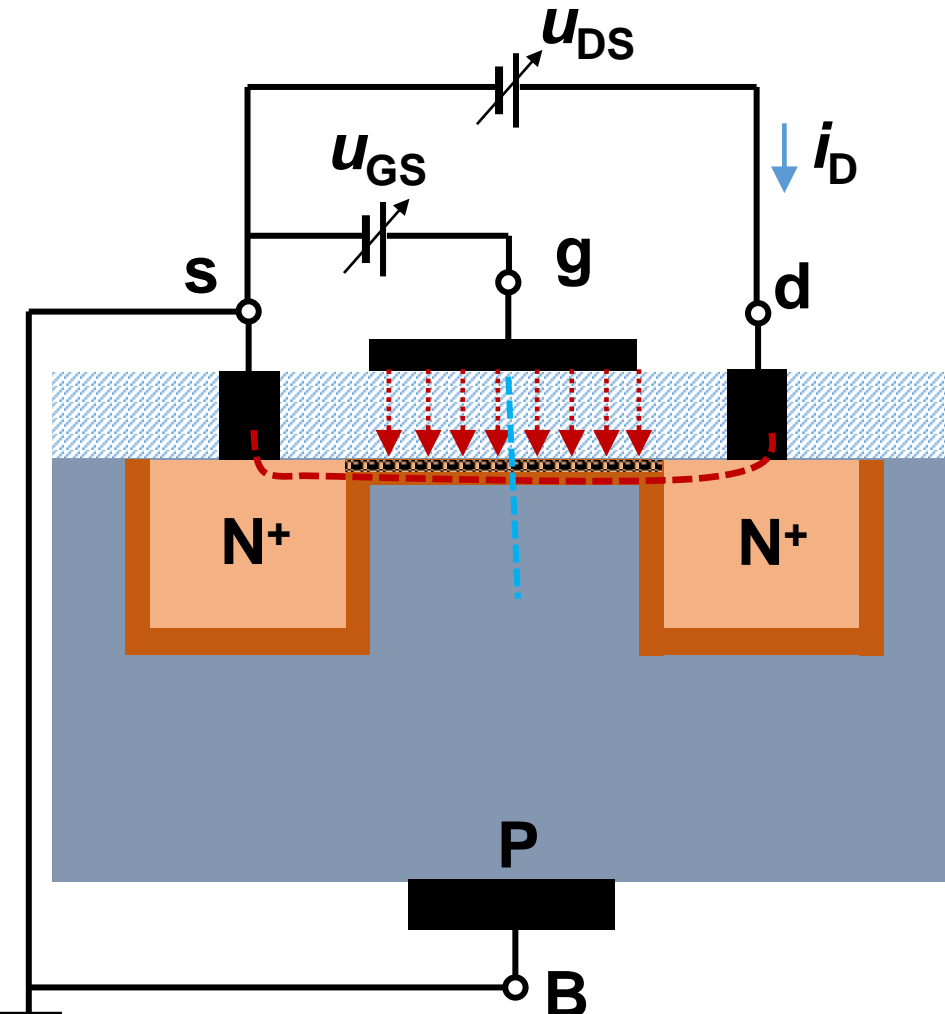


Band diagram along blue line

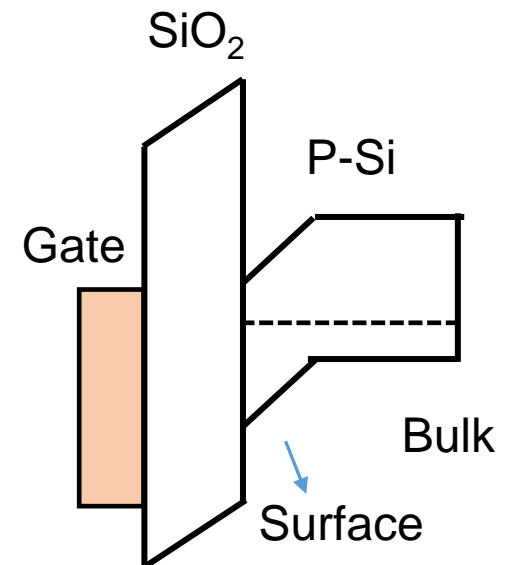


2) When $U_{GS(th)} > u_{GS} > 0$, $u_{DS} = 0$ Band diagram along red line

□ Before electron inversion layer is formed at surface

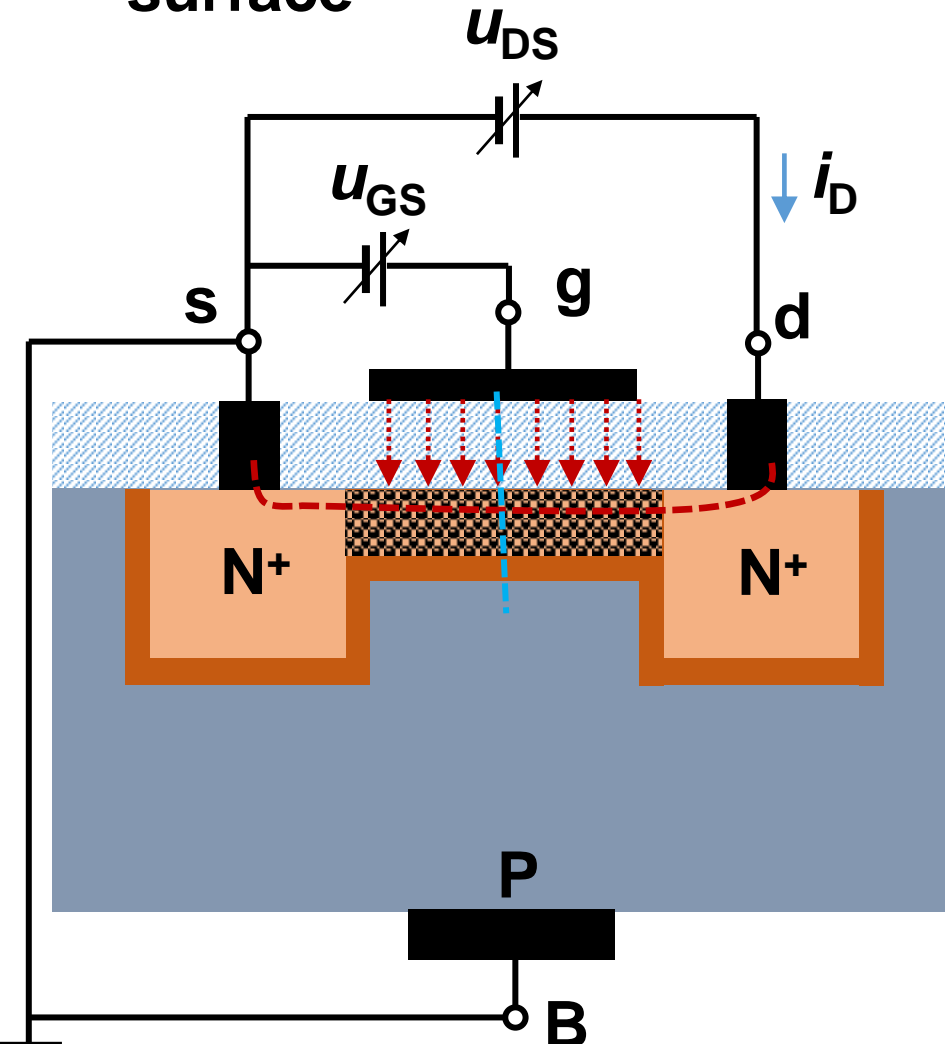


Band diagram along blue line

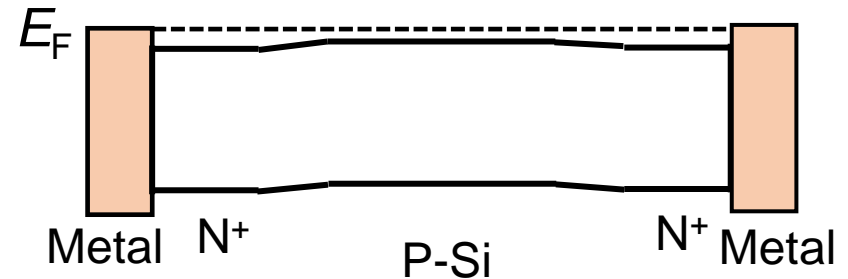


3) When $u_{GS} > U_{GS(th)}$, $u_{DS} = 0$

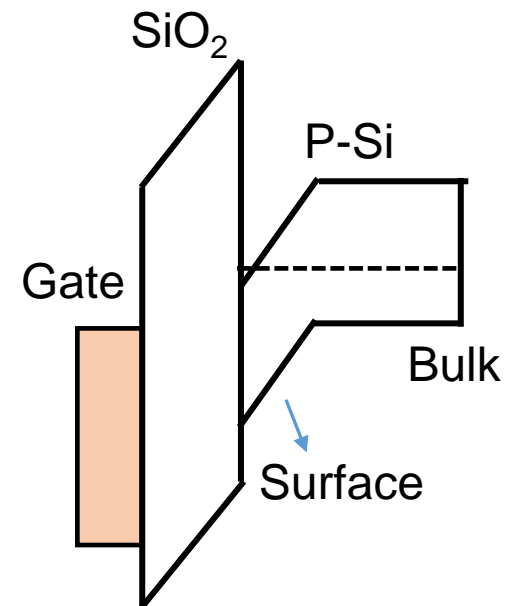
□ Electron inversion layer at surface



Band diagram along red line



Band diagram along blue line



The gate voltage V_{gs} can tune the Fermi energy of silicon near surface.

Homework 1-6: Draw the band diagram of the N-type MOSFET channels along the red dashed lines in page 44-46 (44-46页示意图中红色虚线方向的能带结构示意图, 包括源漏电极和半导体沟道) for below three situations:

(1) $u_{GS} = 0, u_{DS} > 0$ (refer to the device schematic in ppt page 38)

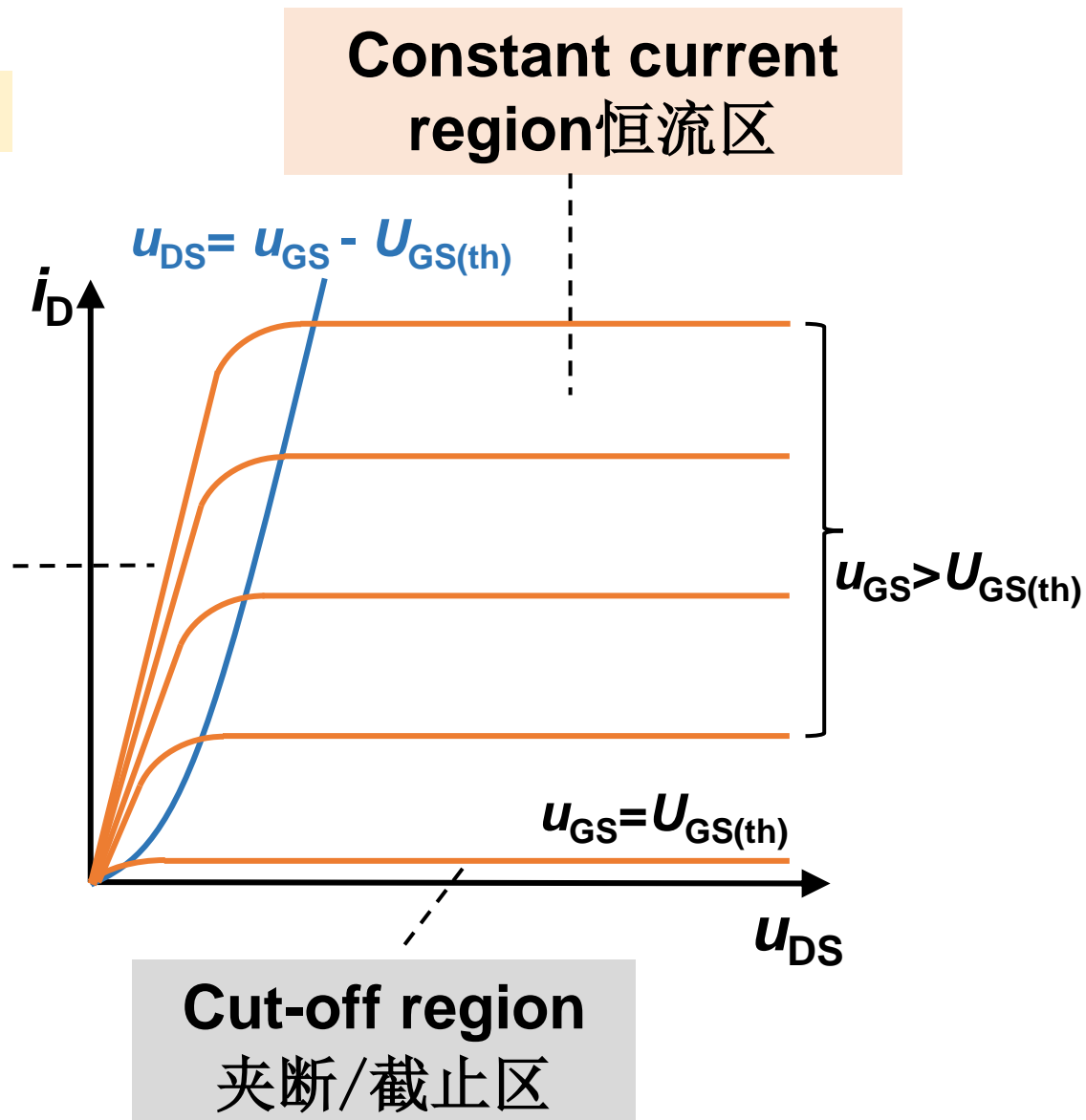
(2) $U_{GS(th)} > u_{GS} > 0, u_{DS} > 0$ (refer to the device schematic in ppt page 39)

(3) $u_{GS} > U_{GS(th)}, u_{DS} > 0$ (refer to the device schematic in ppt page 40)

Output I-V curve

$$i_D = f(u_{DS})|_{u_{GS}=\text{constant}}$$

Variable resistor region
可变电阻区



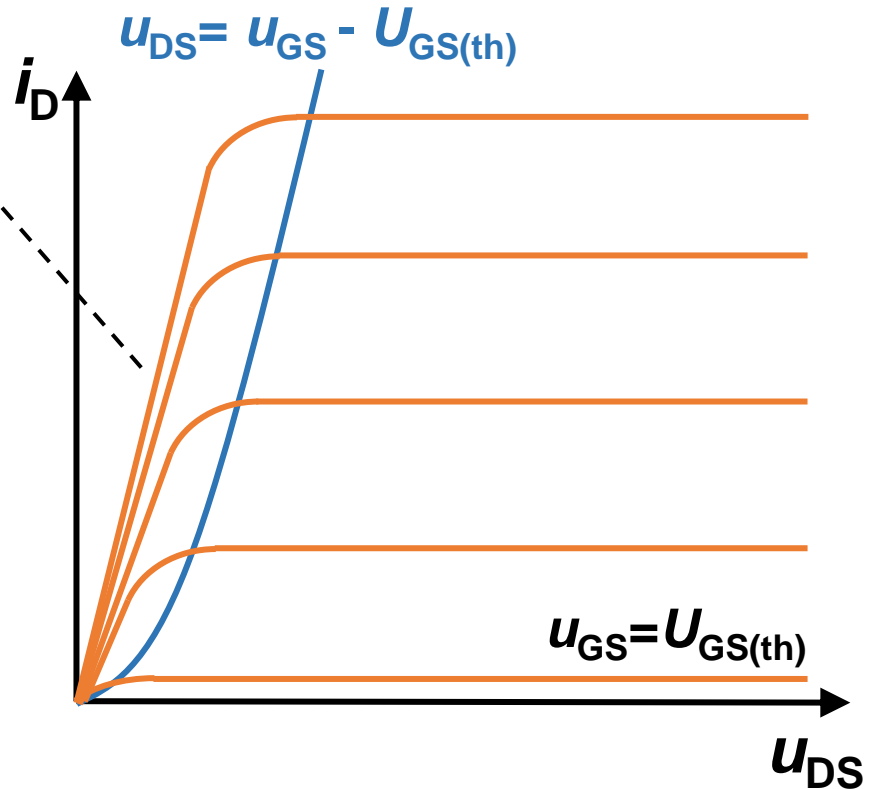
Variable resistor region 可变电阻区

- u_{DS} is small, the channel are conducting

$$u_{DS} < u_{GS} - U_{GS(th)}$$

- FET behaves like a resistance-tunable resistor

Tunable by u_{GS}



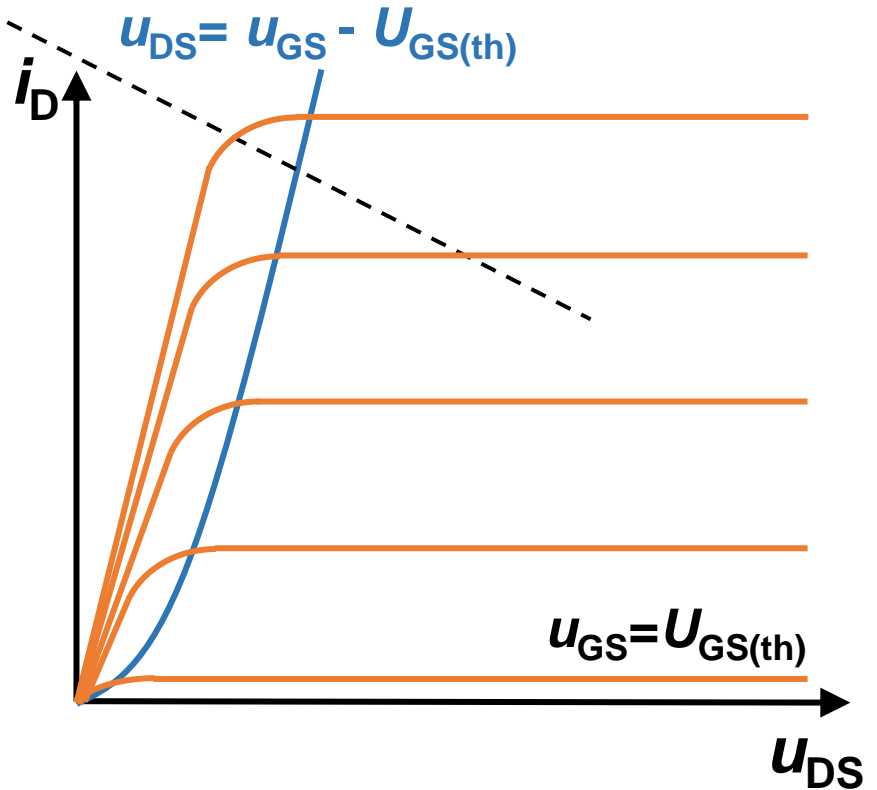
Constant current region 恒流区

□ u_{DS} is large, channel pinches off 沟道预夹断

$$\begin{cases} u_{DS} \geq u_{GS} - U_{GS(th)} \\ u_{GS} \geq U_{GS(th)} \end{cases}$$

□ i_D is almost constant, only depends on u_{GS}

□ Also can be called as amplification region

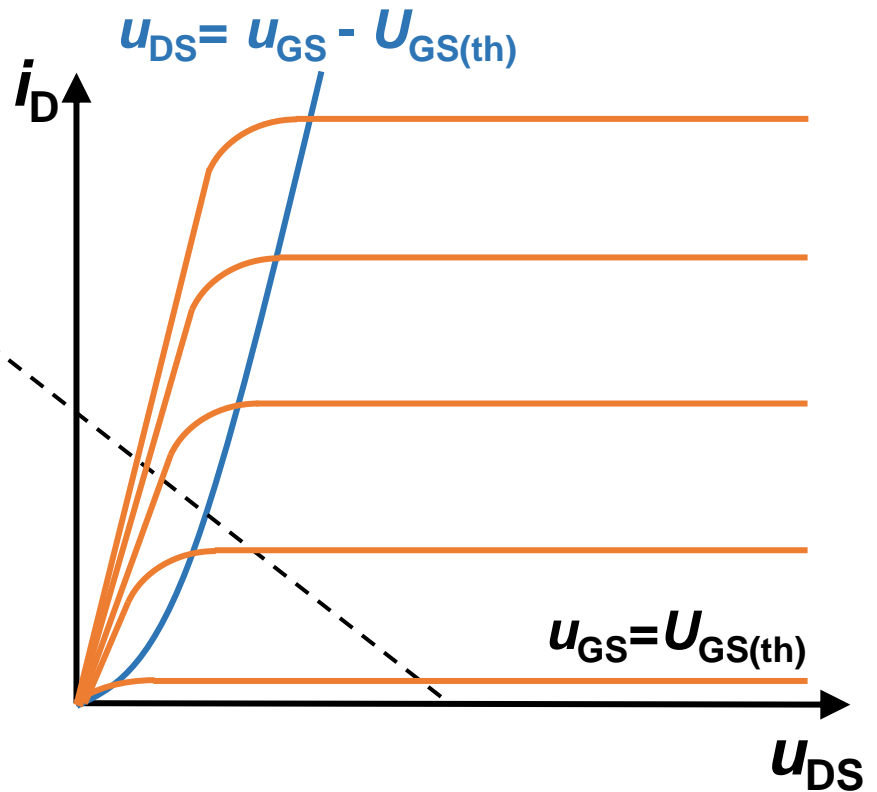


Cut-off region 夹断/截止区

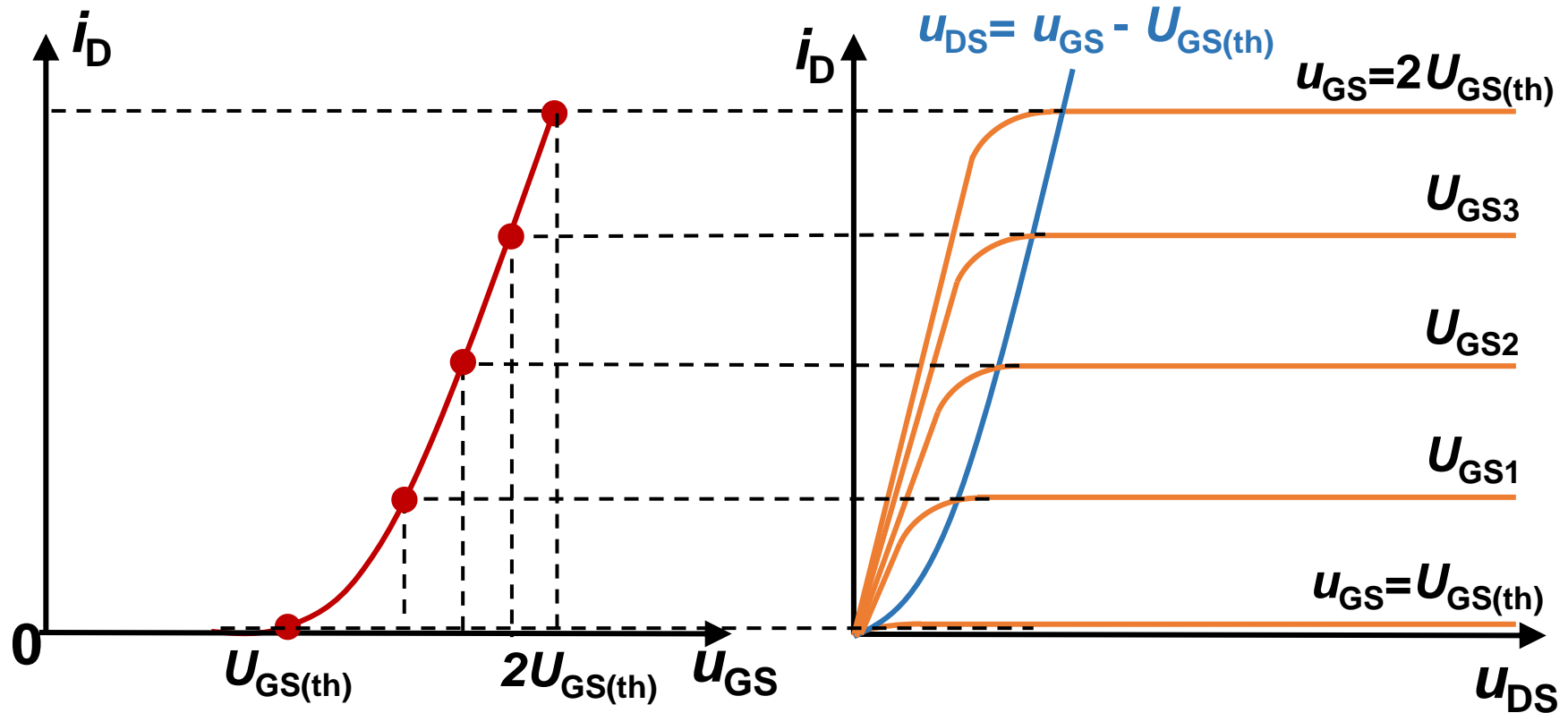
□ Channel fully pinches off

$$u_{GS} < U_{GS(th)}$$

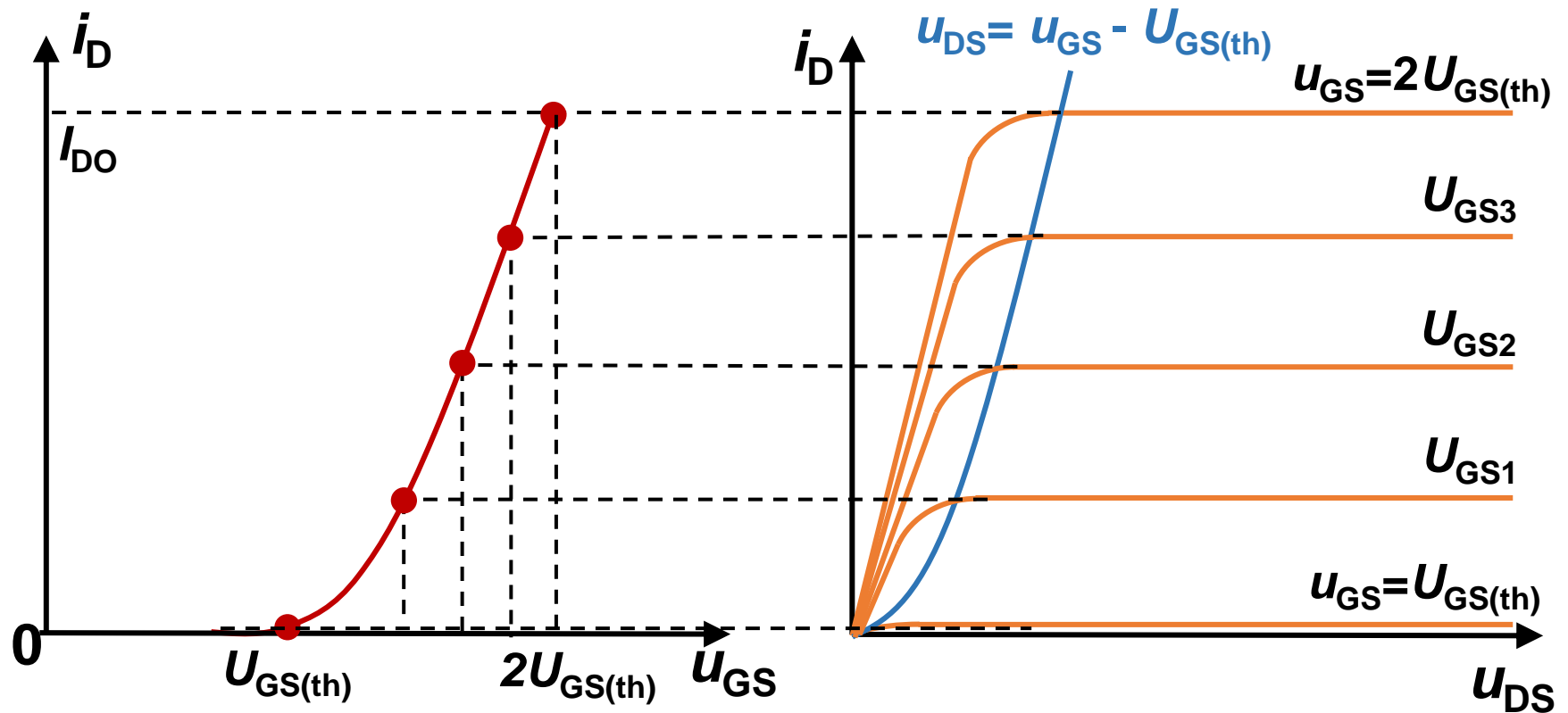
□ $i_D \approx 0$



Transfer curve 转移特性曲线 $i_D = f(u_{GS})|_{u_{DS}=\text{constant}}$



□ In constant-current region, the transfer curves are independent of u_{DS}



At constant-current region:

$$i_D = I_{D0} \left(\frac{u_{GS}}{U_{GS(th)}} - 1 \right)^2 \quad (u_{GS} > U_{GS(th)})$$

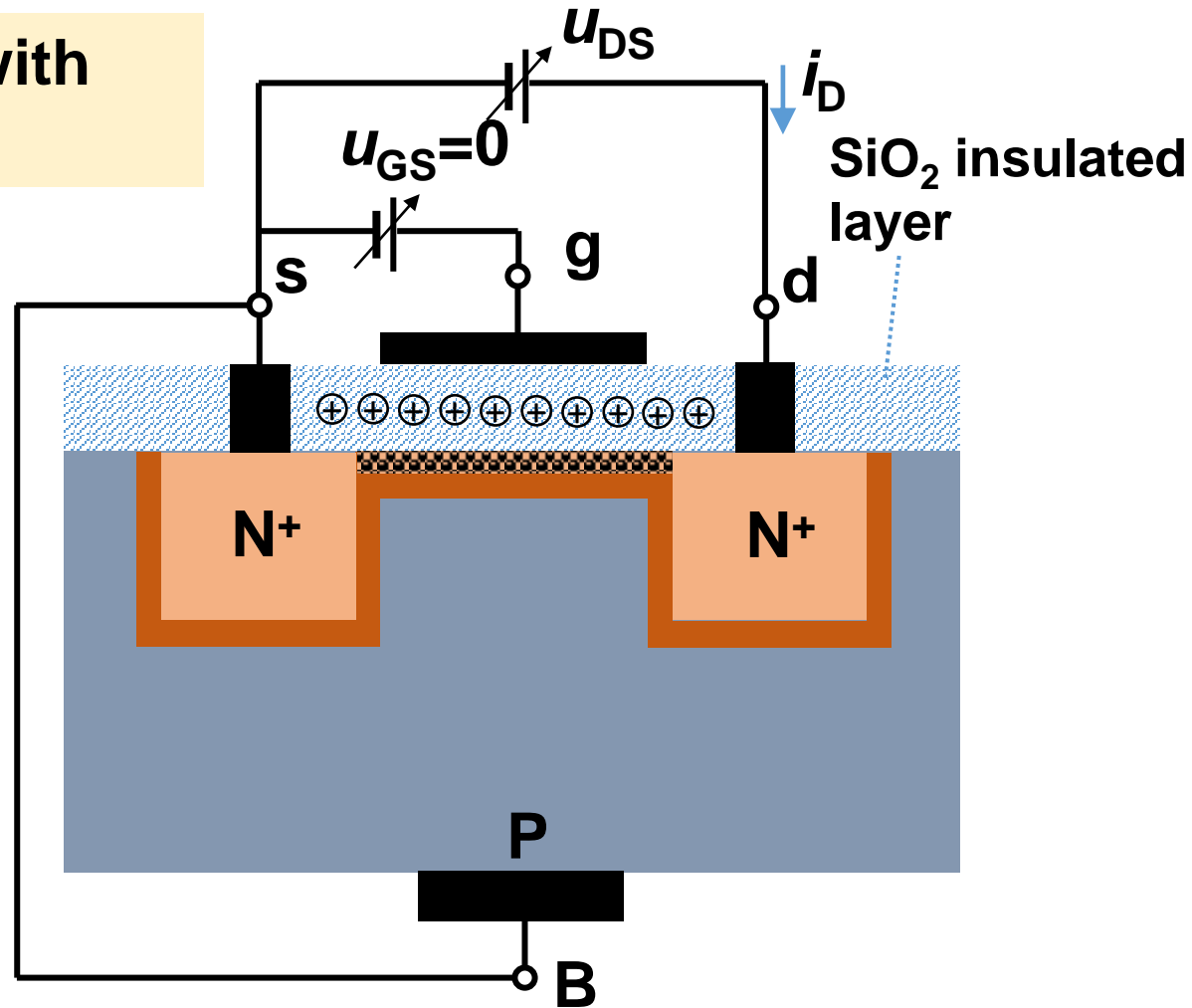
I_{D0} is the drain current at $u_{GS} = 2U_{GS(th)}$

Depleted N-type IGFET/MOSFET

SiO_2 are doped with positive ions

There is an inversion layer even when $u_{DS}=0$ and $u_{GS}=0$

Hence, when $u_{DS}>0$ and $u_{GS}=0$, $i_D>0$



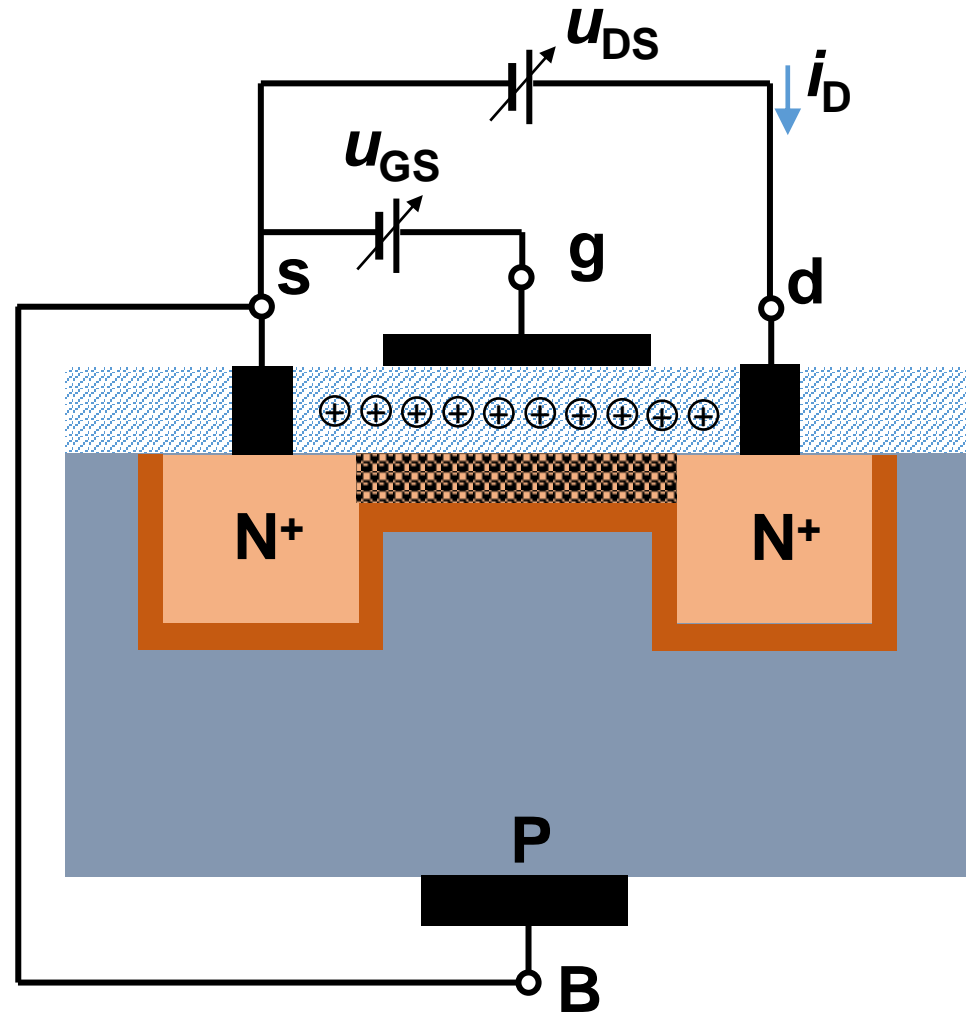
1) $u_{GS} > 0$

□ The inversion layer becomes wider

2) $u_{GS} < 0$

□ The inversion layer becomes narrower

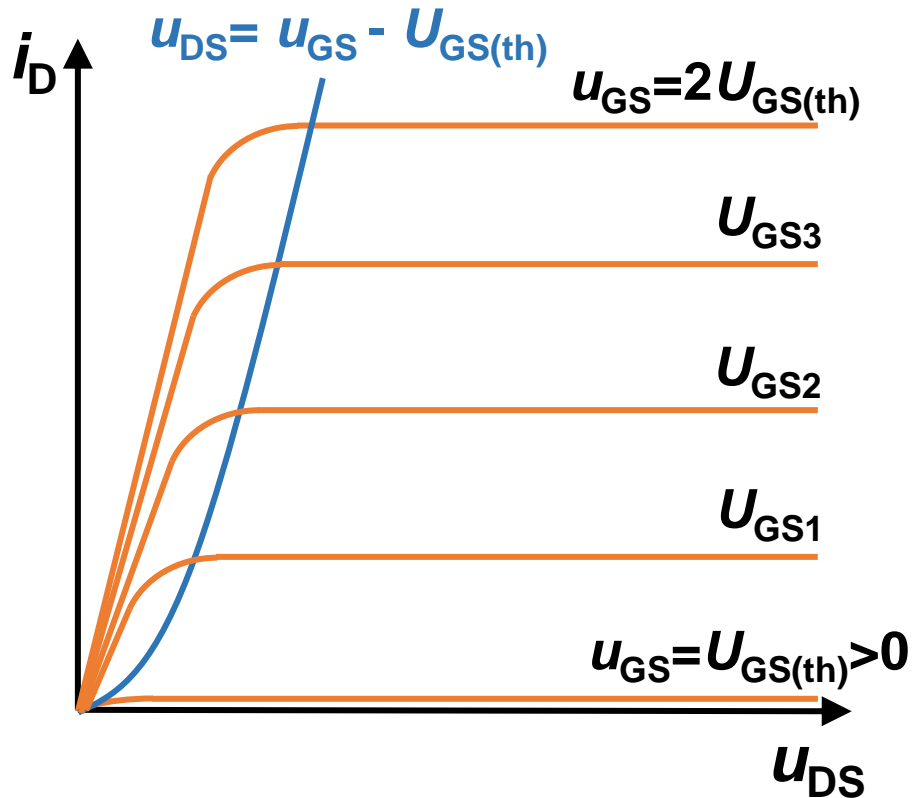
□ The pinch-off voltage
 $U_{GS(off)} < 0$



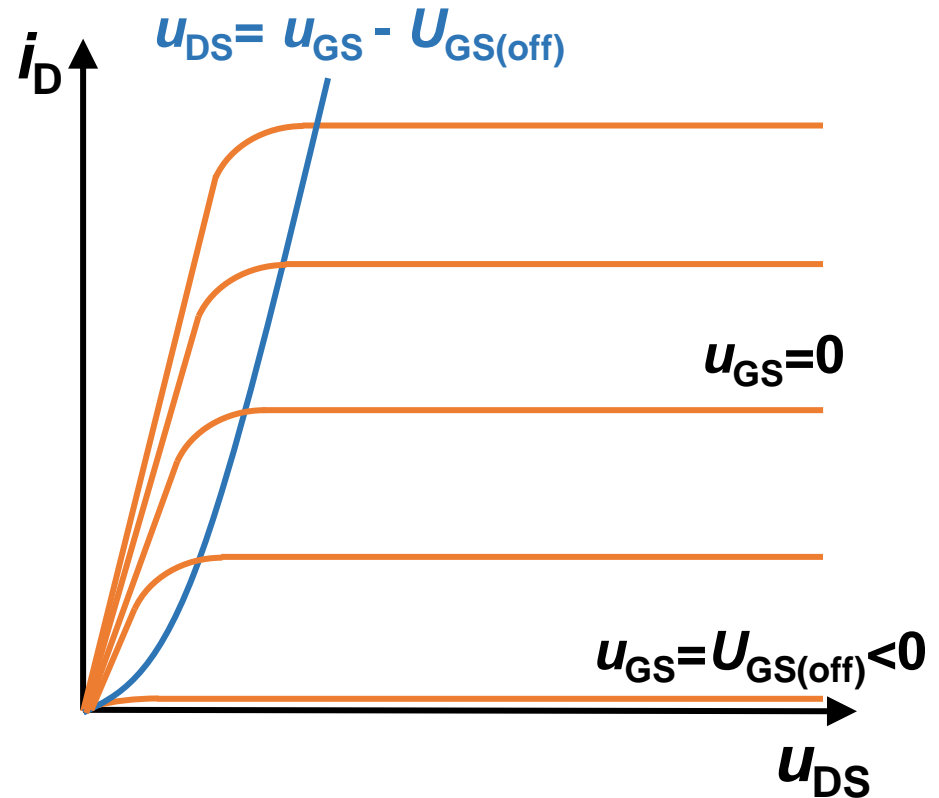
Output I-V curve

$$i_D = f(u_{DS})|_{u_{GS}=\text{constant}}$$

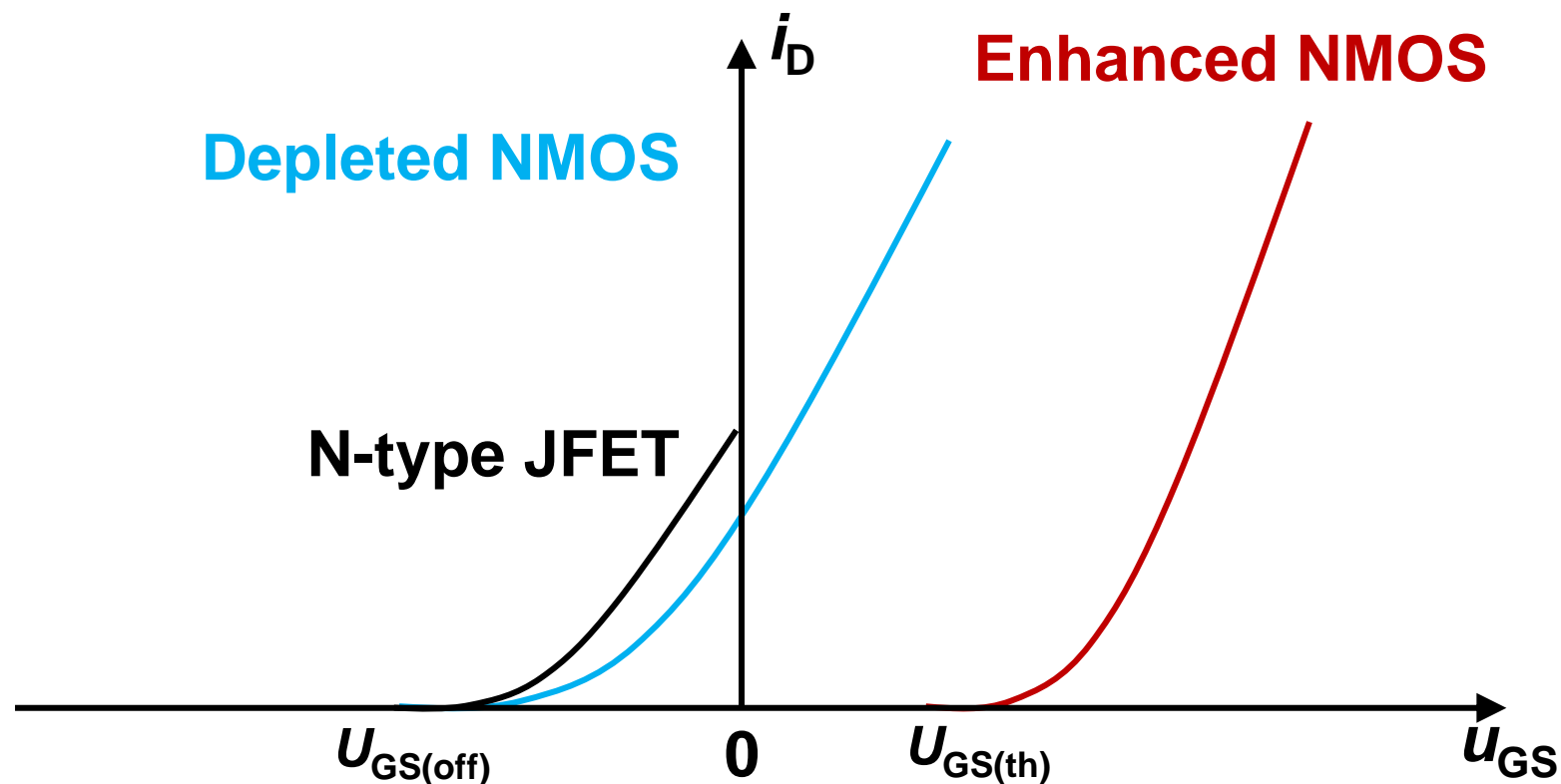
Enhanced NMOS



Depleted NMOS



Transfer curve 转移特性曲线 $i_D = f(u_{GS})|_{u_{DS}=\text{constant}}$

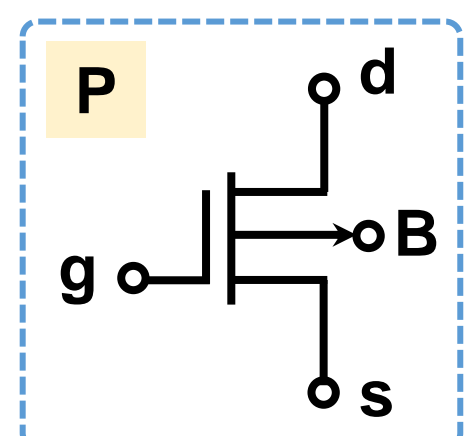
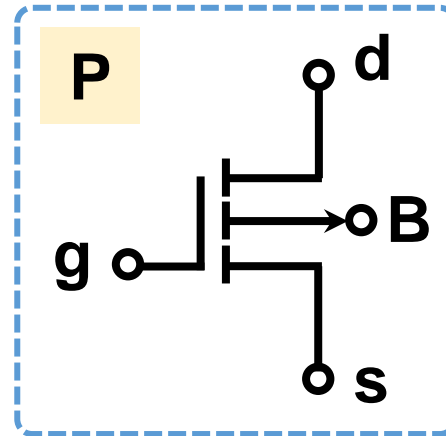
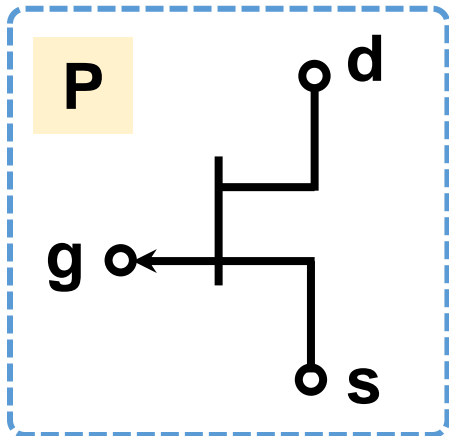
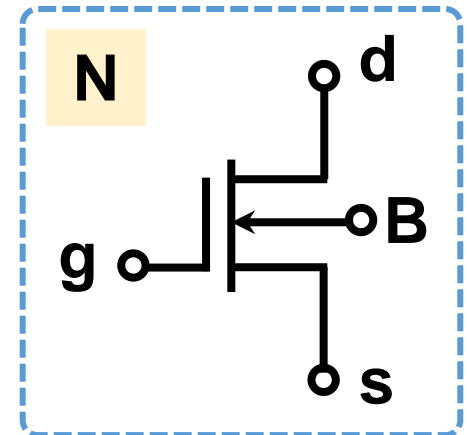
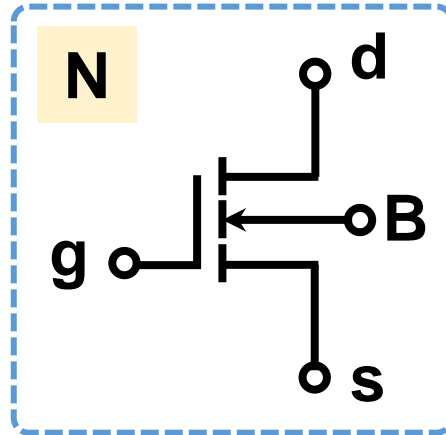
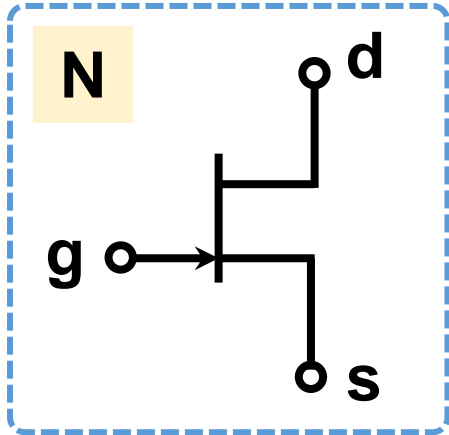


Summary

JFET

Enhanced MOSFET

Depleted MOSFET



FET 场效应晶体管 (Compared with BJT)

□ Gate(栅极), source(源极), and drain(漏极) in FET corresponds to the base(基极), emitter(发射极), and collector(集电极) in BJT

1) FET: Use voltage u_{GS} to control current i_D

BJT: Use current i_B to control current i_C

2) FET: High input resistance R_{GS} : $10^7 \sim 10^{15}\Omega$,
 $i_G \approx 0$

BJT: Low input resistance R_{EB}

3) FET: Only one type of carriers (electrons or holes) is involved in conduction

BJT: Both electrons and holes are involved in conduction

4) FET: Small size, light, low-power consumption, long life span

5) FET: The device structure is symmetric, hence source and drain can be exchanged

6) FET: The size of FET is only about 5% of that of BJT. Hence it is widely used in large-scale integration circuits

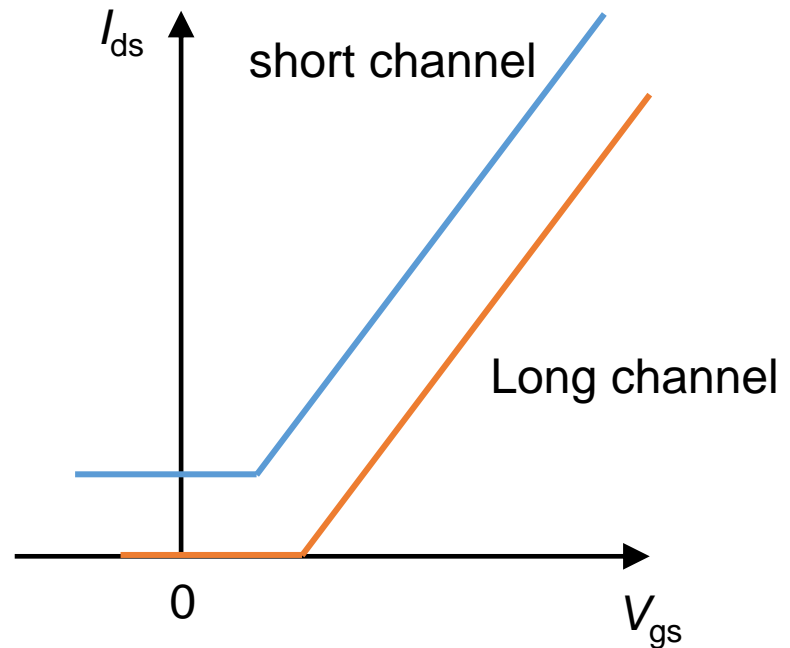
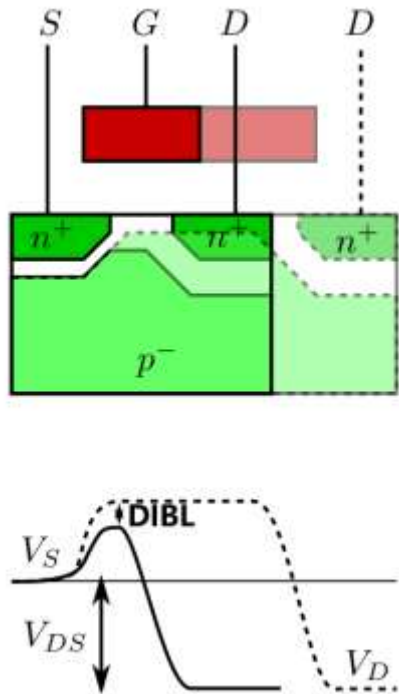
7) FET: The transconductance is smaller than that of BJT. With similar load resistance, the voltage gain is usually smaller than that of BJT.

8) FET: FET is more vulnerable to environment electrostatic charges. The high input resistance and ultra-thin insulating layer make charges accumulate in FET, and breakdown the insulating layer. 由于MOS管的输入电阻高，由外界感应产生的电荷不易泄露，而栅极上的绝缘层又很薄，这将在栅极上产生很高的电场强度，以致引起绝缘层的击穿而损坏管子。

**What's the most challenging issues
faced by MOSFET?**

The limit of channel length of Silicon FETs

- ◆ Scaling of Silicon transistors is predicted to fail below 5 nm- gate lengths because of the short channel length effect



The limit of channel length of Silicon FETs

When the channel length \gg width of depletion region

$$u_{GS} = 0$$

$$u_{DS} = 0$$

$$u_{DS}$$

$$u_{GS}=0$$

$$i_D$$

s

g

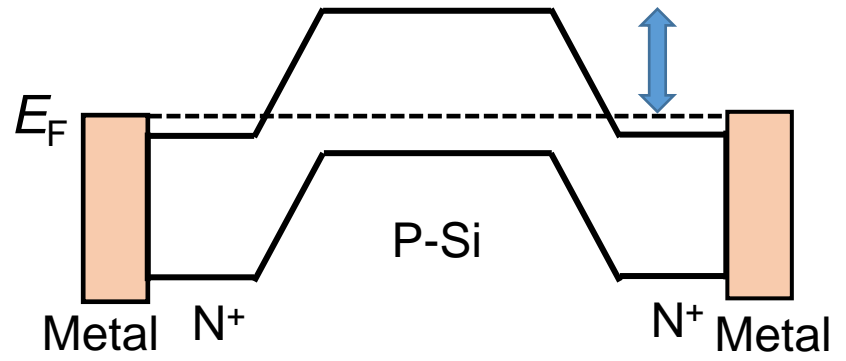
d

N⁺

N⁺

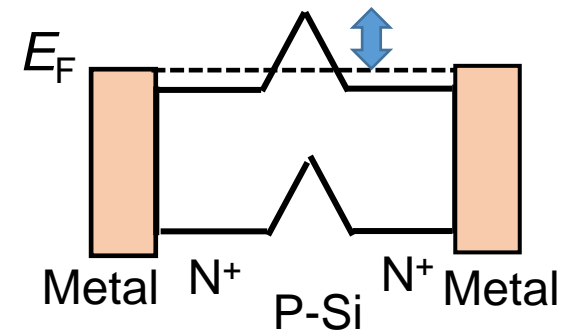
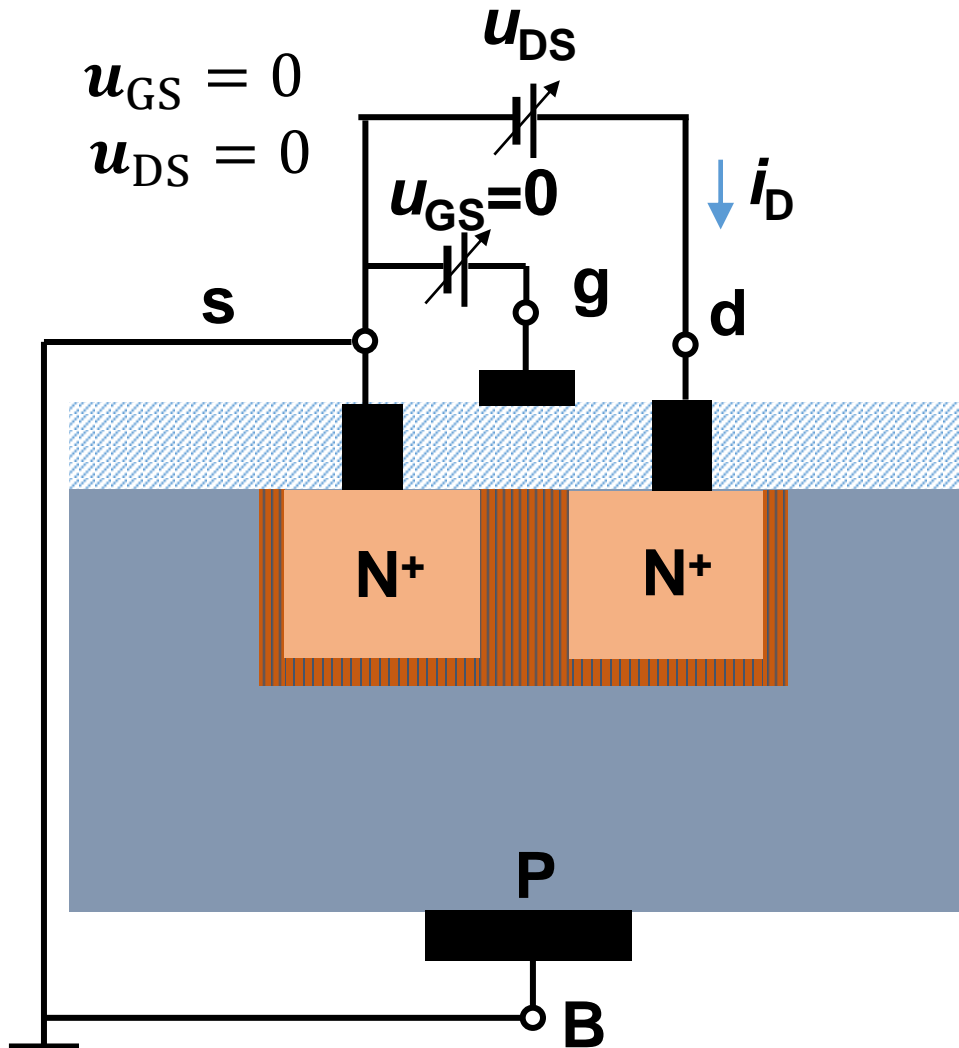
P

B



The limit of channel length of Silicon FETs

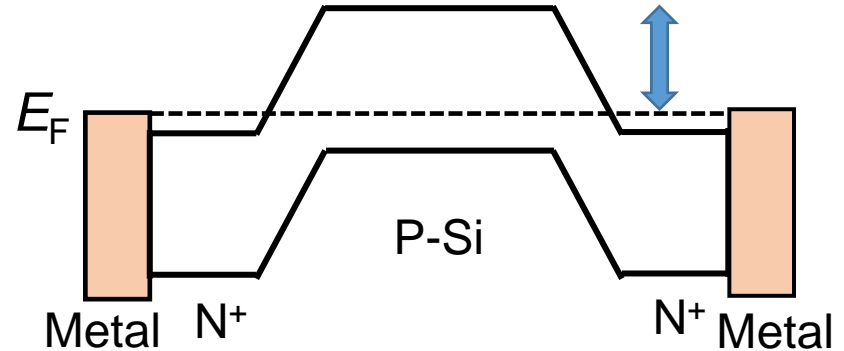
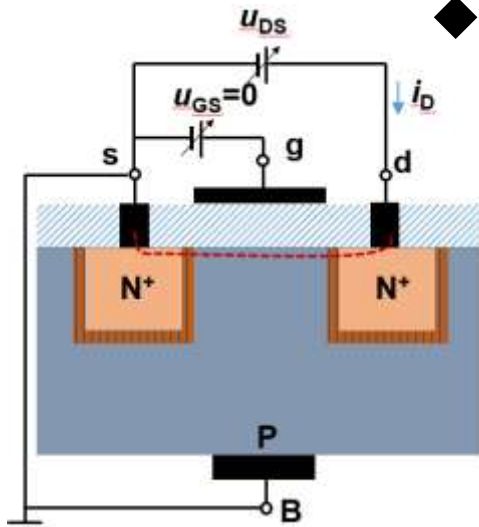
◆ When the channel length \sim the width of depletion region



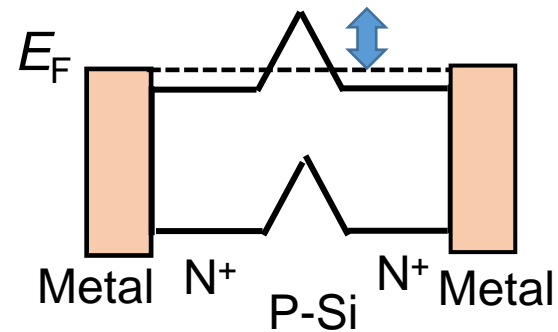
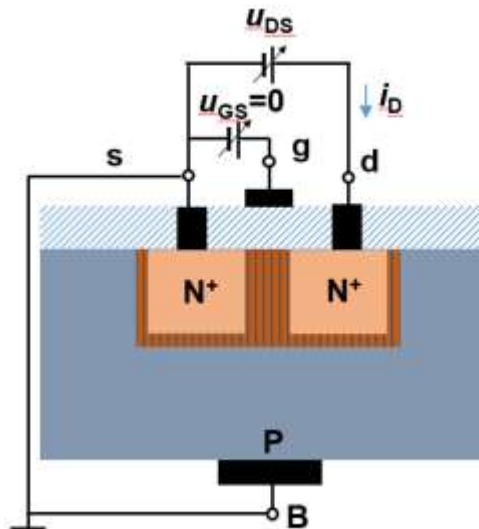
Barrier height is lowered!

The limit of channel length of Silicon FETs

◆ Long channel length

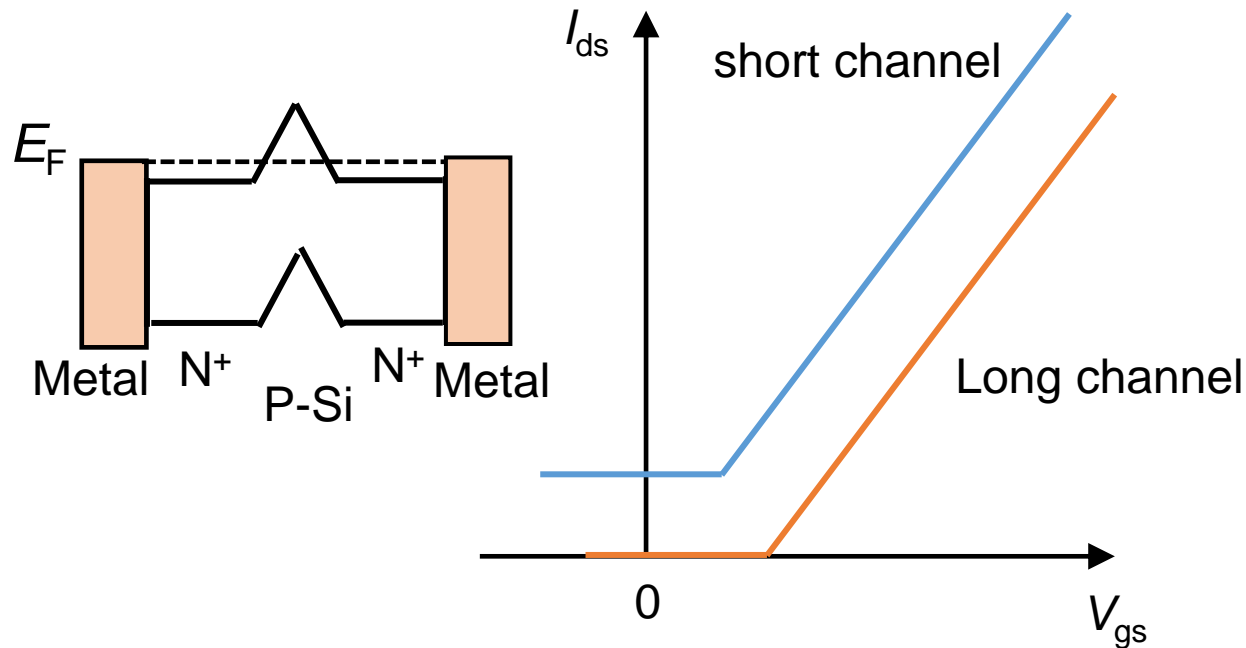


◆ Short channel length



The limit of channel length of Silicon FETs

- ◆ For short channel device, the barrier height is low and current is high, and hence the device cannot fully turn off.

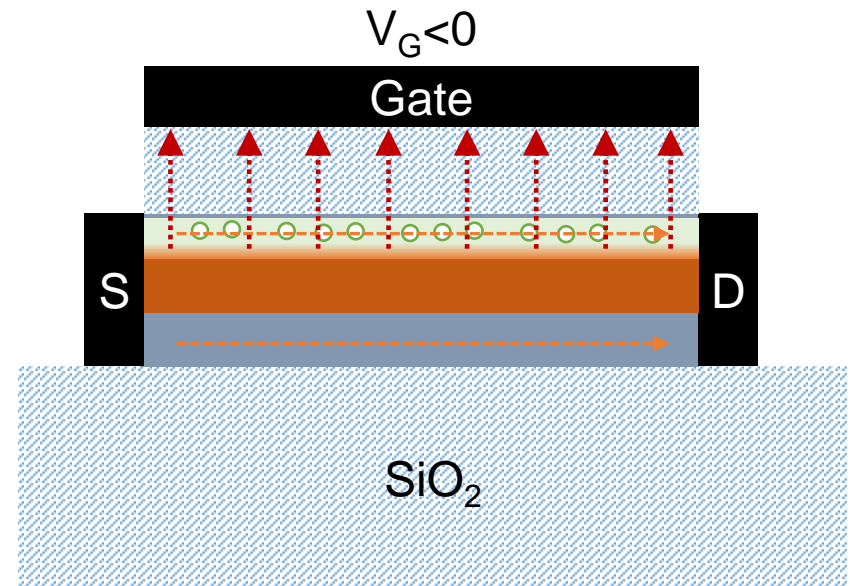
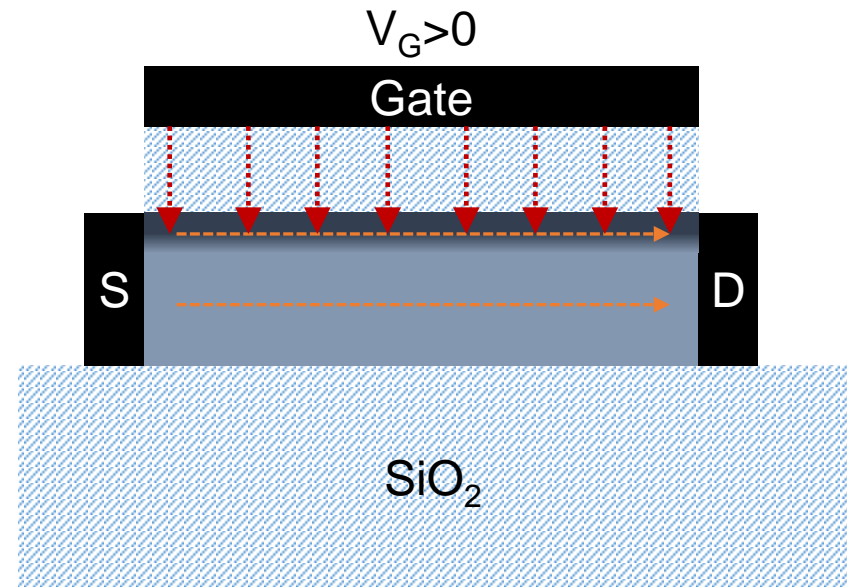
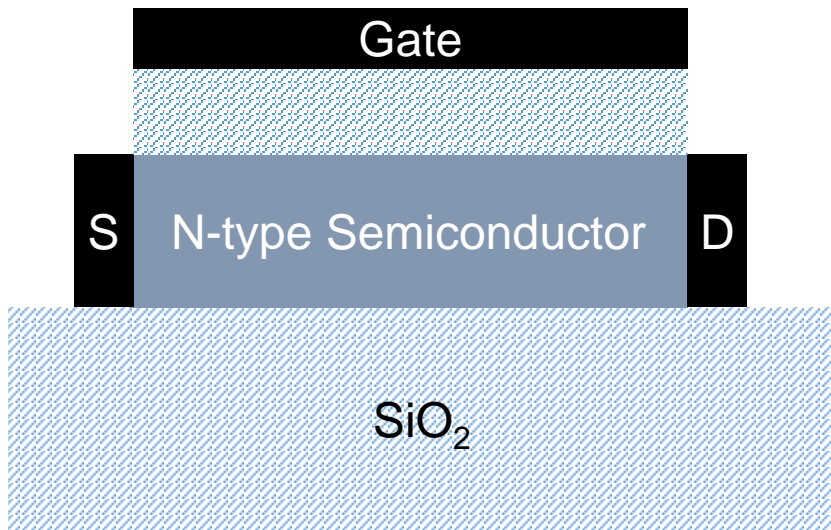


Q: how to further decrease the channel length?

Decrease width of depletion region → Decrease thickness of silicon

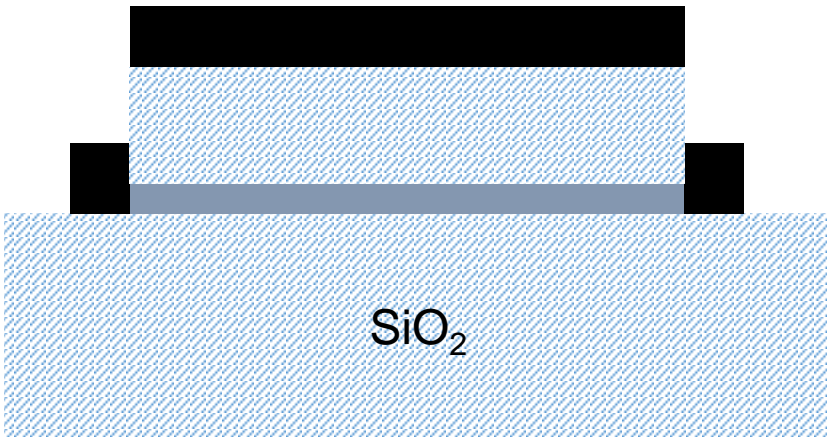
Thin-film transistor

Thickness > depletion region

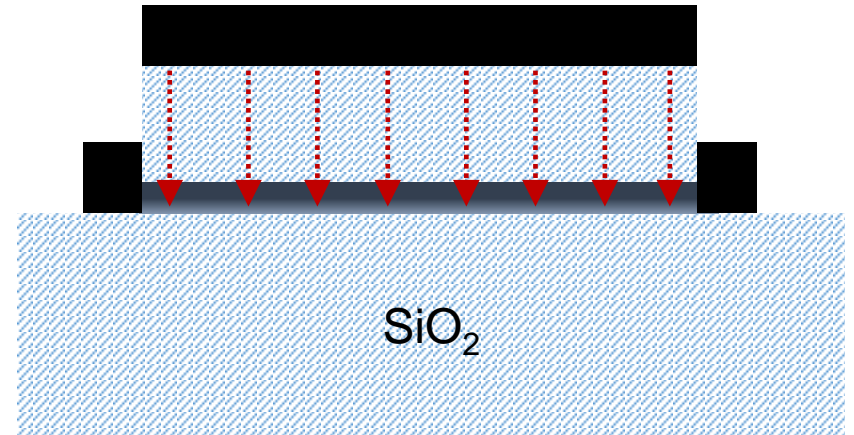


Thin-film transistor

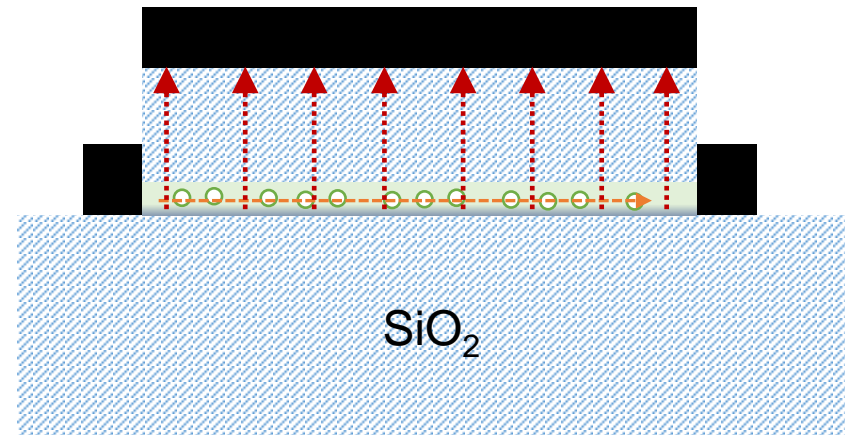
Thickness < depletion region



$V_G > 0$

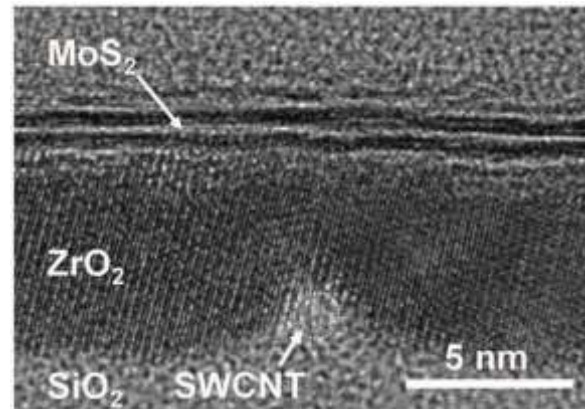
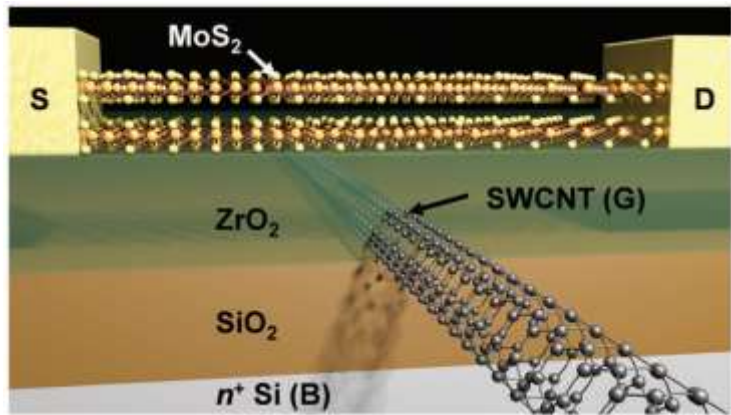


$V_G < 0$



The limit of channel length of 2D FETs

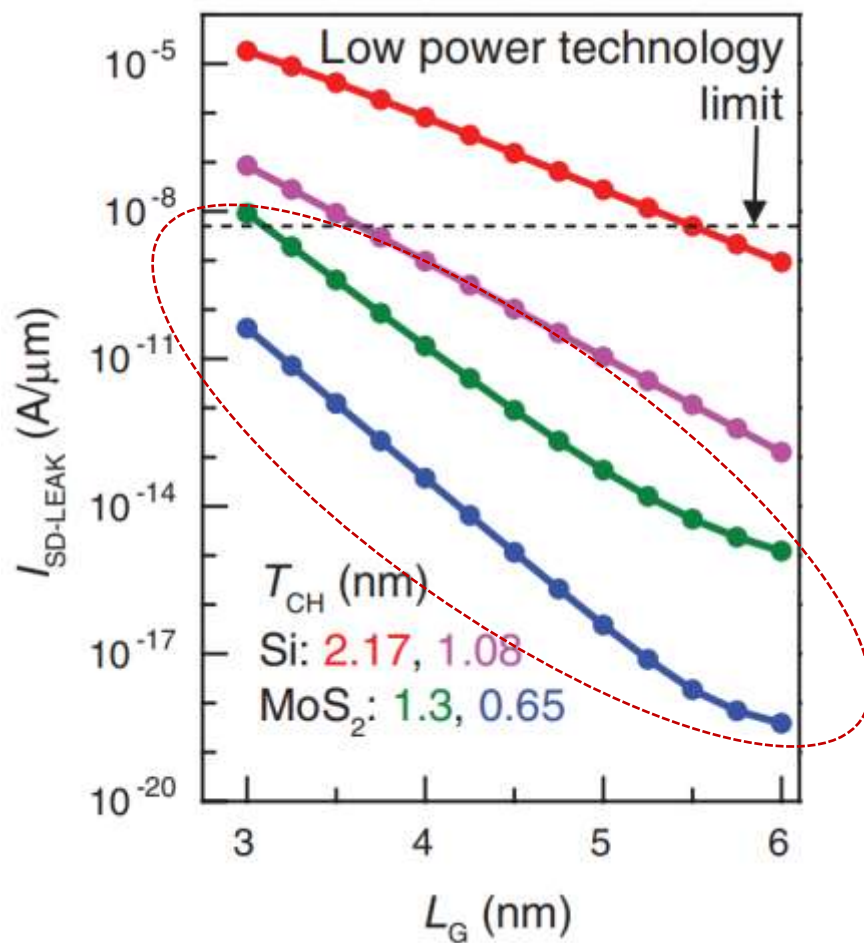
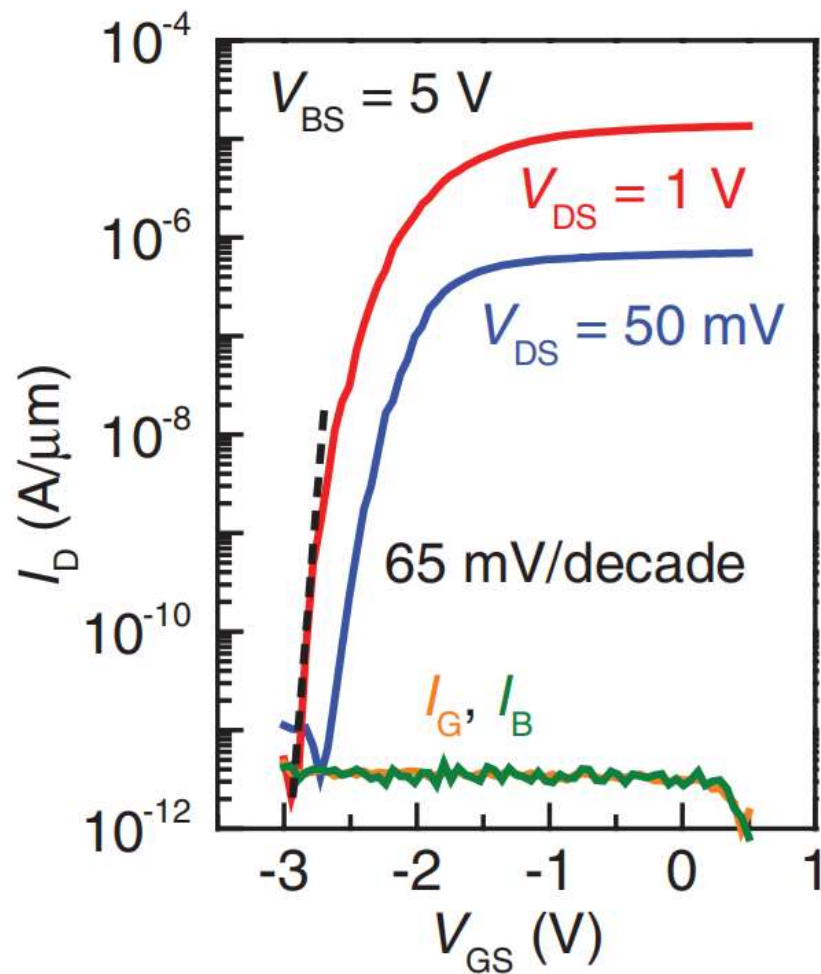
- ◆ 2D material: atomically thin thickness. Depletion region < 1 nm.



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- ◆ Use 2D semiconductor: monolayer and bilayer MoS₂
- ◆ Use carbon nanotube (~ 1 nm) as gate material

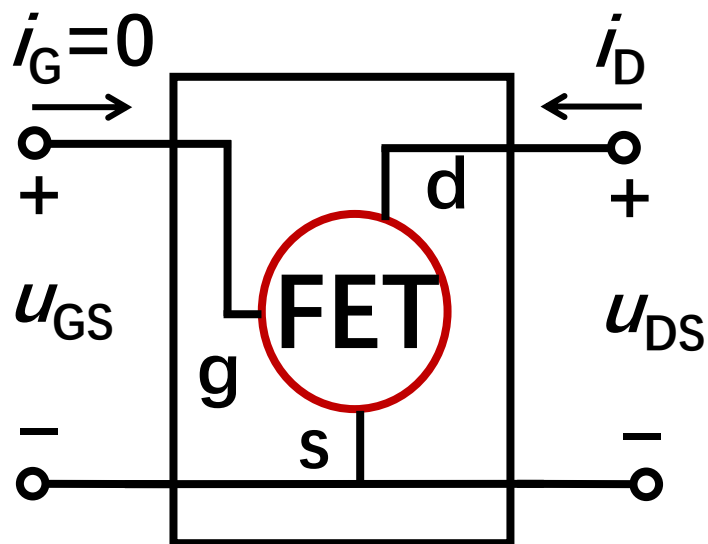
The limit of channel length of 2D FETs



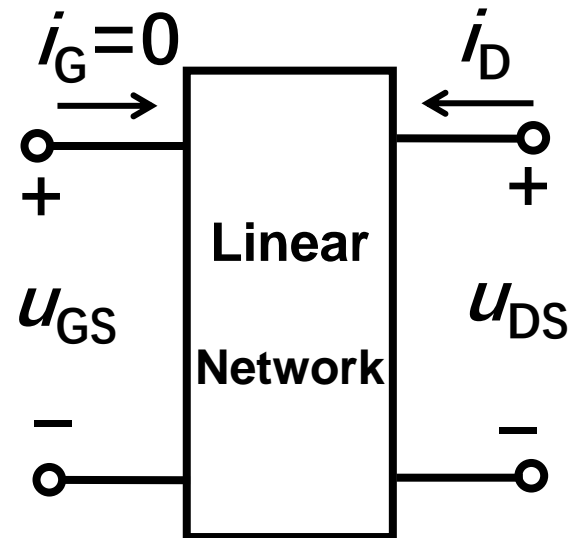
Dynamic analysis of FET amplifier circuit

Find the equivalent circuit of FET: to replace FET with a linear network

Transistor



Equivalent circuit



$$① \quad i_D = f(u_{GS}, u_{DS}) \quad u_{GS} = u_{GS}$$

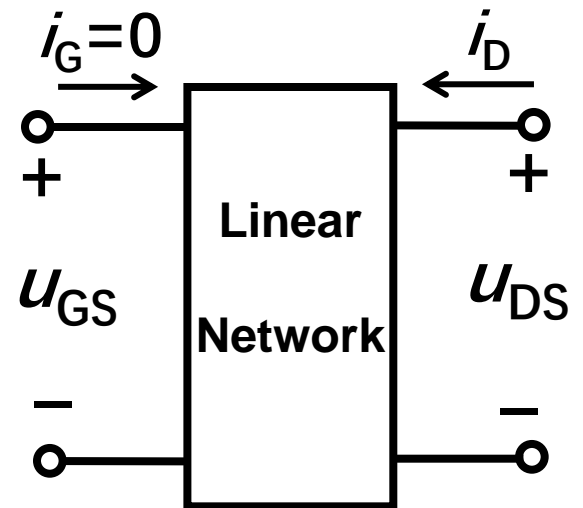
$$② \quad di_D = \frac{\partial i_D}{\partial u_{GS}} \Big|_{U_{DSQ}} du_{GS} + \frac{\partial i_D}{\partial u_{DS}} \Big|_{U_{GSQ}} du_{DS}$$

Transconductance g_m 互导/跨导

$$g_m = \frac{di_D}{du_{GS}} \Big|_{U_{DSQ}}$$

$$g_{ds} = \frac{1}{r_{ds}} = \frac{di_D}{du_{DS}} \Big|_{U_{GSQ}}$$

$$di_D = g_m du_{GS} + \frac{1}{r_{ds}} du_{DS}$$

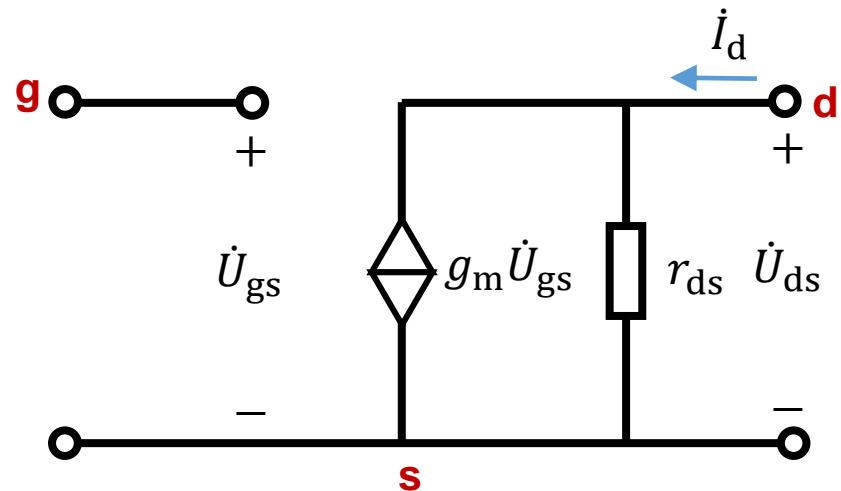
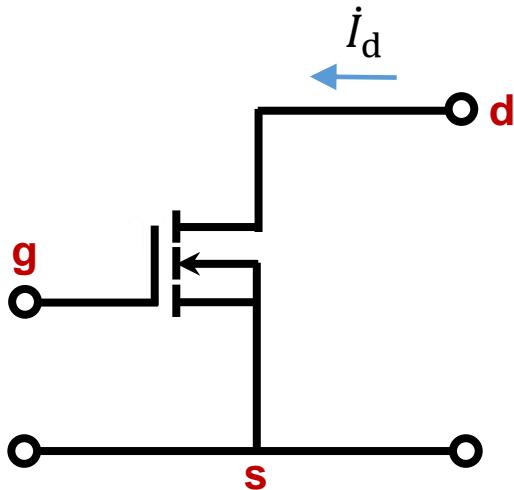


$$di_D = g_m du_{GS} + \frac{1}{r_{ds}} du_{DS}$$

Input signal i_D is small 小信号条件

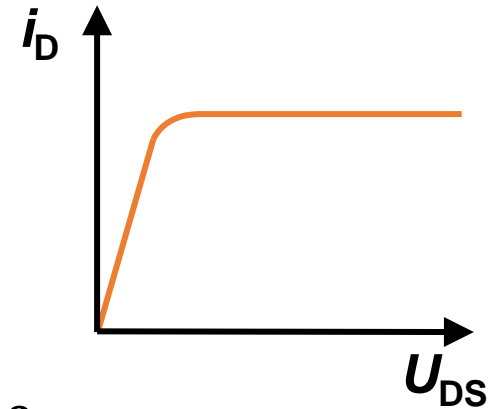
di_D can be replaced by a small quantity: i_d or \dot{I}_d

$$\dot{U}_{gs} = \dot{U}_{gs} \quad \dot{I}_d = g_m \dot{U}_{gs} + \frac{1}{r_{ds}} \dot{U}_{ds}$$



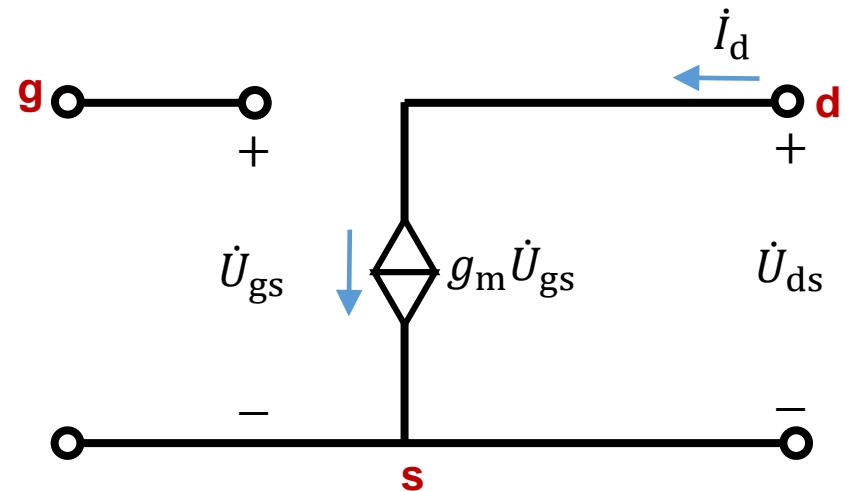
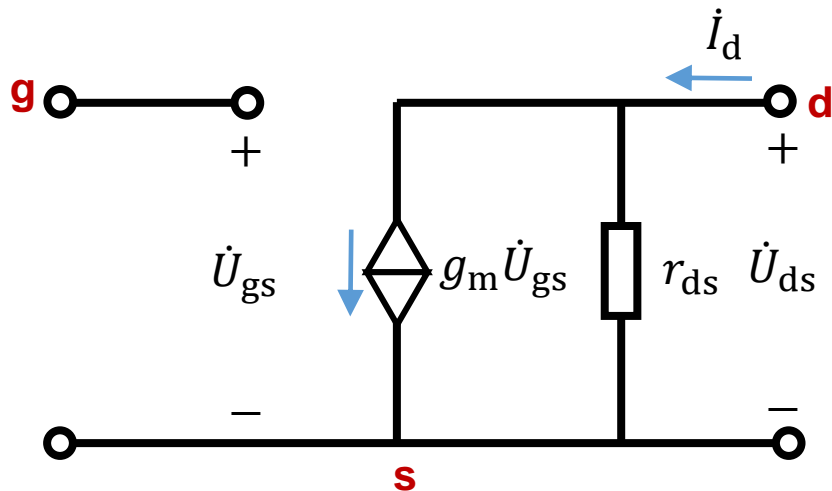
$$\dot{i}_d = g_m \dot{U}_{gs} + \frac{1}{r_{ds}} \dot{U}_{ds}$$

$$g_{ds} = \frac{1}{r_{ds}} = \left. \frac{di_D}{du_{DS}} \right|_{U_{GSQ}}$$



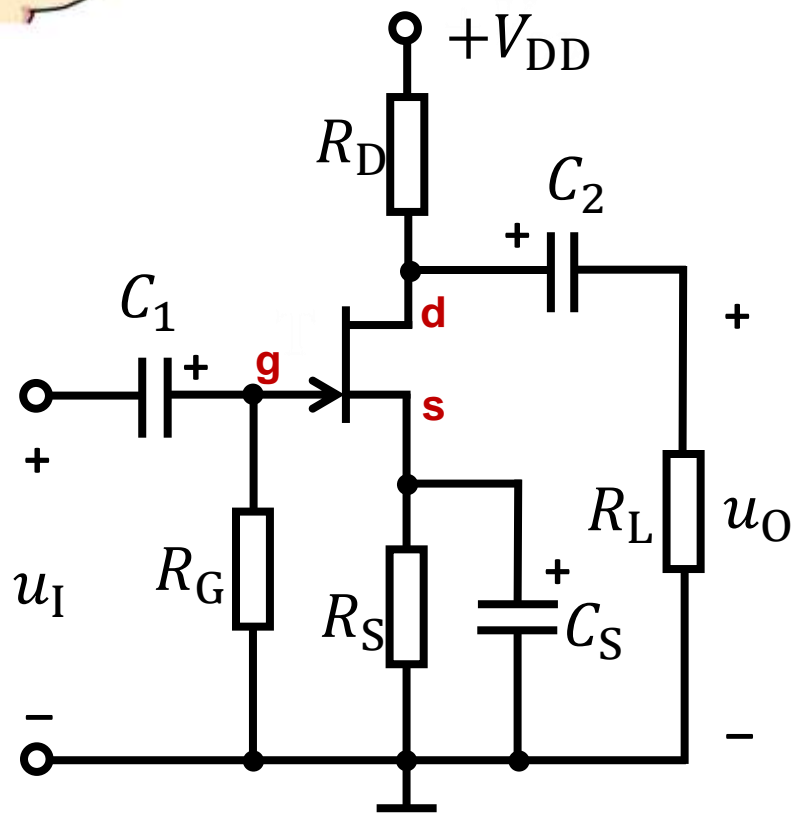
In constant current region, $\left. \frac{di_D}{du_{DS}} \right|_{U_{GSQ}} \approx 0, r_{ds} \rightarrow \infty$.

Simplified model





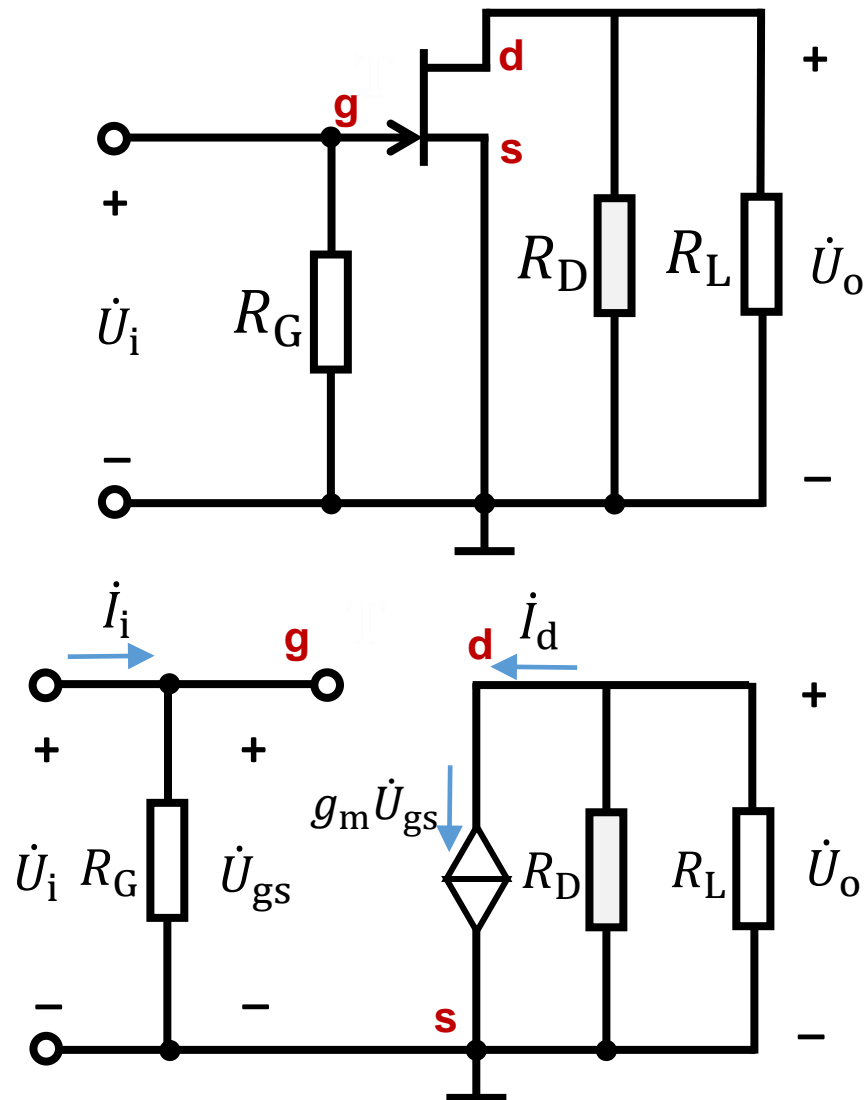
Common-s amplifier circuit



N-type JFET

Self-biased circuit

AC circuit



Flash memory



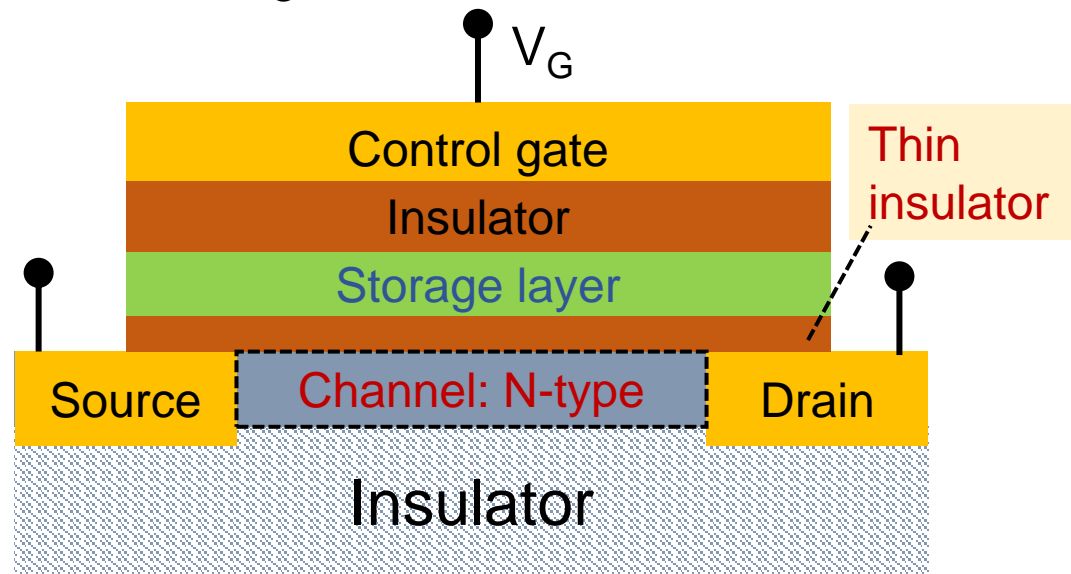
Flash card
闪存卡

- ◆ Portable 便携
- ◆ Low energy consumption 能耗小



Solid state disk 固态硬盘

Positive V_G - channel turns on 沟道开启
Negative V_G - channel is pinched 沟道夹断

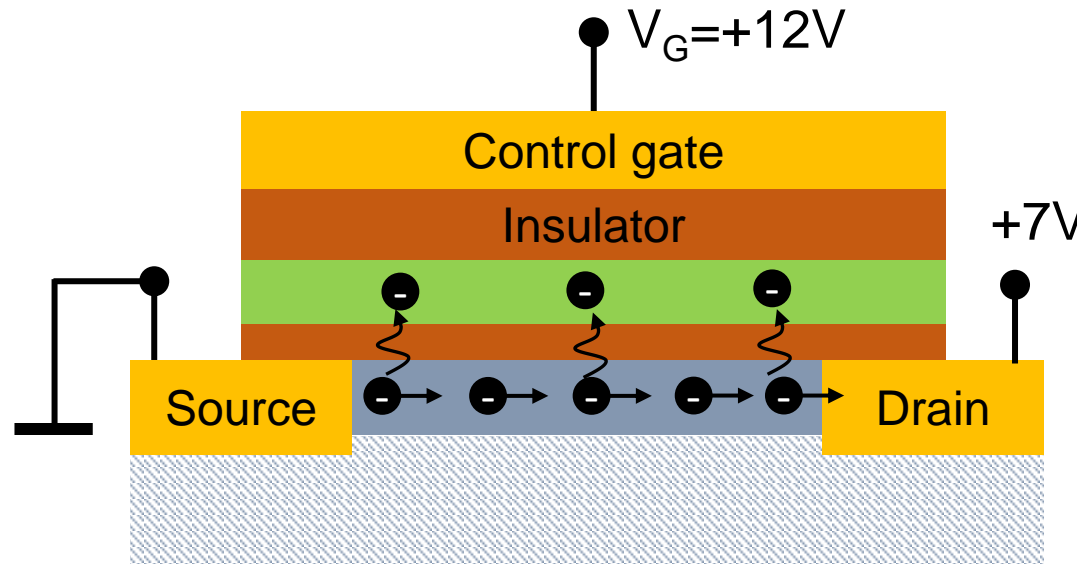


Source, drain, gate: conducting materials

Storage layer: floating thin material
(semiconductor, metal...)

Thin insulator (tunneling barrier 隧穿层):
several nm thick

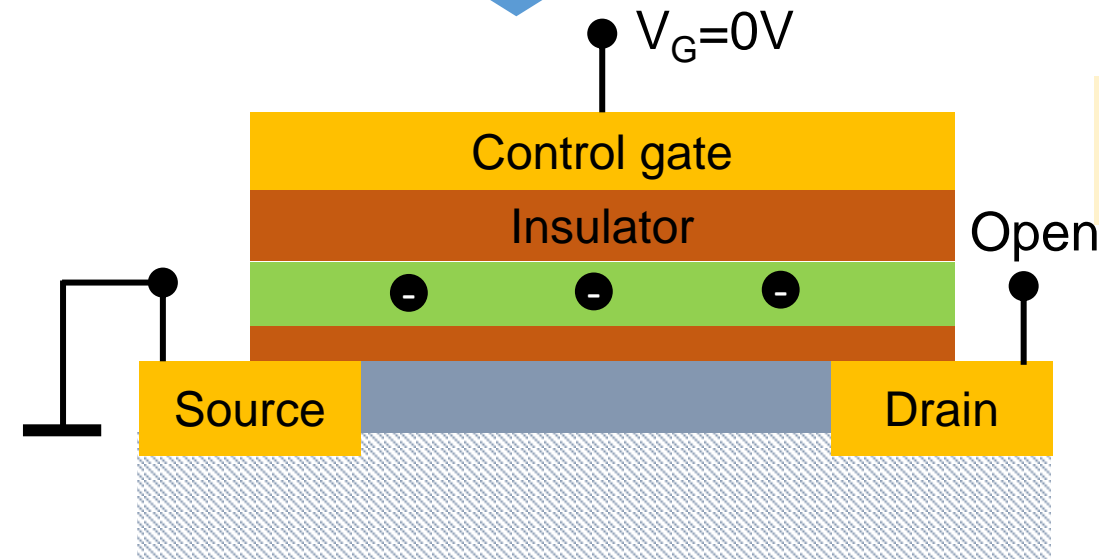
Writing 数据写入



- Apply a large positive voltage to gate

Channel turns on

Pull electrons from channel into storage layer

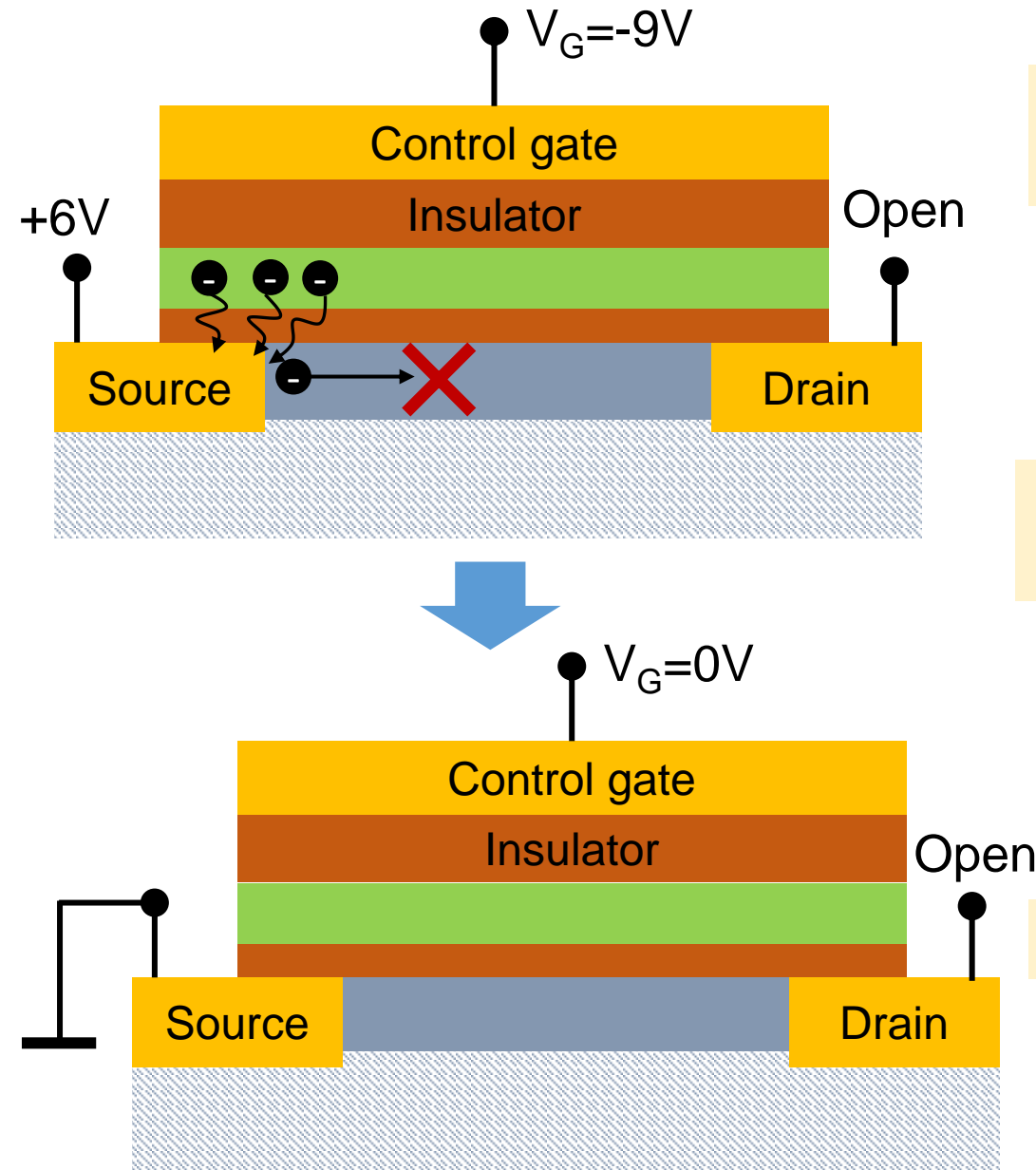


- Electrons don't leakage out without the help of voltage

Electrons in storage layer will repel electrons in the channel

Channel is in high resistance state "0"

Erasing 数据擦除



- Apply a large negative voltage to control gate

Push electrons away

Block the channel

- Apply a large positive voltage to Source

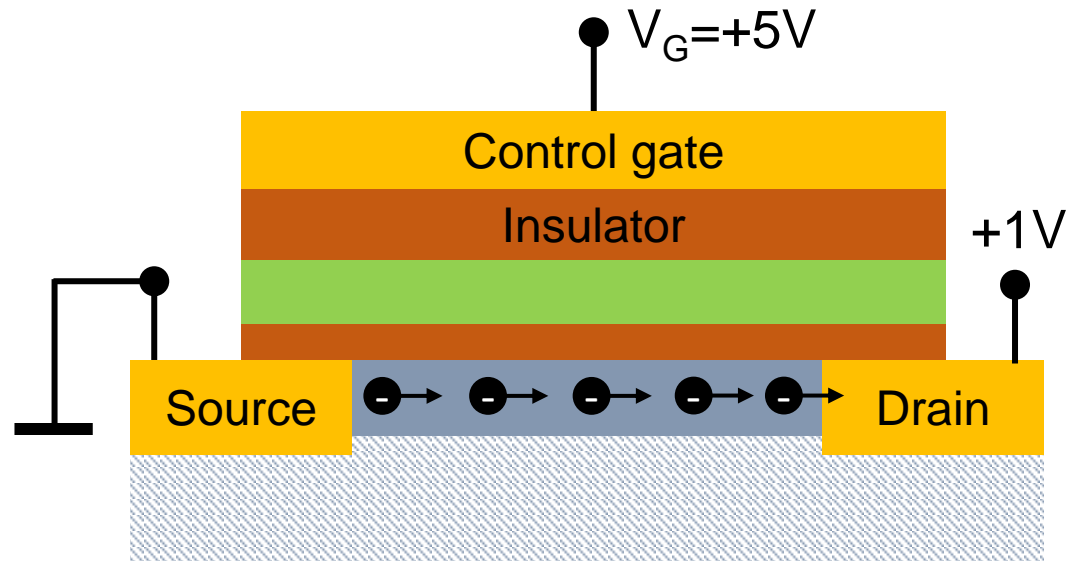
Suck out the electrons, only to Source

No electrons left in storage layer

- Reset bit "0" to "1"

Channel is in low resistance state "1"

Reading 数据读出

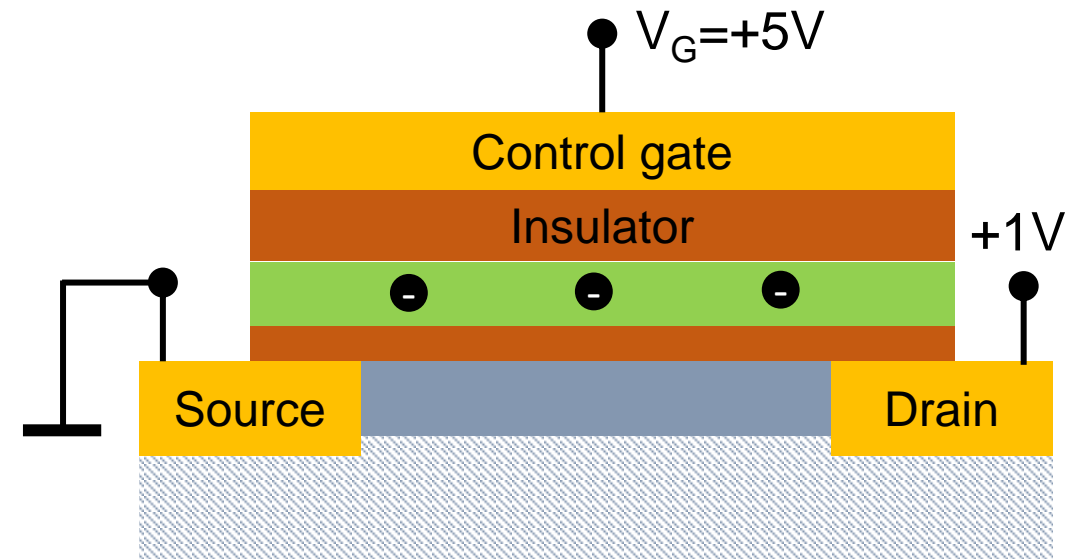


➤ Apply a medium voltage to control gate

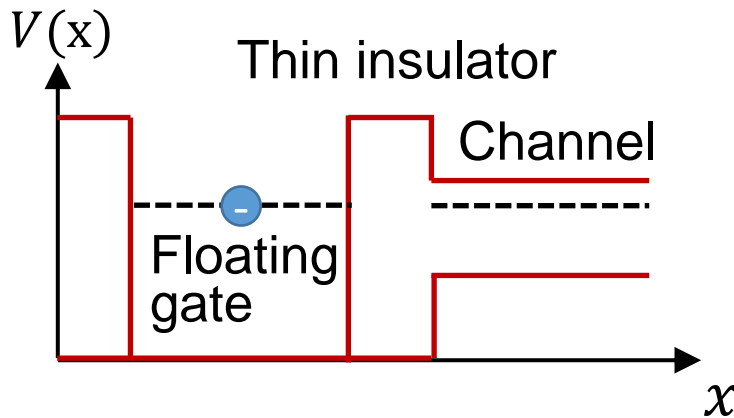
➤ Apply a small voltage to Drain

If there is no electrons in storage layer: low resistance, “1”

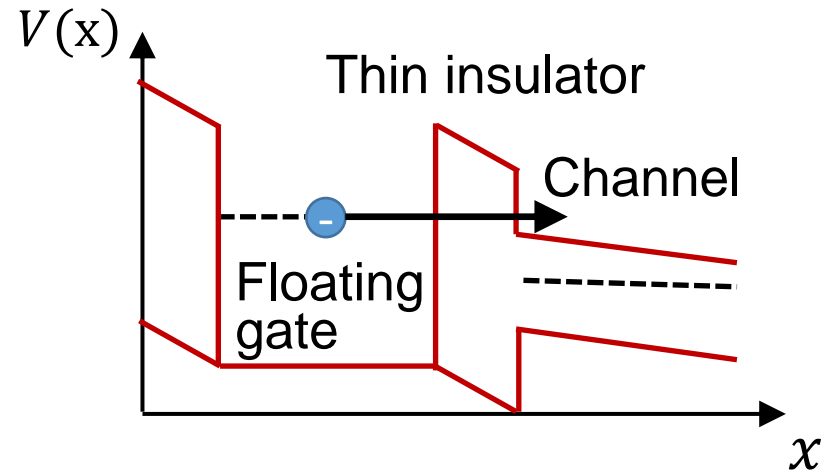
If there is no electrons in storage layer: high resistance, “0”



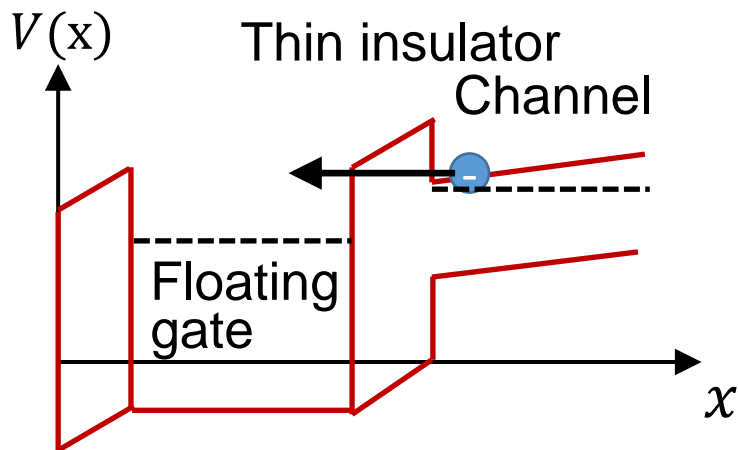
Holding information



Erasing information



Writing information

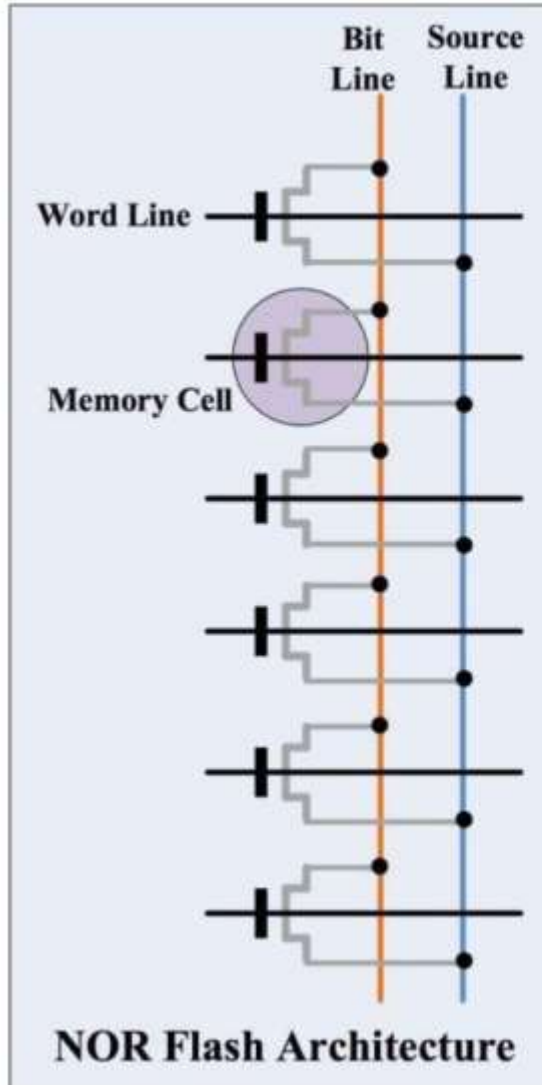


Retention: the ability to hold on to the charge

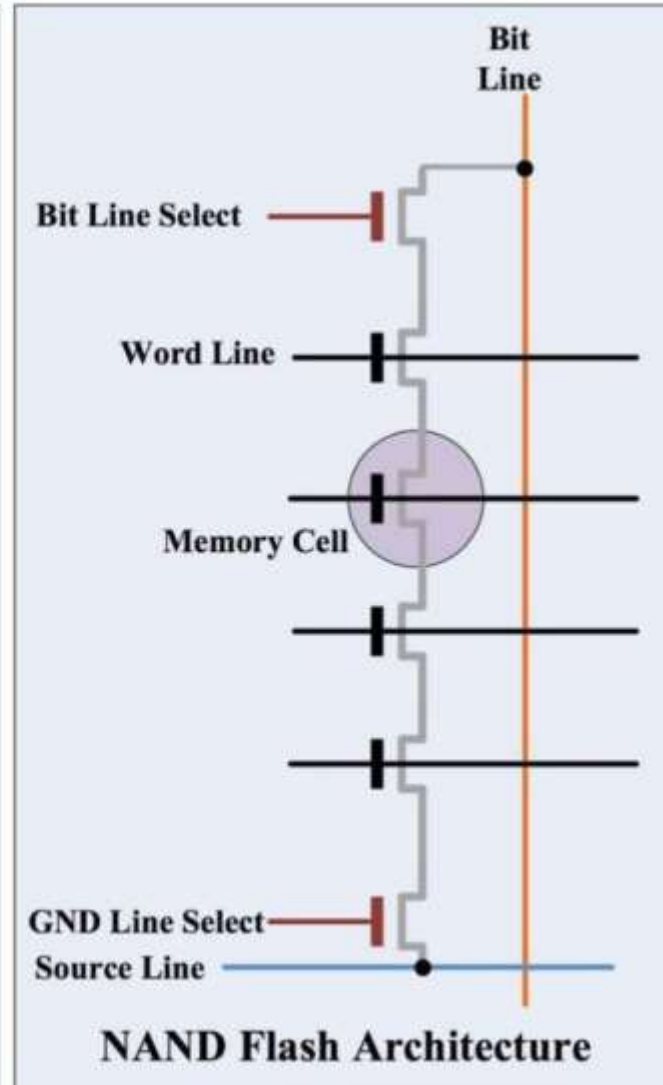
Tunnel oxide thickness	Time for 20% charge loss
4.5 nm	4.4 minutes
5 nm	1 day
6 nm	½ - 6 years

7-8nm thick oxide can retain charge in floating gate for 20 years

NOR Flash Architecture NAND Flash Architecture

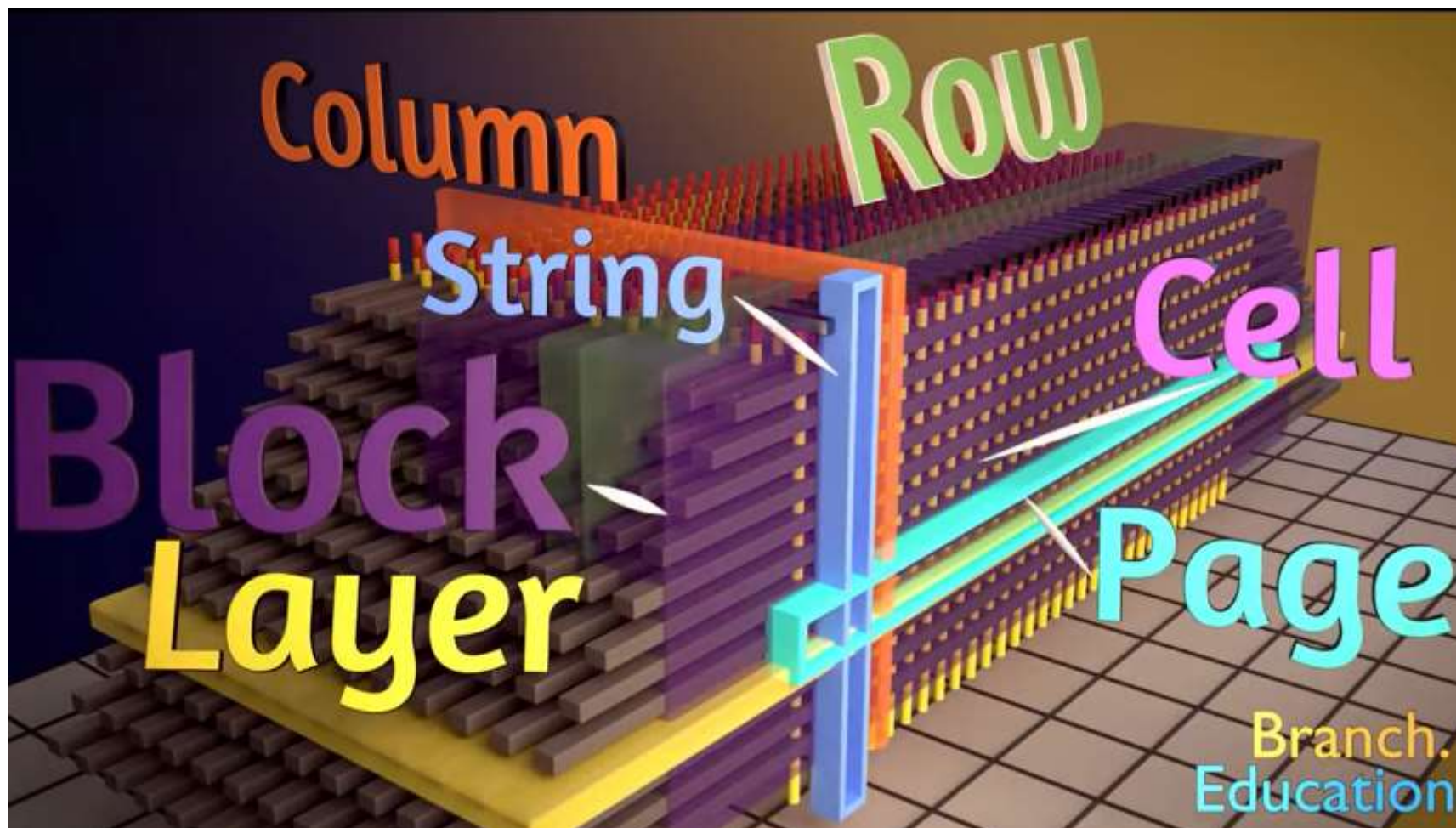


Cell (1 bytes) as the write/erase unit

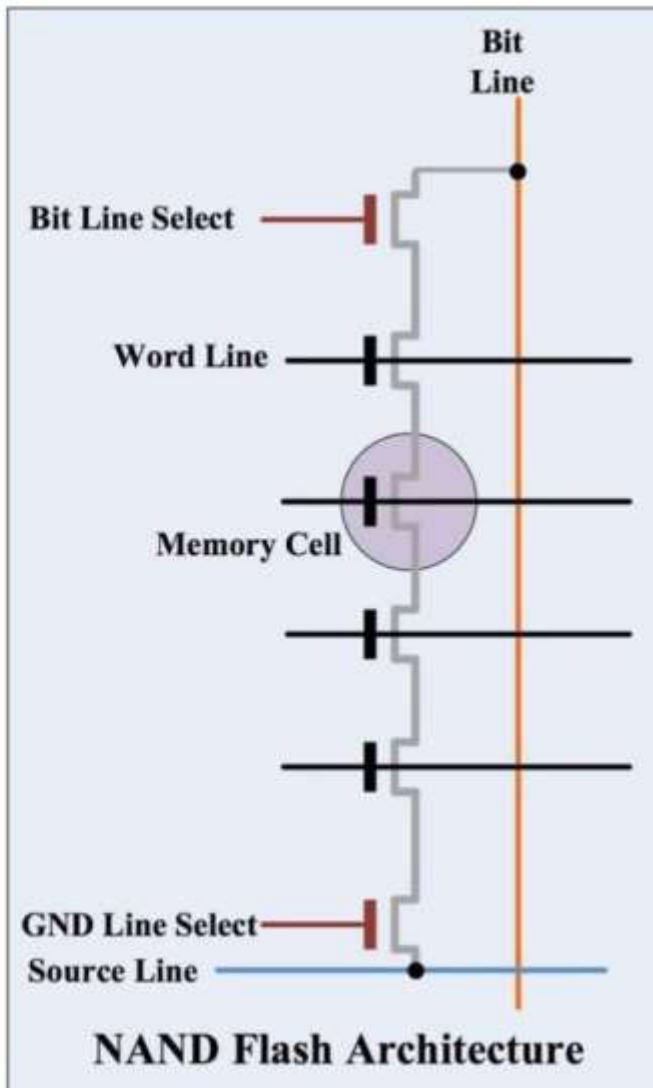
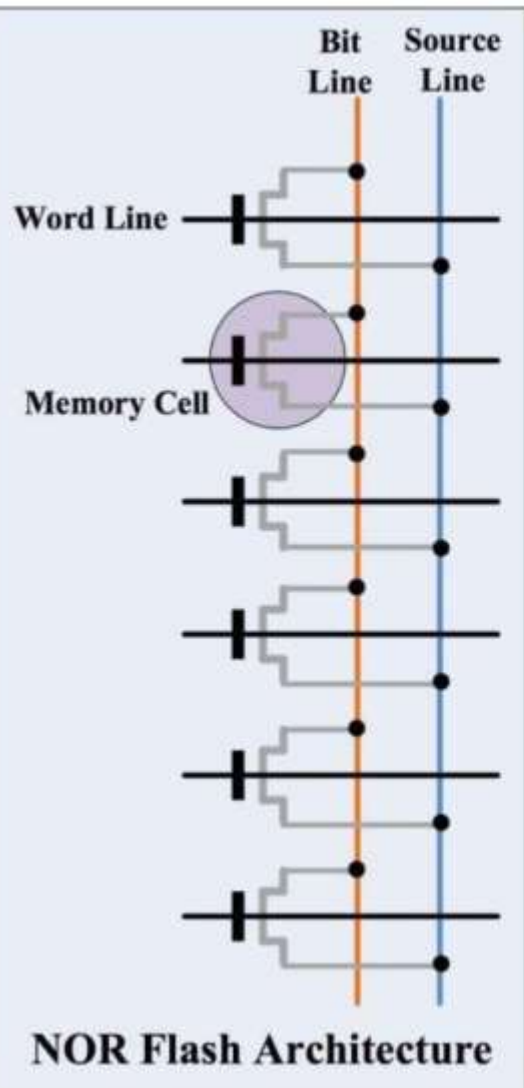


Page (2 kB) as the write/erase unit

NAND Flash Architecture



[Watch a video](#)



NOR Flash Architecture

- High reliability 可靠性高
- Fast for randomly write and read 随机读写速度快
- Relatively low capacity 容量较小

NAND Flash Architecture

- High capacity 容量大
- Faster for write 写入速度非常快
- Slower for read 读取速度慢
- Low cost 造价低

Cell (1 bytes) as the write/read unit

Page (2 kB) as the write/read unit

Feature	NOR Flash		NAND Flash	
	General	S70GL02GT	General	S34ML04G2
Capacity	8MB – 256MB	256MB	256MB – 2GB	256MB
Cost per bit	Higher	6.57×10^{-9} USD/bit for 1ku	Lower	2.533×10^{-9} USD/bit for 1ku
Random Read speed	Faster	120ns	Slower	30 μ S
Write speed	Slower		Faster	
Erase speed	Slower	520ms	Faster	3.5ms
Power on current	Higher	160mA (max)	Lower	50mA (max)
Standby current	Lower	200 μ A (max)	Higher	1mA (max)
Bit-flipping	Less common		More common	
Bad blocks while shipping	0%		Up to 2%	
Bad block development	Less frequent		More frequent	
Bad block handling	Not mandatory		Mandatory	
Data Retention	Very high	20 years for 1K program-erase cycles	Lower	10 years (typ)
Program-erase cycles	Lower	100,000	Higher	100,000
Preferred Application	Code storage & execution		Data storage	