Synthesis report

使用到的 Component

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Detailed RTL Component Info :
+---Adders :
  2 Input   32 Bit       Adders := 2  (FIR 運算只用到一個)
  2 Input    1 Bit       Adders := 1
+---Registers :
               32 Bit    Registers := 1
               12 Bit    Registers := 1
                4 Bit    Registers := 1
                2 Bit    Registers := 2
                1 Bit    Registers := 6
+---Multipliers :
             32x32  Multipliers := 1
+---Muxes :
  2 Input   32 Bit        Muxes := 7
 16 Input   32 Bit        Muxes := 1
  2 Input   12 Bit        Muxes := 5
 16 Input   12 Bit        Muxes := 2
 12 Input   12 Bit        Muxes := 1
 14 Input    4 Bit        Muxes := 1
  2 Input    4 Bit        Muxes := 1
  2 Input    3 Bit        Muxes := 1
  4 Input    2 Bit        Muxes := 1
  2 Input    1 Bit        Muxes := 45
 12 Input    1 Bit        Muxes := 1
 11 Input    1 Bit        Muxes := 2
 15 Input    1 Bit        Muxes := 2
 16 Input    1 Bit        Muxes := 2
 14 Input    1 Bit        Muxes := 1
---------------------------------------------------------------------
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```

Part Resources:

DSPs: 220 (col length:60)
BRAMs: 280 (col length: RAMB18 60 RAMB36 30)

Report Cell Usage:

	Cell	Count
1	BUFG	7
2	CARRY4	20
3	DSP48E1	3
4	LUT1	2
5	LUT2	90
6	LUT3	9
7	LUT4	55
8	LUT5	19
9	LUT6	95
10	FDRE	49
11	FDSE	1
12	LD	1
13	LDC	205
14	LDCP	3
15	IBUF	159
16	OBUF	169
