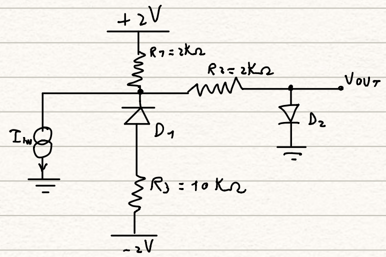
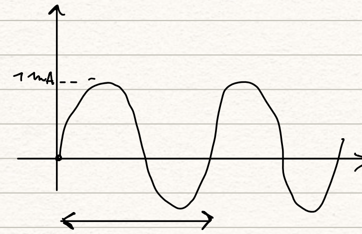
esercizio 4 prova in itinere 2018



I_{in} sinusoide:

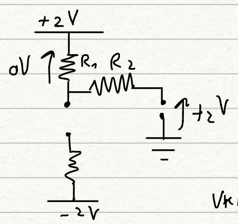
$$\begin{cases} A = 1\,mA \\ f = 500\,Hz \end{cases}$$



A) Disegnare V_{OUT}

per $I_{in} = 0$ D_1 sicuramente spento

Se D_2 fosse spento

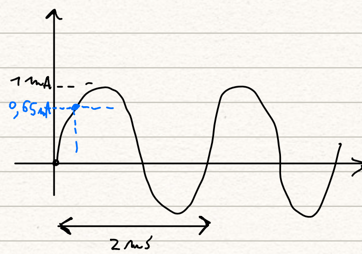


D_2 NON è spento

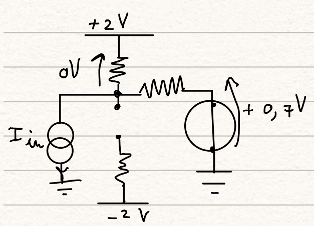
↓

D_2 è acceso

$$V_{KD1} = (2V - 0{,}7V)\frac{R_1}{R_1+R_2} = 2V - \frac{1{,}3V}{2} = 1{,}35V$$



quindi ho:



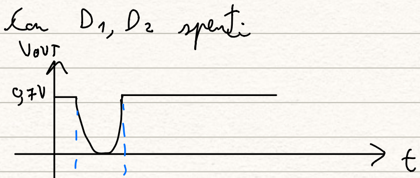
D_2 è acceso finché

$$2V - I_{in}R_1 > 0{,}7V$$

$$I_{in} < 0{,}65\,mA$$

con $I_{in} = 0{,}65\,mA$ $V_{K1} = 0{,}7V$

con D_1, D_2 spenti

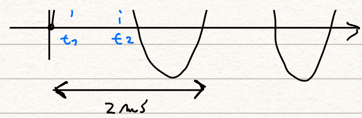


Per $I_{in} = 1\,mA$

$V_{OUT} = 2V - 1mA\,R_1 = 0V$

Per $I_{in} < 0$ D_2 è sempre acceso

$V_{OUT} = 0{,}7V$

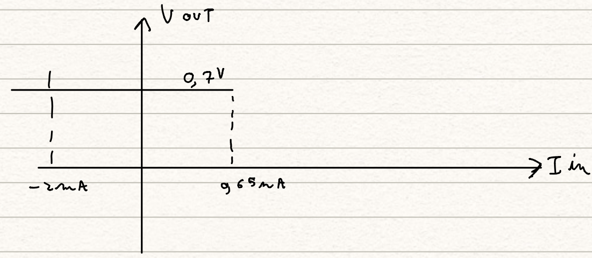


B) Tracciare la caratteristica di trasferimento del circuito $V_{OUT} - I_{in}$

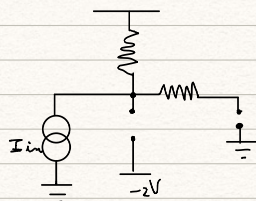
D_1, D_2 $\quad V_{BD} = -4{,}7\,V$

$I_{in} \in [-2\,mA, +2\,mA]$

per $I_{in} < 0{,}65\,mA$ $\quad D_2$ è acceso in diretta



per $I_{in} > 0{,}65\,mA$ $\quad D_2$ è spento



Se D_1 è spento

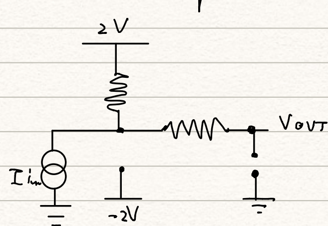
$V_{K1} = 2V - I_{in} R_1$

finché $V_{K1} > -2{,}7\,V$ $\quad D_1$ è spento

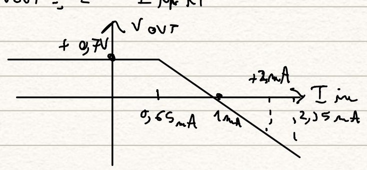
$I_{in} < 3{,}35\,mA$ $\quad$ (Hp è verificata)

Per $0{,}65\,mA < I_{in} < 2\,mA$

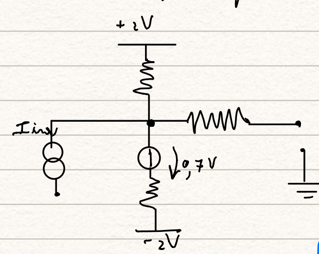
D_1 e D_2 spenti



$V_{OUT} = 2V - I_{in} \cdot R_1$



Con D_1 acceso, D_2 spento



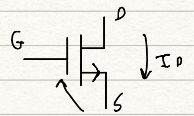
$R_1 // R_3$

$V_{OUT} = 1{,}2V - I_{in} \cdot 1{,}67\,K\Omega$

$V_{OUT_{MIN}} = -4{,}7\,V$

ESERCIZI SUI TRANSISTOR:

NMOS:



parametri

$V_{Tn} > 0$

$K_n > 0$

NMOS è acceso se

$V_{GS} > V_{TN}$ $\quad$ I_D è positiva

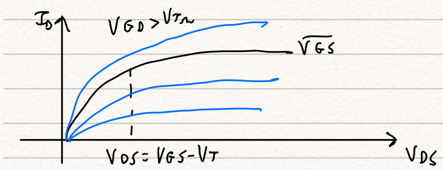
in saturazione se

$V_{DS} > V_{GS} - V_T$

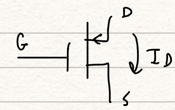
in ohmica se

$V_{DS} < V_{GS} - V_T$

$V_D - \cancel{V_S} < V_G - \cancel{V_S} - V_T$



PMOS



parametri

$V_{TP} < 0$

$K_p < 0$

PMOS è acceso se:

$V_{GS} < V_{TP}$ $\quad$ I_D è negativa

in saturazione se:

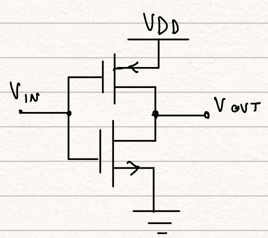
$V_{DS} < V_{GS} - V_{TP}$

in zona ohmica se

$V_{DS} > V_{GS} - V_{TP}$

$V_{GD} < V_{TP}$

INVERTER CMOS:



DATI:

$V_{DD} = 5V$

$V_{TN} = 0{,}8V$ $\quad$ $V_{TP} = -0{,}8V$

$\frac{1}{2}\mu_n C_{ox} = 75\ \mu A/V^2$

$\frac{1}{2}\mu_p C_{ox} = -30\ \mu A/V^2$

$\left.\frac{W}{L}\right|_n = \frac{2\mu m}{1\mu m}$ $\qquad$ $\left.\frac{W}{L}\right|_p = \frac{5\mu m}{1\mu m}$

$k_n = |K_p| = 150\ \mu A/V^2$

simbolo

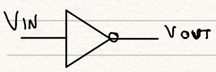
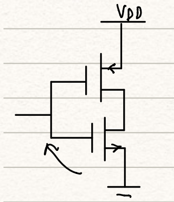
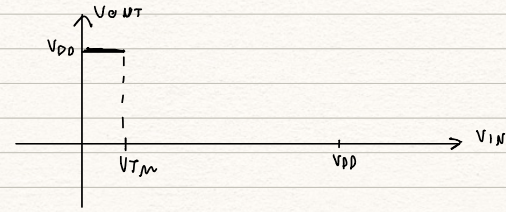


TABELLA DELLA VERITÀ:

V_{IN}	V_{OUT}
0	1
1	0

$V_{IN} = 0\,V$

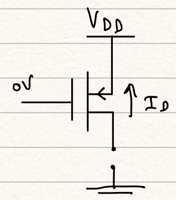




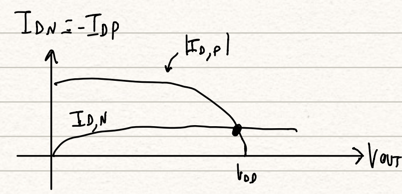
$V_{GS_N} = 0V$ NMOS spento

$V_{GS} = -5V < V_{GS_P}$ PMOS ACCESO

Con V_{IN} leggermente $> V_{TN}$ "overdrive"
NMOS è acceso con V_{OV} piccolo
$(V_{OV} = V_{GS} - V_{TN})$

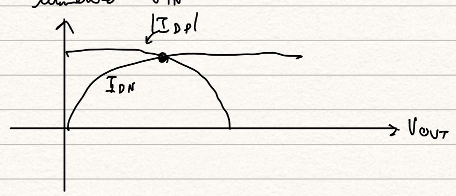


PMOS è acceso con $|V_{OV}|$ grande
$(|V_{OV}| = |V_{GS} - V_{TP}|)$



$I_D \simeq 0 \rightarrow V_{DS} = 0V \rightarrow V_D = V_S = V_{DD}$

aumento V_{IN}



Esiste un punto della caratteristica statica tale per cui sia PMOS che NMOS sono in saturazione?

(HP) NMOS e PMOS in saturazione

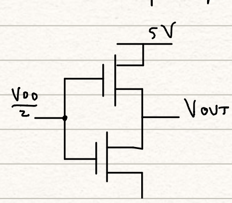
$$|K_P|\,(V_{GS_P} - V_{TP})^2 = K_n\,(V_{GS_N} - V_{TN})^2$$

$V_{GS_P} = V_{IN} - V_{DD}$; $V_{GS_N} = V_{IN}$

$$|K_P|(V_{IN} - V_{DD} - V_{TP})^2 = K_n\,(V_{IN} - V_{TN})^2$$

$$V_{IN} = \frac{V_{DD}}{2}$$

V_{OUT} può assumere qualunque valore purché entrambi i MOS siano in saturazione



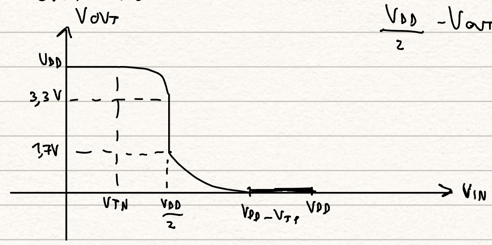
NMOS è in saturazione
$V_{GD} < V_{TN}$
$\frac{V_{IN}}{2} - V_{OUT} < V_{TN}$

pMOS è in saturazione

$V_{GD} > V_{TP}$

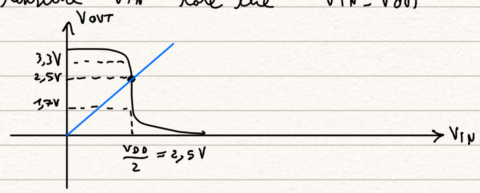
$\frac{V_{DD}}{2} - V_{OUT} > V_{TP} \longrightarrow V_{OUT} < \frac{V_{DD}}{2} - V_{TP}$

CARATTERISTICA STATICA



SOGLIA LOGICA:

tensione V_{IN} tale che $V_{IN} = V_{OUT}$



$V_{Th} = \frac{V_{DD}}{2} = 2{,}5\ V$

Calcolare V_{Th} con NMOS e PMOS con W=L=1μm:

$K_n = 75\ \mu A/V^2$

$K_p = -30\ \mu A/V^2$

Hp: entrambi i mos siano accesi

per definizione $V_{IN} = V_{OUT} \longrightarrow V_{GD} = \emptyset V \rightarrow$ entrambi i mos in saturazione

$I_{Dn} = -I_{Dp}$

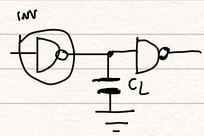
$K_n (V_{GSn} - V_{TN})^2 = |K_p| (V_{GSp} - V_{TP})^2$

$K_n (V_{Th} - V_{Tn})^2 = |K_p| (V_{Th} - V_{DD} - V_{TP})^2$

SOLUZIONE $V_{Th} = 2{,}11\ V$

$K_n = -K_p$

COMPORTAMENTO DINAMICO:



consideriamo $C_L = 0{,}5\ pF$

Tempi di propagazione → per raggiungere la soglia logica della porta successiva

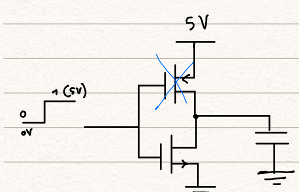
t_{PHL}

t_{PLH}

ritardo di propagazione

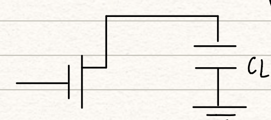
$$\tau_p = \frac{t_{PHL} + t_{PLH}}{2}$$

t_{PHL} dell'uscita $(1 \longrightarrow 0) \longrightarrow$ quando ingresso $0 \longrightarrow 1$ istantaneamente

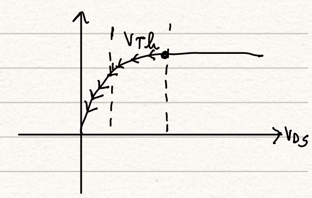


$V_C(0_-) = +5V$

$V_{CL}(0^+) = 5V$



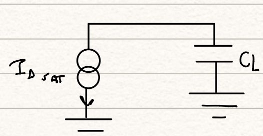
$V_{DS}(0^+) = 5V$



APPROSSIMAZIONI PER CALCOLARE I TEMPI:

1) approssimazione satura

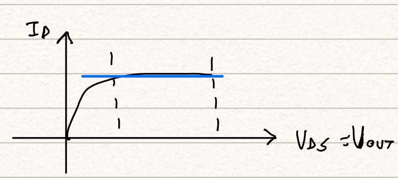
$I_D = I_{DSAT}$



$\Delta V = V_{DD} - \frac{V_{DD}}{2} = 2{,}5V$

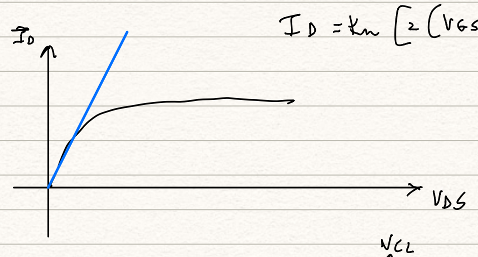
$I_{DSAT} = K_n (V_{GS} - V_{TN})^2 = 150\mu A/V^2 (5V - 0{,}8V)^2 = 2{,}65\ mA$

$t_{PHL} = \frac{C_L}{I_{DSAT}} \Delta V = \frac{0{,}5\ pF}{2{,}65\ mA} \cdot 2{,}5V = 472\ ps$ → sottostima del tempo di propagazione



2) approssimazione ohmica

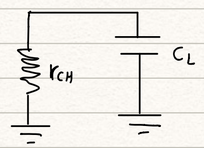
$r_{CH} = R_{DS_{ON}}\big|_{V_{DS}\simeq 0}$

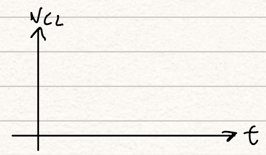


$$I_D = k_n\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right]$$

$$\frac{\partial I_D}{\partial V_{DS}} = k_n\left[2\left(V_{GS}-V_{Tn}\right)-2V_{DS}\right]$$

$$r_{CH} = \frac{1}{2k\left(V_{GS}-V_{Tn}\right)} = 794\,\Omega$$





$\tau = R_{Th}\cdot C_L$

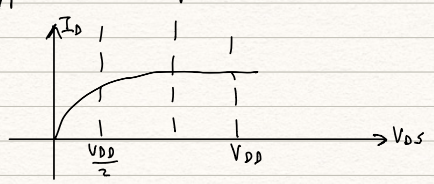
$V_{CL} = 5V\cdot e^{-\frac{t}{\tau}}$

↓

raggiunge $\frac{V_{DD}}{2}$

$t_{PHL} = 0{,}69\; r_{th}\, C_L = 274$ ps

3) approssimazione per eccesso



$$t_{PHL} = t_{PHL}^{SAT} + t_{PHL}^{OHMICA}$$

t_{PHL}^{SAT}

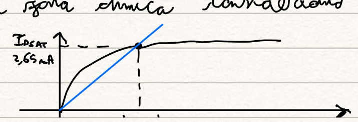
$\Delta V = V_{DD} - \left(V_{GS}-V_T\right) = 5V - 4{,}2V = 0{,}8V$

$I_{DSAT} = 2{,}65$ mA

$C_L = 0{,}5$ pF

$$t_{PHL}^{SAT} = \frac{C_L}{I_{DSAT}}\cdot\Delta V = \frac{0{,}5\,pF}{2{,}65\,mA}\cdot 0{,}8V = 151\text{ ps}$$

in zona ohmica consideriamo R_{eq}



| $V_{GS}-V_T$

$t_{PHL}^{OHMICA} = 410\ ps$

$t_{PHL} = 151\,ps + 410\ ps = 561\ ps$ → sottostimiamo <u>la corrente</u>