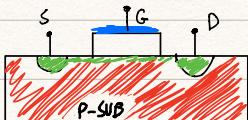


## IL TRANSISTORE P-MOSFET (e differenze con l'N MOSFET)

N MOSFET



- $V_{Tn} > 0$ , canale di elettroni

- substrato di tipo P

- zona ohmica

$$V_{GSn} > V_{Tn}$$

$$V_{GDr} > V_{Tr}$$

$$V_{GD} = V_G - V_D = V_G - V_S + V_S - V_D = V_{GS} - V_{DS}$$

$$\downarrow V_{GD} = V_T$$

$$V_{GS} - V_{DS} = V_T \rightarrow V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [2(V_{GS} - V_{Tn})V_{DS} - V_{DS}^2]$$

FATTORE DI TRANSDUTTANZA

$$[K_n] = \frac{I}{V^2} \quad \left[ \frac{mA}{V^2} \right]$$

$$K_n > 0$$

- zona di saturazione

$$V_{GSn} > V_{Tn}$$

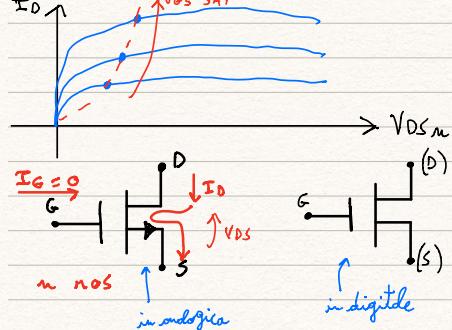
$$V_{GDr} < V_{Tr}$$

$$I_D = K_n (V_{GSn} - V_{Tn})^2$$

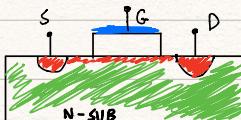
- MOS aperto

$$V_{GSn} < V_{Tn} \quad \text{non c'è canale}$$

$$V_{GDr} < V_{Tr} \quad V_{GS} \text{ SAT}$$



P MOSFET



- $V_{Tp} < 0$ , canale di lacune

- substrato di tipo n

- MOS off, no canale

$$V_{GSp} > V_{Tp}$$

$$V_{GDr} > V_{Tp}$$

- MOS acceso

$$V_{GSp} < V_{Tp} \quad \text{canale laterale source}$$

$$V_{GD} < V_{Tp}$$

canale laterale drain

(pinch-off laterale drain)

↓

zona ohmica

$$V_{GD} > V_{Tp}$$

canale laterale drain

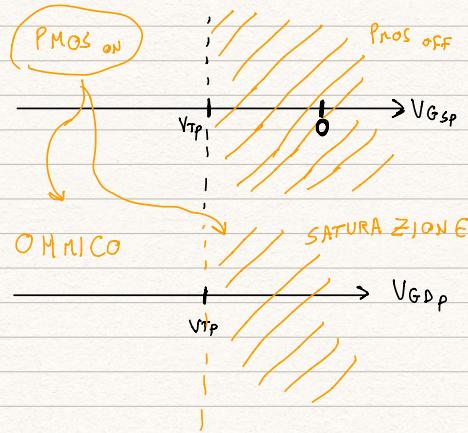
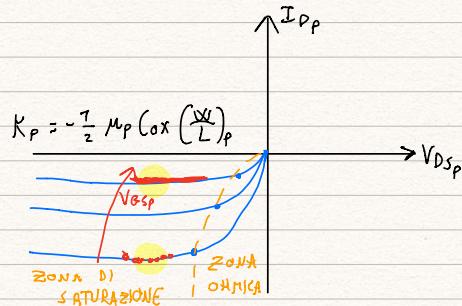
(pinch-off laterale drain)

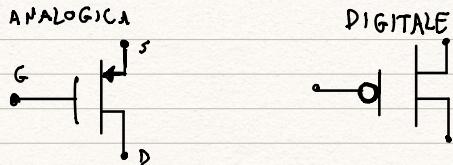
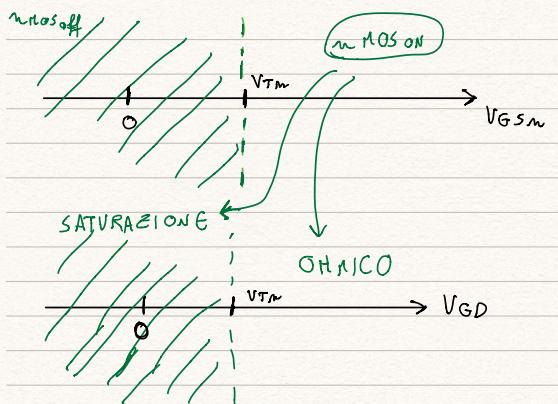
↓

zona di saturazione

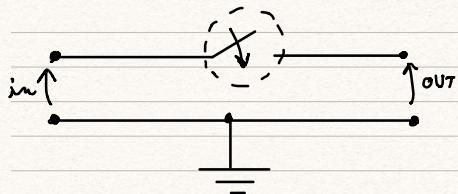
$$I_{Dp} = K_p [2(V_{GSp} - V_{Tp})V_{DSp} - V_{DSp}^2]$$

$$I_{Dp} = K_p (V_{GSp} - V_{Tp})^2$$





### TRANSISTORE MOS COME INTERRUTTORE:



- interruttore aperto → circuito aperto
- ↙ OUT e in scarico
- mos aperto
- interruttore chiuso → cortocircuito
- ↙ OUT e in cortocircuito
- mos acceso
- in zona ohmica

#### • MOS ACCESO IN ZONA OHMICA:

$$R_{DS_{on}} \triangleq \left. \frac{\partial V_{DS}}{\partial I_{DS_{on}}} \right|_{V_{DS}=0} = \left[ \frac{1}{\left. \frac{\partial I_{DS_{on}}}{\partial V_{DS}} \right|_{V_{DS}=0}} \right] \quad \begin{cases} V_{G_S_m} > V_{T_m} \\ V_{G_D_m} > V_{T_m} \end{cases}$$

(in mos)

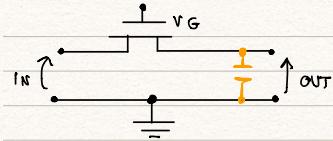
$$I_D = K_m \left[ 2 \left( V_{G_S_m} - V_{T_m} \right) V_{DS_m} - V_{DS_m}^2 \right]$$

$$\frac{\partial I_{DS_{on}}}{\partial V_{DS}} = 2 K_m \left( V_{G_S} - V_{T_m} \right) - 2 K_m V_{DS} \underset{V_{DS_m}=0}{\cancel{= 0}}$$

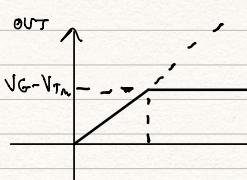
$$R_{DS_{on}} = \frac{1}{2 \left[ \frac{1}{2} \mu_m C_{ox} \frac{W}{L} \left( V_{G_S_m} - V_{T_m} \right) \right]} \quad \text{TENSIONE DI OVERDRIVE}$$

FATTORE DI FORMA  
un transistor più "lungo" ha resistenza minore

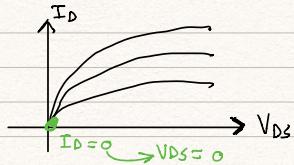
### PORTA DI TRASMISSIONE nMOS:



\*  $\begin{cases} V_{GS} < V_{Tn} \\ V_{GD} < V_{Tn} \end{cases} \rightarrow \text{NMOS off}$   
 IN e OUT scollegati



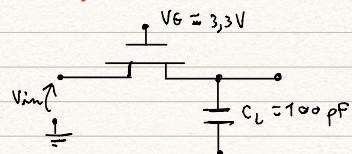
\*  $V_{GS} > V_{Tn}$  NMOS on



$$V_G - V_{GT} = V_{Tn}$$

$$IN = V_G - V_{Tn}$$

esercizio:



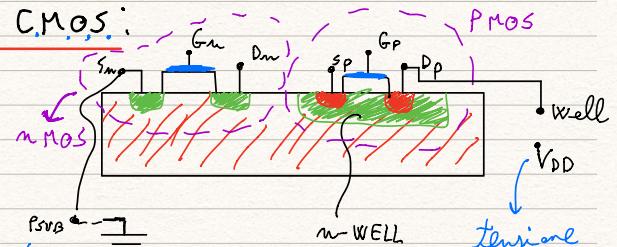
$$V_{Tn} = 0,8V$$

(a)  $V_{OUT}$  se  $V_{IN} = 0V$ ?  
 (cerca i tranzistori)

(b)  $V_{OUT}$  se  $V_{IN} = 3,3V$ ?  
 (cerca i tranzistori)

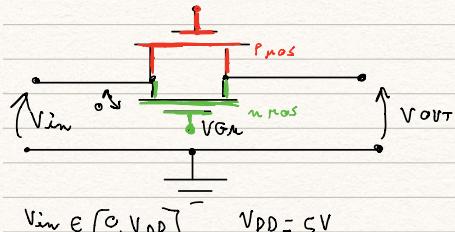
### PORTE DI TRASMISSIONE C.MOS:

- Complementary
- Metal
- Oxide
- Semiconductor



per polarizzare il diodo  
 porosità in inversa

tensione  
 più positiva  
 possibile,  
 per polarizzare  
 il diodo porosità  
 in inversa



$$* V_{Gn} = 0, V_{Gp} = 5V - V_{DD}$$

$V_{IN} = 0V$  NMOS interdetto

$V_{IN} = 5V$  PMOS interdetto

NMOS on

$$I_D = 0 \rightarrow V_{DS} = 0$$

$$V_{OUT} = 0$$

PMOS interdetto

$$* V_{Gn} = V_{DD}, V_{Gp} = 0V$$

$$V_{IN} = V_{DD}$$

ad esempio  $V_{Gn} = 0V$

$$\downarrow$$

$$V_{Gp} = V_{DD} (5V)$$

$$* V_{Gm} = V_{DD}, V_{Ep} = 0V$$

$$V_{in} = V_{DD}$$

per os accendere

$$V_{out} = V_{DD}$$

$$V_{out} = V_{in}$$

### VANTAGGI:

- $V_{out} = V_{in}$  senza necessità di  $V_G$  maggiore dell'intervallo di tensione di  $V_{in}$
- $R_{DS_{on,off}} = R_{DS_{on,n}} // R_{DS_{on,p}}$ , più piccolo di quello di un solo transistor

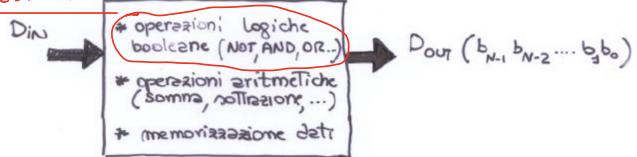
### SVENTAGGI:

- 2 transistori complementari con tensioni di comando duali

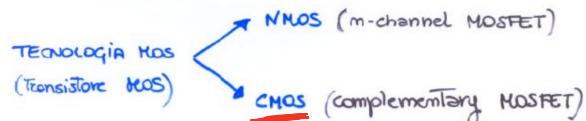
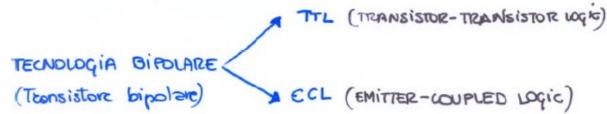
## LOGICA CMOS

### \* SISTEMA DIGITALE

IN QUESTO CORSO

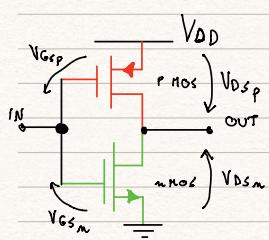


### \* FAMIGLIE LOGICHE



C. Guazzoni, Fondamenti di Elettronica

## INVERTER CMOS:



$$V_{GSn} = IN - 0 = IN$$

$$V_{DSn} = OUT - 0 = OUT$$

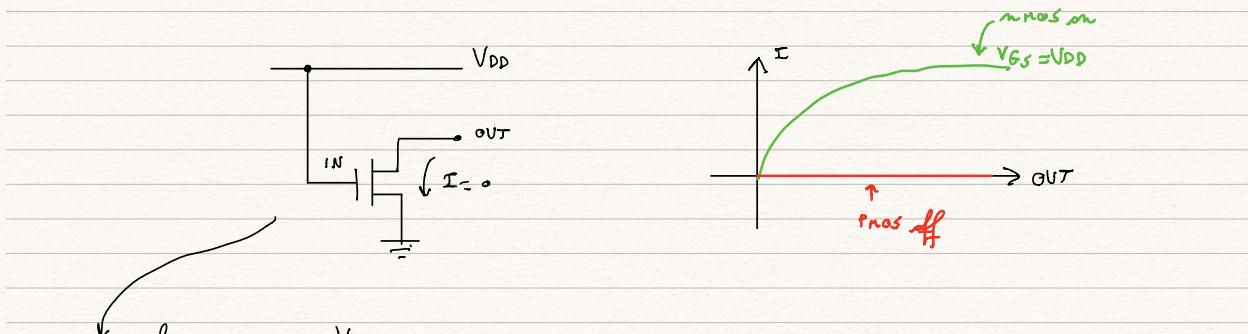
$$V_{GSp} = IN - V_{DD}$$

$$V_{DSp} = OUT - V_{DD}$$

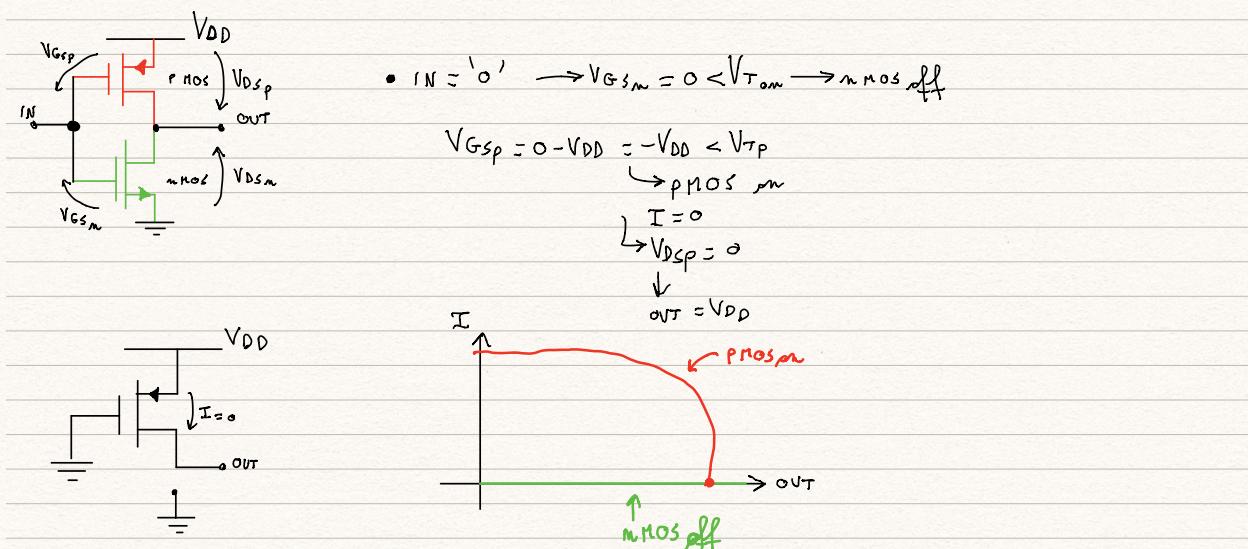
$$IN = 1 \rightarrow IN = V_{DD}$$

$$V_{GSn} = V_{DD} > V_{Tn} \rightarrow nMOS \text{ on}$$

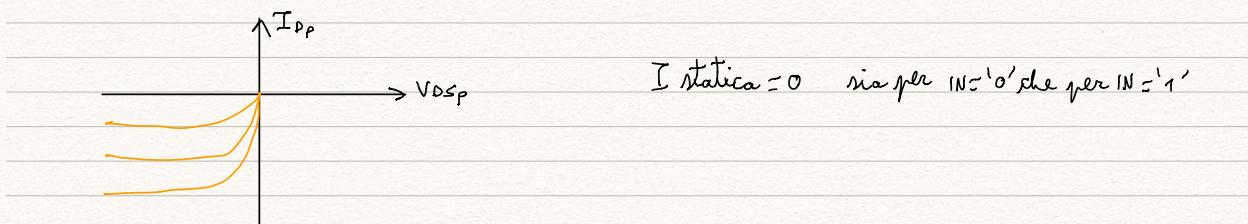
$$V_{GSp} = V_{DD} - V_{DD} = 0 \rightarrow pMOS \text{ off}$$



nMOS chiuso con  $V_{DSn} = 0$   
 $\rightarrow OUT = 0V \rightarrow OUT = '0'$

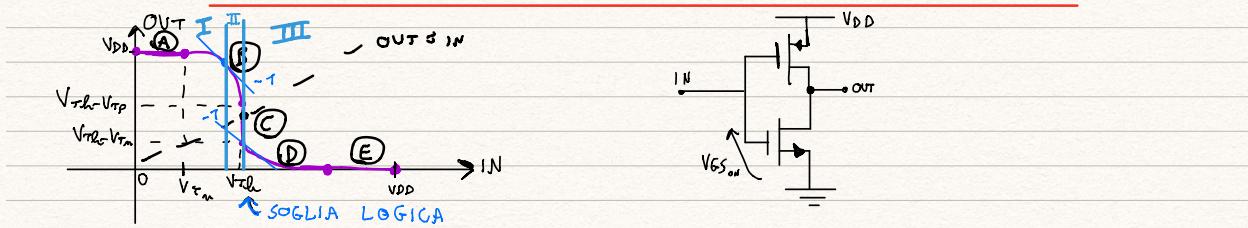


caratteristica IV pmos



$I_{statica} = 0$  ma per  $IN = '0'$  che per  $IN = '1'$

### CARATTERISTICA DI TRASFERIMENTO STATICO:

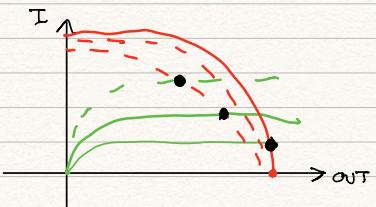


(A) nMOS off

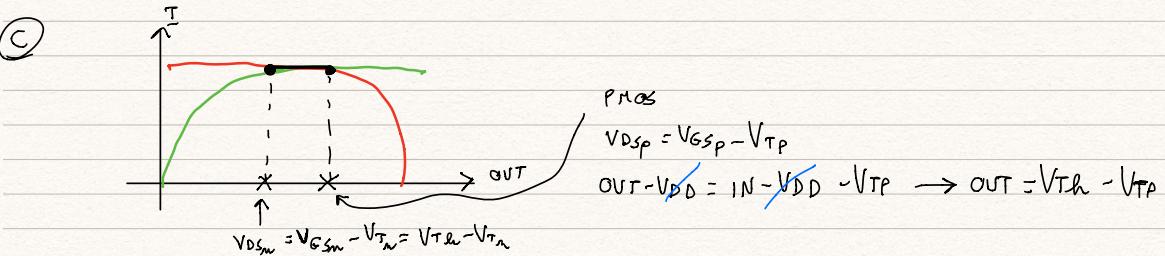
pMOS on in zona ohmica



(B) nMOS on in zona di saturazione  
pMOS on in zona ohmica



(C)



$$\frac{1}{2} \mu_n C_{ox} \left( \frac{w}{L} \right)_n = \frac{1}{2} \mu_p C_{ox} \left( \frac{w}{L} \right)_p \quad \rightarrow \mu_n \left( \frac{w}{L} \right)_n = \mu_p \left( \frac{w}{L} \right)_p$$

*INVERTER SIMMETRICO*

$K_n = |K_p|$

### CALCOLO DELLA SOGLIA LOGICA:

$$I_{Dn, \text{sat}} = |I_{Dp, \text{sat}}|$$

$$K_n (V_{GSn} - V_{Tn})^2 = |K_p| (V_{GSp} - V_{Tp})^2$$

*inverter simmetrico*

$K_n = |K_p|$

$$(IN - V_{Tn})^2 = [(IN - V_{DD}) - V_{Tp}]^2 \quad V_{Tn} = |V_p| = V_T > 0$$

$$(IN - V_T)^2 = [(IN - V_{DD}) + V_T]^2$$

estraggo le radici quadrate

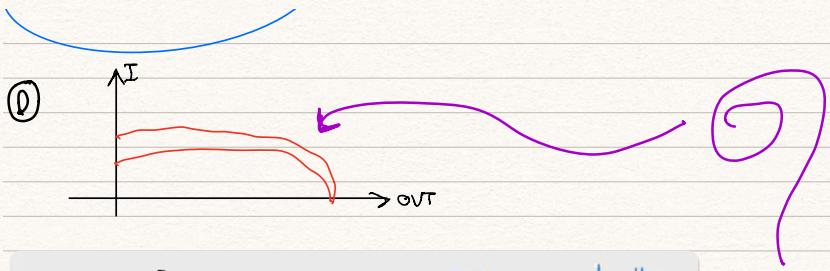
$$IN - V_T = [(IN - V_{DD}) + V_T]$$

$$IN - V_T = IN + V_{DD} - VT$$

$$2 IN = V_{DD}$$

$$IN \underset{\text{SOGLIA LOGICA}}{\stackrel{\triangle}{=}} V_{Thn} = \frac{V_{DD}}{2}$$

SOGLIA LOGICA DI COMMUTAZIONE



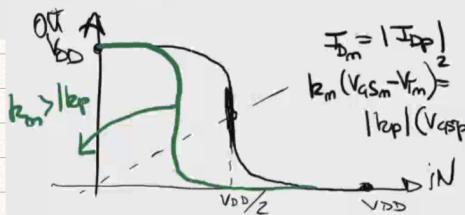
$V_{IL} = \max$  IN interpretato come livello logico basso

$V_{IH} = \min$  IN interpretato come livello logico alto.

### EFFETTO DELLA TENS. DI ALIMENTAZ.



INVERTER NON SIMMETRICO



$$I_D = |I_{DP}|$$

$$k_m(V_{GSm} - V_{fm})^2 = |I_{DP}|(V_{GSp} - V_{Tp})^2$$

