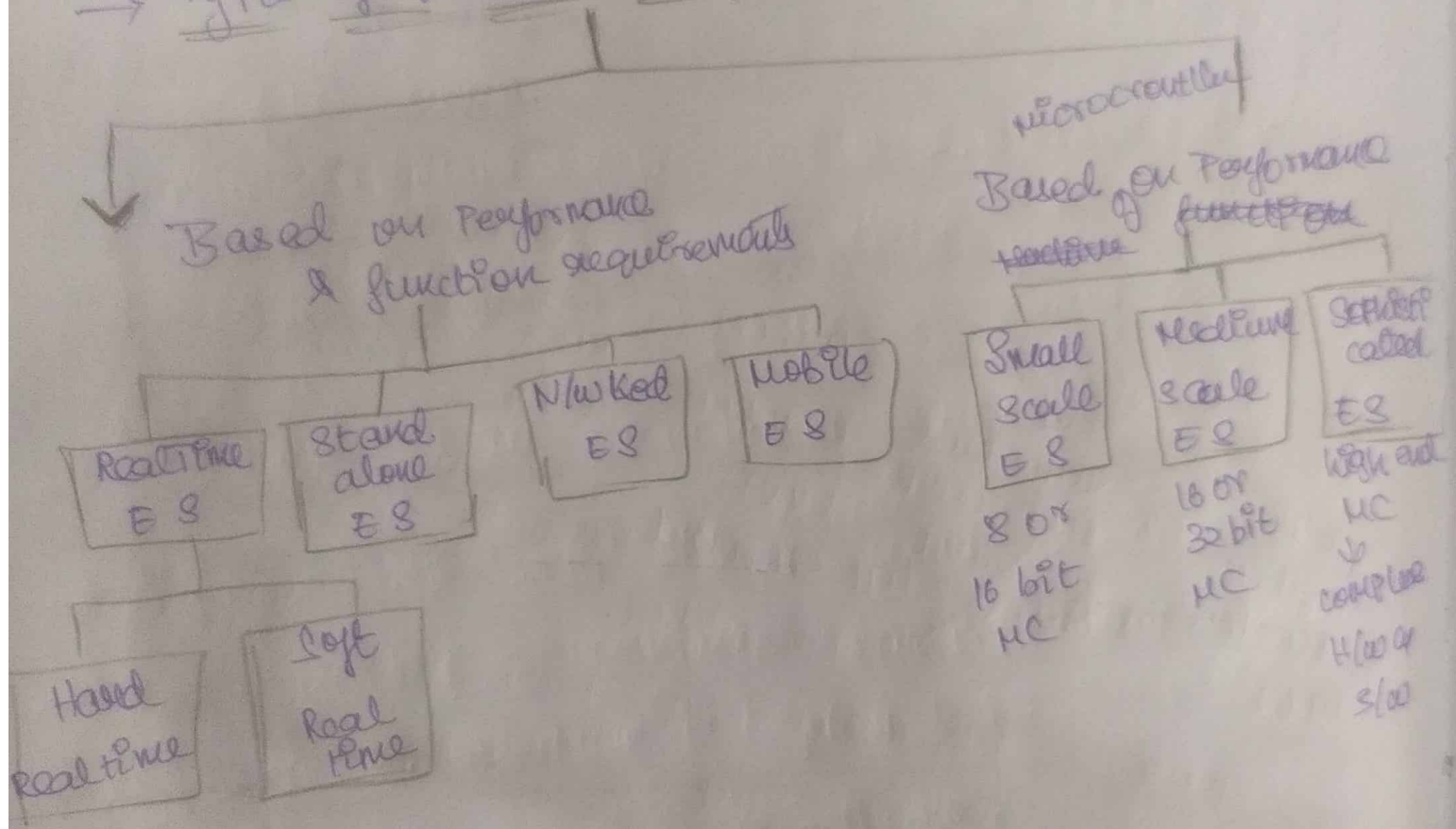


→ Embedded Systems <sup>special purpose</sup> 2m

\* It is a combination of hardware & software to perform a specific task throughout the life time.

→ Types of Embedded Systems :-



## → Types of Computers :-

Special Purpose Computer

Developed to perform the spec spec.

Eg:- calculator, washing machine ac etc...

General Purpose Computer

Developed

to perform more than one task.

Eg:- Laptop, Mobile phone etc.

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## → Components of ES :-

### ES Hardware components

Power Supply

Micro-controller  
8, 16, 64 bit.

Memory  
RAM, ROM, EPROM, flash

Timer/Counter  
ON, OFF  
or compressed  
or 8-compressed

Communication Port

→ transmit & receive

→ compare → USB → ext

→ simple one mode of com

Serial  
16 bit

Par  
8 bit

I/P  
O/P  
Port



## → Application :-

\* Consumer Electronics.

\* Industrial Machinery.

\* Automobiles.

\* Agriculture.

\* Processing Industrial Devices.

\* Airplanes.

\* Digital watches.

\* Digital camera.

\* Washing Machine.

\* AC.

\* Mobile device etc.

UI → NO User Interface

GUI →

PSU

## → Automated System → no human interface <sup>essence</sup>..

\* Conveyor belt with sensor count no. of filled bottles, display on computer screen without human interference.

## → Electrical Circuit :-

\* Printed Circuit Board

\* Resistors

\* Capacitors

\* Inductors

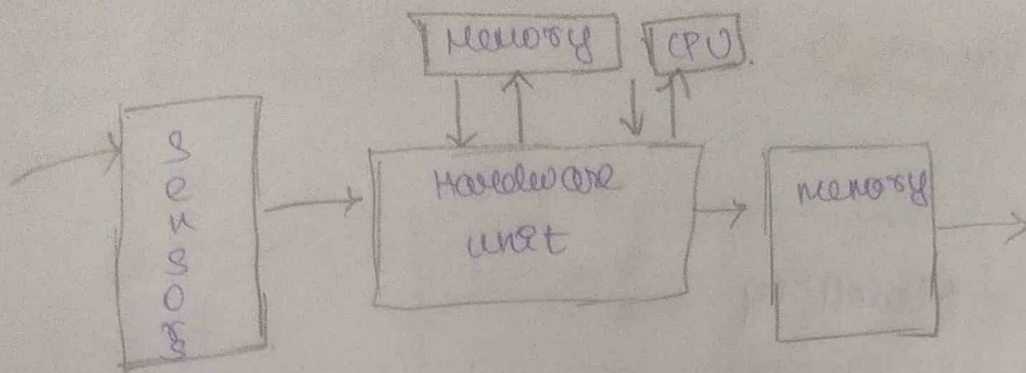
\* Transistors,

\* DIODES

\* Integrated Circuit

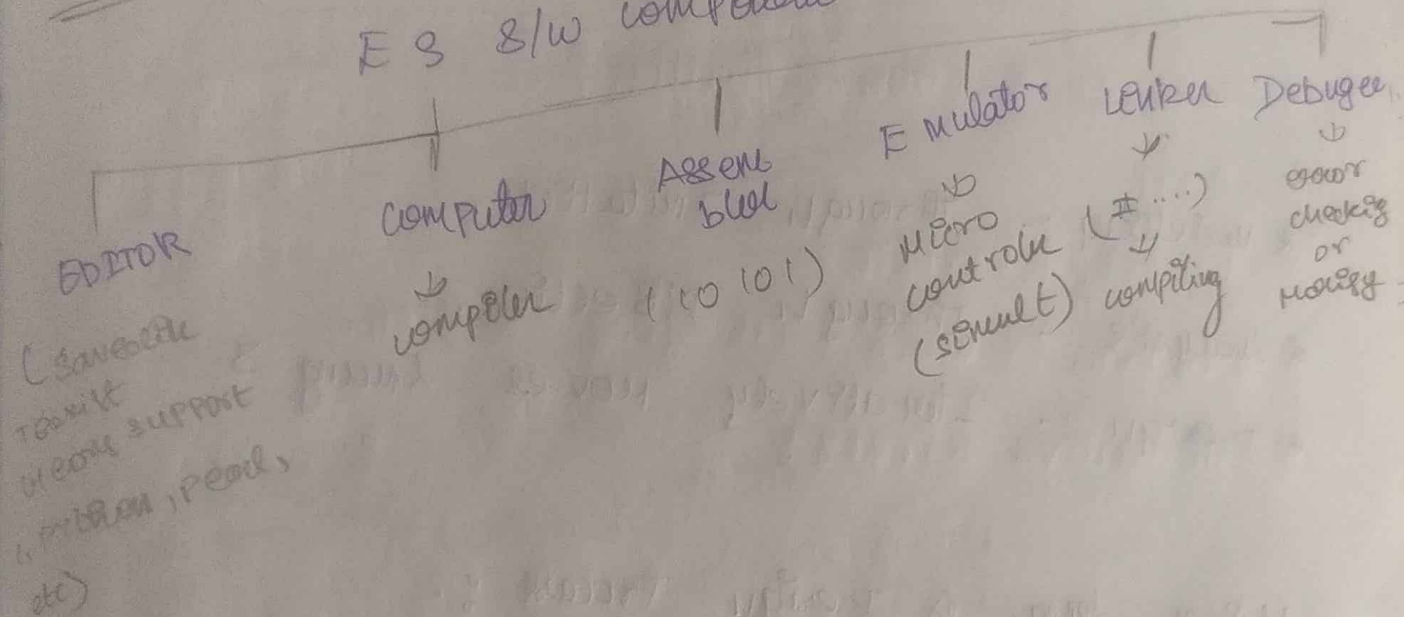
\* LED (Light Emit Diode)

\* LCD. (Liquid crystal display)

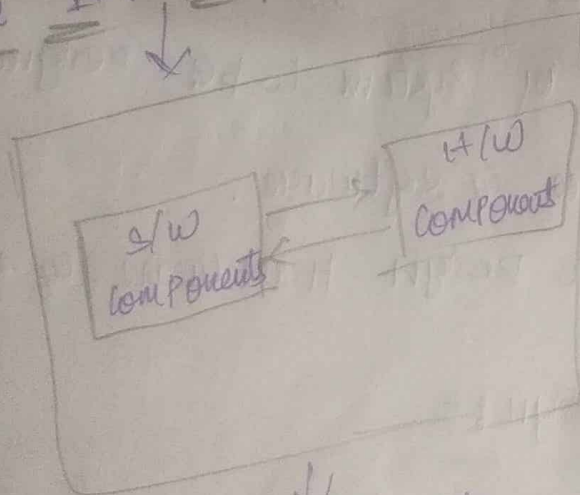


→ Embedded system software

ES s/w component



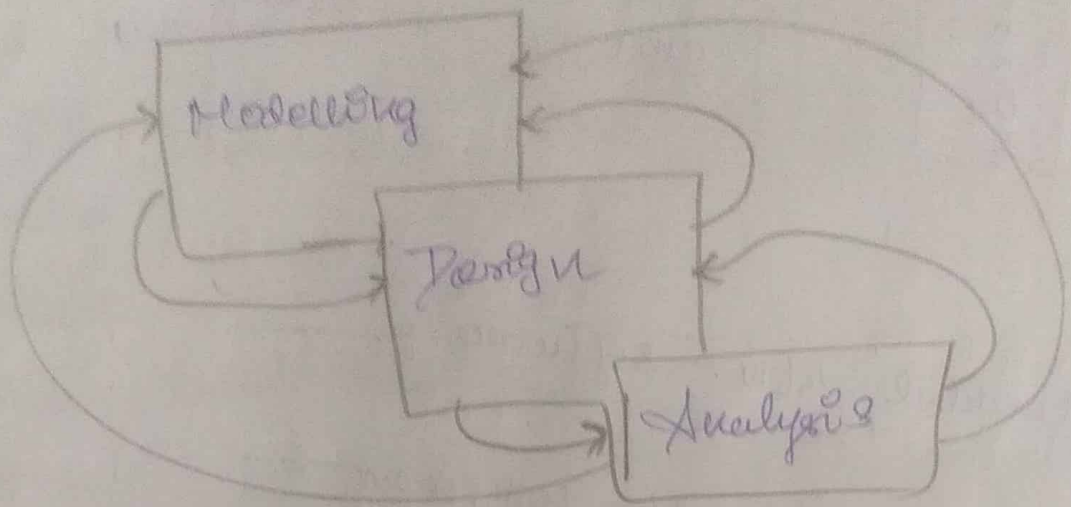
→ System INPUT



↓  
System b/p.



## → Design Process D ES:



\* Modelling :- Through Initiation.

\* Analysis :- Through Dissection.

\* Design :- Iteratively moves among 3

## → Major Area of Design Process :-

\* Sound Software & Hardware Specifications.

\* Formulate architecture of system to be designed.

\* Partitioning Hardware & Software.

\* Iterative Approach to Design Hardware & Software.

## → Important Steps in Design :-

① Requirements

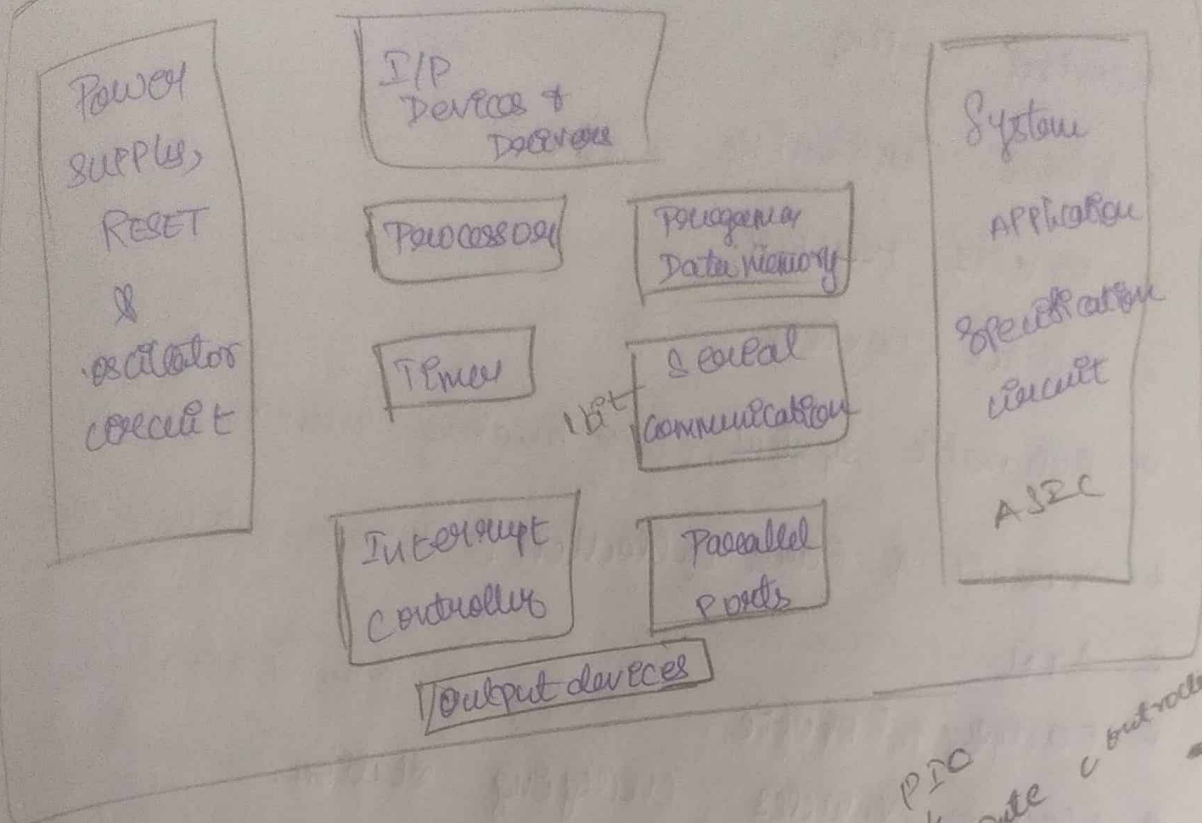
⑤ Prototyping

② System Specification

③ Functional Design

④ Architecture Design

## YES Hardware :-



## Other Hardware :-

- \* ADC
- \* DAC
- \* LED
- \* LCD

\* Keypad

PIC  
+  
Port Data controller  
Peripheral

## Software :-

C, C++, DOTNET, Simulator - MASM.  
Compiler - KEIL

## Requirements :-

- \* Reliability
- \* Cost - effectiveness
- \* Low power consumption
- \* Efficient -> use of processing power.
- \* Appropriate execution time.

ASIC  
↓  
APP of Data circuit



→ Embedded Examples :-

= cure all sort from Malaria  
Cholera, Chancery etc.

\* Inter.     Putnabive     Experience  
\* Ors      $\downarrow$       $\downarrow$   
free  $\rightarrow$  complete     working Machine

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# → Embedded Programming Languages :- 12m

- |           |              |                |           |
|-----------|--------------|----------------|-----------|
| * C       | * Java       | * ELIker       | * Arduino |
| * C++     | * VHDL       | * FORTH        |           |
| * C#      | * Embedded C | * TcL          |           |
| * Verilog | * Python     | * Erlang       |           |
| * Rust    | * LABVIEW    | * Ladder Logic |           |
| * LUA     |              |                |           |

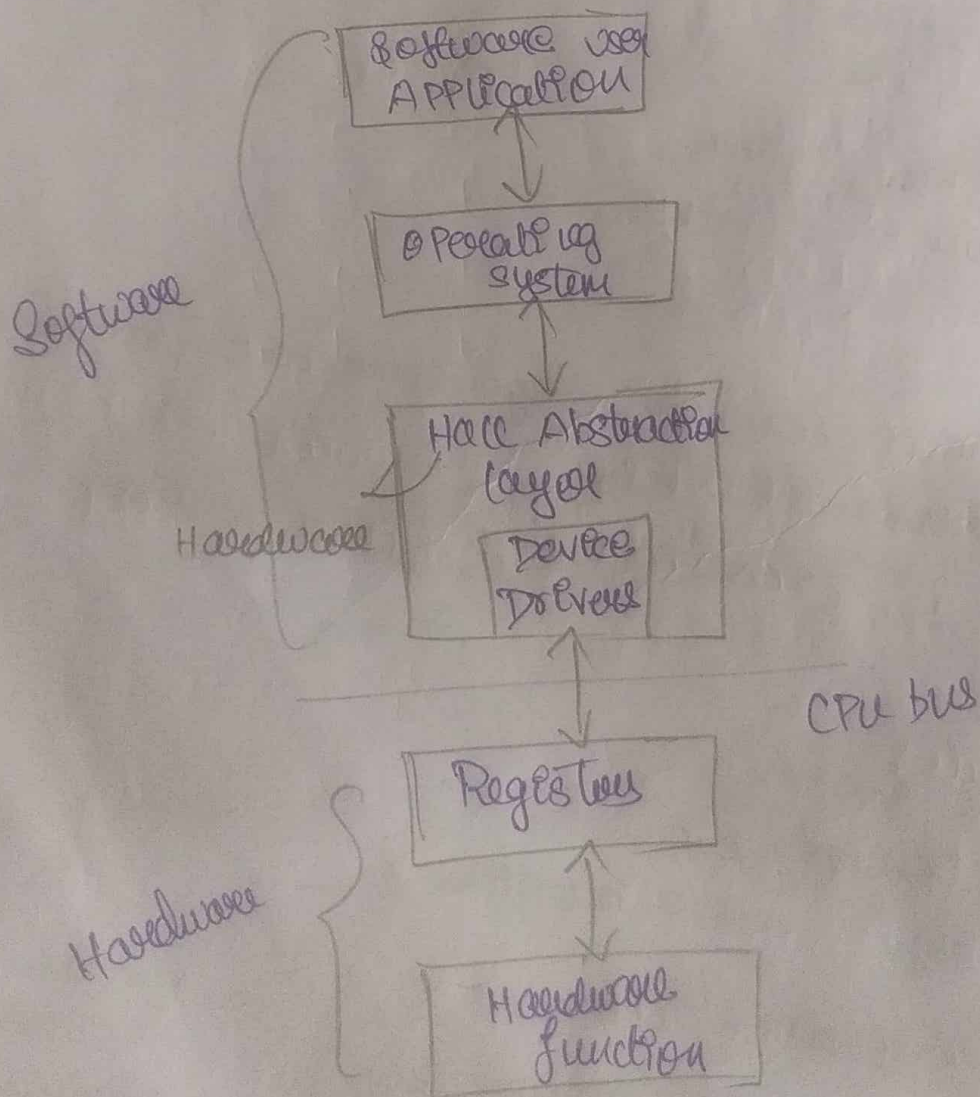
→ C++  
→

→ Memory space is possible



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Abstraction :- (Hardware devices, to



\* Allow users to interact w/ the hardware devices.

\* Allows Device Independent Programming by standard call to hardware.

User apply

H/W (HAL)  
ABSTRACTION  
LAYER

H/W

\* NO need to understand and physical interface

slow

HW

### Interpretation :-

- \* realize :- Semantics of a language
- \* Instructions visible to programmer are implemented by low level processor, which interpret program visible instructions.

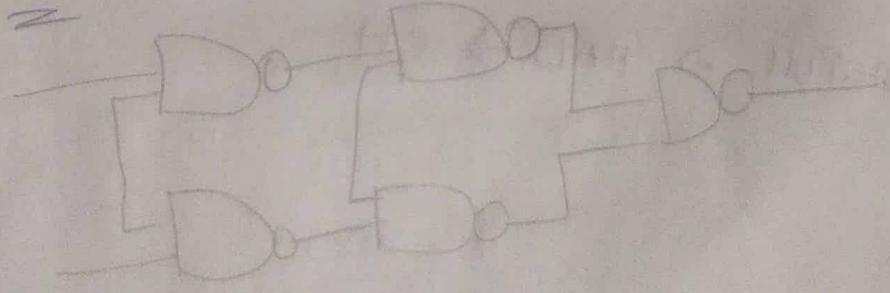
### → Translation :-

- \* Easy form of abstraction.
- \* RTL (Register transfer level)

### Behavioural Synthesis :-

- Logical synthesis.

### XOR Gate :-





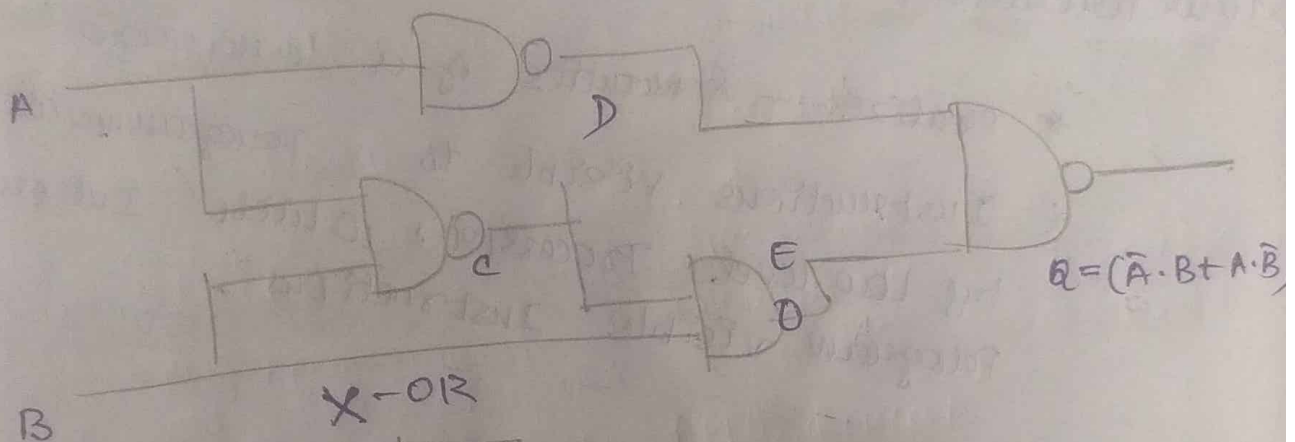
→ Extension :-

\* Define New data types.

\* System → Hardware level.

Implement by extension of C++.

→ XOR USING NAND Gate:-



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

very easy

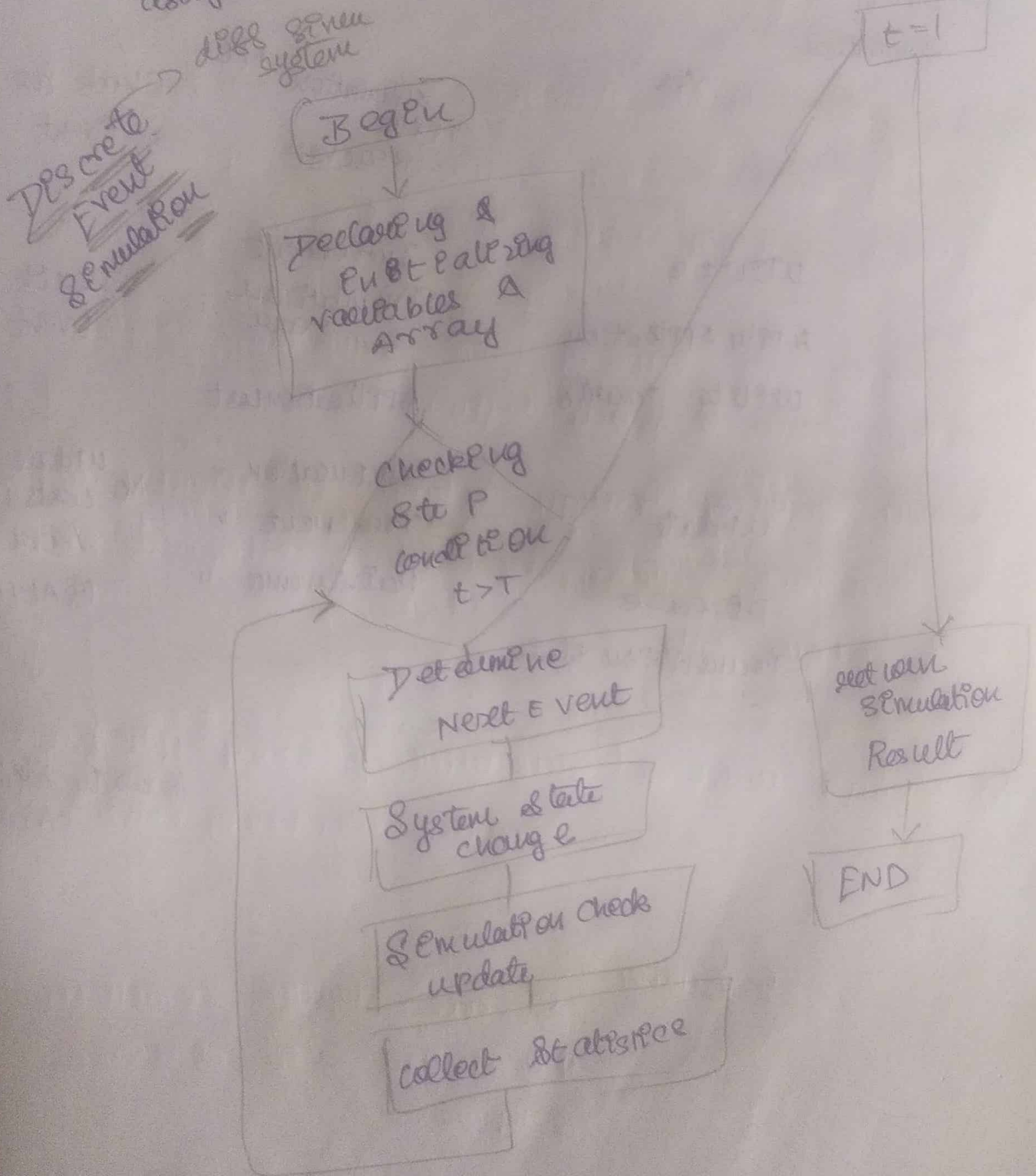
→ Interpretation - VLIW

→ Translation - RTL → Direct to Logic gates.

→ Extension → HAL → CH

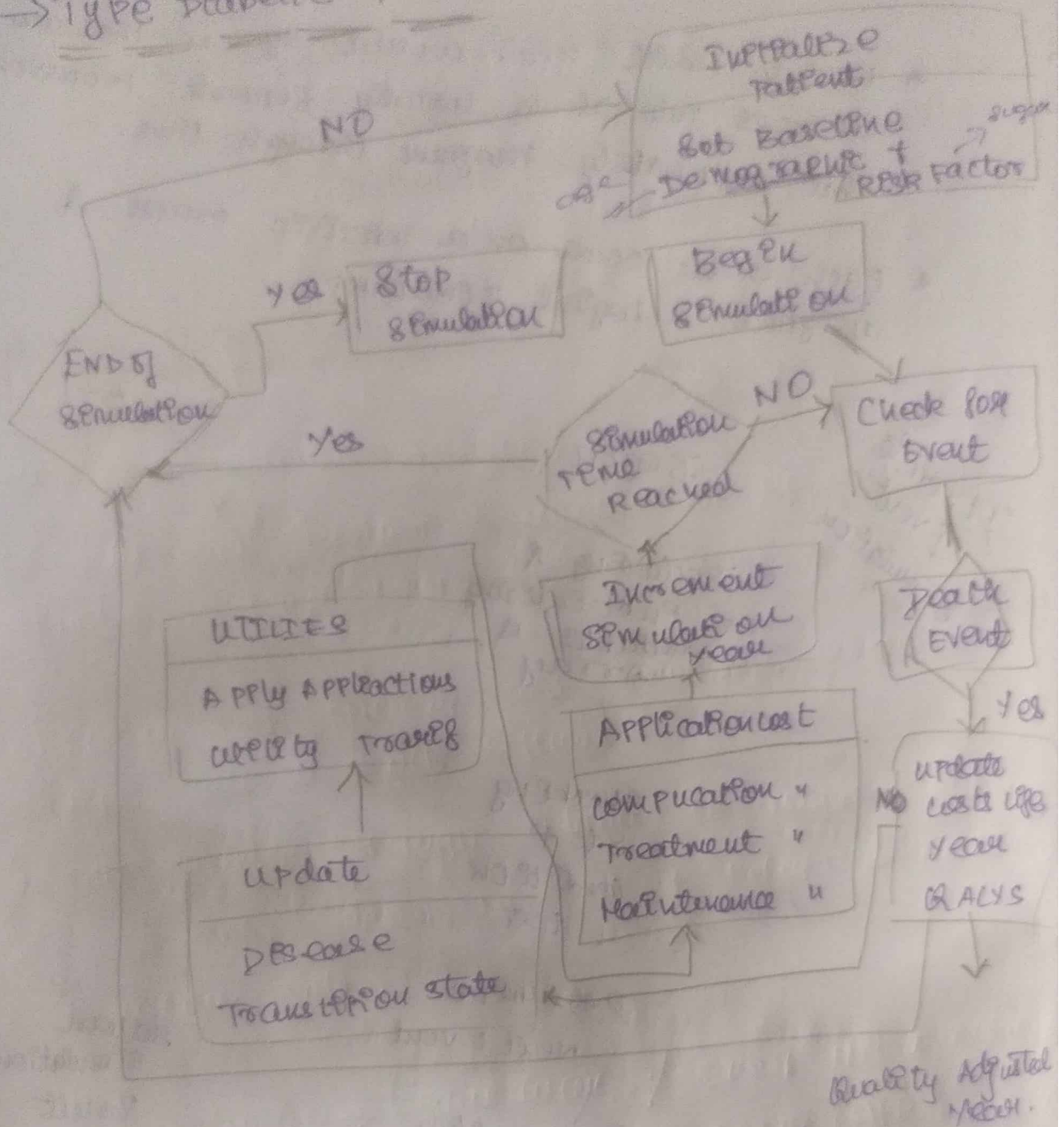
## → Discrete Event Simulation :-

- \* Used to Model real world system that can be decomposed into set of logically separate processes that automatically program through time.
- \* Each event occurs on a specific process & assigned a logical timestamp.





# → Type Diabetes Patient :-



Quality Adjusted Year.