ECE 460M
Digital System Design using Verilog
Lab Manual

Lab Assignment #1

Guideline

This lab is to be done individually. Everyone should turn in his/her own assignment.

Objective

The objective of this lab is to learn designing basic combinational circuits in Verilog and checking the correctness of the functionality using waveforms.

Problem 1: Subtractor Design

a. Write Verilog code for a 1-bit full subtractor using logic equations. You may not use the subtraction operator '-'. Rather, use the given 1-bit subtractor truth table given below to derive logic functions.
b. Write Verilog code for a 4-bit subtractor using the module defined in part (a) as a component. Test it for the following input combinations:
    i. A = 1001, B = 0011, Bin = 1
    ii. A = 0011, B = 0110, Bin = 1

1-bit full subtractor truth table:

A	B	Bin	Diff	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Verify that you design works correctly with one of the following:

1. Your own testbench
2. The "force" and "run" commands in the tcl command window or GUI to provide inputs and observe outputs on the waveform window.

ECE 460M
Digital System Design using Verilog
Lab Manual

Submission Details

All parts of this lab will be submitted on Canvas only. You will not need to submit anything as a hard copy. Please zip all relevant files into a single folder with the following naming scheme: **Lastname_Lab#.zip**

Problem	Submission Requirements
1a	• Verilog file(s) • Testbench if applicable
1b	• Verilog file(s) • Testbench if applicable

Checkout Details

You will be expected to describe briefly the codes for the problems, simulate and show waveforms in Vivado, and answer verbal questions.