RISC-V SoftCPU Contest: Enter Now!

Introduction

The RISC-V Foundation is proud to announce a RISC-V soft CPU core design contest sponsored by Google, Antmicro and Microsemi, a subsidiary of Microchip, Founding Platinum members of the RISC-V Foundation.

The aim of the contest is to further promote the use of the vendor-independent, modular and reusable ISA in FPGA applications, and push the limits of state-of-the-art design by encouraging innovative FPGA soft CPU implementations of the RISC-V ISA.

The contest targets two FPGA platforms from RISC-V Foundation members Microsemi and Lattice Semiconductor. Participants have the option of using the larger 25K LUT Microsemi IGLOO™2 or SmartFusion™2, or the 5K LUT Lattice iCE40 UltraPlus™. The contest challenges contest participants to build either very small or high-performance soft RISC-V implementations, with additional points awarded for novel approaches to the implementation itself.

Rules

The entries will be RV32I-compliant soft CPUs. The core can support other standard extensions (e.g. ‘C’ or ‘M’) if the designers decide to do so.

Categories & Scoring

There are four categories the entries will compete in:

- Smallest Microsemi SmartFusion®2 or IGLOO®2 implementation
- Smallest Lattice iCE40 UltraPlus™ implementation
- Highest-performance Microsemi SmartFusion®2 or IGLOO®2 implementation
- Highest-performance Lattice iCE40 UltraPlus™ implementation

For the “smallest implementation” categories, the smallest number of total resources used is better. Total resources shall include Logic Elements, Math Blocks and internal RAM. In case of a draw, the entry with the higher performance is ranked higher.

For the “highest-performance implementation” categories, the performance of the entries will be measured using the **Dhrystone benchmark** compiled with the -O3 -fno-inline option. 50, 30 and 10 points will be awarded to any entry that ranks 1st, 2nd and 3rd in each category, respectively (so for example, if a given entry is the 2nd smallest on the Microsemi platform, it will be awarded 30 points). An entry targeting both the Microsemi and Lattice platforms can potentially be awarded points in categories for both vendors, if necessary files and instructions to reproduce are provided for both.

An additional pool of 100 points will be distributed between projects by a panel of five judges, selected from the members of the RISC-V Foundation, awarding up to 20 points each based on the creativeness of the entries submitted – participants are encouraged to try out novel approaches to creating their cores.

Minimum Requirements

The resulting design must be in Verilog (the core itself can be written in a framework such as Chisel, SpinalHDL or MiGen which generates Verilog) and be possible to be simulated using Verilator. The design must be a complete FPGA implementation targeting at least one of the two platforms and run the provided **Zephyr RTOS** application. The Zephyr 1.13 release should be used and can only be modified in a way that does not touch the OS core. Any modifications to the standard RISC-V GCC provided by Zephyr are strictly forbidden. The CPU must pass the **RISC-V RV32I compliance tests**.
Also, the CPU must boot the following Zephyr applications:

- **Philosophers**
- **Synchronization**

Entries have to be submitted in the form of repositories on github.com with a clearly stated BSD-style license (the Apache 2.0 license is preferred) including:

- the Soft CPU’s HDL code
- constraint and other FPGA-related files necessary to produce a binary bitstream for the respective hardware
- a README with a complete list instructions and prerequisites, as well as Makefiles or other scripts, needed to produce the bitstream. The README should also include instructions how to simulate the design in Verilator.
- a binary version of the bitstream which can be fully and identically reproduced using the files and instructions mentioned above
- any necessary **Zephyr 1.13** files in the zephyr/ subdirectory (can be a git submodule)
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Hardware

Microsemi **IGLOO2 M2GL025**/**SmartFusion2 M2S025**
25K 4-input LUTs
SmartFusion2 boards can be purchased from **Future Electronics** for $99.95.
Both boards feature the same 25K LUT FPGA fabric. SmartFusion2 is essentially identical to Igloo2 except that it is a SoC FPGA with a built-in Cortex-M3 hard CPU – the soft CPU to be designed should not use the hard CPU subsystems as such but interesting ways to enhance the design using the built-in hard CPU can be implemented.

Lattice iCE40 Ultra Plus – iCE40UP5K
5K 4-input LUTs

There are several boards with this part that can be used for the development:

- **iCE40 UltraPlus Breakout Board** ($49.00)
- **iCE40 UltraPlus MDP** ($99.00)
- **Gnarly Grey UPDuinoBoard V1/V2** ($7.99/$13.99)
- **iceVision** ($73.99)

Prizes

1st prize: USD $6,000
2nd prize: USD $3,000 + **Splash Kit** + **iCE40 UltraPlus MDP**
3rd prize: USD $1,000 + **PolarFire Evaluation Kit** + **iCE40 UltraPlus Breakout Board**

Timeline

Entries with links to the relevant GitHub repositories will be accepted at **softcpu-contest@riscv.org** by **Nov. 26, 2018 at 11:59 p.m. PST.**
Results will be announced at the 1st **RISC-V Summit** taking place in Santa Clara, Calif. from Dec. 3-6. Participants are not required to attend the RISC-V Summit to win. You can check out the agenda for the RISC-V Summit **here** and register **here**.

FAQ

1. **If I have a question not answered by this FAQ, who should I contact?**

- Please write to **softcpu-contest@riscv.org**

2. **Can I use SystemVerilog?**
   - Your design must simulate in Verilator, you can use any SystemVerilog features found in Verilator.
3. **Can I use VHDL?**
   - Your design must simulate in Verilator. Verilator does not support VHDL.
4. **Can I use my HDL language?**
   - As long as your HDL language generates Verilog that works with Verilator. Please include both:
     - A Makefile to generate your Verilog
     - A copy of the generated Verilog that was used to generate the bitstream.
5. **Why are you requiring Verilator?**
   - The aim is to enable new innovative designs. We want everyone to be able to test and simulate these new designs without having to purchase expensive commercial tools.
6. **Does the core have to pass all the compliance suite tests?**
   - As mentioned in the contest page, it must pass all the **RISC-V RV32I** compliance tests. Software emulation of less used CPU instructions (by trapping on invalid instructions) is an okay approach.
7. **How do I test if my CPU is compatible with the Zephyr demo applications?**
   - The demo applications to run include:
     - **Philosophers**
     - **Synchronization**

     Need to output messages as provided in the README for those applications.

8. **What must I include in my GitHub repository?**
   - The Soft CPU's HDL code
   - Constraint and other FPGA-related files necessary to produce a binary bitstream for the respective hardware

- A README with a complete list of instructions and prerequisites, as well as Makefiles or other scripts, needed to produce the bitstream. The README should also include instructions how to simulate the design in Verilator.
- A binary version of the bitstream which can be fully and identically reproduced using the files and instructions mentioned above
- Any necessary Zephyr 1.13 files in the zephyr/ subdirectory (can be a git submodule)

9. **What is included in the resource calculate?**
   - All resources used inside the FPGA (as determined by the bitstream) are included as part of the resource calculation. This includes all peripherals required.
10. **How is the "smallest" implementation determined?**
    - For the "smallest implementation" categories, the smallest number of total resources used is better. Total resources shall include Logic Elements, Math Blocks and internal RAM. In case of a draw, the entry with the higher performance is ranked higher.
    - We are working on a more detailed description of the measurement procedure.
11. **Is RAM initialization data considered free for the resource usage calculation?**
    - No.
12. **Is there a discussion group, mailing list, forum, gitter.im account for participants to discuss designs?**
    - There is no endorsed discussion mechanism. Some potential existing groups are the RISC-V HW dev group.
    - If tweeting about the design use the hashtag #RISCVcontest
13. **How is performance measured?**
    - Short answer: we will be measuring performance in absolute DMIPS. We will expand on this point in the coming days.
14. **How are the three final winners selected?**
    - There are 4 categories as listed above. 50, 30 and 10 points will be awarded to any entry that ranks 1st, 2nd and 3rd in each category, respectively (so for example, if a given entry is the 2nd

smallest on the Microsemi platform, it will be awarded 30 points). An entry targeting both the Microsemi and Lattice platforms can potentially be awarded points in categories for both vendors, if necessary files and instructions to reproduce are provided for both.

15. **Can I use paid tools to synthesize my design?**
    - No, you are only allowed to use open source or free-of-charge tools so that the results you have obtained can be reproduced by anyone (within reason).
16. **Do I need to be physically present at the RISC-V Summit to claim my prize?**
    - No, you just need to submit before the deadline. Of course, you're encouraged to come to the RISC-V Summit and be there for the announcement of winners, but we are aware that not all of the contestants can attend.

The above 6 pages are copy paste from the official contest website, fetched on 27 October 2018.

Fetched from: https://riscv.org/2018contest/

Reason for fetching the webpage – to provide a fixed downloadable document for offline reading.

A copy of this document will be available from github URL

https://github.com/micro-FPGA/riscv-contest-2018

It is assumed that for the contest rules (the first 3 pages) following copyright would apply