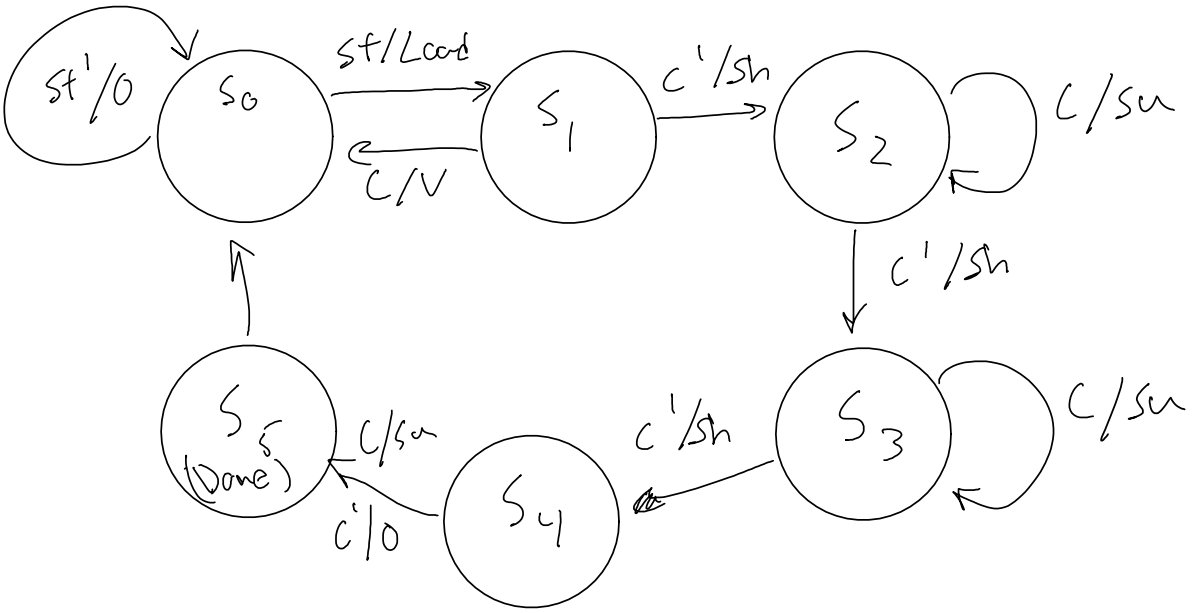
Lab 7 State Diagram

Tuesday, November 29, 2016 7:01 PM

State Graph



S1: 6-bit dividend & 3 bit divisor are loaded
- if Overflow Condition B met (top 4 bits of dividend are > divisor), C is set to 1 and operation returns to S_0 (stop state)

S2: if Overflow from S1 is not met, operation will left shift into S2, Now if C=1 subtraction can occur, after finishing C=0 and operation progress to S3.

S3: Same as S2 (Continues until 3 shifts occur)

S4: Now either one last subtraction will occur

and it will get sent to (Step, S_0) or subtraction will not occur and it will still go to (Step, S_0).
