TestModel

Design Description

tmahlman

TestModel: Design Description

by tmahlman

Published 29-Jun-2023 06:12:31

Table of Contents

Chapter 1. Model Version

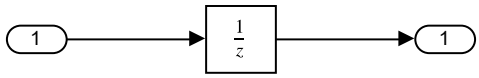
Version: 6.2

Last modified: Tue May 16 08:38:31 2023

Checksum: Could not compute checksum for "TestModel" (possibly because model could not be compiled).

Chapter 2. Root System

Figure 2.1. TestModel



Description

This is the base model from which the DO model template is derived.

Interface

Input Signals

Table 2.1. Input Signals

Signal Name	Block	Description	Data Type	Width	Dimensions
	TestModel/In1			0	

Output Signals

Table 2.2. Output Signals

Signal Name	Block	Description	Data Type	Width	Dimensions
	TestModel/Unit Delay			0	

Blocks

Parameters

"In1" (Inport)

Table 2.3. "In1" Parameters

Parameter	Value
Port number	1
Port dimensions (-1 for inherited)	-1
Sample time (-1 for inherited)	-1
Minimum	[]
Maximum	[]
Data type	Inherit: auto

"Out1" (Outport)

Table 2.4. "Out1" Parameters

Parameter	Value
Port number	1
Icon display	Port number
Output function call	off
Minimum	[]
Maximum	[]
Data type	Inherit: auto
Lock output data type setting against changes by the fixed-point tools	off
Output as nonvirtual bus in parent model	off
Bus virtuality	inherit
Data mode	inherit
Unit (e.g., m, m/s^2, N*m)	inherit
Port dimensions (-1 for inherited)	-1
Variable-size signal	Inherit
Sample time (-1 for inherited)	-1
Ensure outport is virtual	off
Source of initial output value	Dialog
Output when disabled	held
Initial output	[]
MustResolveToSignalObject	off
Specify output when source is unconnected	off

Parameter	Value
Constant value	0
Interpret vector parameters as 1-D	off

"Unit Delay" (UnitDelay)

Table 2.5. "Unit Delay" Parameters

Parameter	Value
Initial condition	0
Input processing	Elements as channels (sample based)
Sample time (-1 for inherited)	-1
State name must resolve to Simulink signal object	off

Block Execution Order

"TestModel" is a multitasking model. Block execution order is not available for multitasking models.

Chapter 3. Requirements

TestModel does not contain requirements traceability links.

Chapter 4. System Model Configuration

Source: Data dictionary
Source Name: csSingleInstance

Table 4.1. TestModel Configuration Set

Property	Value
Description	
Components	[TestModel Configuration Set.Components(1), TestModel Configuration Set.Components(2), TestModel Configuration Set.Components(3), TestModel Configuration Set.Components(4), TestModel Configuration Set.Components(5), TestModel Configuration Set.Components(6), TestModel Configuration Set.Components(7), TestModel Configuration Set.Components(8), TestModel Configuration Set.Components(9), TestModel Configuration Set.Components(10)]
Name	csSingleInstance

Table 4.2. TestModel Configuration Set.Components(1)

Property	Value
Name	Solver
Description	
Components	
StartTime	0.0
StopTime	10.0
AbsTol	auto
AutoScaleAbsTol	on
FixedStep	auto
InitialStep	auto
MaxOrder	5
ZcThreshold	auto
ConsecutiveZCsStepRelTol	10*128*eps
MaxConsecutiveZCs	1000
ExtrapolationOrder	4
NumberNewtonIterations	1
MaxStep	auto

MinStep	auto
MaxConsecutiveMinStep	1
RelTol	1e-3
EnableMultiTasking	on
AllowMultiTaskInputOutput	off
ConcurrentTasks	off
SolverName	FixedStepDiscrete
SolverType	Fixed-step
SolverJacobianMethodControl	auto
DaesscMode	auto
ShapePreserveControl	DisableAll
ZeroCrossControl	UseLocalSettings
ZeroCrossAlgorithm	Nonadaptive
SolverResetMethod	Fast
PositivePriorityOrder	off
AutoInsertRateTranBlk	off
SampleTimeConstraint	Unconstrained
InsertRTBMode	Whenever possible
SampleTimeProperty	
DecoupledContinuousIntegration	off
MinimalZcImpactIntegration	off
ODENIntegrationMethod	ode3
EnableFixedStepZeroCrossing	off
MaxZcPerStep	2
MaxZcBracketingIterations	10

Table 4.3. TestModel Configuration Set.Components(2)

Property	**Value**
Name	Data Import/Export
Description	
Components	
Decimation	1
ExternalInput	[t, u]
FinalStateName	xFinal
InitialState	xInitial
LimitDataPoints	on

MaxDataPoints	1000
LoadExternalInput	off
LoadInitialState	off
SaveFinalState	off
SaveOperatingPoint	off
SaveFormat	Dataset
SaveOutput	on
SaveState	off
SignalLogging	on
DSMLogging	on
StreamToWks	on
InspectSignalLogs	off
SaveTime	on
ReturnWorkspaceOutputs	on
StateSaveName	xout
TimeSaveName	tout
OutputSaveName	yout
SignalLoggingName	logsout
DSMLoggingName	dsmout
OutputOption	RefineOutputTimes
OutputTimes	[]
ReturnWorkspaceOutputsName	out
Refine	1
LoggingToFile	off
DatasetSignalFormat	timeseries
LoggingFileName	out.mat
LoggingIntervals	[-inf, inf]

Table 4.4. TestModel Configuration Set.Components(3)

Property	**Value**
Name	Optimization
Description	
Components	
BlockReduction	off
BooleanDataType	on
ConditionallyExecuteInputs	on

DefaultParameterBehavior	Inlined
InlineParams	on
UseDivisionForNetSlopeComputation	on
GainParamInheritBuiltInType	off
UseFloatMulNetSlope	on
InheritOutputTypeSmallerThanSingle	off
DefaultUnderspecifiedDataType	double
UseSpecifiedMinMax	off
InlineInvariantSignals	on
OptimizeBlockIOStorage	on
BufferReuse	on
ReuseModelBlockBuffer	on
GlobalBufferReuse	on
GlobalVariableUsage	Use global to hold temporary results
StrengthReduction	off
AdvancedOptControl	-SLCI
ExpressionFolding	on
BooleansAsBitfields	off
BitfieldContainerType	uint_T
BitwiseOrLogicalOp	Same as modeled
EnableMemcpy	on
MemcpyThreshold	64
PassReuseOutputArgsAs	Individual arguments
PassReuseOutputArgsThreshold	12
LocalBlockOutputs	on
RollThreshold	5
StateBitsets	off
DataBitsets	off
ActiveStateOutputEnumStorageType	Native Integer
ZeroExternalMemoryAtStartup	on
ZeroInternalMemoryAtStartup	on
InitFltsAndDblsToZero	off
NoFixptDivByZeroProtection	off
EfficientFloat2IntCast	on
EfficientMapNaN2IntZero	off
LifeSpan	inf

EvaledLifeSpan	1
ClockResolution	-1
MaxStackSize	inf
BufferReusableBoundary	on
RemoveLocalVariableInitialization	on
SimCompilerOptimization	off
AccelVerboseBuild	off
OptimizeBlockOrder	speed
OptimizeDataStoreBuffers	on
BusAssignmentInplaceUpdate	on
DifferentSizesBufferReuse	off
UseRowMajorAlgorithm	off
OptimizationLevel	level2
OptimizationPriority	Balanced
OptimizationCustomize	on
LabelGuidedReuse	off
MultiThreadedLoops	off
DenormalBehavior	GradualUnderflow
EfficientTunableParamExpr	on

Table 4.5. TestModel Configuration Set.Components(4)

Property	**Value**
Name	Diagnostics
Description	
Components	
RTPrefix	error
ConsistencyChecking	none
ArrayBoundsChecking	none
SignalInfNanChecking	error
StringTruncationChecking	error
SignalRangeChecking	error
ReadBeforeWriteMsg	EnableAllAsError
WriteAfterWriteMsg	EnableAllAsError
WriteAfterReadMsg	EnableAllAsError
AlgebraicLoopMsg	error
ArtificialAlgebraicLoopMsg	error

SaveWithDisabledLinksMsg	error
SaveWithParameterizedLinksMsg	error
CheckSSInitialOutputMsg	on
UnderspecifiedInitializationDetection	Simplified
MergeDetectMultiDrivingBlocksExec	error
SignalResolutionControl	UseLocalSettings
BlockPriorityViolationMsg	error
MinStepSizeMsg	warning
TimeAdjustmentMsg	none
MaxConsecutiveZCsMsg	error
MaskedZcDiagnostic	warning
IgnoredZcDiagnostic	warning
SolverPrmCheckMsg	error
InheritedTsInSrcMsg	error
MultiTaskDSMMsg	error
MultiTaskCondExecSysMsg	error
MultiTaskRateTransMsg	error
SingleTaskRateTransMsg	error
TasksWithSamePriorityMsg	error
SigSpecEnsureSampleTimeMsg	error
CheckMatrixSingularityMsg	error
IntegerOverflowMsg	error
Int32ToFloatConvMsg	warning
ParameterDowncastMsg	error
ParameterOverflowMsg	error
ParameterUnderflowMsg	error
ParameterPrecisionLossMsg	error
ParameterTunabilityLossMsg	error
FixptConstUnderflowMsg	none
FixptConstOverflowMsg	none
FixptConstPrecisionLossMsg	none
UnderSpecifiedDataTypeMsg	error
UnnecessaryDatatypeConvMsg	warning
VectorMatrixConversionMsg	error
FcnCallInpInsideContextMsg	error
SignalLabelMismatchMsg	error

UnconnectedInputMsg	error
UnconnectedOutputMsg	error
UnconnectedLineMsg	error
UseOnlyExistingSharedCode	error
SFcnCompatibilityMsg	error
FrameProcessingCompatibilityMsg	error
UniqueDataStoreMsg	error
BusObjectLabelMismatch	error
RootOutportRequireBusObject	error
AssertControl	DisableAll
AllowSymbolicDim	off
ModelReferenceIOMsg	error
ModelReferenceVersionMismatchMessage	none
ModelReferenceIOMismatchMessage	error
UnknownTsInhSupMsg	error
ModelReferenceDataLoggingMessage	error
ModelReferenceNoExplicitFinalValueMsg	none
ModelReferenceSymbolNameMessage	none
ModelReferenceExtraNoncontSigs	error
StateNameClashWarn	warning
OperatingPointInterfaceChecksumMismatchMsg	warning
NonCurrentReleaseOperatingPointMsg	error
PregeneratedLibrarySubsystemCodeDiagnostic	none
SubsystemReferenceDiagnosticForUnitTest	error
InitInArrayFormatMsg	warning
StrictBusMsg	ErrorOnBusTreatedAsVector
BusNameAdapt	WarnAndRepair
NonBusSignalsTreatedAsBus	error
SFUnusedDataAndEventsDiag	warning
SFUnexpectedBacktrackingDiag	error
SFInvalidInputDataAccessInChartInitDiag	error
SFNoUnconditionalDefaultTransitionDiag	error
SFTransitionOutsideNaturalParentDiag	error
SFUnreachableExecutionPathDiag	error
SFUndirectedBroadcastEventsDiag	error
SFTransitionActionBeforeConditionDiag	error

SFOutputUsedAsStateInMooreChartDiag	error
SFTemporalDelaySmallerThanSampleTimeDiag	error
SFSelfTransitionDiag	error
SFExecutionAtInitializationDiag	error
IntegerSaturationMsg	error
AllowedUnitSystems	all
UnitsInconsistencyMsg	warning
AllowAutomaticUnitConversions	on
RCSCRenamedMsg	warning
RCSCObservableMsg	warning
ForceCombineOutputUpdateInSim	off
UnderSpecifiedDimensionMsg	none
DebugExecutionForFMUViaOutOfProcess	off
ArithmeticOperatorsInVariantConditions	warning
VariantConditionMismatch	none
InheritVATfromSVC	warning
VariantConfigNotUsedByTopModel	warning
ParamWriterValidationControl	UseLocalSettings

Table 4.6. TestModel Configuration Set.Components(5)

Property	**Value**
Name	Hardware Implementation
Description	
Components	
ProdBitPerChar	8
ProdBitPerShort	16
ProdBitPerInt	32
ProdBitPerLong	32
ProdBitPerLongLong	64
ProdBitPerFloat	32
ProdBitPerDouble	64
ProdBitPerPointer	32
ProdBitPerSizeT	32
ProdBitPerPtrDiffT	32
ProdLargestAtomicInteger	Long
ProdLargestAtomicFloat	Float

ProdIntDivRoundTo	Zero
ProdEndianess	LittleEndian
ProdWordSize	32
ProdShiftRightIntArith	on
ProdLongLongMode	off
ProdHWDeviceType	ARM Compatible->ARM 10
TargetBitPerChar	8
TargetBitPerShort	16
TargetBitPerInt	32
TargetBitPerLong	32
TargetBitPerLongLong	64
TargetBitPerFloat	32
TargetBitPerDouble	64
TargetBitPerPointer	32
TargetBitPerSizeT	32
TargetBitPerPtrDiffT	32
TargetLargestAtomicInteger	Char
TargetLargestAtomicFloat	None
TargetShiftRightIntArith	on
TargetLongLongMode	off
TargetIntDivRoundTo	Undefined
TargetEndianess	Unspecified
TargetWordSize	32
TargetPreprocMaxBitsSint	32
TargetPreprocMaxBitsUint	32
TargetHWDeviceType	Specified
TargetUnknown	off
ProdEqTarget	on
UseEmbeddedCoderFeatures	on
UseSimulinkCoderFeatures	on
HardwareBoardFeatureSet	EmbeddedCoderHSP

Table 4.7. TestModel Configuration Set.Components(6)

Property	**Value**
Name	Model Referencing
Description	

Components	
UpdateModelReferenceTargets	IfOutOfDateOrStructuralChange
EnableRefExpFcnMdlSchedulingChecks	on
CheckModelReferenceTargetMessage	error
EnableParallelModelReferenceBuilds	off
ParallelModelReferenceErrorOnInvalidPool	on
ParallelModelReferenceMATLABWorkerInit	None
ModelReferenceNumInstancesAllowed	Single
PropagateVarSize	Infer from blocks in model
ModelDependencies	
ModelReferencePassRootInputsByReference	on
ModelReferenceMinAlgLoopOccurrences	off
PropagateSignalLabelsOutOfModel	off
SupportModelReferenceSimTargetCustomCode	off
UseModelRefSolver	off

Table 4.8. TestModel Configuration Set.Components(7)

Property	**Value**
Name	Simulation Target
Description	
Components	
SimCustomSourceCode	
SimCustomHeaderCode	
SimCustomInitializer	
SimCustomTerminator	
SimReservedNameArray	
SimUserSources	
SimUserIncludeDirs	
SimUserLibraries	
SimUserDefines	
SimCustomCompilerFlags	
SimCustomLinkerFlags	
SFSimEnableDebug	off
SFSimEcho	on
SimCtrlC	on
SimIntegrity	on

SimUseLocalCustomCode	on
SimParseCustomCode	on
SimAnalyzeCustomCode	off
SimDebugExecutionForCustomCode	off
SimGenImportedTypeDefs	off
CompileTimeRecursionLimit	0
EnableRuntimeRecursion	off
EnableImplicitExpansion	on
MATLABDynamicMemAlloc	off
MATLABDynamicMemAllocThreshold	65536
LegacyBehaviorForPersistentVarInContinuousTime	off
CustomCodeFunctionArrayLayout	
DefaultCustomCodeFunctionArrayLayout	NotSpecified
CustomCodeUndefinedFunction	UseInterfaceOnly
CustomCodeGlobalsAsFunctionIO	off
DefaultCustomCodeDeterministicFunctions	None
CustomCodeDeterministicFunctions	
SimHardwareAcceleration	generic
SimTargetLang	C
GPUAcceleration	off
SimGPUMallocThreshold	200
SimGPUStackLimitPerThread	1024
SimGPUErrorChecks	off
SimGPUCustomComputeCapability	
SimGPUCompilerFlags	
SimDLTargetLibrary	mkl-dnn
SimDLAutoTuning	on

Table 4.9. TestModel Configuration Set.Components(8)

Property	**Value**
Name	Code Generation
Description	Embedded Coder
SystemTargetFile	ert.tlc
EmbeddedCoderDictionary	
HardwareBoard	None
ShowCustomHardwareApp	off

ShowEmbeddedHardwareApp	off
TLCOptions	
GenCodeOnly	on
MakeCommand	make_rtw
GenerateMakefile	on
PackageGeneratedCodeAndArtifacts	off
PackageName	
TemplateMakefile	ert_default_tmf
PostCodeGenCommand	
GenerateReport	on
RTWVerbose	on
RetainRTWFile	off
ProfileTLC	off
TLCDebug	off
TLCCoverage	off
TLCAssert	off
BuiltinFFTWCallback	off
RTWUseLocalCustomCode	on
RTWUseSimCustomCode	off
CustomSourceCode	
CustomHeaderCode	
CustomInclude	
CustomSource	
CustomLibrary	
CustomDefine	
CustomBLASCallback	
CustomLAPACKCallback	
CustomFFTCallback	
CustomInitializer	
CustomTerminator	
Toolchain	Automatically locate an installed toolchain
BuildConfiguration	Faster Runs
CustomToolchainOptions	
IncludeHyperlinkInReport	on
LaunchReport	on
PortableWordSizes	off

CreateSILPILBlock	None
CodeExecutionProfiling	off
CodeExecutionProfileVariable	executionProfile
CodeProfilingSaveOptions	SummaryOnly
CodeProfilingInstrumentation	off
CodeStackProfiling	off
CodeStackProfileVariable	stackProfile
CodeCoverageSettings	TestModel Configuration Set.Components(8).CodeCoverageSettings
SILPILDebugging	off
DataTypeReplacement	CoderTypedefs
CoderTypedefsCompatibility	off
TargetLang	C
GenerateGPUCode	None
HalideCodeGeneration	off
GenerateTraceInfo	on
GenerateTraceReport	on
GenerateTraceReportSl	on
GenerateTraceReportSf	on
GenerateTraceReportEml	on
GenerateWebview	off
GenerateCodeMetricsReport	on
GenerateCodeReplacementReport	off
RTWCompilerOptimization	off
ObjectivePriorities	
RTWCustomCompilerOptimizations	
CheckMdlBeforeBuild	Off
GPUKernelNamePrefix	
GPUDeviceID	-1
GPUMallocMode	discrete
GPUMallocThreshold	200
GPUEnableMemoryManager	off
GPUStackLimitPerThread	1024
GPUcuBLAS	on
GPUcuSOLVER	on
GPUcuFFT	on
GPUErrorChecks	off

GPUComputeCapability	3.5
GPUCustomComputeCapability	
GPUCompilerFlags	
GPUMaximumBlocksPerKernel	0
DLTargetLibrary	none
DLAutoTuning	on
DLArmComputeVersion	19.05
DLArmComputeArch	unspecified
DLLearnablesCompression	None
Components	[TestModel Configuration Set.Components(8).Components(1), TestModel Configuration Set.Components(8).Components(2)]

Table 4.10. TestModel Configuration Set.Components(9)

Property	Value
Description	Simulink Coverage Configuration Component
Components	
Name	Simulink Coverage
CovEnable	off
CovScope	EntireSystem
CovIncludeTopModel	on
RecordCoverage	off
CovPath	/
CovSaveName	covdata
CovCompData	
CovMetricSettings	dwe
CovFilter	
CovHTMLOptions	
CovNameIncrementing	off
CovForceBlockReductionOff	on
CovEnableCumulative	on
CovSaveCumulativeToWorkspaceVar	off
CovSaveSingleToWorkspaceVar	off
CovCumulativeVarName	covCumulativeData
CovCumulativeReport	off
CovSaveOutputData	on

CovOutputDir	slcov_output/$ModelName$
CovDataFileName	$ModelName$_cvdata
CovReportOnPause	on
CovModelRefEnable	off
CovModelRefExcluded	
CovExternalEMLEnable	on
CovSFcnEnable	on
CovBoundaryAbsTol	1.0000e-05
CovBoundaryRelTol	0.0100
CovUseTimeInterval	off
CovStartTime	0
CovStopTime	0
CovMetricStructuralLevel	Decision
CovMetricLookupTable	off
CovMetricSignalRange	off
CovMetricSignalSize	off
CovMetricObjectiveConstraint	off
CovMetricSaturateOnIntegerOverflow	off
CovMetricRelationalBoundary	off
CovLogicBlockShortCircuit	off
CovUnsupportedBlockWarning	on
CovMcdcMode	Masking
CovExcludeInactiveVariants	off

Table 4.11. TestModel Configuration Set.Components(10)

Property	Value
Description	HDL Coder custom configuration component
Components	
Name	HDL Coder

Table 4.12. TestModel Configuration Set.Components(8).CodeCoverageSettings

Property	Value
TopModelCoverage	off
ReferencedModelCoverage	off

CoverageTool	None

Table 4.13. TestModel Configuration Set.Components(8).Components(1)

Property	Value
Name	Code Appearance
Description	
Components	
ForceParamTrailComments	on
GenerateComments	on
CommentStyle	Auto
IgnoreCustomStorageClasses	off
IgnoreTestpoints	off
MaxIdLength	31
ShowEliminatedStatement	on
OperatorAnnotations	off
SimulinkDataObjDesc	off
SFDataObjDesc	off
MATLABFcnDesc	on
MangleLength	4
SharedChecksumLength	8
CustomSymbolStrGlobalVar	RN$M
CustomSymbolStrType	NR$M_T
CustomSymbolStrField	NM
CustomSymbolStrFcn	RNMF
CustomSymbolStrFcnArg	rt$I$N$M
CustomSymbolStrBlkIO	rtb_NM
CustomSymbolStrTmpVar	NM
CustomSymbolStrMacro	RN$M
CustomSymbolStrUtil	NC
CustomSymbolStrEmxType	emxArray_MN
CustomSymbolStrEmxFcn	emx$M$N
CustomUserTokenString	
CustomCommentsFcn	
DefineNamingRule	None
DefineNamingFcn	
ParamNamingRule	None

ParamNamingFcn	
SignalNamingRule	None
SignalNamingFcn	
InsertBlockDesc	off
InsertPolySpaceComments	off
SimulinkBlockComments	on
BlockCommentType	BlockPathComment
StateflowObjectComments	on
MATLABSourceComments	off
EnableCustomComments	off
InternalIdentifier	Shortened
InlinedPrmAccess	Literals
ReqsInCode	on
UseSimReservedNames	off
ReservedNameArray	
EnumMemberNameClash	error

Table 4.14. TestModel Configuration Set.Components(8).Components(2)

Property	Value
Name	Target
Description	
Components	
IsERTTarget	on
TargetLibSuffix	
TargetPreCompLibLocation	
TargetLangStandard	C99 (ISO)
CodeReplacementLibrary	None
UtilityFuncGeneration	Shared location
MultiwordTypeDef	System defined
MultiwordLength	256
DynamicStringBufferSize	256
GenerateFullHeader	on
InferredTypesCompatibility	off
ExistingSharedCode	
GenerateSampleERTMain	on
GenerateTestInterfaces	off

ModelReferenceCompliant	on
ParMdlRefBuildCompliant	on
CompOptLevelCompliant	on
ConcurrentExecutionCompliant	on
IncludeMdlTerminateFcn	off
CombineOutputUpdateFcns	on
CombineSignalStateStructs	off
GroupInternalDataByFunction	off
SuppressErrorStatus	on
IncludeFileDelimiter	Auto
ERTCustomFileBanners	on
SupportAbsoluteTime	off
LogVarNameModifier	rt_
MatFileLogging	off
MultiInstanceERTCode	off
CodeInterfacePackaging	Nonreusable function
PurelyIntegerCode	off
SupportNonFinite	off
SupportComplex	on
SupportContinuousTime	off
SupportNonInlinedSFcns	off
RemoveDisableFunc	on
RemoveResetFunc	on
SupportVariableSizeSignals	off
ParenthesesLevel	Maximum
CastingMode	Standards
ModelStepFunctionPrototypeControlCompliant	on
CPPClassGenCompliant	on
GRTInterface	off
GenerateAllocFcn	off
UseToolchainInfoCompliant	on
GenerateSharedConstants	off
LUTObjectStructOrderExplicitValues	Size,Breakpoints,Table
LUTObjectStructOrderEvenSpacing	Size,Breakpoints,Table
ArrayLayout	Column-major
UnsupportedSFcnMsg	error

ERTHeaderFileRootName	RE
ERTSourceFileRootName	RE
ERTDataFileRootName	$R_data
InstructionSetExtensions	{None}
OptimizeReductions	off
IsSLRTTarget	off
DSAsUniqueAccess	off
ExtMode	off
ExtModeTransport	0
ExtModeStaticAlloc	off
ExtModeAutomaticAllocSize	on
ExtModeMaxTrigDuration	10
ExtModeStaticAllocSize	1000000
ExtModeTesting	off
ExtModeMexFile	ext_comm
ExtModeMexArgs	
ExtModeIntrfLevel	Level1
TargetOS	BareBoardExample
MultiInstanceErrorCode	Error
RootIOFormat	Individual arguments
RTWCAPISignals	off
RTWCAPIParams	off
RTWCAPIStates	off
RTWCAPIRootIO	off
ERTSrcFileBannerTemplate	ert_code_template.cgt
ERTHdrFileBannerTemplate	ert_code_template.cgt
ERTDataSrcFileTemplate	ert_code_template.cgt
ERTDataHdrFileTemplate	ert_code_template.cgt
ERTCustomFileTemplate	example_file_process.tlc
EnableDataOwnership	off
SignalDisplayLevel	10
ParamTuneLevel	10
GlobalDataDefinition	Auto
DataDefinitionFile	global.c
GlobalDataReference	Auto
ERTFilePackagingFormat	Modular

RateTransitionBlockCode	Inline
DataReferenceFile	global.h
PreserveExpressionOrder	on
PreserveIfCondition	on
ConvertIfToSwitch	on
PreserveExternInFcnDecls	on
PreserveStaticInFcnDecls	on
SuppressUnreachableDefaultCases	off
EnableSignedLeftShifts	off
EnableSignedRightShifts	off
ImplementImageWithCVMat	off
IndentStyle	K&R
IndentSize	2
NewlineStyle	Default
MaxLineWidth	80
EnableUserReplacementTypes	off
ReplacementTypes	TestModel Configuration Set.Components(8).Components(2).ReplacementTypes
MaxIdInt64	MAX_int64_T
MinIdInt64	MIN_int64_T
MaxIdUint64	MAX_uint64_T
MaxIdInt32	MAX_int32_T
MinIdInt32	MIN_int32_T
MaxIdUint32	MAX_uint32_T
MaxIdInt16	MAX_int16_T
MinIdInt16	MIN_int16_T
MaxIdUint16	MAX_uint16_T
MaxIdInt8	MAX_int8_T
MinIdInt8	MIN_int8_T
MaxIdUint8	MAX_uint8_T
BooleanTrueId	true
BooleanFalseId	false
TypeLimitIdReplacementHeaderFile	
MemSecPackage	--- None ---
MemSecFuncInitTerm	Default

MemSecFuncExecute	Default
MemSecFuncSharedUtil	Default
ArrayContainerType	C-style array

Table 4.15. TestModel Configuration Set.Components(8).Components(2).ReplacementTypes

Field	Value
double	
single	
int32	
int16	
int8	
uint32	
uint16	
uint8	
boolean	
int	
uint	
char	
uint64	
int64	

Table 4.16. HDL Coder

Property	Value
HDLSubsystem	
Workflow	Generic ASIC/FPGA
TargetPlatform	
ReferenceDesign	
ReferenceDesignPath	
CoeffPrefix	coeff
DownToArrayIndexing	off
InputType	std_logic_vector
OutputType	Same as input type
ScalarizePorts	off
ScalarizedPortIndexing	Zero-based

SamplesPerCycle	1
InputFIFOSize	10
OutputFIFOSize	10
DelaySizeThreshold	10000
CoeffMultipliers	Multiplier
ResetType	Asynchronous
FIRAdderStyle	linear
MultiplierInputPipeline	0
MultiplierOutputPipeline	0
FoldingFactor	1
NumMultipliers	-1
OptimizeForHDL	off
TimingControllerPostfix	_tc
OptimizeTimingController	on
TimingControllerArch	default
CastBeforeSum	on
TCCounterLimitCompOp	>=
CheckHDL	off
EnablePrefix	enb
ClockEnableInputPort	clk_enable
ClockEnableOutputPort	ce_out
ClockInputPort	clk
ClockEdge	Rising
ResetInputPort	reset
SimulatorFlags	
HDLCompileFilePostfix	_compile.do
HDLCompileInit	vlib %s\n
HDLCompileTerm	
HDLCompileVerilogCmd	vlog %s %s\n
HDLCompileVHDLCmd	vcom %s %s\n
EnableForGenerateLoops	on
HDLMapFilePostfix	_map.txt
HDLMapSeparator	
HDLSimCmd	vsim -voptargs=+acc %s.%s\n
HDLSimFilePostfix	_sim.do
HDLSimProjectFilePostfix	_init.do

HDLSimInit	onbreak resume\nonerror resume\n
HDLSimProjectCmd	project addfile %s\n
HDLSimProjectTerm	project compileall\n
HDLSimProjectInit	project new . %s work\n
HDLSimTerm	run -all\n
HDLSimViewWaveCmd	add wave sim:%s\n
HDLSynthTool	None
HDLSynthCmd	
HDLSynthFilePostfix	
HDLSynthInit	
HDLSynthLibCmd	
HDLSynthLibSpec	
HDLSynthTerm	
ReservedWordPostfix	_rsvd
BlockGenerateLabel	_gen
VHDLLibraryName	work
UseSingleLibrary	off
VHDLArchitectureName	rtl
ClockProcessPostfix	_process
ComplexImagPostfix	_im
ComplexRealPostfix	_re
EntityConflictPostfix	_block
InstancePrefix	u_
InstancePostfix	
InstanceGenerateLabel	_gen
OutputGenerateLabel	outputgen
PackagePostfix	_pkg
SplitEntityArch	off
SplitMooreChartStateUpdate	on
SplitEntityFilePostfix	_entity
SplitArchFilePostfix	_arch
VectorPrefix	vector_of_
ClockInputs	Single
TriggerAsClock	off
AsyncResetPort	off
ConditionalizePipeline	off

InferControlPorts	off
UseRisingEdge	off
ProjectFolder	
TargetDirectory	hdlsrc
TargetSubdirectory	Model
EDAScriptGeneration	on
AddInputRegister	on
AddOutputRegister	on
AddPipelineRegisters	off
PipelinePostfix	_pipe
InputPort	filter_in
OutputPort	filter_out
FracDelayPort	filter_fd
Name	filter
RemoveResetFrom	None
ResetAssertedLevel	Active-high
ReuseAccum	off
ScaleWarnBits	3
SerialPartition	-1
DALUTPartition	-1
DARadix	2
CoefficientSource	Internal
CoefficientMemory	Registers
InputComplex	off
AddRatePort	off
InputDataType	
GenerateHDLCode	on
GenerateModel	on
GenerateTB	off
GenerateCEGenModel	off
ObfuscateGeneratedHDLCode	off
GenerateRecordType	off
Traceability	off
RuntimeReport	off
ResourceReport	off
OptimizationReport	off

ErrorCheckReport	on
HDLGenerateWebview	off
IPCoreReport	off
Recommendations	off
RequirementComments	on
EnableComments	on
ModelName	
Backannotation	off
HierarchicalDistPipelining	off
PreserveDesignDelays	off
AllowDelayDistribution	on
AcquireDesignDelaysForEMLOptimizations	off
ClockRatePipelining	on
CRPWithoutFlattening	on
CRPDelayBalancingIterLimit	10
AdaptivePipelining	off
LUTMapToRAM	on
CloneModules	on
MinDelaysRequiredAtLocalMultirateOutput	1
ClockRatePipelineOutputPorts	off
BalanceClockRateOutputPorts	off
CriticalPathEstimation	off
TimingDatabaseDirectory	
StaticLatencyPathAnalysis	off
shareequalwl	on
sharedmulsign	Signed
MultiplierPromotionThreshold	0
RoutingFudgeFactor	0.5000
OptimizationCompatibilityCheck	off
NumCriticalPathsEstimated	1
CriticalPathEstimationFile	criticalPathEstimated
SLPAFile	staticLatPathAnalysis

SLPALoopsFile	staticLatLoops
SLPABackEdgeFile	staticLatLoopBackEdge
SLPAGMMapMATFile	staticLatGMMap
HardwarePipeliningCharacterizationFile	
HardwarePipeliningParamWarning	0
HighlightFeedbackLoops	on
HighlightFeedbackLoopsFile	highlightFeedbackLoop
HighlightClockRatePipeliningDiagnostic	on
HighlightClockRatePipeliningFile	highlightClockRatePipelining
HighlightRemovedDeadBlocks	on
DistributedPipeliningBarriers	on
DistributedPipeliningBarriersFile	highlightDistributedPipeliningBarriers
HighlightDelayAbsorptionDiagnostic	on
HighlightDelayAbsorptionDiagnosticFile	highlightDelayAbsorption
HighlightLUTPipeliningDiagnostic	on
HighlightLUTPipeliningDiagnosticFile	highlightLUTPipeliningDiagnostic
SetLUTPipeliningOffScriptFile	setLUTPipelineOffScript
BlocksWithNoCharacterizationFile	highlightCriticalPathEstimationOffendingBlocks
AXIStreamingTransformFeatureControl	off
AXIInterface512BitDataPortFeatureControl	off
SerializerRatioThreshold	8192
RetimingCP	off
RetimingCPFile	highlightRetimingCP
ClearHighlightingFile	clearhighlighting
FunctionallyEquivalentRetiming	on

DistributedPipeliningPrecision	-1
DistributedPipelining	off
UseSynthesisEstimatesForDistributedPipelining	off
DistributedPipeliningPriority	Numerical Integrity
PipelineDistributionPriority	Numerical Integrity
RetimingDetails	on
CriticalPathDetails	off
SignalNamesMangling	off
GuidedRetiming	off
LatencyConstraint	0
ReduceMatchingDelays	on
OptimizeBusDelayBalancing	on
OptimizationData	
CPGuidanceFile	
CPAnnotationFile	
OptimizeMdlGen	on
OptimizeHDLIP	off
MulticyclePathInfo	off
MulticyclePathConstraints	off
FloatingPointTargetConfiguration	
GenerateTargetComps	on
NativeFloatingPoint	off
FPToleranceValue	1.0000e-07
FPToleranceStrategy	DEFAULT
nfpLatency	DEFAULT
nfpDenormals	DEFAULT
UseFloatingPoint	off
sschdlMatrixProductSumCustomLatency	-1
AlteraBackwardIncompatibleSinCosPipeline	off
FamilyDevicePackageSpeed	
ToolName	
SynthesisToolChipFamily	

SynthesisToolDeviceName	
SynthesisToolPackageName	
SynthesisToolSpeedValue	
SynthesisTool	
SynthesisProjectAdditionalFiles	
SimulationLibPath	
XilinxSimulatorLibPath	
AdderSharingMinimumBitwidth	0
MultiplierSharingMinimumBitwidth	0
MultiplyAddSharingMinimumBitwidth	0
ShareAdders	off
ShareMultipliers	on
ShareMultiplyAdds	on
ShareMATLABBlocks	on
ShareAtomicSubsystems	on
ShareCounterSerDes	off
UniqueGlobalSchedulingCounters	on
ShareFloatingPointIPs	on
PipelinedSharing	on
EnableFPGAWorkflow	off
FPGAWorkflowParameters	
GainMultipliers	Multiplier
ProductOfElementsStyle	linear
UserComment	
CustomFileHeaderComment	
CustomFileFooterComment	
DateComment	on
SafeZeroConcat	on
SumOfElementsStyle	linear
TargetLanguage	VHDL
TreatRatesAsHardwareRates	off
Oversampling	1

Verbosity	1
TestBenchName	filter_tb
MultifileTestBench	off
IgnoreDataChecking	0
TestBenchPostfix	_tb
TestBenchDataPostfix	_data
TestBenchStimulus	
TestBenchUserStimulus	
TestBenchFracDelayStimulus	
TestBenchCoeffStimulus	
TestBenchRateStimulus	
ForceClockEnable	on
MinimizeClockEnables	off
MinimizeGlobalResets	off
GenerateValidSignalInterface	off
StabilizeInputsForAperiodicRate	on
NoResetInitializationMode	InsideModule
NoResetInitScript	noresetinitscript.tcl
ComplexMulElaboration	MultiplyAddBlock
FlattenBus	off
TestBenchClockEnableDelay	1
ForceClock	on
ClockHighTime	5
ClockLowTime	5
HoldTime	2
InputDataInterval	0
ForceReset	on
ErrorMargin	4
HoldInputDataBetweenSamples	on
InitializeTestBenchInputs	off
ResetLength	2
TestBenchReferencePostFix	_ref
GenerateValidationModel	off
RAMMappingThreshold	256

IOThreshold	5000
TreatIOThresholdAs	Error
MapPipelineDelaysToRAM	off
RemoveRedundantCounters	on
ReplaceUnitDelayWithIntegerDelay	on
ConcatenateDelays	on
MergeDelaysOnFanouts	on
FoldDelaysToConstant	on
RAMArchitecture	WithClockEnable
RAMStyleAttributeName	
UseMatrixTypesInEML	on
InlineMATLABBlockCode	off
SubsystemReuse	Atomic only
InlineHDLCode	off
MaskParameterAsGeneric	off
InlineSubsystems	on
StringTypeSupport	off
DeleteUnusedBlocks	on
DeleteUnusedBlocksUnderMask	off
DeleteUnusedPorts	on
BalanceDelays	on
BalanceDelaysControlsFeedbackLoops	on
DelayAbsorption	on
TargetFrequency	0
ExtraEffortMargin	1
MaxOversampling	Inf
MaxComputationLatency	1
MultiplierPartitioningThreshold	Inf
TreatDelayBalancingFailureAs	Error
TransformDelaysWithControlLogic	on
TransformNonZeroInitValDelay	on
DelayElaborationLimit	20

TapDelayNoElab	on
GenerateCoSimBlock	off
HDLCodeCoverage	off
GenerateHDLTestBench	on
GenerateCoSimModel	None
GenerateSVDPITestBench	None
SimulationTool	Mentor Graphics ModelSim
CoSimModelSetup	CosimBlockAndDut
SynthesisOnDirective	
SynthesisOffDirective	
LoopUnrolling	off
InlineConfigurations	on
UseAggregatesForConst	off
UseVerilogTimescale	on
Timescale	`timescale 1 ns / 1 ns
VerilogFileExtension	.v
SystemVerilogFileExtension	.sv
VHDLFileExtension	.vhd
CodeGenerationOutput	GenerateHDLCode
GeneratedModelName	
GeneratedModelNamePrefix	gm_
ValidationModelNameSuffix	_vnl
LayoutStyle	Default
UseDotLayout	off
ShowCodeGenPIR	off
SerializeModel	0
SerializeIO	0
AutoRoute	on
AutoPlace	on
InterBlkHorzScale	1.7000
InterBlkVertScale	1.2000
CustomDotPath	
HighlightAncestors	on
HighlightColor	cyan
InitializeBlockRAM	on
InitializeRealPort	off

MapVectorPortToStream	off
UseFileIOInTestBench	on
TurnkeyWorkflow	off
AlteraWorkflow	off
GenerateFILBlock	off
CoSimLibPostfix	_cosim
TestBenchInitializeInputs	off
MinimizeIntermediateSignals	off
GenerateCodeInfo	off
GatewayoutWithDTC	off
IncrementalCodeGenForTopModel	off
HDLWFSmartbuild	on
HDLCodingStandard	None
HDLCodingStandardCustomizations	
ReferenceDesignParameter	
HDLLintTool	None
HDLLintInit	
HDLLintTerm	
HDLLintCmd	
ModulePrefix	
DetectBlackBoxNameCollision	Warning
PIRTC	on
UsePipelinedToolboxFunctions	on
savepirtoscript	off
ConcatenateHDLModules	off
ML2PIR	off
OptimBetweenMATLABAndSimulink	off
EnableTestpoints	off
BalanceDelaysForTestpoints	on
GenDUTPortForTunableParam	on
BalanceDelaysForTunableParam	on

TraceabilityStyle	Line Level
TraceabilityProcessing	off
TreatRealsInGeneratedCodeAs	Error
TreatBalanceDelaysOffAs	Error
EnumEncodingScheme	default
CompileStrategy	CompileAll
BuildToProtectModel	off
OptimizeConstants	on
OptimizeFixedPointConstants	off
FrameToSampleConversion	off
InputProcessingOrder	RowMajor
HDLDTO	off
UseArrangeSystem	off
TriggerAsClockWithoutSyncRegisters	on
CompactSwitch	off
SimIndexCheck	off
ScheduleZeroProtection	on
DeploymentSettings	

Chapter 5. Glossary

Atomic Subsystem. A subsystem treated as a unit by an implementation of the design documented in this report. The implementation computes the outputs of all the blocks in the atomic subsystem before computing the next block in the parent system's block execution order (sorted list).

Block Diagram. A Simulink block diagram represents a set of simultaneous equations that relate a system or subsystem's inputs to its outputs as a function of time. Each block in the diagram represents an equation of the form y = f(t, x, u) where t is the current time, u is a block input, y is a block output, and x is a system state (see the Simulink documentation for information on the functions represented by the various types of blocks that make up the diagram). Lines connecting the blocks represent dependencies among the blocks, i.e., inputs whose current values are the outputs of other blocks. An implementation of a design described in this document computes a root or atomic system's outputs at each time step by computing the outputs of the blocks in an order determined by block input/output dependencies.

Block Parameter. A variable that determines the output of a block along with its inputs, for example, the gain parameter of a Gain block.

Block Execution Order. The order in which Simulink evaluates blocks during simulation of a model. The block execution order determined by Simulink ensures that a block executes only after all blocks on whose outputs it depends are executed.

Checksum. A number that indicates whether different versions of a model or atomic subsystem differ functionally or only cosmetically. Different checksums for different versions of the same model or subsystem indicate that the versions differ functionally.

Design Variable. A symbolic (MATLAB) variable or expression used as the value of a block parameter. Design variables allow the behavior of the model to be altered by altering the value of the design variable.

Enumeration Type. Enumerated data is data that is restricted to a finite set of values. An enumerated data type is a MATLAB® class that defines a set of enumerated values. Each enumerated value consists of an enumerated name and an underlying integer which the software uses internally and in generated code.

Signal. A block output, so-called because block outputs typically vary with time.

Virtual Subsystem. A subsystem that is purely graphical, i.e., is intended to reduce the visual complexity of the block diagram of which it is a subsystem. An implementation of the design treats the blocks in the subsystem as part of the first nonvirtual ancestor of the virtual subsystem (see Atomic Subsystem).

Chapter 6. About this Report

Report Overview

This report describes the design of the TestModel system. The report was generated automatically from a Simulink model used to validate the design. It contains the following sections:

Model Version. Specifies information about the version of the model from which this design description was generated. Includes the model checksum, a number that indicates whether different versions of the model differ functionally or only cosmetically. Different checksums for different versions indicate that the versions differ functionally.

Root System. Describes the design's root system.

Subsystems. Describes each of the design's subsystems.

Design Variables. Describes system design variables, i.e., MATLAB variables and expressions used as block parameter values.

Enumeration Type. Describes the enumeration types used by this model.

System Model Configuration. Lists the configuration parameters, e.g., start and stop time, of the model used to simulate the system described by this report.

Requirements. Shows design requirements associated with elements of the design model. This section appears only if the design model contains requirements links.

Glossary. Defines Simulink terms used in this report.

Root System Description

This section describes a design's root system. It contains the following sections:

Diagram. Simulink block diagram that represents the algorithm used to compute the root system's outputs.

Description. Description of the root system. This section appears only if the model's root system has a Documentation property or a Doc block.

Interface. Name, data type, width, and other properties of the root system's input and output signals. The number of the block port that outputs the signal appears in angle brackets appended to the signal name. This section appears only if the root system has input or output ports.

Blocks. This section has two subsections:

- **Parameters.** Describes key parameters of blocks in the root system. This section also includes graphical and/or tabular representations of lookup table data used by lookup table blocks, i.e., blocks that use lookup tables to compute their outputs.
- **Block Execution Order.** Order in which blocks must be executed at each time step in order to ensure that each block's inputs are available when it executes.

State Charts. Describes state charts used in the root system. This section appears only if the root system contains Stateflow blocks.

Subsystem Descriptions

This section describes a design's subsystems. Each subsystem description contains the following sections:
Checksum. This section appears only if the subsystem is an atomic subsystem. The checksum indicates whether the version of the model subsystem used to generate this report differs functionally from other versions of the model subsystem. If two model checksums differ, the corresponding versions of the model differ functionally.
Diagram. Simulink block diagram that graphically represents the algorithm used to compute the subsystem's outputs.
Description. Description of the subsystem. This section appears only if the subsystem has a Documentation property or contains a Doc block.
Interface. Name, data type, width, and other properties of the subsystem's input and output signals. The number of the block port that outputs the signal appears in angle brackets appended to the signal name. This section appears only if the subsystem is atomic and has input or output ports.
Blocks. Blocks that this subsystem contains. This section has two subsections:

- **Parameters.** Key parameters of blocks in the subsystem. This section also includes graphical and/or tabular representations of lookup table data used by lookup table blocks, blocks that use lookup tables to compute their outputs.
- **Block Execution Order.** Order in which the subsystem's blocks must be executed at each time step in order to ensure that each block's inputs are available when the block executes .This section appears only if the subsystem is atomic. Note: in Acrobat(PDF) reports, the number in square brackets next to the block name is a hyperlink to the block parameter table. The number has no model significance.

State Charts. Describes state charts used in the subsystem. This section appears only if the root system contains Stateflow blocks.

State Chart Descriptions

This section describes the state machines used by Stateflow blocks to compute their outputs, i.e., Stateflow blocks. Each state machine description contains the following sections:
Chart. Diagram representing the state machine.
States. Describes the state machine's states. Each state description includes the state's diagram and diagrams and/or descriptions of graphical functions, Simulink functions, truth tables, and MATLAB functions parented by the state.

Transitions. Transitions between the state machine's states. Each transition description specifies the values of key transition properties. Appears only if a transition has properties that do not appear on the chart.
Junctions. Transition junctions. Each junction description specifies the values of key junction properties. Appears only if a junction has properties that do not appear on the chart.
Events. Events that trigger state transitions. Each event description specifies the values of key event properties.
Data. Data types and other properties of the Stateflow block's inputs, outputs, and other state machine data.
Targets. Executable implementations of the state machine used to compute the outputs of the corresponding Stateflow block.
MATLAB Supporting Functions. List of functions invoked by MATLAB functions defined in the chart.