Pham Tuan Minh

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Objective

A highly motivated Electronic and Communication Engineering student with a strong focus on analog IC design and power management circuits. Seeking opportunities to apply and further develop skills in schematic design, simulation, and verification using industry-standard tools such as Cadence Virtuoso. Eager to contribute to innovative projects in semiconductor and analog design environments.

Education

Hanoi University of Science and Technology, Engineer of Electronics and Communication — Sept 2021 – July 2025

- GPA: 3.45/4.0
- Scholarship for Academic Excellence – Semester 2023.2
- Core Subjects:
  - Verilog Design – A
  - Analog Electronics – A
  - Semiconductor Electronics – A
  - C/C++ Programming – A
  - Digital System Design I II – B+/A
  - Circuit Theory – B

IC LAB Design, Hanoi University of Science and Technology — 2023 – Present

- Supervised by Dr. Nguyen Vu Thang
- Practical analog IC design projects
- Focused on power management circuits
- Joined weekly seminars and design reviews with IC research team

Skills

Tools: Cadence Virtuoso, ModelSim, Arduino IDE

Languages: C/C++, Verilog, Python

Other: VSTEP B2 (7.0), English reading proficiency, Presentation skills, Documentation writing

Projects

Buck Converter Design (Thesis Project) — Mar 2025 – Jul 2025

- Took full responsibility for the design and simulation of a low-voltage Buck DC-DC converter in Cadence Virtuoso
- Defined design specifications including output voltage, efficiency targets, and transient response requirements
- Performed steady-state waveform simulations to validate switching behavior
- Documented results in a detailed thesis with waveform analysis and design trade-offs

Folded Cascode Operational Amplifier Design — Aug 2024 – Oct 2024

- Designed and optimized a folded cascode op-amp targeting high gain, wide bandwidth, and low power
- Achieved open-loop gain >40 dB and GBW >10 MHz under target loading conditions
- Analyzed stability with phase margin checks

UART Communication System on FPGA Apr 2024 – Jul 2024

- Designed a Universal Asynchronous Receiver Transmitter (UART) fully in Verilog HDL
- Implemented Tx, Rx, and Frame Check submodules with configurable baud rates and parity
- Verified operation using testbenches in ModelSim and deployed on FPGA board for real-time testing

Semiconductor Q&A Chatbot Feb 2024 – Apr 2024

- Developed a chatbot using Rasa that answers conceptual and technical questions about semiconductor devices
- Created a training dataset with 100+ intents and story flows using YAML files
- Integrated a fallback mechanism and response variation using NLP confidence scoring

Door Locking System using Arduino & ESP32 Sep 2023 – Dec 2023

- Built a secure door access control system using Arduino Uno and ESP32 communication
- Designed data exchange protocol using UART and implemented on both microcontrollers
- Developed a mobile application interface to control access remotely via Wi-Fi

Experience

Analog IC Design Intern, VIETA Solutions Vietnam Co., Ltd Mar 2025 – Jun 2025

- Joined the analog IC design team specializing in power management circuits
- Conducted schematic design, simulation verification using Cadence Virtuoso
- Assisted in debugging analog blocks and optimizing key performance metrics (gain, power, area)
- Gained hands-on experience with industry-standard analog design flow

Activities

Youth Union Member, Hanoi University of Science and Technology 2021 – 2024
Student Assistance Program 2022 – Present