

Level_V2

Table of contents

Level_V2

PLC_1 [CPU 315-2 PN/DP]	4 - 1
Program blocks	
Main [OB1]	5 - 1
Block_1 [FC1]	6 - 1
Block_2 [FC2]	7 - 1
PID [FC3]	8 - 1
Data_block_1 [DB1]	9 - 1
CYC_INT5 [OB35]	10 - 1
Technology objects	11 - 1
PLC tags	12 - 1
Default tag table [15]	13 - 1
PLC data types	14 - 1
Watch and force tables	
Force table	15 - 1
Watch table_1	16 - 1
PLC supervisions & alarms	
PLC alarms	17 - 1
User diagnostics alarms	18 - 1
System alarms	19 - 1
PLC alarm text lists	20 - 1
Local modules	
PS 307 5A_1	21 - 1
PLC_1 [CPU 315-2 PN/DP]	22 - 1
DI 8/DO 8x24VDC/0.5A_1	23 - 1
AI 2x12BIT_1	24 - 1
AO 4x12BIT_1	25 - 1
Ungrouped devices	26 - 1
Security settings	27 - 1
Cross-device functions	
Project traces	
Measurements	28 - 1
Common data	
Alarm classes	29 - 1
Logs	30 - 1
Languages & resources	
Project languages	31 - 1
Project texts	

Owner	Project name	Level_V2	Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
	Location			
Designed By	Description 1st			
Checked By	Description 2nd	Language	en-US	
Approved By	1st View	Version	Sheet 2 - 1	

	1	2	3	4
A	Project texts		32 - 1	
B				
C				
D				
E				
F	Owner	Projectname Level_V2		Date 12/15/2022
	Operator	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
		Location		
	Designed By	Description 1st		
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	Approved By	1st View	Version	Sheet 2 - 2

Level_V2

Project			
Name:	Level_V2	Creation time:	12/3/2022 3:38:30 AM
Last change	12/10/2022 10:01:47 AM	Author:	Admin
Last modified by:	Admin	Version:	
Comment:			

Operating system	
Name	Description
Operating system	Microsoft Windows 11 Home Single Language
Version of the operating system	6.3.9600.0
Operating system service pack	
Version of the Internet Explorer	11.1.22621.0
Computer name	VU_THACH
User name	VU_THACH\daveb
Installation path of the TIA Portal	C:\Program Files\Siemens\Automation\Portal V16

Components		
Name	Version	Release
TIA Portal Project Server V16 - TIA Portal Project Server Single SetupPackage V16.0 (MUSERVERV16)	V16.0	V16.00.00.00_31.02.00.01
Siemens Totally Integrated Automation Portal V16 - SIMATIC S7-PLCSIM V16.0 (S7_PLCSIM_V16)	V16.0	V16.00.00.00_31.00.13.01
TIA Administrator - AWB Licensing Module V1.0 + SP2 (TIAADMIN)	V1.0 + SP2	V01.00.02.00_01.10.00.01
TIA Administrator - AWB Software Management V1.0 + SP2 (TIAADMIN)	V1.0 + SP2	V01.00.02.00_01.10.00.01
TIA Administrator - TIA UMC Agent Configurator Module V1.0 + SP2 (TIAADMIN)	V1.0 + SP2	V01.00.02.00_01.10.00.01
TIA Administrator - TIA Administrator V1.0 SP2 (TIAADMIN)	V1.0 + SP2	V01.00.02.00_01.10.00.01
Siemens Totally Integrated Automation Portal V16 - HM All Editions Single SetupPackage V16.0 (TIAP16)	V16.0	V16.00.00.00_31.02.00.01
Siemens Totally Integrated Automation Portal V16 - HM NoBasic Single SetupPackage V16.0 (TIAP16)	V16.0	V16.00.00.00_31.02.00.01
Siemens Totally Integrated Automation Portal V16 - Hardware Support Base Package 0 V16.0 (TIAP16)	V16.0	V16.00.00.00_27.01.00.01
Siemens Totally Integrated Automation Portal V16 - Multiuser Client Single SetupPackage V16.0 (TIAP16)	V16.0	V16.00.00.00_31.02.00.01
Siemens Totally Integrated Automation Portal V16 - Version Control Interface SetupPackage V16.0 (TIAP16)	V16.0	V16.00.00.00_31.02.00.01
Siemens Totally Integrated Automation Portal V16 - STEP 7 Safety Single SetupPackage V16.0 (TIAP16)	V16.0	V16.00.00.00_31.02.00.01

Owner	Project name Level_V2		Date 12/15/2022
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Approved By	1st View	Version	Sheet 3 - 1

1		2	3	4
A				
B				
C				
D				
E				
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Siemens Totally Integrated Automation Portal V16 - STEP 7 Single SetupPackage V16.0 (TIAP16)	V16.0	V16.00.00.00_31.02.00.01
Siemens Totally Integrated Automation Portal V16 - Hardware Support Base Package 02 V16.0 (TIAP16)	V16.0	V16.00.00.00_27.01.00.01
Siemens Totally Integrated Automation Portal V16 - Hardware Support Base Package 03 V16.0 (TIAP16)	V16.0	V16.00.00.00_27.01.00.01
Siemens Totally Integrated Automation Portal V16 - Hardware Support Base Package 04 V16.0 (TIAP16)	V16.0	V16.00.00.00_27.01.00.01
Siemens Totally Integrated Automation Portal V16 - Support Base Package TO-01 V16.0 (TIAP16)	V16.0	V16.00.00.00_27.01.00.01
Siemens Totally Integrated Automation Portal V16 - Support Base Package TO-02 V16.0 (TIAP16)	V16.0	V16.00.00.00_27.01.00.01
Siemens Totally Integrated Automation Portal V16 - Hardware Support Base Package WCF-01 V16.0 (TIAP16)	V16.0	V16.00.00.00_27.01.00.01
Siemens Totally Integrated Automation Portal V16 - TIACOMP CHECK Single SetupPackage V16.0 (TIAP16)	V16.0	V16.00.00.00_31.02.00.01
Siemens Totally Integrated Automation Portal V16 - Simatic Single SetupPackage V16.0 (TIAP16)	V16.0	V16.00.00.00_31.02.00.01
Siemens Totally Integrated Automation Portal V16 - WinCC Single SetupPackage V16.0 (TIAP16)	V16.0	V16.00.00.00_31.02.00.01
Siemens Totally Integrated Automation Portal V16 - Openness SetupPackage V16.0 (TIAP16)	V16.0	V16.00.00.00_31.02.00.01
Siemens Totally Integrated Automation Portal V16 - WinCC Transfer Mandatory Single SetupPackage V16.0 (TIAP16)	V16.0	V16.00.00.00_31.02.00.01
User Management Component - UserManagementComponentx64 V2.7 (UMC64)	V2.7	V02.07.00.00_04.06.00.07
WinCC Runtime Advanced V16.0 - HMIRTM Tagging Package 01 Single SetupPackage V16.0 (HMIRTM_V11)	V16.0	V16.00.00.00_31.02.00.01
Siemens Totally Integrated Automation Portal V16 - Simatic Single SetupPackage 32 Bit V16.0 (TIAP16)	V16.0	V16.00.00.00_31.02.00.01
Siemens Totally Integrated Automation Portal V16 - WinCC Single SetupPackage 32 Bit V16.0 (TIAP16)	V16.0	V16.00.00.00_31.02.00.01
SIMATIC HMI License Manager Panel Plugin (x64)	16.0.0.0	V16.00.00.00_31.02.00.01
SIMATIC WinCC Runtime Advanced Driver (x64)	16.0.0.0	V16.00.00.00_31.02.00.01
ETWEEventCollector	16.0.0.0	V16.00.00.00_31.02.00.01
SIMATIC NCM FWL 64	5.6.0.3	K5.6.0.3_1.1.0.2
NCM GPRS 64	01.02.00.00	V1.2.0.0_2.1.0.1

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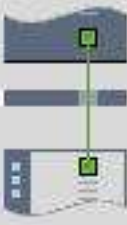
Level_V2

PLC_1 [CPU 315-2 PN/DP]

PLC_1			
General			
Name	PLC_1	Author	Admin
Comment		Rack	0
Slot	2		
General\Catalog information			
Short designation	CPU 315-2 PN/DP	Description	Work memory 384KB; 0.05ms/1000 instructions; PROFINET interface; S7 communication (loadable FBs/FCs); PROFINET IO controller; supports RT/IRT; 2 ports; PROFINET CBA; PROFINET CBA Proxy; TCP/IP transport protocol; combined MPI/DP interface (MPI or DP master or DP slave); multi-tier configuration up to 32 modules; constant bus cycle time; routing; firmware V3.2
Article number	6ES7 315-2EH14-0AB0	Firmware version	V3.2
General\Identification & Maintenance			
Plant designation		Location identifier	
MPI/DP interface\General			
Name	MPI/DP interface_1	Comment	
MPI/DP interface\MPI address\Interface networked with			
Subnet:	Not networked		
MPI/DP interface\MPI address\Parameters			
Interface type:	Mpi	Address:	2
Highest address:		Transmission speed:	
MPI/DP interface\Time-of-day synchronization\SIMATIC mode			
Type of synchronization	None	Time interval	None
MPI/DP interface\Diagnostics addresses\Diagnostics addresses			
Start address	2047		
PROFINET interface [X2]\General			
Name	PROFINET interface_1	Comment	
PROFINET interface [X2]\Ethernet addresses\Interface networked with			
Subnet:	Not connected		
PROFINET interface [X2]\Ethernet addresses\IP protocol			
IP configuration	Set IP address in the project	IP address:	192.168.0.1
Subnet mask:	255.255.255.0	Use router	False
PROFINET interface [X2]\Ethernet addresses\PROFINET			
PROFINET device name is set directly at the device	False	Generate PROFINET device name automatically	True
PROFINET device name:	plc_1	Converted name:	plcxb1d0ed
Device number:	0		

Owner	Project name	Level_V2	Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
	Location			
Designed By	Description 1st			
Checked By	Description 2nd	Language	en-US	
Approved By	1st View	Version	Sheet 4 - 1	

1		2		3		4	
A	PROFINET interface [X2]\Time-of-day synchronization\NTP mode						
	Enable time synchronization via NTP server	False				IP addresses	
	Server 1	0.0.0.0		Server 2	0.0.0.0		
	Server 3	0.0.0.0		Server 4	0.0.0.0		
	Update interval	10s					
B	PROFINET interface [X2]\Operating mode						
	IO controller	True		IO system			
	Device number	0		IO device	False		
	PROFINET interface [X2]\Advanced options\Interface options						
	Call the user program if communication errors occur	False		Support device replacement without exchangeable medium	True		
C	Use IEC V2.2 LLDP mode	True		Keep-Alive connection monitoring:	0s		
	PROFINET interface [X2]\Advanced options\Real time settings\IO communication						
	Send clock:	1.000ms					
	PROFINET interface [X2]\Advanced options\Real time settings\Synchronization						
	RT class:	RT,IRT					
	PROFINET interface [X2]\Advanced options\Real time settings\Real time options						
	Calculated bandwidth for cyclic IO data:	0.000ms		Calculated bandwidth for cyclic IO data:	0.000%		
	PROFINET interface [X2]\Advanced options\Port [X2 P1]\General						
	Name	Port_1		Comment			
	PROFINET interface [X2]\Advanced options\Port [X2 P1]\Port interconnection\Local port:						
Local port:	PLC_1\PROFINET interface_1 [X2]\Port_1 [X2 P1 R]		Medium:	Copper			
Cable name:	---						
							
E	PROFINET interface [X2]\Advanced options\Port [X2 P1]\Port interconnection\Partner port:						
		Monitoring of partner port is not possible		Partner port:	Any partner		
	PROFINET interface [X2]\Advanced options\Port [X2 P1]\Port options\Activate						
	Activate this port for use	True					
	PROFINET interface [X2]\Advanced options\Port [X2 P1]\Port options\Connection						
	Transmission rate / duplex:	Automatic		Monitor	False		
	Enable autonegotiation	True					
F	PROFINET interface [X2]\Advanced options\Port [X2 P1]\Port options\Boundaries						
	End of detection of accessible devices	False		End of topology discovery	False		
Owner		Project name Level_V2				Date 12/15/2022	
Operator		Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2					
		Location					
Designed By		Description 1st					
Checked By		Description 2nd				Language en-US	
Approved By		1st View				Version	
						Sheet 4 - 2	

1		2		3		4		
A	End of the sync domain		False					
	PROFINET interface		[X2]\Advanced options\Port [X2 P1]\Diagnostics addresses\Diagnostics addresses					
	Start address		2045					
	PROFINET interface		[X2]\Advanced options\Port [X2 P2]\General					
	Name		Port_2		Comment			
	PROFINET interface		[X2]\Advanced options\Port [X2 P2]\Port interconnection\Local port:					
	Local port:		PLC_1\PROFINET interface_1 [X2]\Port_2 [X2 P2 R]		Medium:		Copper	
	Cable name:		---					
								
C	PROFINET interface		[X2]\Advanced options\Port [X2 P2]\Port interconnection\Partner port:					
			Monitoring of partner port is not possible		Partner port:		Any partner	
	PROFINET interface		[X2]\Advanced options\Port [X2 P2]\Port options\Activate					
	Activate this port for use		True					
	PROFINET interface		[X2]\Advanced options\Port [X2 P2]\Port options\Connection					
	Transmission rate / duplex:		Automatic		Monitor		False	
	Enable autonegotiation		True					
D	PROFINET interface		[X2]\Advanced options\Port [X2 P2]\Port options\Boundaries					
	End of detection of accessible devices		False		End of topology discovery		False	
	End of the sync domain		False					
	PROFINET interface		[X2]\Advanced options\Port [X2 P2]\Diagnostics addresses\Diagnostics addresses					
	Start address		2044					
	PROFINET interface		[X2]\Diagnostics addresses\Diagnostics addresses					
	Start address		2046					
	Startup							
	Startup if preset configuration does not match actual configuration		True		Startup after POWER ON		Warm restart	
	E	Startup\Monitoring time for						
Ready message from modules		650x 100 ms		Parameter transfer to modules		100x 100 ms		
Cycle								
Cycle monitoring time		500ms		Cycle load due to communication		20%		
Size of the process image input:		128		Size of the process image output:		128		
OB85 call if I/O access error occurs		No OB85 call						
F	Owner		Project name Level_V2				Date 12/15/2022	
	Operator		Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2					
			Location					
	Designed By		Description 1st					
	Checked By		Description 2nd			Language en-US		
	Approved By		1st View			Version		
		Sheet 4 - 3						

	1	2	3	4		
A	Cycle\Prioritized OCM communication					
	Prioritized OCM communication	False				
	Clock memory					
	Clock memory	False	Memory byte	0		
	Interrupts\Time-of-day interrupts\					
	OB number	Priority	Active	Execution	Start time	
	OB 10	2	False	None	1994-01-01 00:00:00.000	
B	Interrupts\Time-delay interrupts\					
	OB number	Priority	Process image partition(s)			
	OB 20	3	None			
	OB 21	4	None			
	Interrupts\Cyclic interrupts\					
	OB number	Priority	Execution	Phase offset	Unit	
	OB 32	9	1000	0	ms	
	OB 33	10	500	0	ms	
	OB 34	11	200	0	ms	
	OB 35	12	250	0	ms	
	Interrupts\Hardware interrupts\					
	OB number	Priority	Process image partition(s)			
	OB 40	16	None			
C	Interrupts\Interrupts for DPV1\					
	OB number	Priority				
	OB 55	2				
	OB 56	2				
	OB 57	2				
	Interrupts\Isochronous mode interrupts					
	OB number	Priority	Distributed I/O	Process image partition(s)	Delay time (ms)	Automatic setting
	OB 61	25	0		0.000	True
D	Interrupts\Isochronous mode interrupts\OB 61					
	Application cycle:	0ms	Delay time:	0.000ms		
	Automatic setting	True	Distributed I/O:	0		
	Interrupts\Isochronous mode interrupts\OB 61\Process image partition					
	PIP:					
	Interrupts\Asynchronous error interrupts\					
	OB number	Priority				
	OB 82	26				
	OB 83	26				
	OB 85	26				
	OB 86	26				
	OB 87	26				
	Diagnostics system					
	Report cause of STOP	True	Number of alarms in the diagnostics buffer	10		
E	System diagnostics\General					
	Activate system diagnostics for this device	False				
F	Owner	Project name Level_V2		Date 12/15/2022		
	Operator	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2				
		Location				
	Designed By	Description 1st				
	Checked By	Description 2nd	Language en-US			
	Approved By	1st View	Version	Sheet 4 - 4		

	1	2	3	4		
A	Time of day					
	Correction factor	0ms				
B	Time of day\Synchronization on PLC					
	Type of synchroni- zation	None	Time interval	None		
	Time of day\Synchronization on MPI					
	Type of synchroni- zation	None	Time interval	None		
	Web server\General					
	Activate web server on this module	False	Permit access only with HTTPS	False		
	Web server\Automatic update					
	Enable automatic update	False	Update interval	0s		
	Web server\Languages					
	Active	Web server language		Assign project language		
C	False	German		None		
	False	English		None		
	False	French		None		
	False	Spanish		None		
	False	Italian		None		
	False	Japanese		None		
	False	Chinese (simplified)		None		
	Web server\User management					
	User name		User rights			
	Everybody					
D	Web server\User-defined web pages					
	Application name	HTML source path	Default HTML page	Files with dy- namic content	Web DB number	Fragment DB number
			index.htm	.htm;.html	333	334
	Web server\Text_Display_classes_of_messages					
	Display class			Active		
	0			True		
	1			True		
	2			True		
	3			True		
	4			True		
5			True			
6			True			
7			True			
8			True			
9			True			
10			True			
11			True			
12			True			
13			True			
14			True			
15			True			
16			True			
E	Owner		Project name Level_V2		Date 12/15/2022	
	Operator		Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2			
			Location			
	Designed By		Description 1st			
	Checked By		Description 2nd		Language en-US	
	Approved By		1st View		Version	
F					Sheet 4 - 5	

	1	2	3	4
A	Retentive memory			
	Number of memory bytes starting at MB 0	0	Number of S7 timers starting at T 0	0
	Number of S7 counters starting at C 0	0		
	Protection			
	Password		Confirm password	
	Protection\			
	Level of protection	No protection		
	Protection\Can be canceled with password			
	Can be canceled with password	False		
	B	Connection resources		
PG communication:		1	OP communication:	1
S7 basic communication:		0	S7 communication:	0
Maximum number of S7 connection resources:		16		
Overview of addresses\Overview of addresses\Overview of addresses				
Inputs		True	Outputs	True
Address gaps		False	Slot	True
C				
D				
E				
F	Owner	Projectname Level_V2		Date 12/15/2022
	Operator	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
		Location		
	Designed By	Description 1st		
	Checked By	Description 2nd	Language en-US	
	Approved By	1st View	Version	Sheet 4 - 6

1		2		3		4	
A	Type	I*	Addr. from	2047	Addr. to	2047	
	Module	MPI/DP interface_1	PIP	---	Device name	PLC_1 [CPU 315-2 PN/DP]	
	Device number	-	Size	0 Bits	Master / IO system	-	
B	Rack	0	Slot	2 X1			
	Type	I*	Addr. from	2046	Addr. to	2046	
	Module	PROFINET interface_1	PIP	---	Device name	PLC_1 [CPU 315-2 PN/DP]	
B	Device number	-	Size	0 Bits	Master / IO system	-	
	Rack	0	Slot	2 X2			
	Type	I*	Addr. from	2045	Addr. to	2045	
C	Module	Port_1	PIP	---	Device name	PLC_1 [CPU 315-2 PN/DP]	
	Device number	-	Size	0 Bits	Master / IO system	-	
	Rack	0	Slot	2 X2 P1 R			
C	Type	I*	Addr. from	2044	Addr. to	2044	
	Module	Port_2	PIP	---	Device name	PLC_1 [CPU 315-2 PN/DP]	
	Device number	-	Size	0 Bits	Master / IO system	-	
D	Rack	0	Slot	2 X2 P2 R			
	Type	I	Addr. from	272	Addr. to	275	
	Module	AI 2x12BIT_1	PIP	OB1-PI	Device name	PLC_1 [CPU 315-2 PN/DP]	
D	Device number	-	Size	4 Bytes	Master / IO system	-	
	Rack	0	Slot	5			
	Type	O	Addr. from	288	Addr. to	295	
E	Module	AO 4x12BIT_1	PIP	OB1-PI	Device name	PLC_1 [CPU 315-2 PN/DP]	
	Device number	-	Size	8 Bytes	Master / IO system	-	
	Rack	0	Slot	6			
E	Type	I	Addr. from	0	Addr. to	0	
	Module	DI 8/DO 8x24VDC/0.5A_1	PIP	OB1-PI	Device name	PLC_1 [CPU 315-2 PN/DP]	
	Device number	-	Size	1 Bytes	Master / IO system	-	
F	Rack	0	Slot	4			
	Type	O	Addr. from	0	Addr. to	0	
	Module	DI 8/DO 8x24VDC/0.5A_1	PIP	OB1-PI	Device name	PLC_1 [CPU 315-2 PN/DP]	
F	Device number	-	Size	1 Bytes	Master / IO system	-	
	Rack	0	Slot	4			

Owner	Project name		Level_V2	Date	12/15/2022
	Operator	Project path			
		E:\Đại học\Năm 3\HKII\Thực tập ĐKTĐ\On thi\Level_V2			
Designed By		Description 1st			
Checked By		Description 2nd		Language en-US	
Approved By		1st View		Version	Sheet 4 - 7

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / Program blocks

Main [OB1]

Main Properties

General

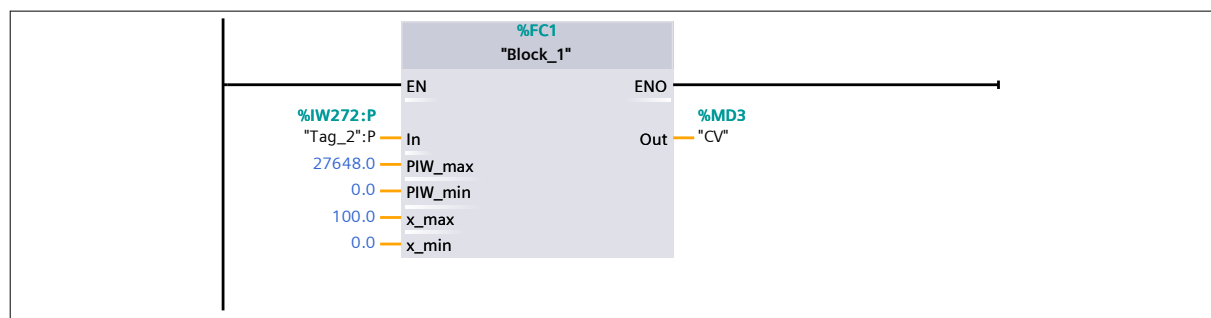
Name	Main	Number	1
Type	OB	Language	LAD
Numbering	Manual		

Information

Title	"Main Program Sweep (Cycle)"	Author	
Comment		Family	
Version	0.1	User-defined ID	

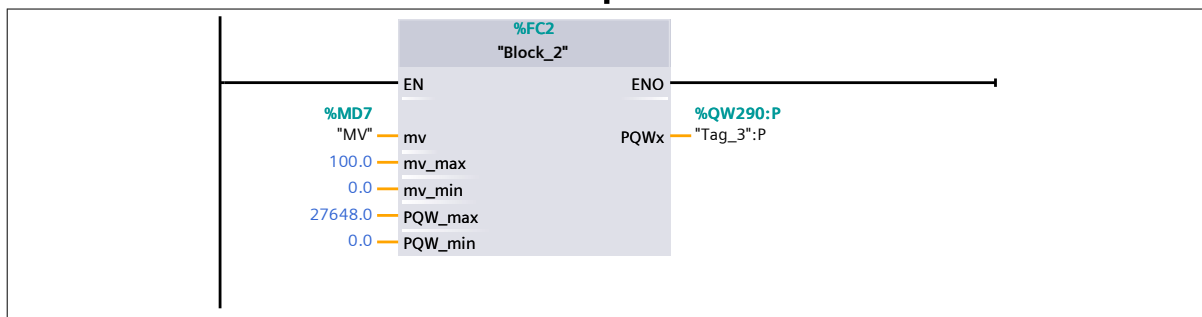
Name	Data type	Offset	Default value	Comment
▼ Temp				
OB1_EV_CLASS	Byte	0.0		Bits 0-3 = 1 (Coming event), Bits 4-7 = 1 (Event class 1)
OB1_SCAN_1	Byte	1.0		1 (Cold restart scan 1 of OB 1), 3 (Scan 2-n of OB 1)
OB1_PRIORITY	Byte	2.0		Priority of OB Execution
OB1_OB_NUMBR	Byte	3.0		1 (Organization block 1, OB1)
OB1_RESERVED_1	Byte	4.0		Reserved for system
OB1_RESERVED_2	Byte	5.0		Reserved for system
OB1_PREV_CYCLE	Int	6.0		Cycle time of previous OB1 scan (milliseconds)
OB1_MIN_CYCLE	Int	8.0		Minimum cycle time of OB1 (milliseconds)
OB1_MAX_CYCLE	Int	10.0		Maximum cycle time of OB1 (milliseconds)
OB1_DATE_TIME	Date_And_Time	12.0		Date and time OB1 started
Constant				

Network 1:



Network 2:

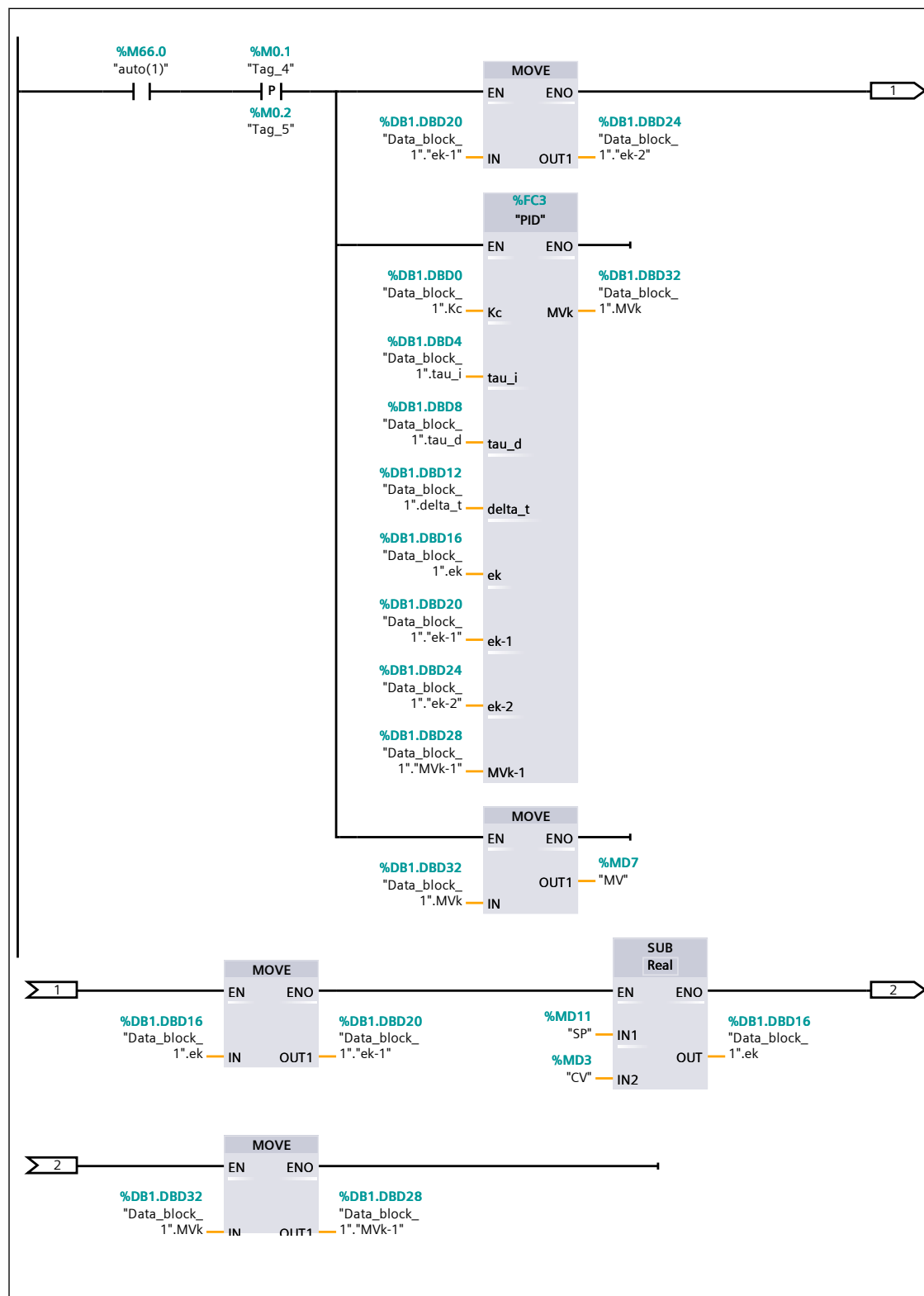
Owner	Project name	Level_V2	Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
	Location			
Designed By	Description 1st			
Checked By	Description 2nd	Language	en-US	
Approved By	1st View	Version	Sheet 5 - 1	



Network 3:

Owner	Projectname Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
Designed By	Description 1st		
Checked By	Description 2nd	Language en-US	
Approved By	1st View	Version	Sheet 5 - 2

Network 3: (1.1 / 2.1)



2.1 (Page5 - 4)

Owner	Projectname Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
	Description 1st		
Designed By	Description 2nd		Language en-US
Checked By	1st View	Version	Sheet 5 - 3
Approved By			

1

2

3

4

A

Network 3: (2.1 / 2.1)

1.1 (Page5 - 3)

B

C

D

E

F

Owner

Projectname Level_V2

Date 12/15/2022

Operator

Project path
E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2

Location

Designed By

Description 1st

Checked By

Description 2nd

Language en-US

Approved By

1st View

Version

Sheet 5 - 4

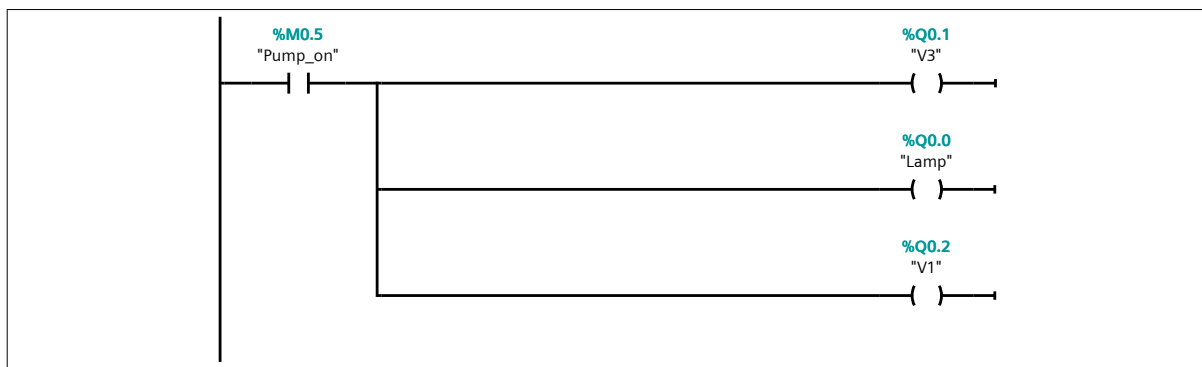
1

2

3

4

A

Network 4:

B

C

D

E

F

Owner	Projectname Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
	Description 1st		
Designed By	Description 2nd		Language en-US
Checked By	1st View		Version
Approved By			Sheet 5 - 5

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / Program blocks

Block_1 [FC1]

Block_1 Properties

General

Name	Block_1	Number	1
Type	FC	Language	LAD
Numbering	Automatic		

Information

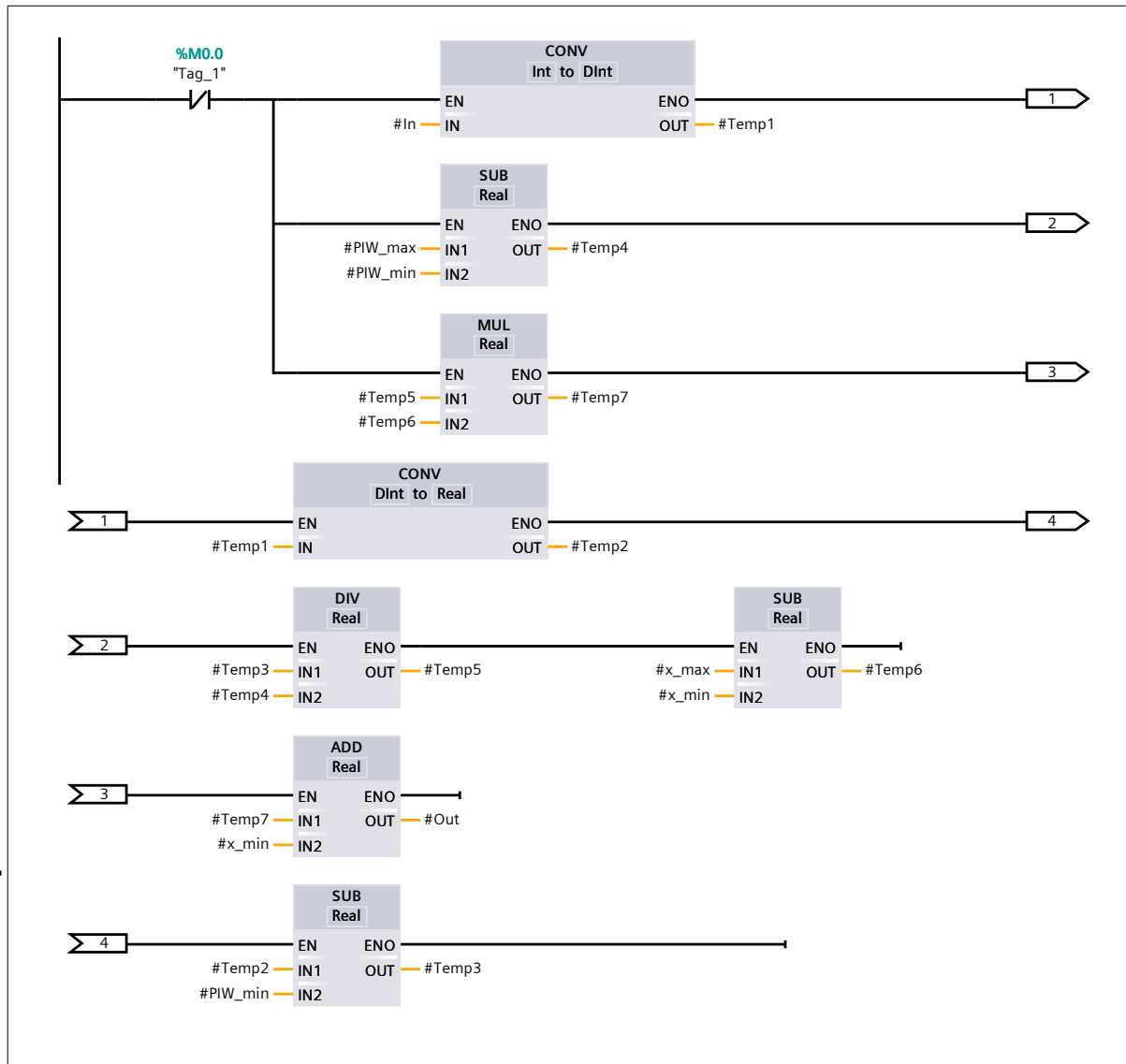
Title		Author	
Comment		Family	
Version	0.1	User-defined ID	

Name	Data type	Offset	Default value	Comment
▼ Input				
In	Int			
PIW_max	Real			
PIW_min	Real			
x_max	Real			
x_min	Real			
▼ Output				
Out	Real			
InOut				
▼ Temp				
Temp1	DInt	0.0		
Temp2	Real	4.0		
Temp3	Real	8.0		
Temp4	Real	12.0		
Temp5	Real	16.0		
Temp6	Real	20.0		
Temp7	Real	24.0		
Constant				
▼ Return				
Block_1	Void			

Network 1:

Owner	Projectname	Level_V2	Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
	Location			
Designed By	Description 1st			
Checked By	Description 2nd	Language	en-US	
Approved By	1st View	Version	Sheet 6 - 1	

Network 1:



Owner	Project name Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
	Description 1st		
Designed By	Description 2nd		Language en-US
Checked By	1st View	Version	Sheet 6 - 2
Approved By			

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / Program blocks

Block_2 [FC2]

Block_2 Properties

General

Name	Block_2	Number	2
Type	FC	Language	LAD
Numbering	Automatic		

Information

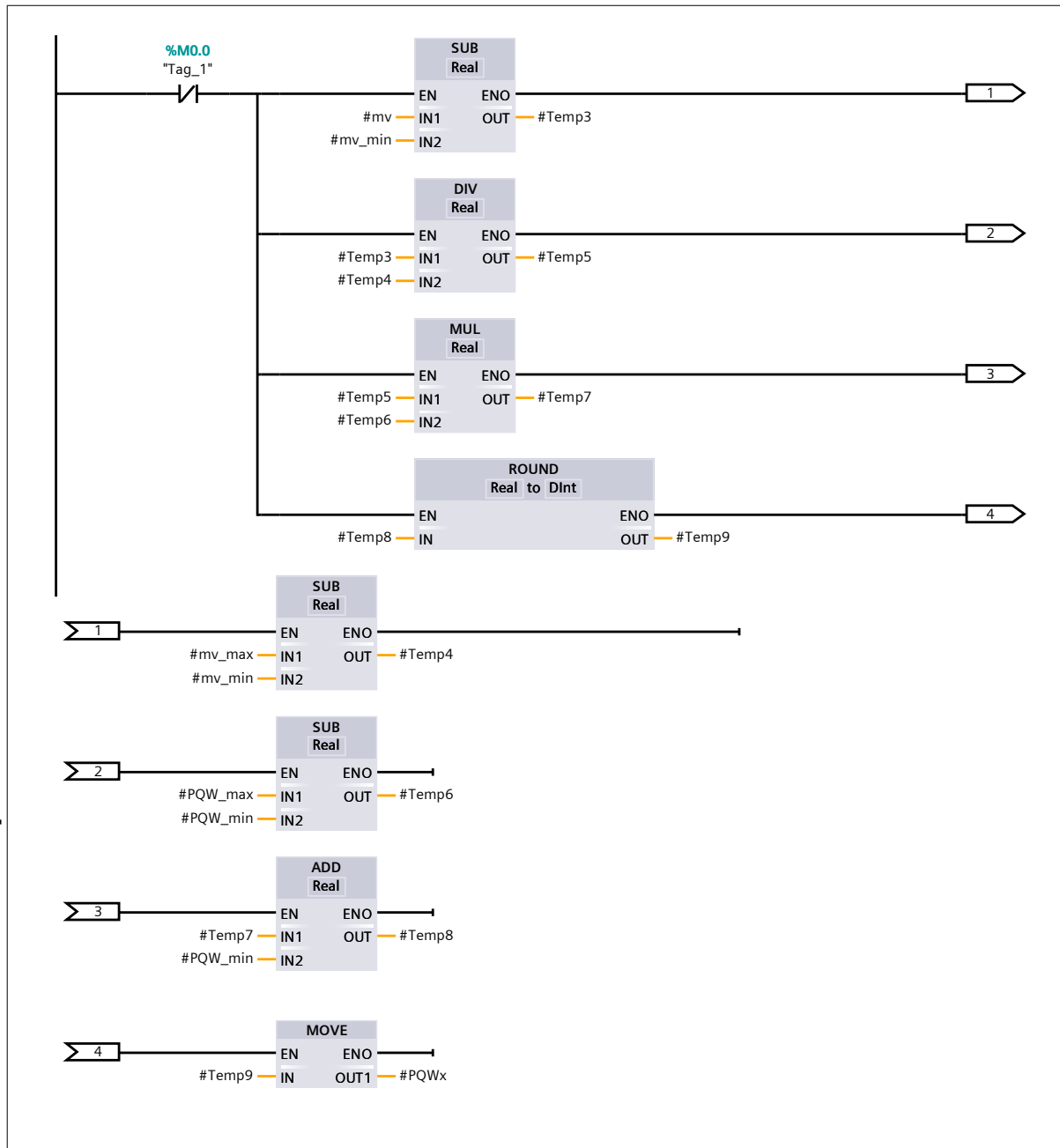
Title		Author	
Comment		Family	
Version	0.1	User-defined ID	

Name	Data type	Offset	Default value	Comment
▼ Input				
mv	Real			
mv_max	Real			
mv_min	Real			
PQW_max	Real			
PQW_min	Real			
▼ Output				
PQWx	Int			
InOut				
▼ Temp				
Temp3	Real	0.0		
Temp4	Real	4.0		
Temp5	Real	8.0		
Temp6	Real	12.0		
Temp7	Real	16.0		
Temp8	Real	20.0		
Temp9	DInt	24.0		
Constant				
▼ Return				
Block_2	Void			

Network 1:

Owner	Projectname	Level_V2	Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
	Location			
Designed By	Description 1st			
Checked By	Description 2nd	Language	en-US	
Approved By	1st View	Version	Sheet 7 - 1	

Network 1:



Owner	Project name Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKII\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
	Description 1st		
Designed By	Description 2nd		Language en-US
Checked By	1st View	Version	Sheet 7 - 2
Approved By			

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / Program blocks

PID [FC3]

PID Properties

General

Name	PID	Number	3
Type	FC	Language	LAD
Numbering	Automatic		

Information

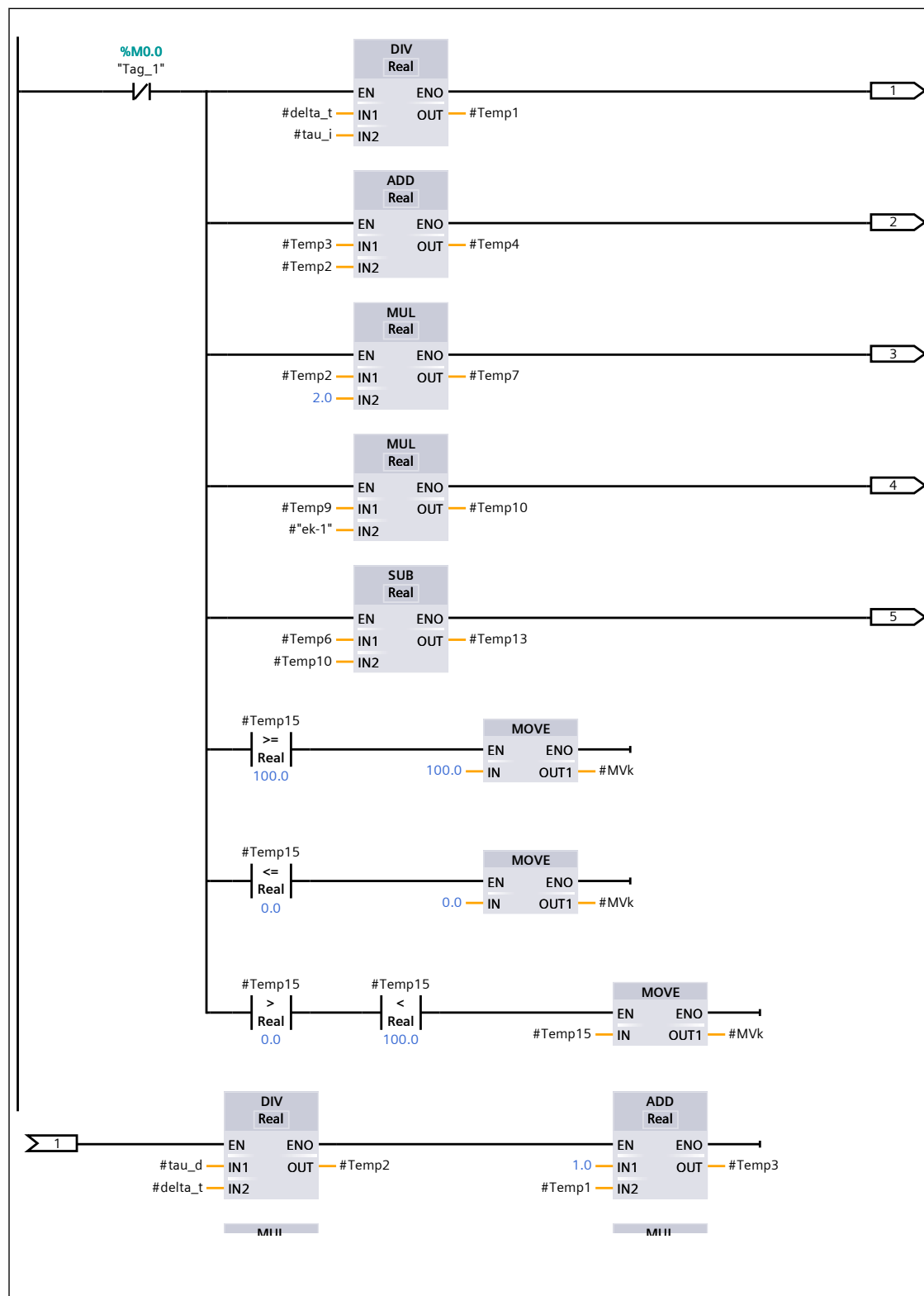
Title		Author	
Comment		Family	
Version	0.1	User-defined ID	

Name	Data type	Offset	Default value	Comment
▼ Input				
Kc	Real			
tau_i	Real			
tau_d	Real			
delta_t	Real			
ek	Real			
ek-1	Real			
ek-2	Real			
MVk-1	Real			
▼ Output				
MVk	Real			
InOut				
▼ Temp				
Temp1	Real	0.0		
Temp2	Real	4.0		
Temp3	Real	8.0		
Temp4	Real	12.0		
Temp5	Real	16.0		
Temp6	Real	20.0		
Temp7	Real	24.0		
Temp8	Real	28.0		
Temp9	Real	32.0		
Temp10	Real	36.0		
Temp11	Real	40.0		
Temp12	Real	44.0		
Temp13	Real	48.0		
Temp14	Real	52.0		
Temp15	Real	56.0		
Constant				
▼ Return				
PID	Void			

Owner	Project name	Level_V2	Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Designed By	Description 1st			
Checked By	Description 2nd	Language	en-US	
Approved By	1st View	Version	Sheet 8 - 1	

	1	2	3	4
A	<div>Network 1:</div>			
B				
C				
D				
E				
F	<div>Owner</div>	<div>Projectname</div> Level_V2		<div>Date</div> 12/15/2022
	<div>Operator</div>	<div>Project path</div> E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
		<div>Location</div>		
	<div>Designed By</div>	<div>Description 1st</div>		
	<div>Checked By</div>	<div>Description 2nd</div>	<div>Language</div> en-US	
	<div>Approved By</div>	<div>1st View</div>	<div>Version</div>	<div>Sheet</div> 8 - 2

Network 1: (1.1 / 2.1)

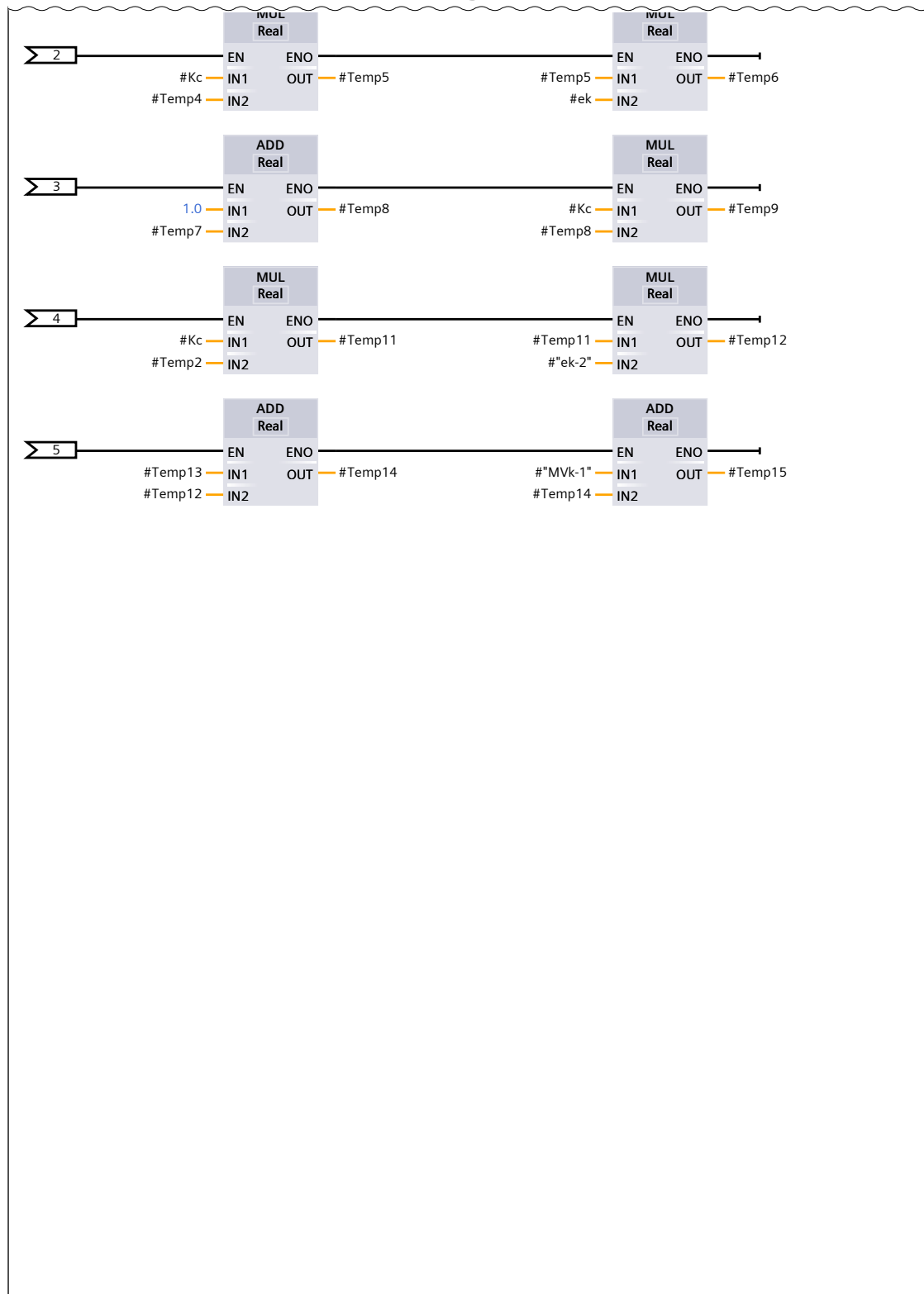


2.1 (Page8 - 4)

Owner	Project name Level_V2	Date 12/15/2022
Operator	Project path E:\Đại học\Năm 3\HK\Thực tập ĐKTĐ\On thi\Level_V2	
Designed By	Location	
Checked By	Description 1st	Description 2nd
Approved By	1st View	Language en-US
	Version	Sheet 8 - 3

Network 1: (2.1 / 2.1)

1.1 (Page8 - 3)



Owner	Projectname Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
	Description 1st		
Designed By	Description 2nd		Language en-US
Checked By	1st View		Version
Approved By			Sheet 8 - 4

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / Program blocks

Data_block_1 [DB1]

Data_block_1 Properties

General

Name	Data_block_1	Number	1
Type	DB	Language	DB
Numbering	Automatic		

Information

Title		Author	
Comment		Family	
Version	0.1	User-defined ID	

▼			
Name	Static	Data type	
Offset		Start value	
Retain		Accessible from HMI/OPC UA/Web API	
Writable from HMI/OPC UA/Web API		Visible in HMI engineering	
Setpoint		Supervision	
Comment			
Name	Kc	Data type	Real
Offset	0.0	Start value	0.0
Retain	True	Accessible from HMI/OPC UA/Web API	True
Writable from HMI/OPC UA/Web API	False	Visible in HMI engineering	False
Setpoint	False	Supervision	
Comment			
Name	tau_i	Data type	Real
Offset	4.0	Start value	0.0
Retain	True	Accessible from HMI/OPC UA/Web API	True
Writable from HMI/OPC UA/Web API	False	Visible in HMI engineering	False
Setpoint	False	Supervision	
Comment			
Name	tau_d	Data type	Real
Offset	8.0	Start value	0.0
Retain	True	Accessible from HMI/OPC UA/Web API	True

Owner	Project name	Level_V2		Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2			
	Location				
Designed By	Description 1st				
Checked By	Description 2nd	Language		en-US	
Approved By	1st View	Version		Sheet 9 - 1	

	1	2	3	4	
A	Writable from HMI/OPC UA/Web API	False	Visible in HMI engineering	False	
	Setpoint	False	Supervision		
	Comment				
	Name	delta_t	Data type	Real	
	Offset	12.0	Start value	0.0	
	Retain	True	Accessible from HMI/OPC UA/Web API	True	
	B	Writable from HMI/OPC UA/Web API	False	Visible in HMI engineering	False
		Setpoint	False	Supervision	
		Comment			
		Name	ek	Data type	Real
		Offset	16.0	Start value	0.0
		Retain	True	Accessible from HMI/OPC UA/Web API	True
C		Writable from HMI/OPC UA/Web API	False	Visible in HMI engineering	False
		Setpoint	False	Supervision	
		Comment			
		Name	ek-1	Data type	Real
		Offset	20.0	Start value	0.0
		Retain	True	Accessible from HMI/OPC UA/Web API	True
	D	Writable from HMI/OPC UA/Web API	False	Visible in HMI engineering	False
		Setpoint	False	Supervision	
		Comment			
		Name	ek-2	Data type	Real
		Offset	24.0	Start value	0.0
		Retain	True	Accessible from HMI/OPC UA/Web API	True
E		Writable from HMI/OPC UA/Web API	False	Visible in HMI engineering	False
		Setpoint	False	Supervision	
		Comment			
		Name	MVk-1	Data type	Real
		Offset	28.0	Start value	0.0
		Retain	True	Accessible from HMI/OPC UA/Web API	True
	F	Writable from HMI/OPC UA/Web API	False	Visible in HMI engineering	False
		Setpoint	False	Supervision	
		Owner		Project name	Level_V2
		Operator		Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2
	Designed By		Description 1st		
	Checked By		Description 2nd	Language	en-US
Approved By		1st View	Version	Sheet 9 - 2	

	1	2	3	4
A				
	Comment			
	Name	MVk	Data type	Real
	Offset	32.0	Start value	0.0
	Retain	True	Accessible from HMI/OPC UA/Web API	True
	Writable from HMI/OPC UA/Web API	False	Visible in HMI engineering	False
	Setpoint	False	Supervision	
B	Comment			
C				
D				
E				
F	Owner	Project name Level_V2		Date 12/15/2022
	Operator	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
		Location		
	Designed By	Description 1st		
	Checked By	Description 2nd	Language en-US	
	Approved By	1st View	Version	Sheet 9 - 3

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / Program blocks

CYC_INT5 [OB35]

CYC_INT5 Properties

General

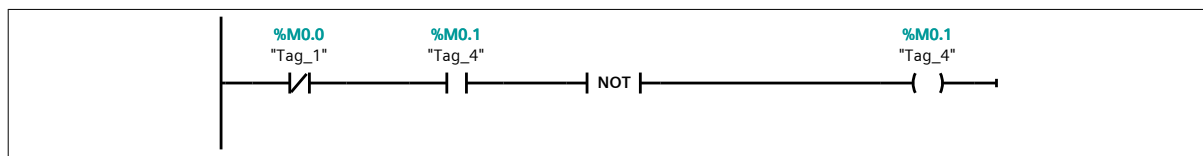
Name	CYC_INT5	Number	35
Type	OB	Language	LAD
Numbering	Manual		

Information

Title	"Cyclic Interrupt"	Author	
Comment		Family	
Version	0.1	User-defined ID	

Name	Data type	Offset	Default value	Comment
▼ Temp				
OB35_EV_CLASS	Byte	0.0		Bits 0-3 = 1 (Coming event), Bits 4-7 = 1 (Event class 1)
OB35_STRT_INF	Byte	1.0		16#36 (OB 35 has started)
OB35_PRIORITY	Byte	2.0		Priority of OB Execution
OB35_OB_NUMBR	Byte	3.0		35 (Organization block 35, OB35)
OB35_RESERVED_1	Byte	4.0		Reserved for system
OB35_RESERVED_2	Byte	5.0		Reserved for system
OB35_PHASE_OFF-SET	Word	6.0		Phase offset (msec)
OB35_RESERVED_3	Int	8.0		Reserved for system
OB35_EXC_FREQ	Int	10.0		Frequency of execution (msec)
OB35_DATE_TIME	Date_And_Time	12.0		Date and time OB35 started
Constant				

Network 1:



Owner	Project name	Level_V2	Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
	Location			
Designed By	Description 1st			
Checked By	Description 2nd	Language	en-US	
Approved By	1st View	Version	Sheet 10 - 1	

1

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3

4

A

Level_V2 / PLC_1 [CPU 315-2 PN/DP]

Technology objects

This folder is empty.

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E

F

Owner	Projectname Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
	Description 1st		
Designed By	Description 2nd		Language en-US
Checked By	1st View		Version
Approved By			Sheet 11 - 1

Level_V2 / PLC_1 [CPU 315-2 PN/DP]
















PLC tags

PLC tags						
Icon	Name	Data type	Address	Visible in HMI engineering	Accessible from HMI/OPC UA/Web API	Comment
	Auto	Bool	%M3.1	True	True	
	auto(1)	Bool	%M66.0	True	True	
	CV	Real	%MD3	True	True	
	Lamp	Bool	%Q0.0	True	True	
	MV	Real	%MD7	True	True	
	Pump_on	Bool	%M0.5	True	True	
	SP	Real	%MD11	True	True	
	Switch	Bool	%M3.0	True	True	
	Tag_1	Bool	%M0.0	True	True	
	Tag_2	Int	%IW272	True	True	
	Tag_3	Int	%QW290	True	True	
	Tag_4	Bool	%M0.1	True	True	
	Tag_5	Bool	%M0.2	True	True	
	V1	Bool	%Q0.2	True	True	
	V3	Bool	%Q0.1	True	True	

Owner	Project name Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
Designed By	Description 1st		
Checked By	Description 2nd	Language en-US	
Approved By	1st View	Version	Sheet 12 - 1

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / PLC tags

Default tag table [15]

PLC tags						
Icon	Name	Data type	Address	Visible in HMI engineering	Accessible from HMI/OPC UA/Web API	Comment
	Auto	Bool	%M3.1	True	True	
	auto(1)	Bool	%M66.0	True	True	
	CV	Real	%MD3	True	True	
	Lamp	Bool	%Q0.0	True	True	
	MV	Real	%MD7	True	True	
	Pump_on	Bool	%M0.5	True	True	
	SP	Real	%MD11	True	True	
	Switch	Bool	%M3.0	True	True	
	Tag_1	Bool	%M0.0	True	True	
	Tag_2	Int	%IW272	True	True	
	Tag_3	Int	%QW290	True	True	
	Tag_4	Bool	%M0.1	True	True	
	Tag_5	Bool	%M0.2	True	True	
	V1	Bool	%Q0.2	True	True	
	V3	Bool	%Q0.1	True	True	

Owner	Project name Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
Designed By	Description 1st		
Checked By	Description 2nd	Language en-US	
Approved By	1st View	Version	Sheet 13 - 1

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4

A

Level_V2 / PLC_1 [CPU 315-2 PN/DP]

PLC data types

This folder is empty.

B

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F

Owner	Projectname Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
	Description 1st		
Designed By	Description 2nd		Language en-US
Checked By	1st View		Version
Approved By	Sheet 14 - 1		

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A

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / Watch and force tables

Force table

Name	Address	Display format	Force value	Comment
------	---------	----------------	-------------	---------

B

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E

F

Owner	Projectname	Level_V2	Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
	Location			
Designed By	Description 1st			
Checked By	Description 2nd	Language	en-US	
Approved By	1st View	Version	Sheet 15 - 1	

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / Watch and force tables

Watch table_1

Name	Address	Display format	Modify value	Comment
"CV"	%MD3	Floating-point number		
"MV"	%MD7	Floating-point number	20.0	
"SP"	%MD11	Floating-point number	40.0	
"Data_block_1".del-ta_t	%DB1.DBD12	Floating-point number	0.5	
"Data_block_1".tau_i	%DB1.DBD4	Floating-point number	0.03	
"Data_block_1".tau_d	%DB1.DBD8	Floating-point number	0.2	
"Switch"	%M3.0	Bool	FALSE	
"Data_block_1".Kc	%DB1.DBD0	Floating-point number	1.0	

Owner	Project name Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
Designed By	Description 1st		
Checked By	Description 2nd	Language en-US	
Approved By	1st View	Version	Sheet 16 - 1

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A

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / PLC supervisions & alarms

PLC alarms

PLC alarms

No entries

B

C

D

E

F

Owner

Projectname Level_V2

Date 12/15/2022

Operator

Project path

E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2

Location

Designed By

Description 1st

Checked By

Description 2nd

Language en-US

Approved By

1st View

Version

Sheet 17 - 1

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A

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / PLC supervisions & alarms

User diagnostics alarms

User diagnostics alarms

No entries

B

C

D

E

F

Owner

Projectname Level_V2

Date 12/15/2022

Operator

Project path

E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2

Location

Designed By

Description 1st

Checked By

Description 2nd

Language en-US

Approved By

1st View

Version

Sheet 18 - 1

1

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4

A

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / PLC supervisions & alarms

System alarms

System alarms

No entries

B

C

D

E

F

Owner	Projectname Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
	Location		
Operator	Description 1st		
	Description 2nd		Language en-US
	1st View	Version	Sheet 19 - 1
Designed By			
Checked By			
Approved By			

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A

Level_V2 / PLC_1 [CPU 315-2 PN/DP]

PLC alarm text lists

This folder is empty.

B

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Owner	Projectname Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
	Description 1st		
Designed By	Description 2nd		Language en-US
Checked By	1st View		Version
Approved By	Sheet 20 - 1		

1

2

3

4

A

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / Local modules

PS 307 5A_1

This folder is empty.

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Owner	Projectname Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
	Description 1st		
Designed By	Description 2nd		Language en-US
Checked By	1st View		Version
Approved By	Sheet 21 - 1		

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / Local modules

PLC_1 [CPU 315-2 PN/DP]

PLC_1

General

Name	PLC_1	Author	Admin
Comment		Rack	0
Slot	2		

General\Catalog information

Short designation	CPU 315-2 PN/DP	Description	Work memory 384KB; 0.05ms/1000 instructions; PROFINET interface; S7 communication (loadable FBs/FCs); PROFINET IO controller; supports RT/IRT; 2 ports; PROFINET CBA; PROFINET CBA Proxy; TCP/IP transport protocol; combined MPI/DP interface (MPI or DP master or DP slave); multi-tier configuration up to 32 modules; constant bus cycle time; routing; firmware V3.2
Article number	6ES7 315-2EH14-0AB0	Firmware version	V3.2

General\Identification & Maintenance

Plant designation		Location identifier	
-------------------	--	---------------------	--

MPI/DP interface\General

Name	MPI/DP interface_1	Comment	
MPI/DP interface\MPI address\Interface networked with			
Subnet:	Not networked		

MPI/DP interface\MPI address\Parameters

Interface type:	Mpi	Address:	2
Highest address:		Transmission speed:	

MPI/DP interface\Time-of-day synchronization\SIMATIC mode

Type of synchronization	None	Time interval	None
-------------------------	------	---------------	------

MPI/DP interface\Diagnostics addresses\Diagnostics addresses

Start address	2047		
---------------	------	--	--

PROFINET interface [X2]\General

Name	PROFINET interface_1	Comment	
PROFINET interface [X2]\Ethernet addresses\Interface networked with			
Subnet:	Not connected		


PROFINET interface [X2]\Ethernet addresses\IP protocol

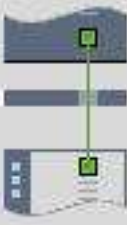
IP configuration	Set IP address in the project	IP address:	192.168.0.1
Subnet mask:	255.255.255.0	Use router	False

PROFINET interface [X2]\Ethernet addresses\PROFINET

PROFINET device name is set directly at the device	False	Generate PROFINET device name automatically	True
PROFINET device name:	plc_1	Converted name:	plcxb1d0ed
Device number:	0		

Owner	Project name	Level_V2	Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
	Location			
Designed By	Description 1st			
Checked By	Description 2nd	Language	en-US	
Approved By	1st View	Version	Sheet 22 - 1	

	1	2	3	4
A	PROFINET interface [X2]\Time-of-day synchronization\NTP mode			
	Enable time synchronization via NTP server	False		IP addresses
	Server 1	0.0.0.0	Server 2	0.0.0.0
	Server 3	0.0.0.0	Server 4	0.0.0.0
B	Update interval	10s		
	PROFINET interface [X2]\Operating mode			
	IO controller	True	IO system	
	Device number	0	IO device	False
	PROFINET interface [X2]\Advanced options\Interface options			
	Call the user program if communication errors occur	False	Support device replacement without exchangeable medium	True
	Use IEC V2.2 LLDP mode	True	Keep-Alive connection monitoring:	0s
	PROFINET interface [X2]\Advanced options\Real time settings\IO communication			
	Send clock:	1.000ms		
	PROFINET interface [X2]\Advanced options\Real time settings\Synchronization			
C	RT class:	RT,IRT		
	PROFINET interface [X2]\Advanced options\Real time settings\Real time options			
	Calculated bandwidth for cyclic IO data:	0.000ms	Calculated bandwidth for cyclic IO data:	0.000%
	PROFINET interface [X2]\Advanced options\Port [X2 P1]\General			
	Name	Port_1	Comment	
	PROFINET interface [X2]\Advanced options\Port [X2 P1]\Port interconnection\Local port:			
	Local port:	PLC_1\PROFINET interface_1 [X2]\Port_1 [X2 P1 R]	Medium:	Copper
	Cable name:	---		
				
	E	PROFINET interface [X2]\Advanced options\Port [X2 P1]\Port interconnection\Partner port:		
		Monitoring of partner port is not possible	Partner port:	Any partner
PROFINET interface [X2]\Advanced options\Port [X2 P1]\Port options\Activate				
Activate this port for use		True		
PROFINET interface [X2]\Advanced options\Port [X2 P1]\Port options\Connection				
Transmission rate / duplex:		Automatic	Monitor	False
Enable autonegotiation		True		
PROFINET interface [X2]\Advanced options\Port [X2 P1]\Port options\Boundaries				
End of detection of accessible devices		False	End of topology discovery	False
F		Owner	Project name Level_V2	
	Operator	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
		Location		
	Designed By	Description 1st		
	Checked By	Description 2nd	Language en-US	
	Approved By	1st View	Version	Sheet 22 - 2

1		2		3		4		
A	End of the sync domain		False					
	PROFINET interface		[X2]\Advanced options\Port [X2 P1]\Diagnostics addresses\Diagnostics addresses					
	Start address		2045					
	PROFINET interface		[X2]\Advanced options\Port [X2 P2]\General					
	Name		Port_2		Comment			
	PROFINET interface		[X2]\Advanced options\Port [X2 P2]\Port interconnection\Local port:					
	Local port:		PLC_1\PROFINET interface_1 [X2]\Port_2 [X2 P2 R]		Medium:		Copper	
	Cable name:		---					
								
C	PROFINET interface		[X2]\Advanced options\Port [X2 P2]\Port interconnection\Partner port:					
			Monitoring of partner port is not possible		Partner port:		Any partner	
	PROFINET interface		[X2]\Advanced options\Port [X2 P2]\Port options\Activate					
	Activate this port for use		True					
	PROFINET interface		[X2]\Advanced options\Port [X2 P2]\Port options\Connection					
	Transmission rate / duplex:		Automatic		Monitor		False	
	Enable autonegotiation		True					
D	PROFINET interface		[X2]\Advanced options\Port [X2 P2]\Port options\Boundaries					
	End of detection of accessible devices		False		End of topology discovery		False	
	End of the sync domain		False					
	PROFINET interface		[X2]\Advanced options\Port [X2 P2]\Diagnostics addresses\Diagnostics addresses					
	Start address		2044					
	PROFINET interface		[X2]\Diagnostics addresses\Diagnostics addresses					
	Start address		2046					
	Startup							
	Startup if preset configuration does not match actual configuration		True		Startup after POWER ON		Warm restart	
	Startup\Monitoring time for							
E	Ready message from modules		650x 100 ms		Parameter transfer to modules		100x 100 ms	
	Cycle							
	Cycle monitoring time		500ms		Cycle load due to communication		20%	
	Size of the process image input:		128		Size of the process image output:		128	
	OB85 call if I/O access error occurs		No OB85 call					
F	Owner		Project name Level_V2				Date 12/15/2022	
	Operator		Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2					
			Location					
	Designed By		Description 1st					
	Checked By		Description 2nd			Language en-US		
	Approved By		1st View			Version	Sheet 22 - 3	

	1	2	3	4		
A	Cycle\Prioritized OCM communication					
	Prioritized OCM communication	False				
	Clock memory					
	Clock memory	False	Memory byte	0		
	Interrupts\Time-of-day interrupts\					
	OB number	Priority	Active	Execution	Start time	
	OB 10	2	False	None	1994-01-01 00:00:00.000	
B	Interrupts\Time-delay interrupts\					
	OB number	Priority	Process image partition(s)			
	OB 20	3	None			
	OB 21	4	None			
	Interrupts\Cyclic interrupts\					
	OB number	Priority	Execution	Phase offset	Unit	
	OB 32	9	1000	0	ms	
	OB 33	10	500	0	ms	
	OB 34	11	200	0	ms	
	OB 35	12	250	0	ms	
	Interrupts\Hardware interrupts\					
	OB number	Priority	Process image partition(s)			
	OB 40	16	None			
C	Interrupts\Interrupts for DPV1\					
	OB number	Priority				
	OB 55	2				
	OB 56	2				
	OB 57	2				
	Interrupts\Isochronous mode interrupts					
	OB number	Priority	Distributed I/O	Process image partition(s)	Delay time (ms)	Automatic setting
	OB 61	25	0		0.000	True
D	Interrupts\Isochronous mode interrupts\OB 61					
	Application cycle:	0ms	Delay time:	0.000ms		
	Automatic setting	True	Distributed I/O:	0		
	Interrupts\Isochronous mode interrupts\OB 61\Process image partition					
	PIP:					
	Interrupts\Asynchronous error interrupts\					
	OB number	Priority				
	OB 82	26				
	OB 83	26				
	OB 85	26				
	OB 86	26				
	OB 87	26				
E	Diagnostics system					
	Report cause of STOP	True	Number of alarms in the diagnostics buffer	10		
	System diagnostics\General					
	Activate system diagnostics for this device	False				
F	Owner	Project name Level_V2		Date 12/15/2022		
	Operator	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2				
		Location				
	Designed By	Description 1st				
	Checked By	Description 2nd	Language en-US			
	Approved By	1st View	Version	Sheet 22 - 4		

	1	2	3	4		
A	Time of day					
	Correction factor	0ms				
B	Time of day\Synchronization on PLC					
	Type of synchroni- zation	None	Time interval	None		
	Time of day\Synchronization on MPI					
	Type of synchroni- zation	None	Time interval	None		
	Web server\General					
	Activate web server on this module	False	Permit access only with HTTPS	False		
	Web server\Automatic update					
	Enable automatic update	False	Update interval	0s		
	Web server\Languages					
	Active	Web server language		Assign project language		
False	German		None			
False	English		None			
False	French		None			
False	Spanish		None			
False	Italian		None			
False	Japanese		None			
False	Chinese (simplified)		None			
C	Web server\User management					
	User name		User rights			
	Everybody					
	Web server\User-defined web pages					
	Application name	HTML source path	Default HTML page	Files with dy- namic content	Web DB number	Fragment DB number
			index.htm	.htm;.html	333	334
D	Web server\Text_Display_classes_of_messages					
	Display class			Active		
	0				True	
	1				True	
	2				True	
	3				True	
	4				True	
	5				True	
	6				True	
	7				True	
	8				True	
	9				True	
	10				True	
	11				True	
	12				True	
	13				True	
	14				True	
	15				True	
	16				True	
	E	Owner		Project name		Date
		Level_V2		12/15/2022		
Operator		Project path				
		E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2				
		Location				
F	Designed By		Description 1st			
	Checked By		Description 2nd		Language en-US	
	Approved By		1st View		Version	
				Sheet 22 - 5		

	1	2	3	4
A	Retentive memory			
	Number of memory bytes starting at MB 0	0	Number of S7 timers starting at T 0	0
	Number of S7 counters starting at C 0	0		
	Protection			
	Password		Confirm password	
	Protection\			
	Level of protection	No protection		
	Protection\Can be canceled with password			
	Can be canceled with password	False		
	B	Connection resources		
PG communication:		1	OP communication:	1
S7 basic communication:		0	S7 communication:	0
Maximum number of S7 connection resources:		16		
Overview of addresses\Overview of addresses\Overview of addresses				
Inputs		True	Outputs	True
Address gaps		False	Slot	True
C				
D				
E				
F	Owner	Projectname Level_V2		Date 12/15/2022
	Operator	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
		Location		
	Designed By	Description 1st		
	Checked By	Description 2nd	Language en-US	
	Approved By	1st View	Version	Sheet 22 - 6

1		2		3		4	
A	Type	I*	Addr. from	2047	Addr. to	2047	
	Module	MPI/DP interface_1	PIP	---	Device name	PLC_1 [CPU 315-2 PN/DP]	
	Device number	-	Size	0 Bits	Master / IO system	-	
B	Rack	0	Slot	2 X1			
	Type	I*	Addr. from	2046	Addr. to	2046	
	Module	PROFINET interface_1	PIP	---	Device name	PLC_1 [CPU 315-2 PN/DP]	
B	Device number	-	Size	0 Bits	Master / IO system	-	
	Rack	0	Slot	2 X2			
	Type	I*	Addr. from	2045	Addr. to	2045	
C	Module	Port_1	PIP	---	Device name	PLC_1 [CPU 315-2 PN/DP]	
	Device number	-	Size	0 Bits	Master / IO system	-	
	Rack	0	Slot	2 X2 P1 R			
C	Type	I*	Addr. from	2044	Addr. to	2044	
	Module	Port_2	PIP	---	Device name	PLC_1 [CPU 315-2 PN/DP]	
	Device number	-	Size	0 Bits	Master / IO system	-	
C	Rack	0	Slot	2 X2 P2 R			
	Type	I	Addr. from	272	Addr. to	275	
	Module	AI 2x12BIT_1	PIP	OB1-PI	Device name	PLC_1 [CPU 315-2 PN/DP]	
D	Device number	-	Size	4 Bytes	Master / IO system	-	
	Rack	0	Slot	5			
	Type	O	Addr. from	288	Addr. to	295	
D	Module	AO 4x12BIT_1	PIP	OB1-PI	Device name	PLC_1 [CPU 315-2 PN/DP]	
	Device number	-	Size	8 Bytes	Master / IO system	-	
	Rack	0	Slot	6			
D	Type	I	Addr. from	0	Addr. to	0	
	Module	DI 8/DO 8x24VDC/0.5A_1	PIP	OB1-PI	Device name	PLC_1 [CPU 315-2 PN/DP]	
	Device number	-	Size	1 Bytes	Master / IO system	-	
E	Rack	0	Slot	4			
	Type	O	Addr. from	0	Addr. to	0	
	Module	DI 8/DO 8x24VDC/0.5A_1	PIP	OB1-PI	Device name	PLC_1 [CPU 315-2 PN/DP]	
E	Device number	-	Size	1 Bytes	Master / IO system	-	
	Rack	0	Slot	4			
F	Owner		Project name			Level_V2	
			Project path			Date	
	Operator		E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2				
			Location				
	Designed By		Description 1st				
F	Checked By		Description 2nd			Language	
						en-US	
F	Approved By		1st View			Version	
						Sheet 22 - 7	

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / Local modules

DI 8/DO 8x24VDC/0.5A_1

DI 8/DO 8x24VDC/0.5A_1

General

Name	DI 8/DO 8x24VDC/0.5A_1	Author	daveb
Comment		Rack	0
Slot	4		

General\Catalog information

Short designation	DI 8/DO 8x24VDC/0.5A	Description	Digital input / output module DI8/DO8 x 24DCV/0.5A; grouping 8; input delay appr. 1.2..4.8ms fix; input type 1 (IEC 61131); 4A per group; 20-pin front connector
Article number	6ES7 323-1BH01-0AA0	Firmware version	

I/O addresses\Input addresses

Start address	0.0	End address	0.7
Process image	OB1-PI	Interrupt OB number	40

I/O addresses\Output addresses

Start address	0.0	End address	0.7
Process image	OB1-PI		

Owner	Projectname	Level_V2	Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
	Location			
Designed By	Description 1st			
Checked By	Description 2nd	Language	en-US	
Approved By	1st View	Version	Sheet 23 - 1	

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / Local modules

AI 2x12BIT_1

AI 2x12BIT_1

General

Name	AI 2x12BIT_1	Author	Admin
Comment		Rack	0
Slot	5		

General\Catalog information

Short designation	AI 2x12BIT	Description	Analog input module AI2 x U/I/R/RTD/TC; 14 bits of resolution; accuracy appr. 1%; grouping 2; common mode voltage appr. 2.3VDC; configurable diagnostics; hardware interrupts; 20-pin front connector
Article number	6ES7 331-7KB02-0AB0	Firmware version	

Inputs\General\Diagnostics

Diagnostics interrupt	Deactivated
-----------------------	-------------

Inputs\General\Hardware interrupts

Hardware interrupt when limit violated	Deactivated	RidPrefixHwInterrupt	49152
Event name:	0	Hardware interrupt:	0
Hardware interrupt	Hardware interrupt	HardwareInterruptChannelForModule	32768

HardwareInterruptEventIdNull	0
------------------------------	---

Inputs\Channel 0 - 1\Diagnostics

Group diagnostics	Deactivated	Check for wire break	Deactivated
-------------------	-------------	----------------------	-------------

Inputs\Channel 0 - 1\Measuring

Measurement type	Voltage	Measuring range	+/- 10 V
Position of measuring range selection module	[B]	Interference frequency suppression	50Hz
Integration time	20ms		

Inputs\Channel 0 - 1\Trigger for hardware interrupt\Channel 0

High limit		Low limit	
------------	--	-----------	--

I/O addresses\Input addresses

Start address	272	End address	275
Process image	None	Interrupt OB number	40

Owner	Project name	Level_V2		Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2			
	Location				
Designed By	Description 1st				
Checked By	Description 2nd	Language	en-US		
Approved By	1st View	Version	Sheet 24 - 1		

Level_V2 / PLC_1 [CPU 315-2 PN/DP] / Local modules

AO 4x12BIT_1

AO 4x12BIT_1

General

Name	AO 4x12BIT_1	Author	Admin
Comment		Rack	0
Slot	6		

General\Catalog information

Short designation	AO 4x12BIT	Description	Analog output module AO4 x U/I 12bits of resolution; accuracy appr. 0.6%; grouping 4; common mode voltage appr. 3VDC; configurable diagnostics; configurable substitute value for output; 20-pin front connector
Article number	6ES7 332-5HD01-0AB0	Firmware version	

Outputs\Enable

Diagnostics interrupt	Deactivated
-----------------------	-------------

Outputs\Channel 0\Diagnostics

Group diagnostics	Deactivated
-------------------	-------------

Outputs\Channel 0\Output

Output type	Current	Output range	4 to 20 mA
Reaction to CPU STOP	Output has no current or voltage	Substitute value	

Outputs\Channel 1\Diagnostics

Group diagnostics	Deactivated
-------------------	-------------

Outputs\Channel 1\Output

Output type	Current	Output range	4 to 20 mA
Reaction to CPU STOP	Output has no current or voltage	Substitute value	

Outputs\Channel 2\Diagnostics

Group diagnostics	Deactivated
-------------------	-------------

Outputs\Channel 2\Output

Output type	Current	Output range	4 to 20 mA
Reaction to CPU STOP	Output has no current or voltage	Substitute value	

Outputs\Channel 3\Diagnostics

Group diagnostics	Deactivated
-------------------	-------------

Outputs\Channel 3\Output

Output type	Current	Output range	4 to 20 mA
Reaction to CPU STOP	Output has no current or voltage	Substitute value	

I/O addresses\Output addresses

Start address	288	End address	295
Process image	None		

Owner	Project name	Level_V2	Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
	Location			
Designed By	Description 1st			
Checked By	Description 2nd	Language	en-US	
Approved By	1st View	Version	Sheet 25 - 1	

1

2

3

4

A

Level_V2

Ungrouped devices

This folder is empty.

B

C

D

E

F

Owner	Project name Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
	Description 1st		
Designed By	Description 2nd		Language en-US
Checked By	1st View		Version
Approved By	Sheet 26 - 1		

1

2

3

4

A

Level_V2

Security settings

This folder is empty.

B

C

D

E

F

Owner	Project name Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
	Description 1st		
Designed By	Description 2nd		Language en-US
Checked By	1st View		Version
Approved By	Sheet 27 - 1		

1

2

3

4

A

Level_V2 / Cross-device functions / Project traces

Measurements

This folder is empty.

B

C

D

E

F

Owner	Projectname Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
	Description 1st		
Designed By	Description 2nd		Language en-US
Checked By	1st View		Version
Approved By	Sheet 28 - 1		

Level_V2 / Common data

Alarm classes

Alarm classes	
Name	Acknowledgement
Display name	A
Acknowledgment	True
Priority	0
Name	No Acknowledgement
Display name	NA
Acknowledgment	False
Priority	0

Owner	Project name	Level_V2	Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
	Location			
Designed By	Description 1st			
Checked By	Description 2nd	Language	en-US	
Approved By	1st View	Version	Sheet 29 - 1	

1

2

3

4

A

Level_V2 / Common data

Logs

This folder is empty.

B

C

D

E

F

Owner	Projectname Level_V2		Date 12/15/2022
	Project path E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
Operator	Location		
	Description 1st		
Designed By	Description 2nd		Language en-US
Checked By	1st View		Version
Approved By	Sheet 30 - 1		

1

2

3

4

A

Level_V2 / Languages & resources

Project languages

Languages

Reference language

English (United States)

Editing language

English (United States)

B

Other project languages

Empty

C

D

E

F

Owner

Project name Level_V2

Date 12/15/2022

Operator

Project path

E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2

Location

Designed By

Description 1st

Checked By

Description 2nd

Language en-US

Approved By

1st View

Version

Sheet 31 - 1

Level_V2 / Languages & resources / Project texts

Project texts

Project texts	
English (United States)	"Cyclic Interrupt"
Category	Block comment
Reference	Level_V2\PLC_1 [CPU 315-2 PN/DP]\Program blocks\CYC_INT5 [OB35]\Block title
English (United States)	"Main Program Sweep (Cycle)"
Category	Block comment
Reference	Level_V2\PLC_1 [CPU 315-2 PN/DP]\Program blocks\Main [OB1]\Block title
English (United States)	A
Category	Alarm class text
Reference	Level_V2\Acknowledgement\AlarmClassData_IDisplayNaming_DisplayName
English (United States)	A
Category	Alarm class text
Reference	Level_V2\Acknowledgement\ShortName
English (United States)	NA
Category	Alarm class text
Reference	Level_V2\No Acknowledgement\AlarmClassData_IDisplayNaming_DisplayName
English (United States)	NA
Category	Alarm class text
Reference	Level_V2\No Acknowledgement\ShortName

Owner	Project name	Level_V2	Date	12/15/2022
Operator	Project path	E:\Đại học\Năm 3\HKI\Thực tập ĐKTĐ\On thi\Level_V2		
	Location			
Designed By	Description 1st			
Checked By	Description 2nd	Language	en-US	
Approved By	1st View	Version	Sheet 32 - 1	