Instruction		Byte 1								Byte 2								Control Lines												Pseudocode
Operation	Description	Opcode					Operands											Immediate	Signed Ext.	Read RA	Read RB	R Writeback	Mem Read	Mem Write	Stack Ptr	LR Read	LR Write	Jump	ALU	Update Flags	Read Flags	
NOP	No operation																	No	No	No	No	No	No	No	No	No	No	No	No	No	No	
LDI	Load immediate						DR			Imm (8)								Yes	Yes	No	No	Yes	No	No	No	No	No	No	No	No	No	DR <= Imm
CMOV	Conditional Move						DR	P	Z	N	C		SR					No	No	Yes	No	Yes	No	No	No	No	No	No	No	No	Yes	DR <= SR if Flags
CMOV	Conditional Move						DR	P	Z	N	C		Immediate (4)					Yes	Yes	No	No	Yes	No	No	No	No	No	No	No	No	Yes	DR <= Imm if Flags
RET	Return																	No	No	No	No	No	No	No	No	Yes	No	Yes	No	No	No	PC <= LR
JAL	Jump and link									Base R				Offset (5)				Yes	Yes	Yes	No	No	No	No	No	No	Yes	Yes	Yes	No	No	LR <= PC; PC <= PC + Offset
BR	Branch					P	Z	N	C	Base R				Offset (5)				Yes	Yes	Yes	No	No	No	No	No	No	No	Yes	Yes	No	Yes	PC <= PC + Offset if Flags
PUSH	Push to stack						SR											No	No	Yes	No	No	No	Yes	Yes	No	No	No	Yes	No	No	Mem[SP] <= SR; SP <= SP - 1
POP	Pop stack						DR											No	No	No	No	Yes	Yes	No	Yes	No	No	No	Yes	No	No	DR <= Mem[SP]; SP <= SP + 1
STR	Memory store						SR			Base R				Offset (5)				Yes	No	Yes	Yes	No	No	Yes	No	No	No	No	Yes	No	No	Mem[Base R + Offset] <= SR
LDR	Memory load						DR			Base R				Offset (5)				Yes	No	No	Yes	Yes	Yes	No	No	No	No	No	Yes	No	No	DR <= Mem[Base R + Offset]
ADD(C)	Add (with carry?)						DR			SR1			C			SR2		No	No	Yes	Yes	Yes	No	No	No	No	No	No	Yes	Yes	Sometimes	DR <= SR1 + SR2 + (C?)
							DR			Imm (8)								Yes	Yes	No	No	Yes	No	No	No	No	No	No	Yes	Yes	No	DR <= DR + Imm
SUB(C)	Subtract (with carry?)						DR			SR1			C			SR2		No	No	Yes	Yes	Yes	No	No	No	No	No	No	Yes	Yes	Sometimes	DR <= SR1 - SR2 (with C?)
							DR			Imm (8)								Yes	Yes	No	No	Yes	No	No	No	No	No	No	Yes	Yes	No	DR <= DR - Imm
AND	Bitwise (N)AND						DR			SR1			N			SR2		No	No	Yes	Yes	Yes	No	No	No	No	No	No	Yes	Yes	No	DR <= (Not?)(SR1 & SR2)
							DR			Imm (8)								Yes	No	No	No	Yes	No	No	No	No	No	No	Yes	Yes	No	DR <= DR & Imm
ORR	Bitwise (N)OR						DR			SR1			N			SR2		No	No	Yes	Yes	Yes	No	No	No	No	No	No	Yes	Yes	No	DR <= (Not?)(SR1 | SR2)
							DR			Imm (8)								Yes	No	No	No	Yes	No	No	No	No	No	No	Yes	Yes	No	DR <= DR | Imm
XOR	Bitwise X(N)OR						DR			SR1			N			SR2		No	No	Yes	Yes	Yes	No	No	No	No	No	No	Yes	Yes	No	DR <= (Not?)(SR1 ^ SR2)
							DR			Imm (8)								Yes	No	No	No	Yes	No	No	No	No	No	No	Yes	Yes	No	DR <= DR ^ Imm
SLL	Logical shift left						DR			SR				Immediate (4)				Yes	No	Yes	No	Yes	No	No	No	No	No	No	Yes	Yes	No	DR <= SR << Imm
SLR	Logical shift right						DR			SR				Immediate (4)				Yes	No	Yes	No	Yes	No	No	No	No	No	No	Yes	Yes	No	DR <= SR >> Imm