NETWORK PACKET TRANSMISSION MONITORING SYSTEM

DIGITAL LOGIC SECR1013

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SECTION 03

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DEDICATION AND ACKNOWLEDGEMENT

This work is dedicated to our lecturer, Dr Farkhana Binti Muchtar whose unwavering support, encouragement, invaluable guidance throughout Digital Logic. Her expertise, insightful feedback, and patience have been invaluable in shaping this project and helping us achieve its objectives. Her teaching not only allowed us to gain knowledge about digital components and concepts but also helped us grow in academically and personally.

We also wanted to extend our special thanks to Dr Mohd Fo'ad Bin Rohani for giving us a brief about this project. His detailed briefing and expert insights at the initial stages of this project laid a strong foundation for its success. His willingness to share his knowledge and provide direction has greatly contributed to the progress and quality of this project.

We are also deeply thankful to our dedicated group members. The teamwork has been the foundation of our success. Each member brought their own unique talents and insights, fostering a collaborative and creative environment.

Lastly, to everyone who contributed, whether directly or indirectly, to the success of this project, we are forever grateful. This project would not have been possible without your guidance, support, and encouragement.

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1.0 BACKGROUND

Our project focuses on developing a network packet transmission monitoring system that leverages the principles of combinational and sequential circuits. This system enables users to select the source and destination of data and route the data efficiently while adhering to predefined rules. Additionally, we have incorporated extra features to enhance functionality and user experience.

Combinational Circuit Components:

- Basic Gates (AND, OR, NOT)
- Input Switches
- 1-bit Output Display
- 4-bit Hex Input
- 4-bit Comparator
- 8x1 Multiplexer
- 1x8 Demultiplexer

Sequential Circuit Components:

- T Flip-Flop
- Clock Generator

Extra Features:

- Fun Concept Display
- Error Detection
- Password system

2.0 PROBLEM STATEMENT

In modern computer networks, efficient and secure packet transmission monitoring is essential to ensure reliable communication. However, many existing monitoring systems lack the ability to dynamically control packet flow based on predefined rules, leading to issues such as inefficient routing, unauthorized data access, and lack of real-time monitoring capabilities.

3.0 SUGGESTED SOLUTION

To address the issue of inefficient routing, we have implemented a 1-of-8 Multiplexer and 1-to-8 Demultiplexer along with 3-bit selector to ensure the data can successfully transmitted to desired destination.

To address the issue of unauthorized data access, we have designed a password protected system ensuring that only authorized personnel can set the maximum number of packets for transmission. Users need to input the correct password to enable the clock and store and transmit the data.

To address the issue of lack of real-time monitoring capabilities, we implemented a comparator and clock enabler in our system, which allow users to control when to transmit the data and monitor the data through screen.

Besides, we also implemented an error detection system in our circuit. This allows users to identify and fix the issues quicker, enhancing the efficiency of troubleshooting the circuit.

Block Diagram

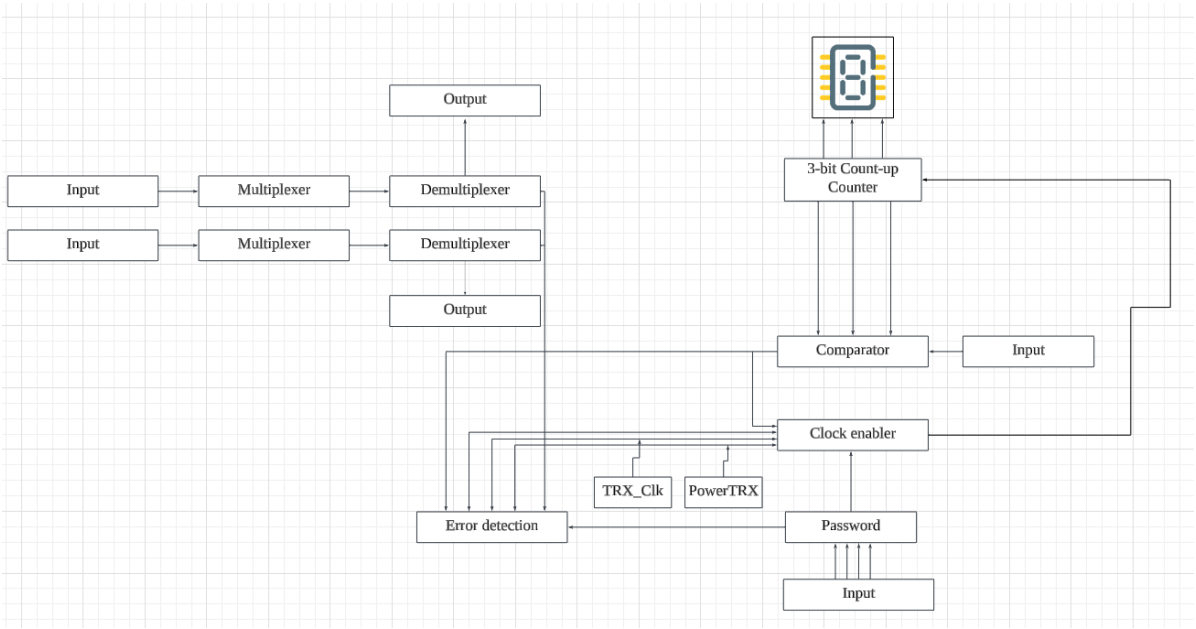

Figure 1 Block Diagram

Explanation

Step 1: Initial Input

-Inputs are entered to the system
-The inputs pass through multiplexer, where specifit input are selected
-The selected inputs are forwarded to the demultiplexer

Step 2: Demultiplexer
-The demultiplexers forward the selected input to their significant output paths
-Some outputs may directly lead to the final output blocks, while others are sent to error detection block for further processing.

Step 3: Counter operation
-The 3-bit count-up counter starts counting according to the clock pulse within the system
-The count output is displayed through 7 segment display
-The counter output is forwarded to the comparator

Step 4: Comparator operation
-The comparator receives inputs from both the counter and external input sources
-It checks for matching conditions between the signals
-The signal is then forwarded to clock enabler and error detection block

Step 5: Error detection
-Signals from demultiplexer, multiplexer, comparator, TRX_Clk and PowerTRX are fed into the error detection block
-The error detection block detects the existing abnormalities and faults from
the signal sources

Step 6: Clock enabler mechanism
-A password input is required to enable clock operations
If the password is correct, the clock enabler activates

Step 7: TRX_Clk and PowerTRX
-The powerTRX controls the turning on and off of the computer
-TRX_Clk controls the enable and disable of the clock

Step 8: Output at 7 segment display

-After the clock and the power are turned on, the output will be displayed through the 7 segment display in the 3-bit count-up counter

4.0 REQUIREMENTS

Input switch

Input switches allow the user to switch on or switch off the input computer and output computer. Besides, the switches are also used to control the status (0 or 1) of PRE_bar and CLR_bar which will be explained further later.

Multiplexer

1-of-8 multiplexers are used to select 1 computer out of 6 computers as the data source.

Demultiplexer

1-to-8 demultiplexers are used to route the data from the input computer to 1 computer out of 6 computers as the output computer.

4-bit input DIP switch

4-bit input DIP switch consists of four individual switches packaged together, with each switch capable of being toggled on or off independently, are used as selector to select the input computer and output computer. Users can set the DIP switches according to Rules 1 to address the input data to the desired output computer accurately.

Clock enabler

Clock enabler is used to control the synchronization of clock pulse between the input and output computers. By toggling the clock enabler, users can enable and disable the clock, ensuring that data transferring occurs precisely as expected.

Comparator

Comparator is used to compare two sets of data values and provide an output indicating whether the input values are equal, greater, or smaller. The comparator helps to verify if the input data matches the expected conditions.

3-bit count-up Counter

3-bit count-up Counter is designed to increase the count value by one with each clock pulse. The 3 output lines allow it to count from 0 to 7 in binary (000 to 111).

Error detector

The error detector, utilizing the 8-bit output LED Array detects error through the status of each single LED. If a particular LED fails to light up, it indicates an error in that part of the system. When a certain light doesn't light up, it indicates that there exists error in that part, such as issue in comparator, issue in password or issue in powerTRX. This visual feedback allows users to quickly identify and troubleshoot system faults for efficient maintenance.

8-bit output LED array

The 8-bit output LED array consists of eight LEDs that visually display the binary output of the system. Each LED represents a single bit, turned on indicates value '1' and turned off indicates value '0.'

Password system

The password system is implemented to ensure security and control access to the system. Users must input a valid hexadecimal code to activate or unlock it. If the input password matches the pre-set value, the system grants access; otherwise, it remains locked.

Input One Hex

The Input One Hex allows user to enter a hexadecimal value as input. It simplifies data entry by converting user-friendly hex inputs into binary data.

PRE_bar

PRE_bar or Preset_bar is used to set the output to high. For example, when PRE_bar switch is set to 0, the seven-segment display will show the highest number of packets stored.

CLR_bar

CLR_bar or Clear_bar is used to clear the output and set it to low (0). For example, when CLR_bar switch is set to 0, the seven-segment display will show 0.

Seven segment display

A seven-segment display is an electronic device that shows numerical digits and some characters. It's made up of seven LED segments that are arranged in a specific pattern.

5.0 SYSTEM IMPLEMENTATION

1. Multiplexer and Demultiplexer

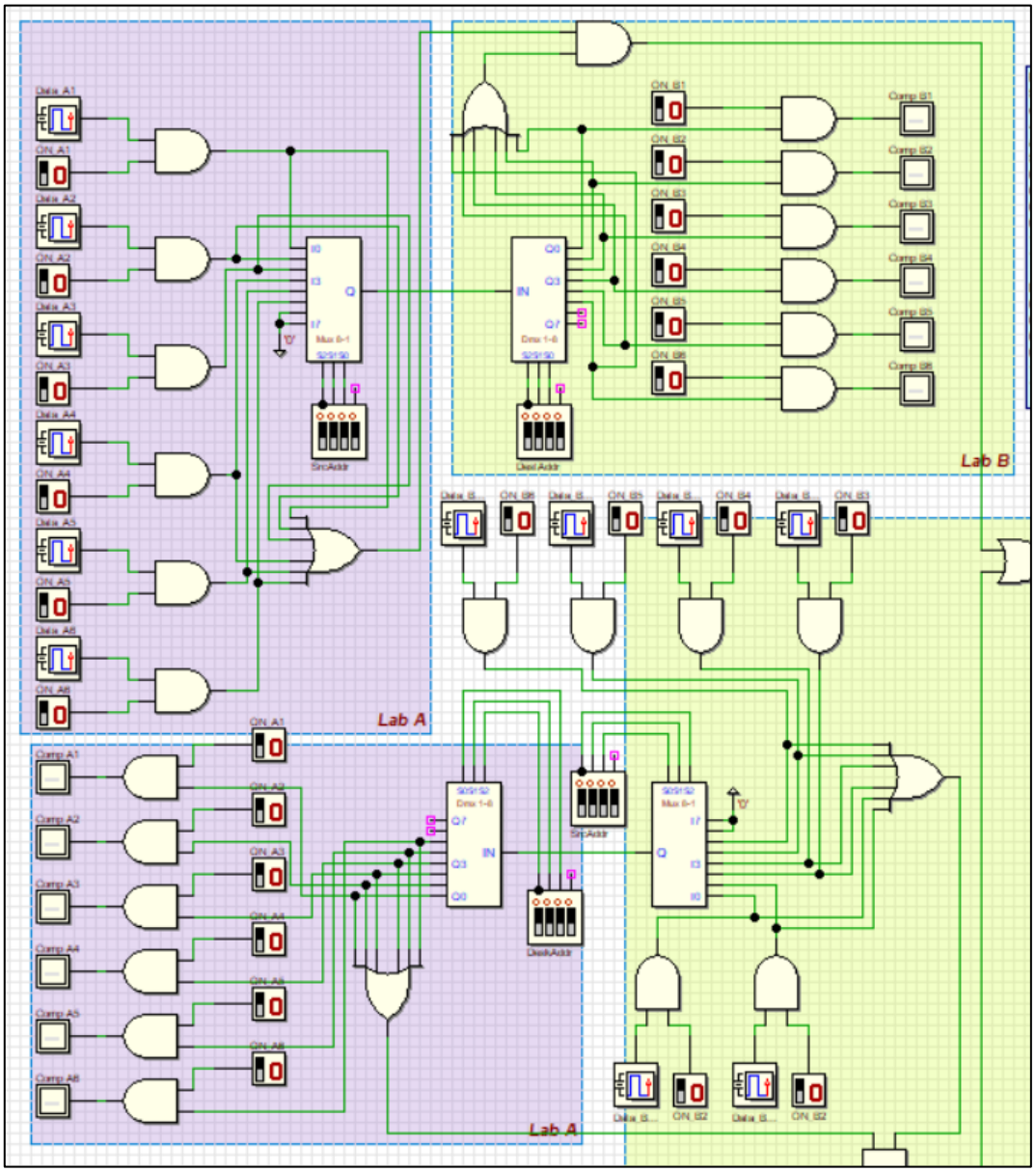

Figure 2 Data Transmit from Lab A to Lab B (vice versa) using MUX & DEMUX

Both Lab A and Lab B consist of 6 computers. MUX and DEMUX play crucial roles in this circuit in transmitting data between devices located in different labs. This circuit has two MUX and two DEMUX which are: Lab A consist of one MUX and one DEMUX and same goes to Lab B, one MUX and one DEMUX. This setup enables data transmitting from Lab A to Lab B and Lab B to Lab A.

2. Input/Output

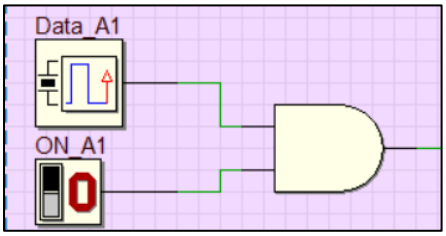

Figure 3 Power On Button and Clock Data Transmission

Data A1 represents the clock signal, which serves as the source data from Computer 1 in Lab A. ON A1 represents the power-on switch for Computer 1 in Lab A. When ON A1 is 1 (HIGH), it means the computer is turned on, and when ON A1 is 0 (LOW), it means the computer is turned down. Then Data A1 and ON A1 are connected to 2-input AND gate. The AND gate is HIGH (1) only if both inputs are 1. This concept is applied same goes for Lab B MUX section.

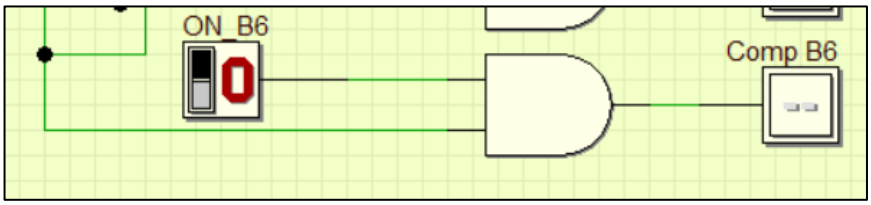

Figure 4 Power On Button and Output Display

ON B6 represents power-on switch for Computer 6 in Lab B. When ON B6 is 1 (HIGH), it means the Computer 6 is turned on, and when ON B6 is 0 (LOW), it means the Computer 6 is turned down. Then ON A6 and the output Q4 from DEMUX are connected to 2-input AND gate. The AND gate is HIGH (1) only if ON B6 is 1 and Q4 is 1. This concept is applied same goes for Lab A DEMUX section.

3. Basic Gates

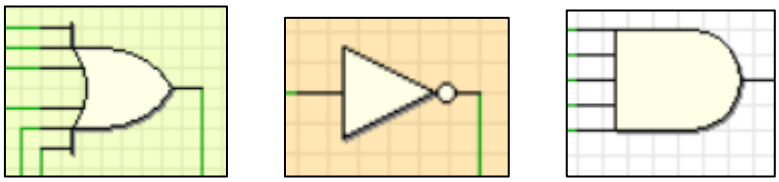

Figure 5 Basic Gates

Basic gates consist of OR, NOT and AND. All these three types of circuit were implemented in this circuit. OR gates; the output will be 1 (HIGH) if and only if one of the input is 1(HIGH). NOT gates; also called an inverter, flips its digital input signal. AND gates; the output will be 1 (HIGH) if and only if all the inputs are 1(HIGH), if one of input is 0 (LOW), the output will be 0 (LOW).

4. 3-bit Synchronous T Flip-Flop Counter

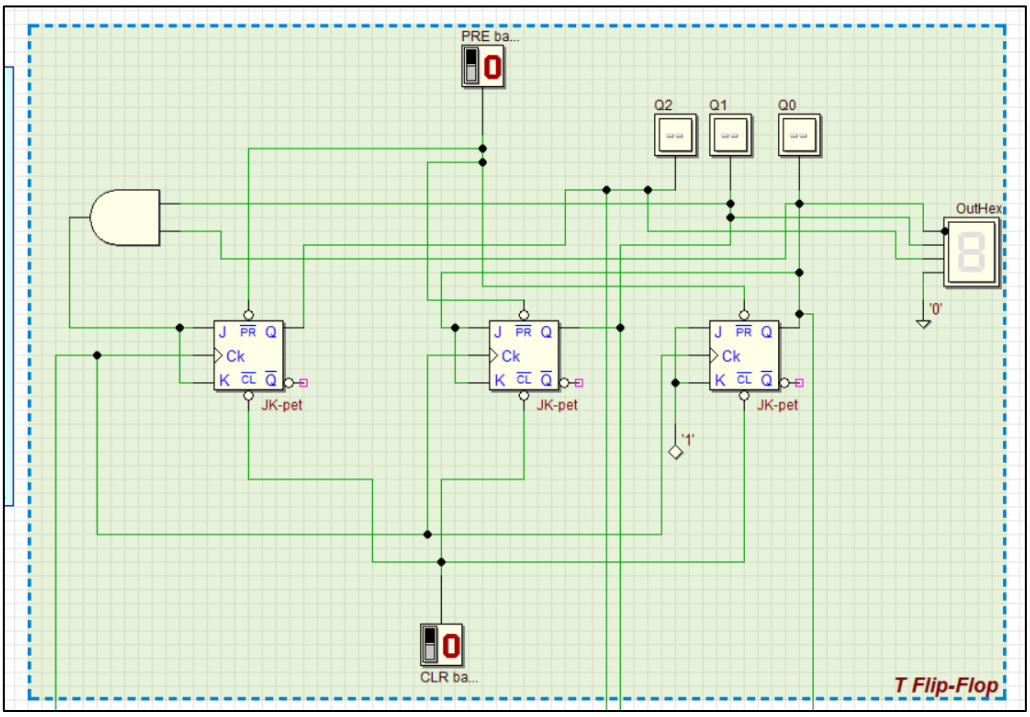

Figure 6 3-bit Synchronous T flip-flop Counter

T Flip-Flop is not provided by deeds simulator. So, we use JK Flip-Flop was used to imitate T Flip-Flop. The input of JK Flip-Flop was set to J=K=1. Therefore, there is only 2 states for the Flip-Flop, which are no change and toggle. All the clock input for the T Flip-Flop comes from a common clock, clock enabler. The Flip-Flop only works if clock input is 1.

5. Comparator

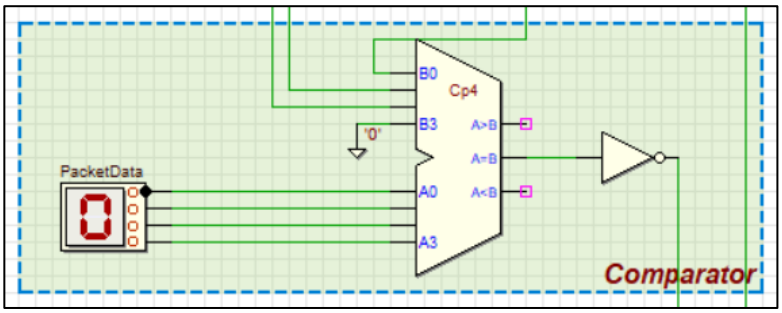

Figure 7 Comparator

4 inputs of comparator (A0-A3) are connected to 4-bit HEX input while 3 inputs comparator (B0-B2) are connected to each output of Flip-Flop.

6. Error Detection

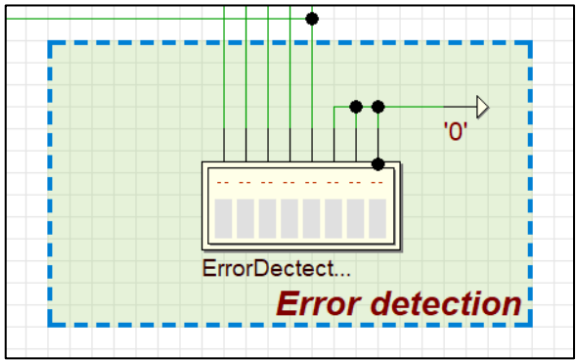

Figure 8 Error Detection

The light in error detection will indicate where the problem occurs:

a. First light doesn't light up: issue in comparator (example code: 01111000)

Suggestion:

- check if the PacketData is set correctly.
- check if the PRE bar and CLR bar are set to 1.

b. Second light doesn't light up: issue in password (example code: 10111000)

Suggestion:

- check if the password is set correctly.

c. Third light doesn't lit: issue in TRX_Clk (example code: 11011000)

Suggestion:

- try enabling the clock using push button.

d. Fourth light doesn't light up: issue in PowerTRX (example code: 11101000)

Suggestion:

- activate the input PowerTRX.

e. Fifth light doesn't light up: issue in source and destination (example code 11110000)

Suggestion:

- make sure the ON_comp is activate correctly for each source and destination.
- make sure the DeskAddr and SrcAddr are setting correctly.
- make sure the clock is enabled and set to enable clock animation.

7. Clock Enabler

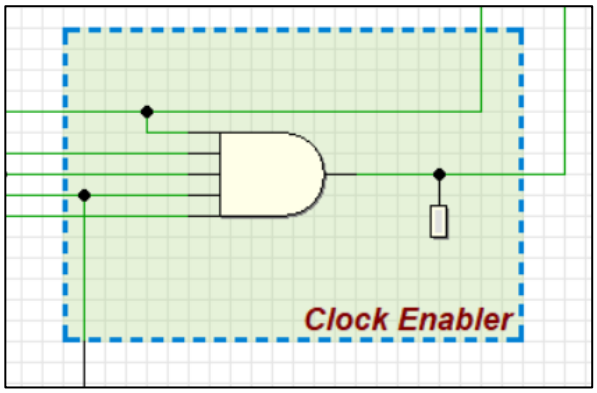

Figure 9 Clock Enabler

We used 5-input AND gate for clock enabler. One of the inputs from OR gates that combines all the clock computers. Another four inputs are from PowerTRX which is to on the computer. If the value is 1 (HIGH), it means the power is on. And if the value is 0 (LOW) it means the power is off. Second, TRX clock. Third, output of password system. Lastly, from comparator in which once it reached the same amount as maximum data packet.

8. Password system

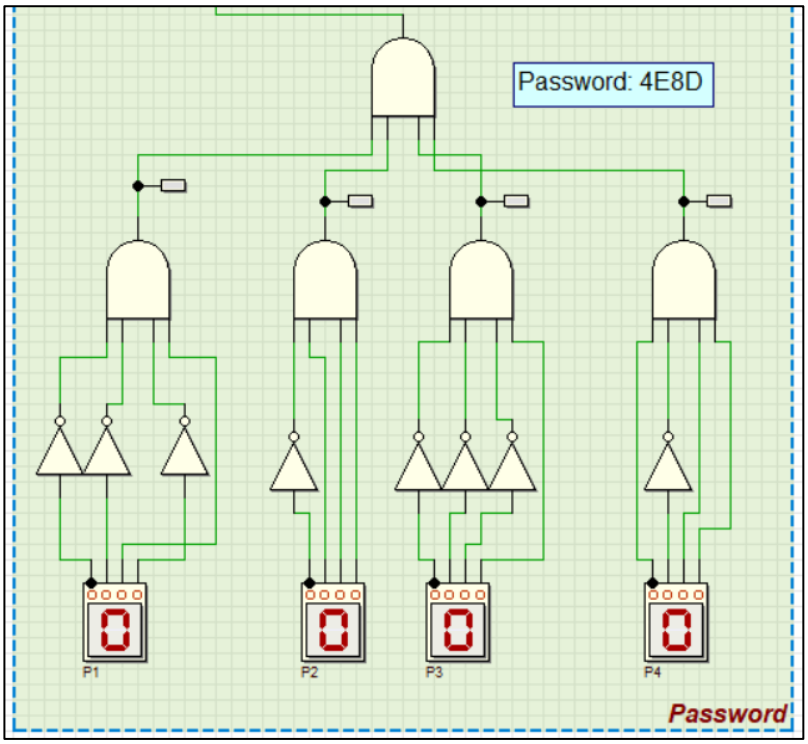

Figure 10 Password System

The password system built using logic gates. The system takes input from four seven-segment displays (P1, P2, P3 and P4), each representing a digit in a hexadecimal password. The password displayed in the circuit is 4E8D, meaning the system is designed to check wheter the entered value match this specific combination. The circuit processes each digit separately using combination of logic gates. The NOT gates are used to invert certain bits, while the AND gates help to verify whether entered value corresponds to the preset password. Each input undergoes logical operations to determine if it is correct. If all four digits match the same as password, the final AND gate combines the results and produces an output signal at error detector, which is 1 (HIGH), indicating a successful password match.

9. Fun Display

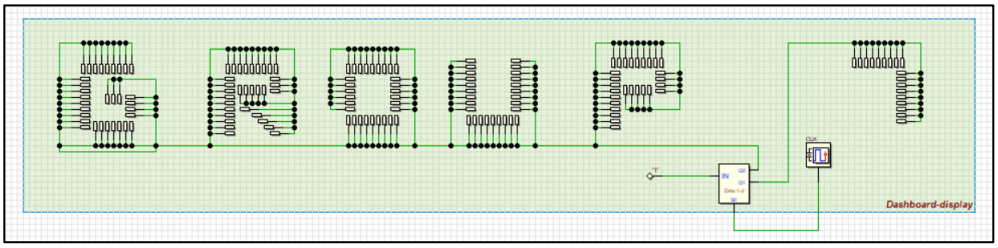

Figure 11 Fun Display

The fun concept display is built using a 1x2 DEMUX, clock generator, switches and the LEDs as the output. This fun concept display with the title "GROUP 7" was built to make the deeds circuit more appealing.

6.0 CONCLUSION

Our project features a simple and user-friendly design, making it accessible for users. The circuit primarily consists of input switches, seven-segment displays, LEDs, an LED array for outputs, a 4-bit comparator, a 3-bit up counter, a multiplexer and demultiplexer, a clock, and basic logic gates.

To enhance security, we integrated a password-protected system connected to the counter, which is built using three T flip-flops. This ensures that incorrect data is not stored when an invalid password is entered. Additionally, the error detection feature enables users to quickly identify and resolve issues, improving system reliability and efficiency.

7.0 REFLECTION

Working on this network packet transmission monitoring system has been a valuable learning experience. Throughout the project, we applied our knowledge of combinational and sequential circuits, reinforcing our understanding of circuit design and optimization. Additional research on DEEDS software was conducted to ensure a simplified yet functional circuit design. This hands-on approach helped us bridge the gap between theoretical concepts and practical implementation.

Challenges and Solutions

One of the key challenges we faced was ensuring accurate packet routing and implementing a secure password system. Initially, integrating the T flip-flop-based counter with the security mechanism was challenging, but through continuous debugging and teamwork, we successfully created a system that prevents unauthorized access. Another challenge was our lack of familiarity with DEEDS software, which led to confusion in selecting components and optimizing the circuit layout. To address this, we plan to further explore and study DEEDS to improve our circuit design skills.

Strengths and Areas for Improvement

Our team's productivity and collaboration were crucial to the success of this project. Shee Tong, the circuit designer, was highly efficient in designing and refining the circuit, while the other team members contributed significantly to the project report and presentation slides. Our ability to work together effectively played a key role in overcoming challenges.

However, there is room for improvement. Currently, our system only supports a maximum of 8 information packets due to the 3-bit flip-flop design. To increase this limit, we can implement additional flip-flops in future iterations.

Future Prospects

This project has deepened our understanding of circuit optimization, data security, and digital design. Moving forward, we aim to develop more advanced circuits with additional features, further enhancing our skills and applying them to real-world applications.

8.0 REFERENCES

Mohd Fo'ad, R. (2024). *Digital Logic Project Manual*. Johor Bahru, Johor: Faculty of Computing, University of Technology Malaysia.

Abd. Bahrim, Y. (2024). *Digital Logic 5th Edition*. Johor Bahru, Johor: Faculty of Computing, University of Technology Malaysia.

9.0 APPENDICES

<table>
<tr><td colspan="2">Name</td><td>Siti Nur Iman Nadhirah Binti Mohd Faizal</td><td>Toh Shee Thong</td><td>Michelle Ho Chia Xin</td><td>Tay Xin Ying</td></tr>
<tr><td rowspan="8">Task</td><td rowspan="4">Designing</td><td colspan="4">Full Circuit Diagram using Deeds Simulator</td></tr>
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Table 1 Task Distribution

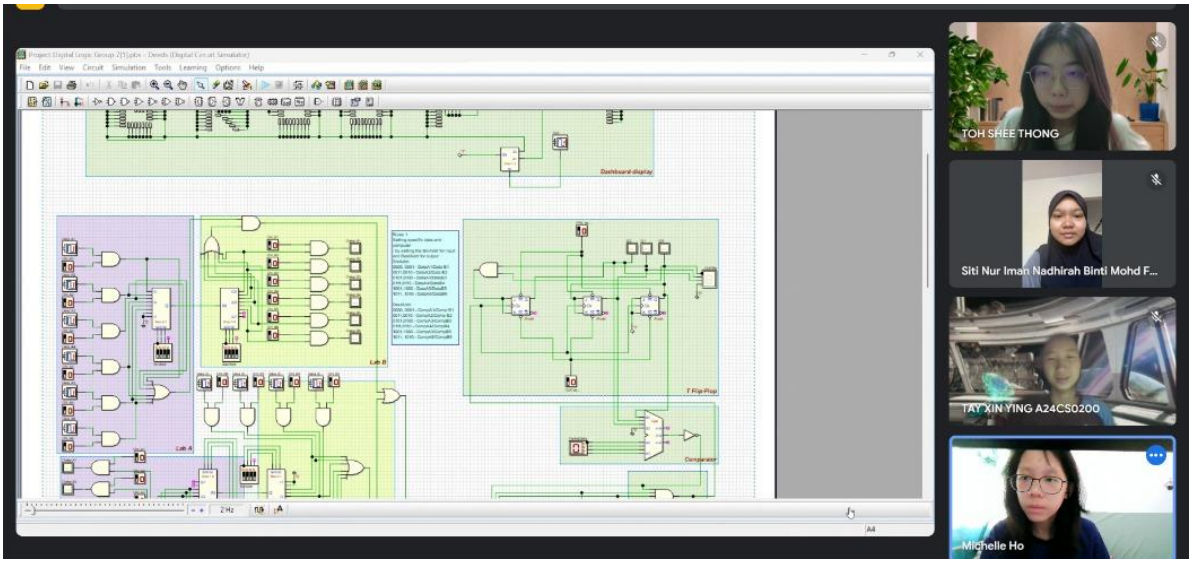

Figure 12 Photo of group discussion

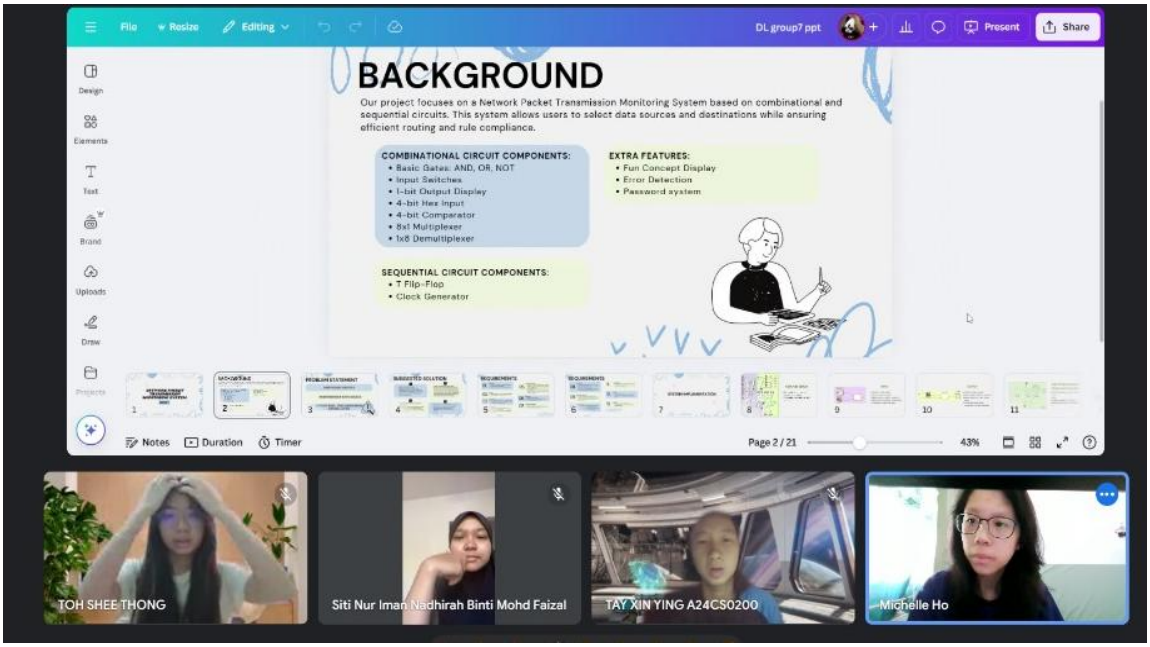

Figure 13 Photo of group discussion