# NETWORK PACKET TRANSMISSION MONITORING SYSTEM

GROUP 7

# BACKGROUND

Our project focuses on a Network Packet Transmission Monitoring System based on combinational and sequential circuits. This system allows users to select data sources and destinations while ensuring efficient routing and rule compliance.

**COMBINATIONAL CIRCUIT COMPONENTS:**

- Basic Gates: AND, OR, NOT
- Input Switches
- 1-bit Output Display
- 4-bit Hex Input
- 4-bit Comparator
- 8x1 Multiplexer
- 1x8 Demultiplexer

**SEQUENTIAL CIRCUIT COMPONENTS:**

- T Flip-Flop
- Clock Generator

**EXTRA FEATURES:**

- Fun Concept Display
- Error Detection
- Password system

# PROBLEM STATEMENT

INEFFICIENT ROUTING

UNAUTHORIZED DATA ACCESS

LACK OF REAL-TIME MONITORING CAPABILLITIES

# SUGGESTED SOLUTION

1

- **Issue: inefficient routing**
- **Solution:** implemented a **1-of-8 Multiplexer and 1-to-8 Demultiplexer along with 3-bit selector** to ensure the data can successfully transmitted to desired destination.

2

- **Issue: unauthorized data access**
- **Solution: password protected system** ensuring that only authorized personnel can set the maximum number of packets for transmission. Users need to **input the correct password to enable the clock and store and transmit the data.**

3

- **Issue: lack of real-time monitoring capabilities**
- **Solution: comparator and clock enabler** which allow users to **control when to transmit the data** and **monitor the data** through screen.

4

- **Extra feature: error detection system**
- Allows users to identify and **fix the issues quicker**, **enhancing the efficiency** of troubleshooting the circuit.

# REQUIREMENTS

01.

**Input switch**

- allow the user to **switch on or switch off the input computer and output computer.**
- control the status (0 or 1) of PRE_bar and CLR_bar

02.

**Multiplexer**

- 1-of-8 multiplexers are used to **select 1 computer out of 6 computers** as the data source.

03.

**Demultiplexer**

- 1-to-8 demultiplexers are used to **route the data from the input computer to 1 computer out of 6 computers** as the output computer.

04.

**Clock Enabler**

- **control the synchronization clock pulse** between the input and output computers.
- By toggling the clock enabler, users can **enable and disable the clock**

05.

**4-bit input DIP switch**

- consists of **four individual switches packaged together**, with each switch capable of being toggled on or off independently
- used as **selector** to **select the input computer and output computer.**
- Users can set the DIP switches according to **Rules 1** to address the input data to the desired output computer accurately.

06.

**Comparator**

- **compare two sets of data**
- provide an output indicating whether the input values are equal, greater, or smaller.

07.

**3-bit count-up Counter**

- designed to increase the count value by one with each clock pulse. The 3 output lines allow it to count from 0 to 7 in binary (000 to 111).

# REQUIREMENTS

08.

**Error detector**

- 8-bit output LED Array that detects error through the status of each single LED.
- When a certain light doesn't light up, it indicates that there exists error in that part
- allows users to **quickly identify** and **troubleshoot** system faults for efficient maintenance.

09.

**8-bit output LED array**

- consists of eight LEDs that display the binary output of the system. Each LED represents a single bit, turned on indicates value '1' and turned off indicates value '0.'

10.

**Password system**

- ensure security and control access to the system.
- Users must input a valid hexadecimal code to unlock it. If the input password matches, the system grants access; otherwise, it remains locked.

11.

**Input One Hex**

- allows user to enter a hexadecimal value as input
- simplifies data entry by converting user-friendly hex inputs into binary data.

12.

**PRE_bar**

- set the output to high
- when PRE_bar is set to 0, the seven-segment display will show the highest number of packets stored.

13.

**CLR_bar**

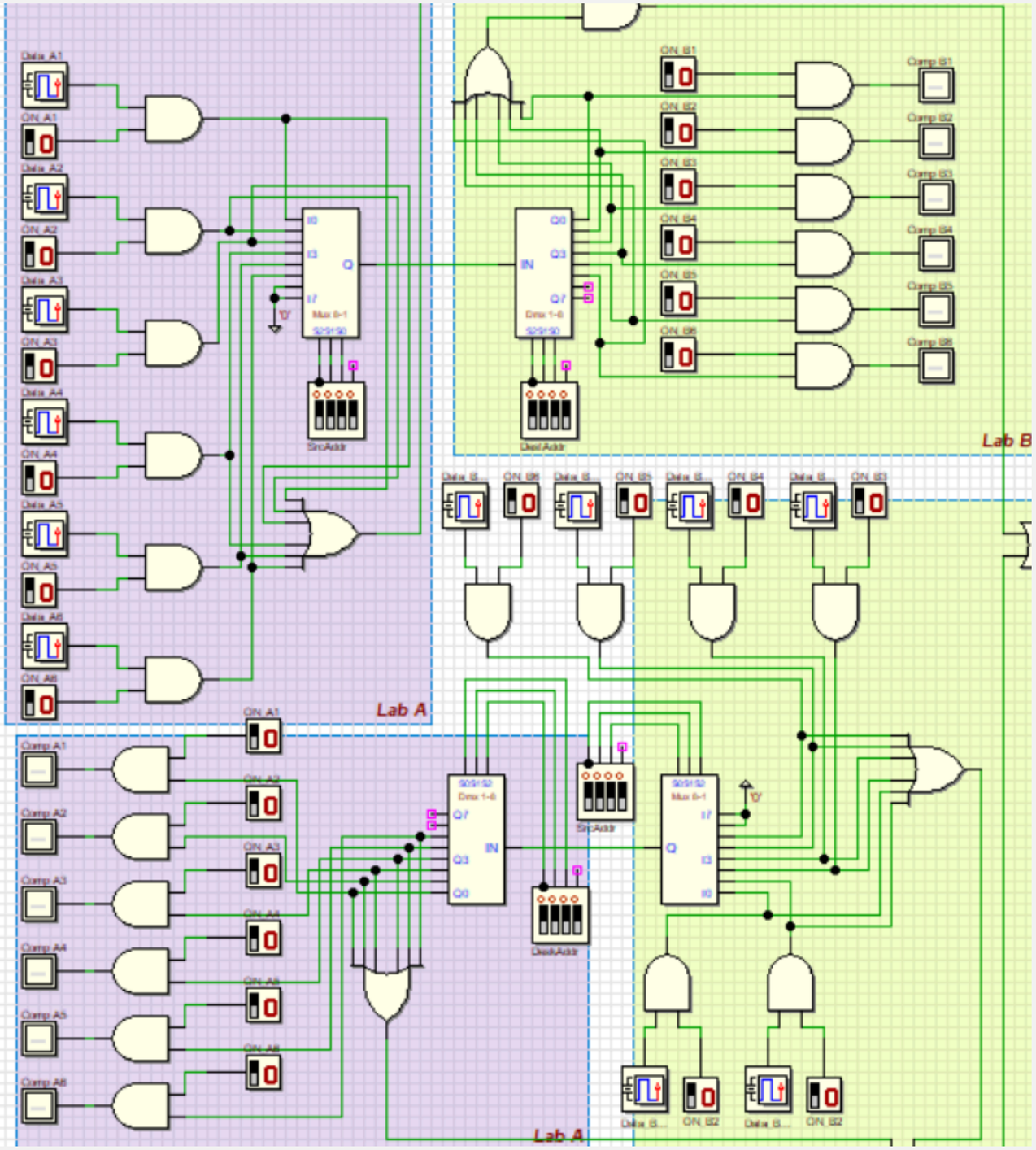
- clear the output and set it to low (0)
- when CLR_bar is set to 0, the seven-segment display will show 0.

14.

**7-segment display**

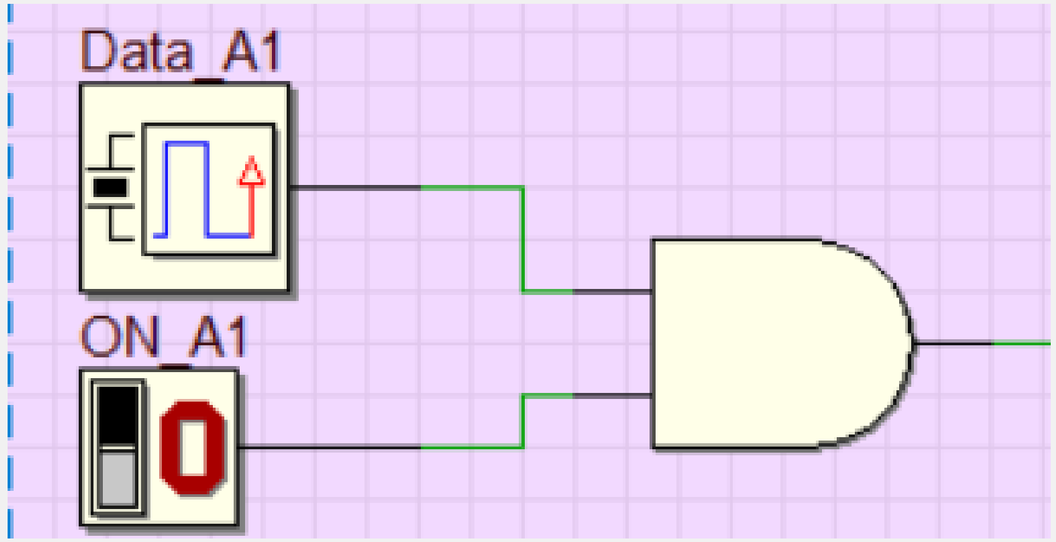
- A 7-segment display is an electronic device that shows numerical digits and some characters. It's made up of seven LED segments that are arranged in a specific pattern.

# SYSTEM IMPLEMENTATION




# MUX AND DEMUX

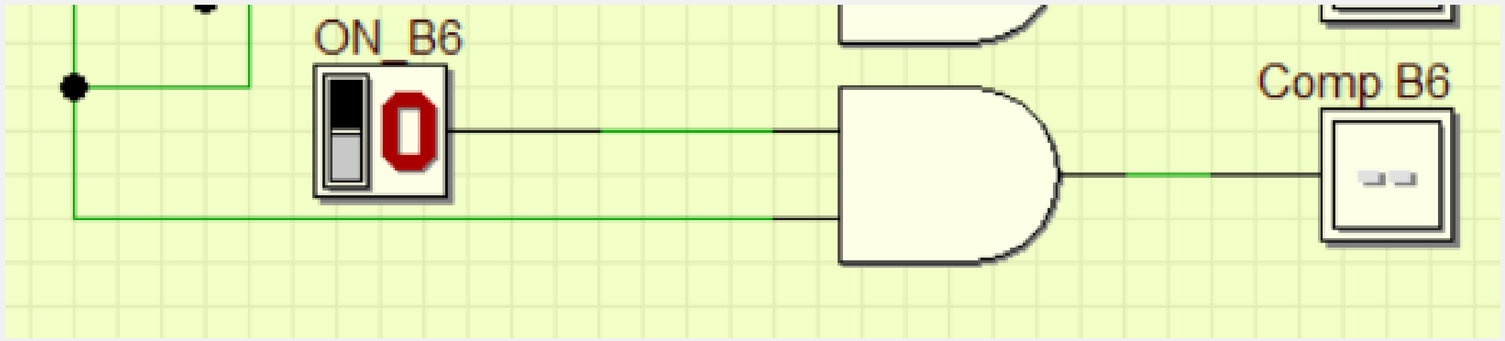
- Both consist of 6 computers
- 2 MUX and 2 DEMUX
- Transmitting data between Lab A and Lab B



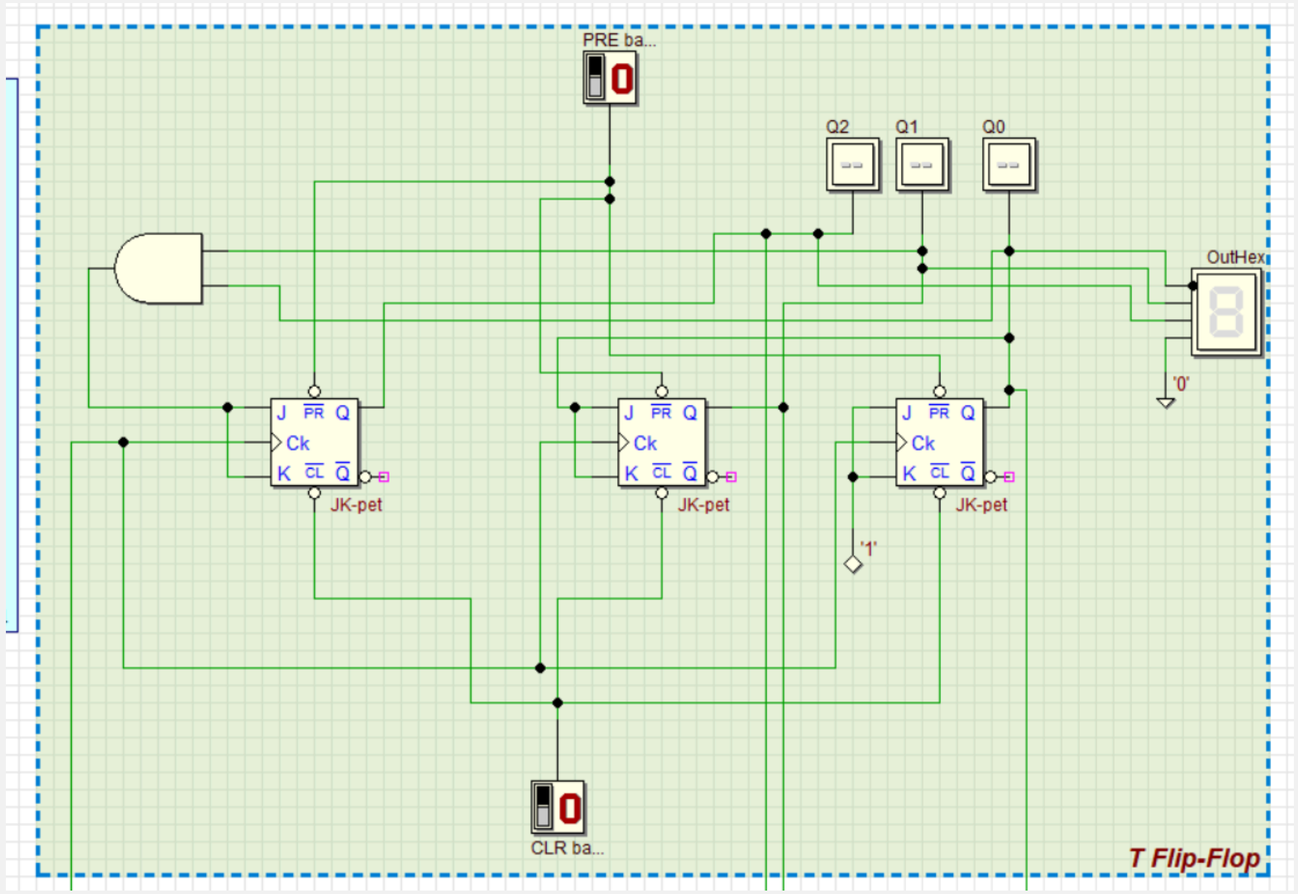

# INPUT

- DATA A1 - Clock signal
- ON A1 - Power on switch
- When ON A1 is 1 (HIGH) - turned on
- When ON A1 is 0 (LOW) - turned down
- Connected 2-input AND gate

# OUTPUT

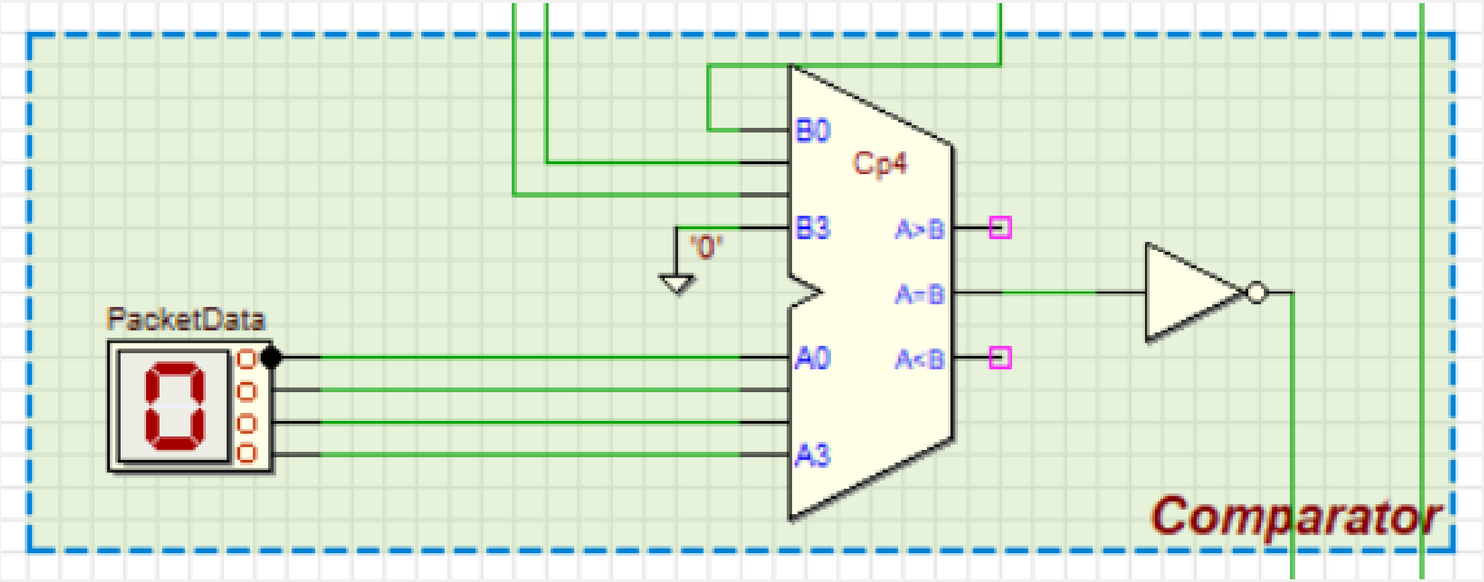



- ON B6 - Power on switch
- When ON B6 is 1 (HIGH) - turned on
- When ON B6 is 0 (LOW) - turned down
- ON B6 and output Q are connected to 2-input AND gate



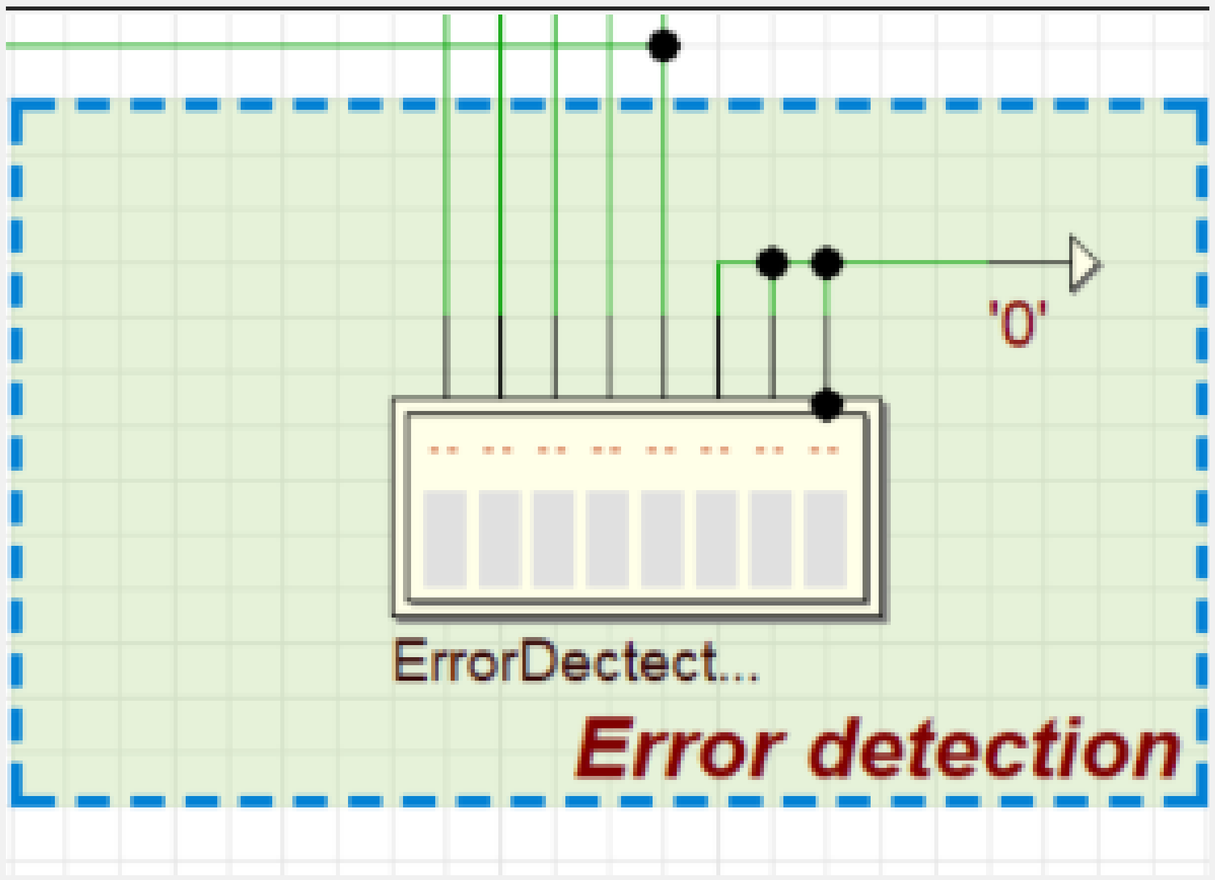

# 3-BIT SYNCHRONOUS T FLIP-FLOP COUNTER

- JK Flip-Flop used to imitate T Flip-Flop
- J=K=1
- 2 states (toggle & no change)
- Flip-Flop only work if clock input is 1



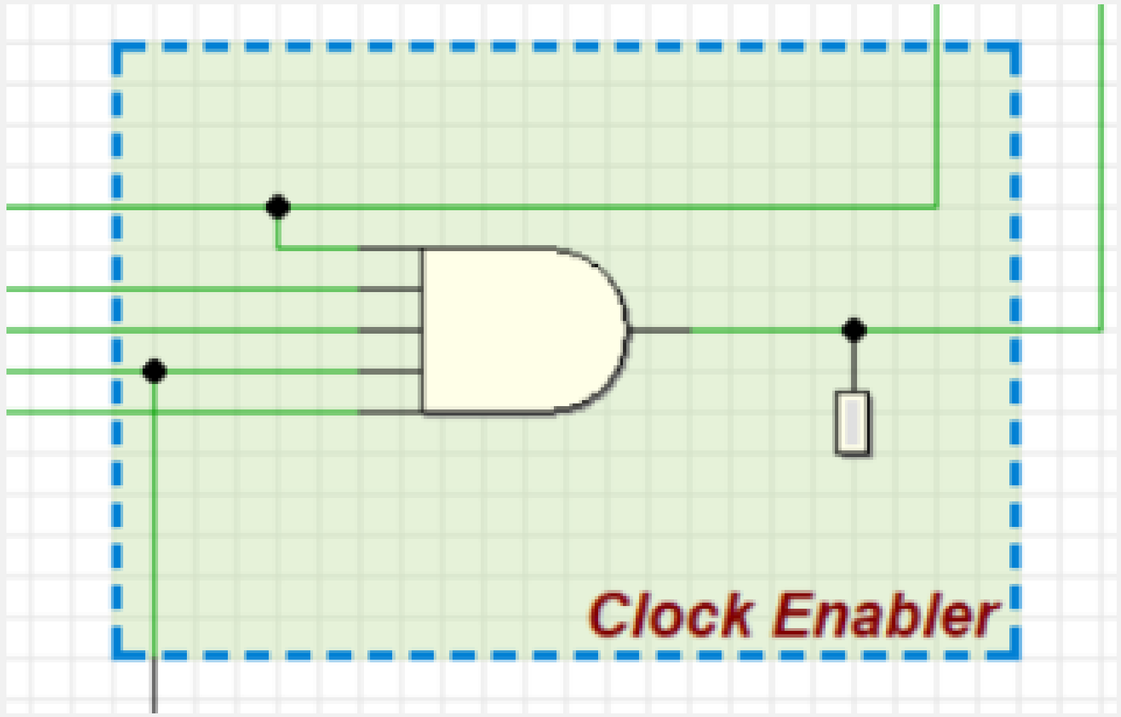

# COMPARATOR

- 4 inputs (A0-A3) - 4-bit HEX input
- Other 3 inputs - each output of Flip-Flop



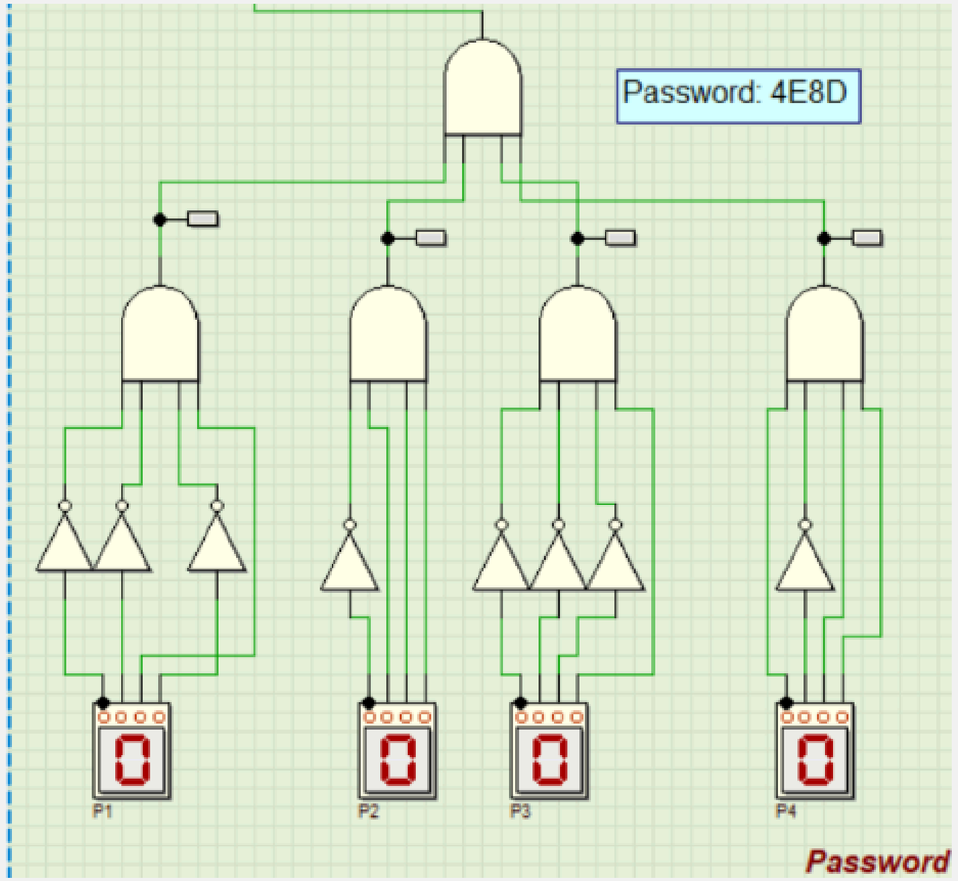

# ERROR DETECTION

- First light doesn't light up: issue in comparator
- Second light doesn't light up: issue in password
- Third light doesn't lit: issue in TRX_Clk
- Fourth light doesn't light up: issue in PowerTRX
- Fifth light doesn't light up: issue in source and destination



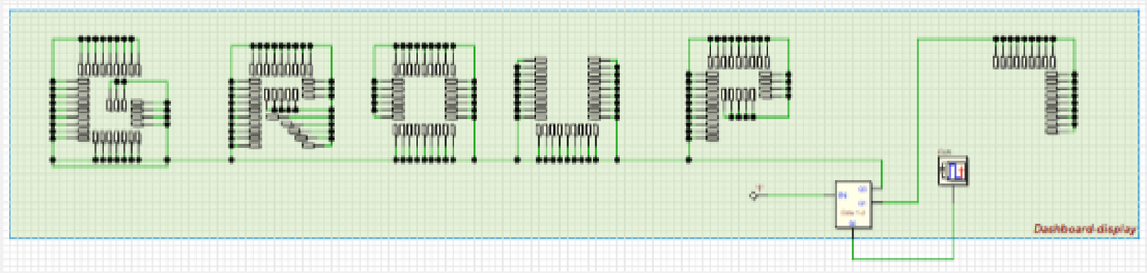

# CLOCK ENABLER

- 5-input AND gate
- 1st input : from OR gates that combines all computers
- 2nd input : from PowerTRX
- 3rd input : from TRX clock
- 4th input : from password system
- 5th input : from comparator




# PASSWORD SYSTEM

- Built using logic gates
- Take input from four seven-segment display
- Checks if the entered password matches 4E8D (hexadecimal).
- NOT gates invert certain bits.
- AND gates verify each digit's correctness.
- A final AND gate combines results.
- Output at error detector = 1 (HIGH) if the password matches.




# FUN DISPLAY

- The fun concept display is built using a 1x2 DEMUX, clock generator, switches and the LEDs as the output. This fun concept display with the title "GROUP 7" was built to make the deeds circuit more appealing.

# CONCLUSION

- simple and user friendly design
- input switches, seven-segment displays, LEDs, an LED array for outputs, a 4-bit comparator, a 3-bit up counter, a multiplexer and demultiplexer, a clock, and basic logic gates.
- to enchance security: integrated password-protected system connected to counter - using 3 bit T flip flop
- ensures incorrect data is not stored when an invalid password is entered
- error detection feature: enables users identify and resolve issues

# REFLECTION

## Challenges and Solutions

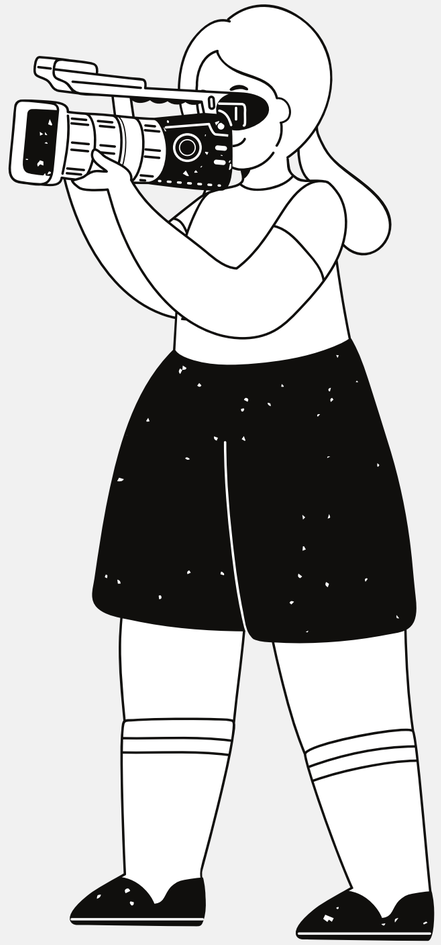
- ensuring accurate packet routing and implementing secure password system - continuous debugging and teamwork
- lack of familiarity with Deeds software - further explore and study more

## Strentghs and Areas for Improvement

- Shee Tong - main designer
- other team member also contribute to project report and presentation slides
- work together - key role
- system only supports a maximum of 8 information packets (3 bit ff)
- implement additional flip-flop

## Future Prospects

- depend on understanding of circuit optimization, data security, digital design
- develop more advanced circuit with additional features
- enhancing our skills
- apply to real-world applications



# Thank you very much!