

CS223

Digital Design

Section: 1

Project Report

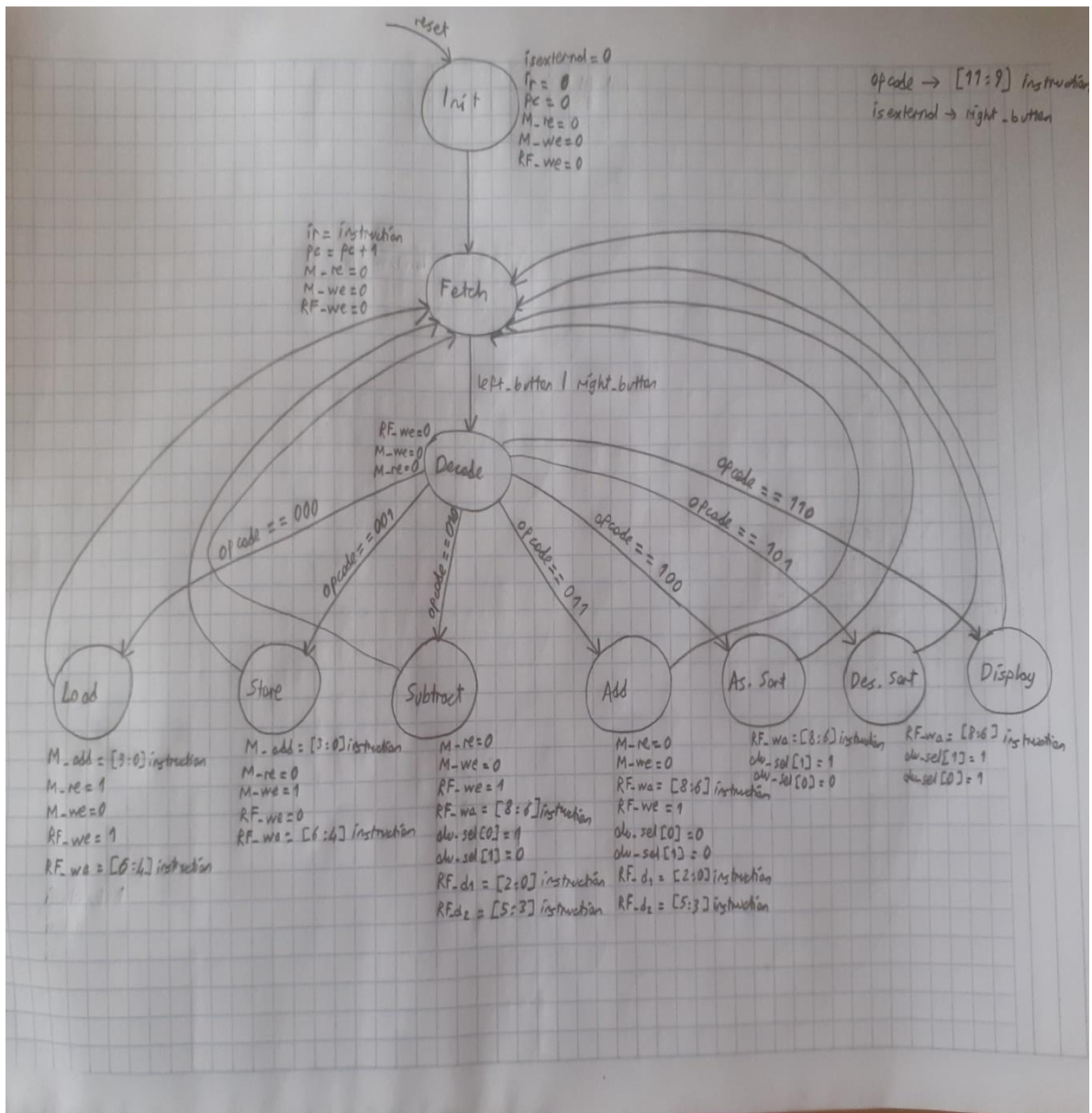
Name: Tolga Han  
Arslan

ID: 22003061

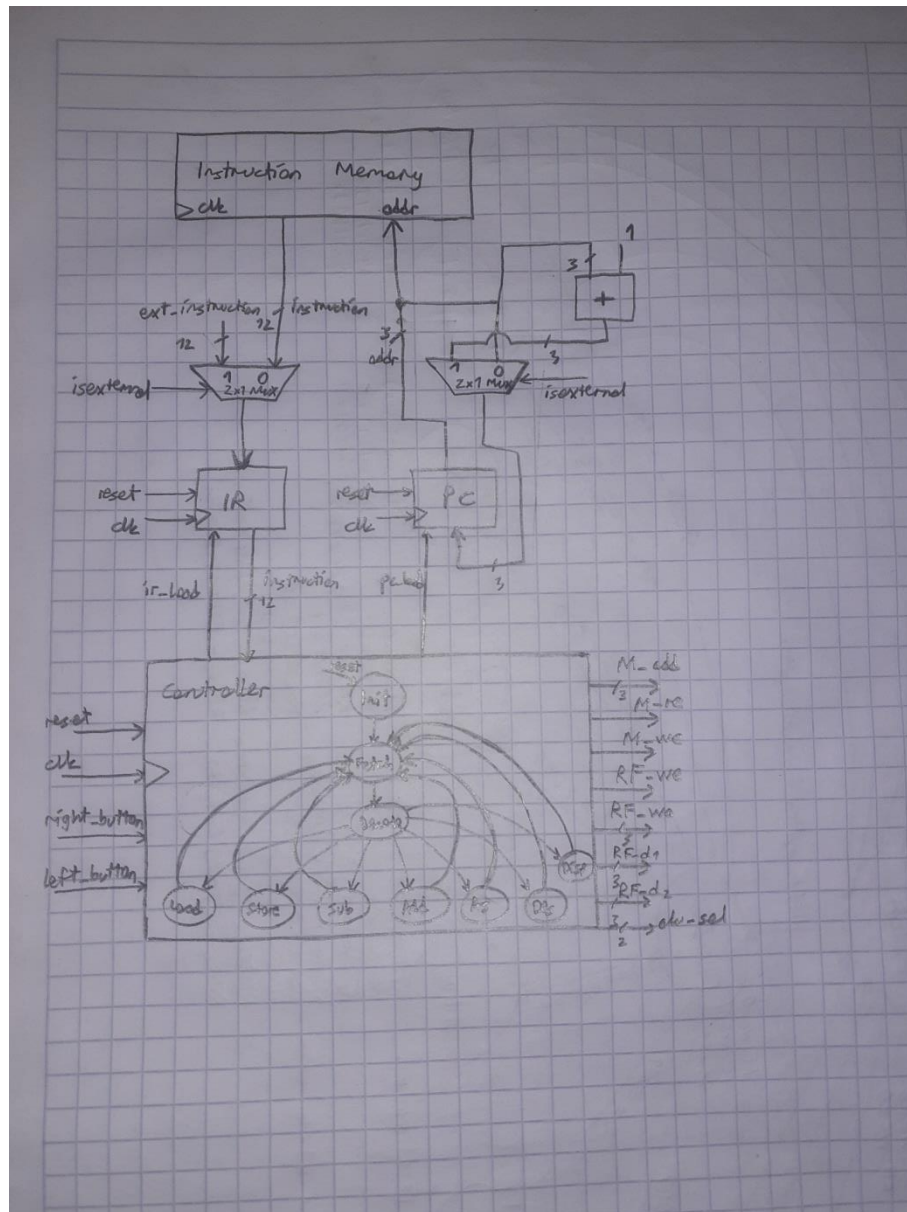
19.12.2022

b) RTL schematics for Ascending and Descending Sorting operations

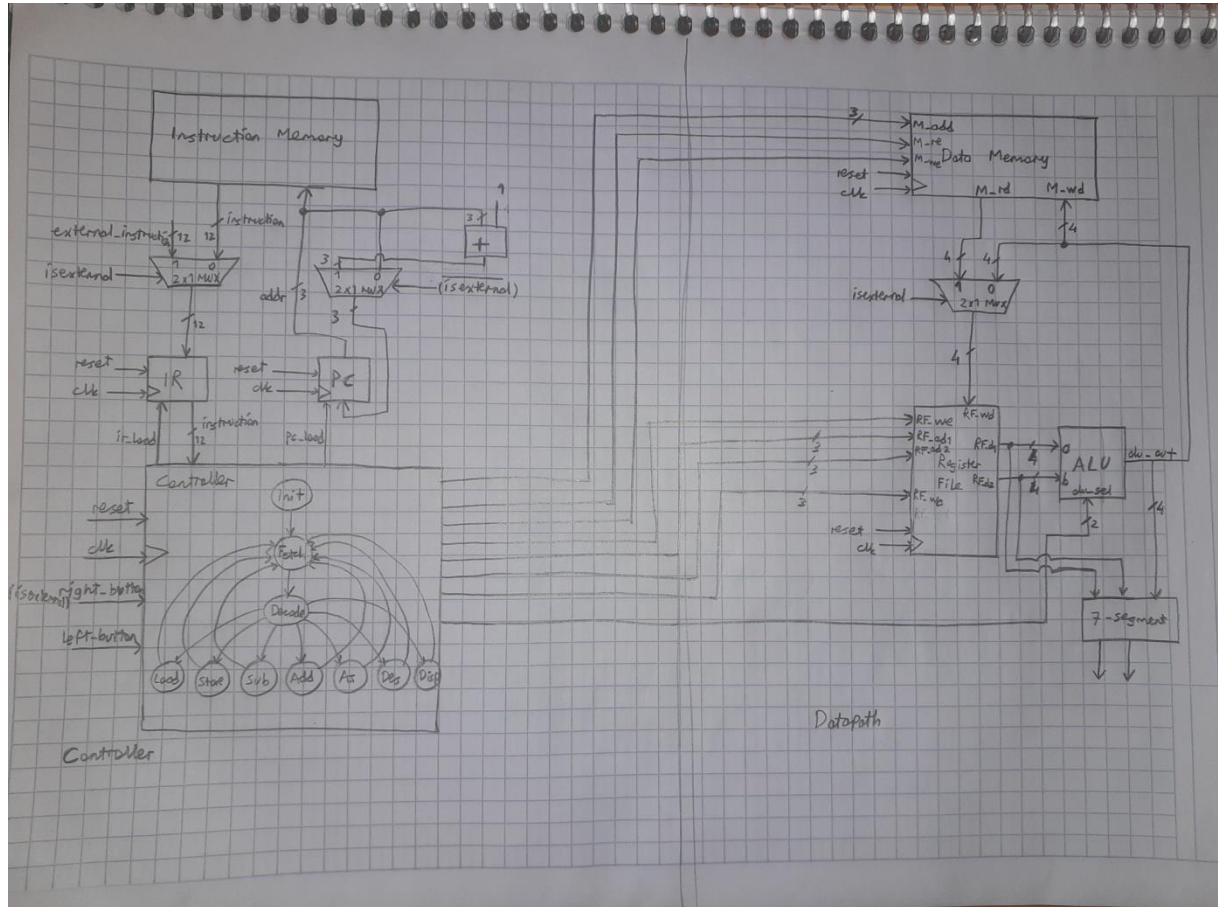
c) Controller High-Level State Machine Diagram



# d) Controller Block Diagram



# e) Controller/Datapath Top Module Block Diagram



## c) Testbenches (This is optional, mainly for partial points if Basys3 doesn't work properly)