CS224
Fall 2020
QUIZ NO. 5

Solution comes later look below

December 23, 2020

**PLEASE READ: 1. Only handwritten answers are accepted. 2. Convert your handwritten answers to pdf and upload one pdf file to Moodle. Make sure that you answer the questions in the order they are given. Provide a neat work and make sure that your answers are numbered and in the order of questions and distinguishable from each other. Do not miss the deadline.**

1. **Cache Memory**

Consider a processor with an architecture similar to MIPS: byte addressable, words are 4 bytes, main memory size is 4 GB.

For the sections A and B below consider the following memory accesses with the given memory addresses. The table shows that for a word that contains a value represented with M1 is at memory location 0X10F and it is accessed for a lw instruction.

| Memory Content | Used For instruction | Memory Address in Hex | Memory Address in Binary |
|---|---|---|---|
| M1 | lw | 10F | 0001 0000 1111 |
| M2 | sw | 0AF | 0000 1010 1111 |
| M3 | lw | 0F0 | 0000 1111 0000 |
| M4 | lw | 05C | 0000 0101 1100 |
| M5 | lw | 10C | 0001 0000 1100 |
| M6 | sw | 0FC | 0000 1111 1100 |
| M7 | sw | 1FC | 0001 1111 1100 |

**A.** Consider the following cache memory configuration for the above memory accesses. N= 1 (direct mapped cache), block size is 4 words, number of sets is 4.

**a.** Give the physical (main) memory address structure as it will be used to access the cache memory. Draw a simple figure and indicate the name and size of each subfield in terms of number of bits.

**b.** Draw the structure of a block in terms of its components: V (valid bit), D[1] (dirty bit), Tag, Data. Indicate the size of each field.
What is the total block size in bits?
What is the SRAM size in bits?
What is the cache memory total data field size in bytes?

**c.** Show the final contents of the cache memory in a figure in terms of its subfield after accessing memory locations in the order given above. Give the values of tag etc. in bits, show block data contents in terms of M1, M2 etc.

**d.** For each memory access indicate if it is a hit or miss. Give the miss type for each case. What is the hit rate?

[1] D bit indicates if the block content is modified during execution time and if it so when that block is emptied due to a conflict its content is written back to physical memory.

**B.** Consider the above memory access sequence with the following cache memory structure: N= 2 (2-way associative cache), block size is 2 words, number of sets is 4. For block replacement LRU is used. To support the LRU policy the U bit is used as illustrated in the textbook (slides). In your answer include the U bit when needed. Answer all sub questions of the question A given above, so in your answers you will have the sub questions B.a, ..., B.d.

**2. Virtual Memory**

**A.** Consider a virtual memory structure of size 4 GB. The physical (main) memory size is given as128 MB. The page size is 1 KB.

**a.** What is the virtual memory address structure in terms of its components and sizes (in bits)? Give a figure for the structure.

**b.** What is the structure of one row of the page table? Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is the size of one row in number of bits. Give a figure for the structure.

**c.** Now consider a 2-way (2-entry) TLB structure. Draw the structure of the TLB. Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is its total size? Assume that LRU is used for replacement. Use the minimum number of U bits.

**d.** Now consider a 4-way TLB structure. Draw the structure of the TLB. Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is the size of one row in number of bits. Draw it. Assume that LRU is used for replacement. Use two U bits for each entry of the TLB (we need 2 U bits since it is it is 4-way: we have to keep track of the utilization age of each of the 4 ways).

**B.** Consider a virtual memory environment of size 4KB with page size of 0.25 KB. Physical memory size is 2KB. (This part is independent of question 2.A.)

**a.** Consider the following memory accesses from left to right. Show the final content of the memory page table including the V bit and D bit after performing "all" memory accesses. For unknown entries assume 0 values.

| **Memory Access No.** | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Virtual Memory Address** | 0B4 | 0F0 | 2A0 | 2AC | 4AC | 0CC | 244 | B00 |
| **Physical Memory Address** | 2B4 | 2F0 | 4A0 | 4AC | 0AC | 2CC | 444 | 700 |
| **Instruction Executed** | sw | lw | lw | sw | lw | lw | sw | lw |

**b.** Consider a TLB structure with two entries and with LRU replacement policy. Draw the TLB include D and U bits. Show the size of each component in number of bits. What is total size in terms of number of bits?

Show TLB contents in hexadecimal after "each" memory access. Indicate if a memory access produces a hit or miss for the TLB contents. State the type of each miss.

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Dec. 26'20

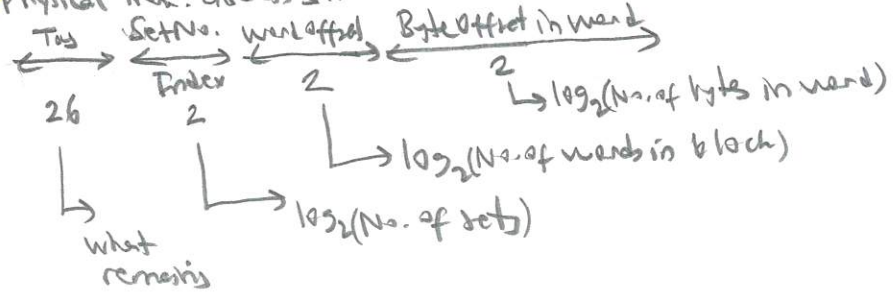
## 1. Cache Memory

MIPS: Byte addressable
Word: 4 bytes
Main Mem Size = 4GB → $2^2 \times 2^{30} = 2^{32}$

### 1.A. Cache Mem.

N = 1, Block Size: 4 words
No. of sets = 4

a. Physical mem. address structure




b. Cache Memory Block Structure


Block size = 1+1+26+128 = 156 bits ← (= set size)
SRAM size = 4 × 156 = 624 bits (Cache mem + overhead)
Cache Mem Total Data Field Size = No. of sets × N × Block Size (in byte)
4 × 1 × (4×4) = 64 bytes

c. Cache Mem Content (Set No)

M1: 0001 0000 1111 — Comp. Miss (Compulsory miss)
M2: 0000 10 11 1111 (sw) — Comp. Miss D=1
M3: 0000 1111 0000 — Comp. Miss
M4: 0000 0101 1100 — Comp. Miss
M5*: 0001 0000 1100 — Hit (Tag = Tag of M1)
M6: 0000 1111 1100 (sw) — Hit (Tag = Tag of M3)
M7: 0001 1111 1100 (sw) — Capacity Miss

Set No: underlined

Set


M2:


M3:


M4:


M7:


M6:


M5:


Cache Mem. Final Contents

| V | D | Tag | Data | SetNo |
|---|---|---|---|---|
| 1 | 1 | 0001 | 11 M7 | 11 |
| 1 | 1 | 0000 | 10 M2 | 10 |
| 1 | 0 | 0000 | 01 M4 | 01 |
| 1 | 0 | 0001 | 00 M1/M5 | 00 |

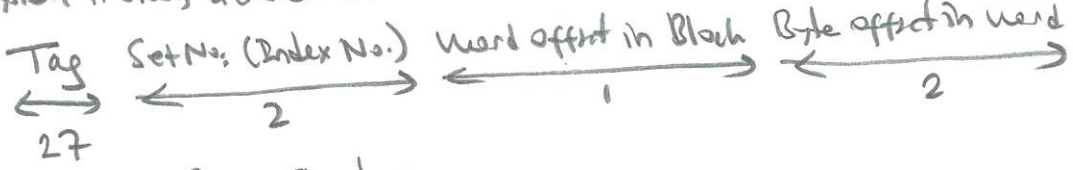
Tag is 32 bits, but only the relevant part is shown.

Hit/Miss Summary
First 4: Compulsory Miss
M5, M6: Hit
M7: Capacity Miss
Hit Rate: 2/7

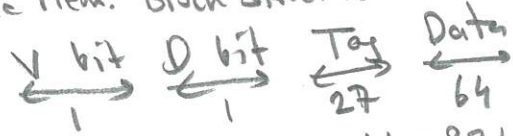
## 1-B Cache Mem. (cont.)

N=2, Block size: 2 words, No. of Sets: 4 Block Replacement: LRU

a. Physical memory address structure




b. Cache Mem. Block Structure




Block size: 1+1+27+64 = 93 bits

Set Size: 2 × Block size: 2×93 = 186 bits

SRAM Size: 4 × Set Size: 4×186 = 744 bits

↳ But we have one more detail: U bits for each set

4 sets × 1 U bit size = 4 bits

∴ Total SRAM size: 748 bits

Note: (No. of U bits for a set) = $\log_2 N$ ← General rule for U bits/set

c. Cache Memory Contents as we access memory

U bit: shows most recently accessed block in a set.

M1: 0001 0000 1111 Comp. Miss

M2: 0000 1010 1111 Comp. Miss

M3: 0000 1111 0000 Comp. Miss

M4: 0000 0101 1100 Comp. Miss

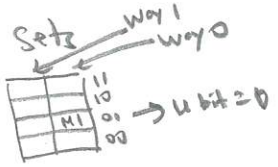
M5: 0001 0000 1100 Conflict Miss

M6: 0000 1111 1100 Comp. Miss

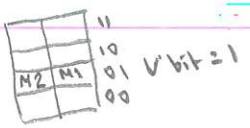
M7: 0001 1111 1100 Conflict Miss

Hit Rate = 0 All misses

M1:

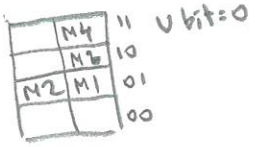



M2:



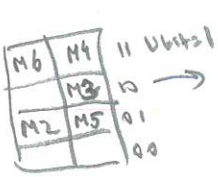

M3:


M4:

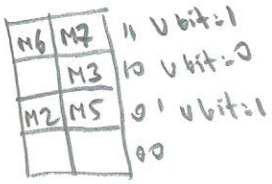



M5:


M6:




M7:

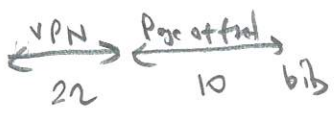



U bit: shows most recently accessed block

## 2. Virtual Memory

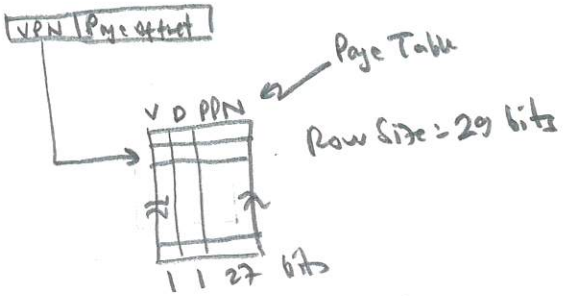
**2.A.** Virtual Mem Size = 4GB, $2^{32}$ Main Mem Size = 128 MB $2^{27}$ Page Size: 1K $2^{10}$

**a.** VM add. structure

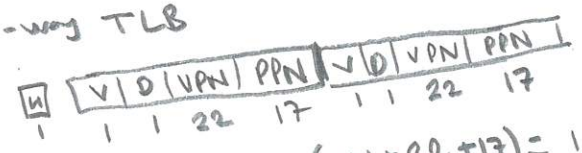



PM add. structure


**b.**




**c.** 2-way TLB




TLB Size = $1 + 2 \times (1+1+22+17) = 1 + 2 \times 41 = 83$ bits

**d.** 4-way TLB

U = 2 bits for each way


$4 \times (2+1+1+22+17) = 4 \times 43 = 172$ bits

We have to keep track of the life of each entry

Answer for this → Why U = 2 bits?

2.B VM Size = 4KB → $2^{12}$, PM Size = 2KB → $2^{11}$

Page Size = 0.25 KB → $\frac{1}{4} \times 2^{10} = 2^8$

8 bit page size --> ppn and vpn 4 bits (first digit)

No. of VM pages = $\frac{2^{12}}{2^8} = 2^4$

No. of PM pages = $\frac{2^{11}}{2^8} = 2^3$

| No | VM Address | PM Address | |
|---|---|---|---|
| 1 | 0B4 | 2B4 | sw |
| 2 | 0F0 | 2F0 | |
| 3 | 2A0 | 4A0 | |
| 4 | 2AC | 1AC | sw |
| 5 | 4AC | 0AC | |
| 6 | 0CC | 2CC | |
| 7 | 244 | 144 | sw |
| 8 | B00 | 700 | |

No. of VM pages = $2^4 = 16$

| | V | D | PPN |
|---|---|---|---|
| 1111 | | | |
| 1110 | | | |
| 1101 | | | |
| 1100 | | | |
| 1011 | 1 | 0 | 111 |
| 1010 | | | |
| 1001 | | | |
| 1000 | | | |
| 0111 | | | |
| 0110 | | | |
| 0101 | | | |
| 0100 | 1 | 0 | 000 |
| 0011 | | | |
| 0010 | 1 | 1 | 100 |
| 0001 | | | |
| 0000 | 1 | 1 | 010 |

TLB Content Progress as we access memory

VPN & PPN are shown in decimal

① 

| No. | Way 1 V | D | VPN | PPN | Way 0 V | D | VPN | PPN | U | |
|---|---|---|---|---|---|---|---|---|---|---|
| X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | → Initial condition |
| 1,2 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 | 0 | → 1st compulsory miss, 2nd hit |
| 3,4 | 1 | 1 | 2 | 4 | 1 | 1 | 0 | 2 | 1 | → 3rd compulsory miss, 4th hit |
| 5 | 1 | 1 | 2 | 4 | 1 | 0 | 4 | 0 | 0 | → 5th conflict miss |
| 6 | 1 | 0 | 0 | 2 | 1 | 0 | 4 | 0 | 1 | → 6th conflict miss |
| 7 | 1 | 0 | 0 | 2 | 1 | 1 | 2 | 4 | 0 | → 7th compulsory miss |
| 8 | 1 | 0 | 11/B | 7 | 1 | 1 | 2 | 4 | 1 | → 8th compulsory miss |

* U: shows the last way/unit used.

Hit Rate = 2/8