



Visually.

Making Invisible Hardware Tangible.

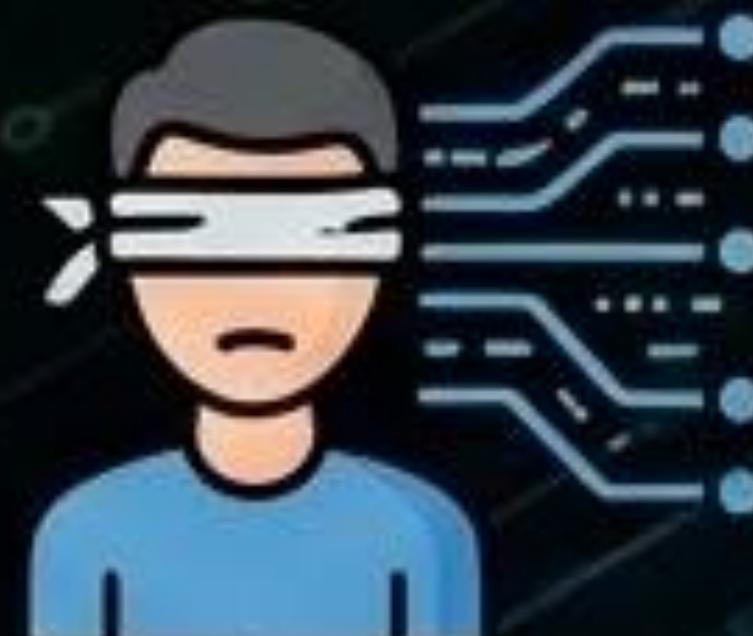
The Problem



Computer Architecture is abstract and difficult to learn.



Current tools are text-based, static, and lack interactivity.



Students cannot ‘see’ the data moving.

The Solution

The screenshot shows the "System Architecture Overview" section of the Memory Hierarchy Simulator. It displays four components in a horizontal hierarchy: "CPU Core" (PC: 0x1000), "L1 Cache" (Hit Rate: 0%), "L2 Cache" (Hit Rate: 0%), and "Main Memory" (Size: 4GB). Below these components is a blue button labeled "Start Simulation (L1 View)". At the bottom of the page, there are three informational boxes: "How it Works", "Visual Feedback", and "Performance".

System Architecture Overview

Explore the complete memory hierarchy from the CPU Core down to Main Memory.
Click on any component to inspect its internal state, view access logs, and analyze performance metrics.

CPU Core
PC: 0x1000

L1 Cache
Hit Rate: 0%

L2 Cache
Hit Rate: 0%

Main Memory
Size: 4GB

Start Simulation (L1 View)

How it Works
The CPU issues memory requests (Loads/Stores). These requests traverse the hierarchy, checking L1, then L2, and finally RAM.

Visual Feedback
Watch the data flow animations to see hits and misses in real-time. Green indicates a hit, while red indicates a miss.

Performance
Monitor Hit Rates and AMAT (Average Memory Access Time) to understand the efficiency of your cache configuration.

A web-based, interactive CPU simulator.
Visualizes the full memory hierarchy (L1 Cache, L2 Cache, RAM).
Features real-time animation of data flow and hit/miss logic.

Deep Tech Features

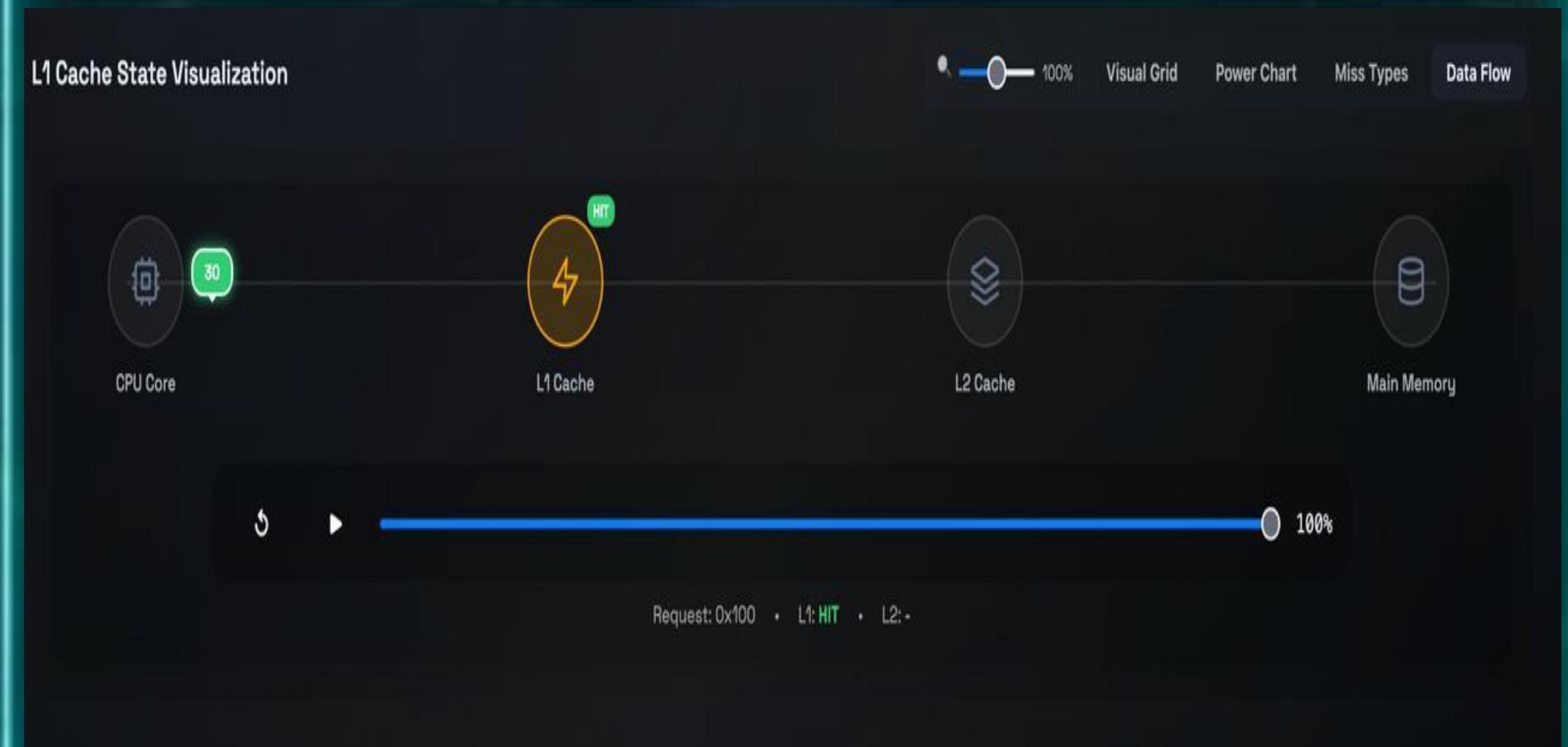
Multi-level Hierarchy Simulation



Multi-level Hierarchy Simulation

Simulates L1, L2, and RAM interactions with realistic latency.

Live Dataflow Animation



Live Dataflow Animation

Real-time animation showing the precise timeline of memory accesses.

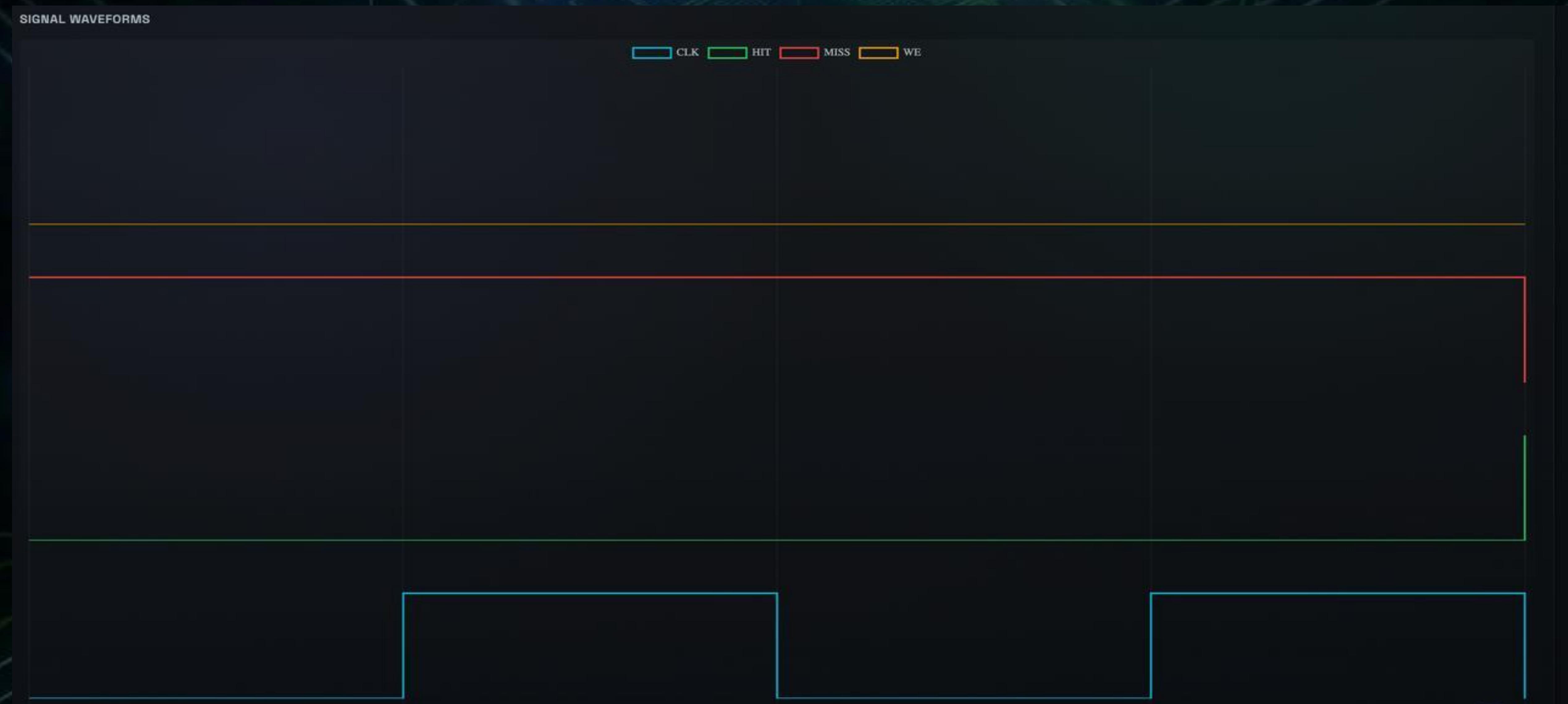
CPU Register View

Register File (x0 - x31)							
x0 0x00000000	x1 0x00000000	x2 0x7FFFFFFF	x3 0x00000000	x4 0x00000000	x5 0x00000000	x6 0x00000000	x7 0x00000000
x8 0x00000000	x9 0x00000000	x10 0x30	x11 0x00000000	x12 0x00000000	x13 0x00000000	x14 0x00000000	x15 0x00000000
x16 0x00000000	x17 0x00000000	x18 0x00000000	x19 0x00000000	x20 0x00000000	x21 0x00000000	x22 0x00000000	x23 0x00000000
x24 0x00000000	x25 0x00000000	x26 0x00000000	x27 0x00000000	x28 0x00000000	x29 0x00000000	x30 0x00000000	x31 0x00000000

CPU Register View

Live view of CPU registers showing changing values inside the processor.

Power & Waveforms



Real-time power analysis of memory accesses.



Dynamic energy consumption graphs and estimations.



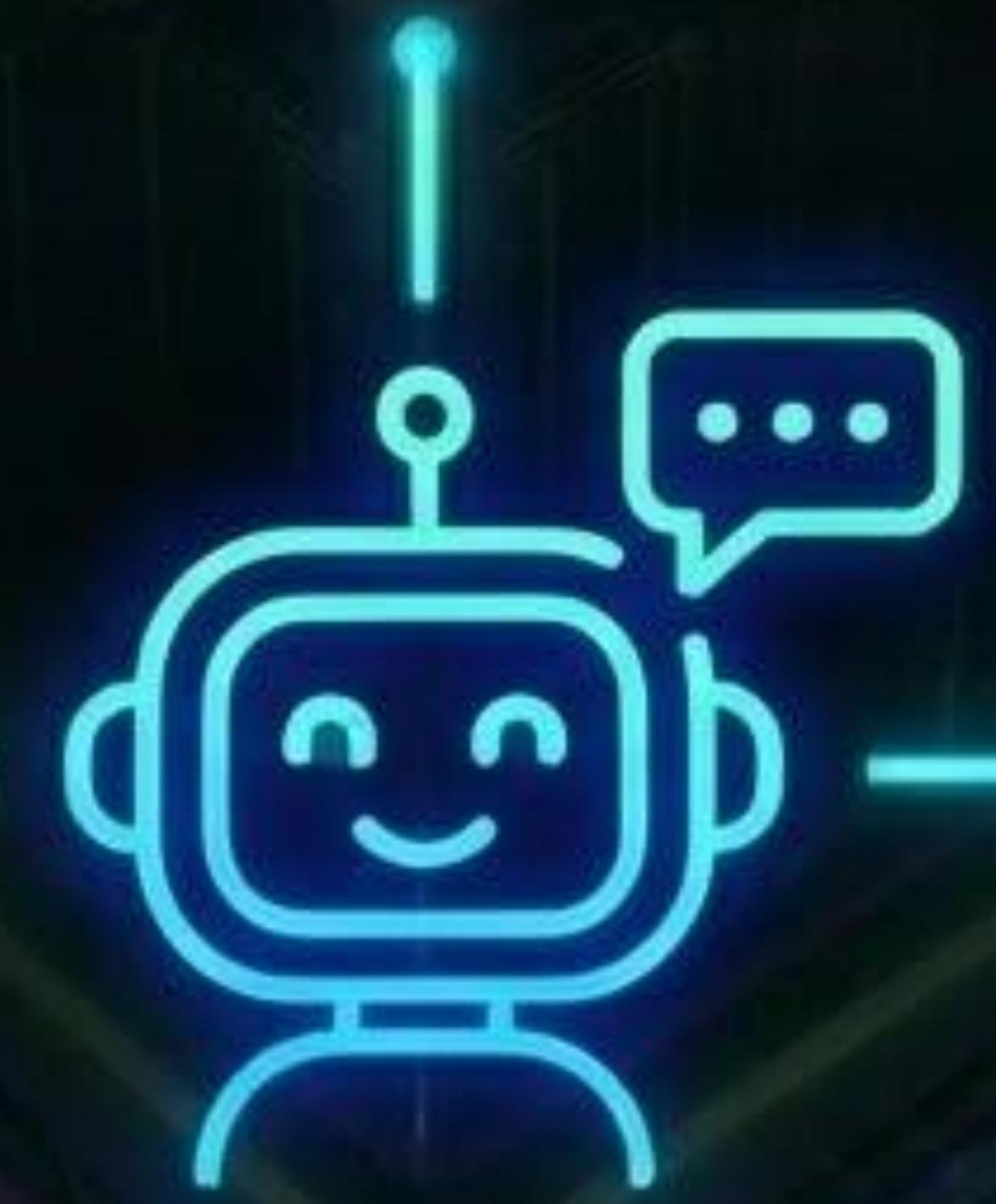
Cycle-accurate latency metrics for performance analysis.

The AI Tutor & Integration



Integrated AI Chatbot (BYO-Key)

Virtual professor explains misses
and answers questions.



University Login Integration
Seamless login for persistence
and progress tracking.



Gamified Learning
Engaging challenges and
leaderboards for students.

Adoption Strategy

Milestone 1



Phase 1:
Hackathon Showcase
Free tier for immediate
use and feedback.

Milestone 2



Phase 2:
University Pilot
Pilot with University
Architecture courses.

Milestone 3



Phase 3:
Analytics Dashboard
Analytics for professors
to track student progress.

Project CacheFlow: The Future of Architecture Education

The Technical Innovation



- **Full Hierarchy Simulation:** Visualizing the complete data path between L1, L2, and RAM (not just single-level).



- **Physics-Based Metrics:** Real-time Power Waveforms, energy consumption, and cycle-accurate latency.



- **Deep Inspection:** Live view of CPU Registers, Branch Prediction (1-bit/2-bit), and Dataflow animation.

The User Experience & Strategy



- **AI-Integrated Learning:** Integrated Chatbot (BYO-Key) acts as a personalized tutor for analyzing misses.



- **University-Ready:** Built-in SSO Login for student persistence and progress tracking.



- **Adoption Model:** Gamified challenges to ensure student engagement and easy professor integration.

▶ Status: Live Demo Available.

→ Goal: Replacing static text tools with dynamic simulation.