



Visually.

Making Invisible Hardware Tangible.

The Problem



Computer Architecture is abstract and difficult to learn.

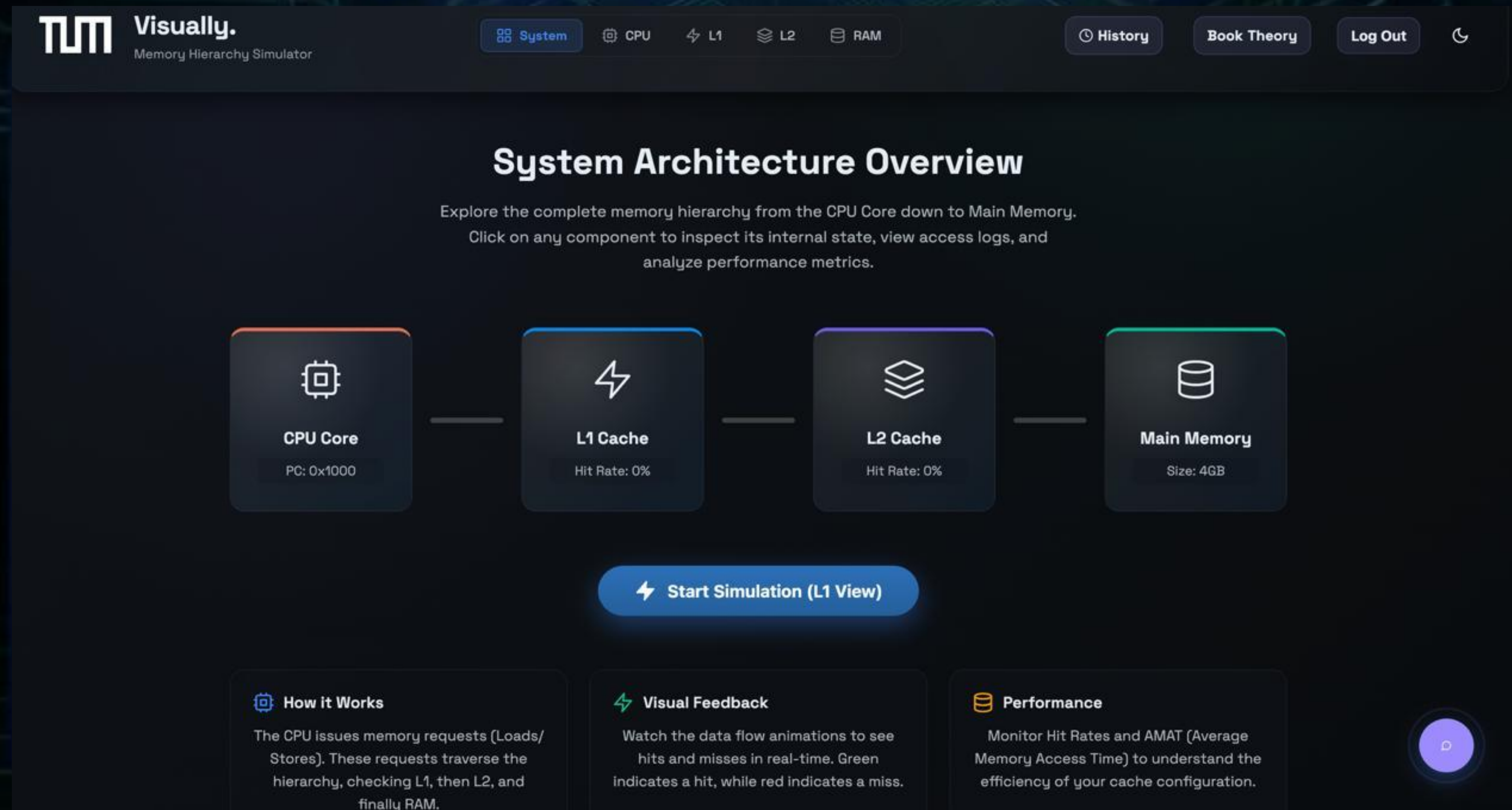


Current tools are text-based, static, and lack interactivity.



Students cannot 'see' the data moving.

The Solution



A web-based, interactive CPU simulator.
Visualizes the full memory hierarchy (L1 Cache, L2 Cache, RAM).
Features real-time animation of data flow and hit/miss logic.

Deep Tech Features

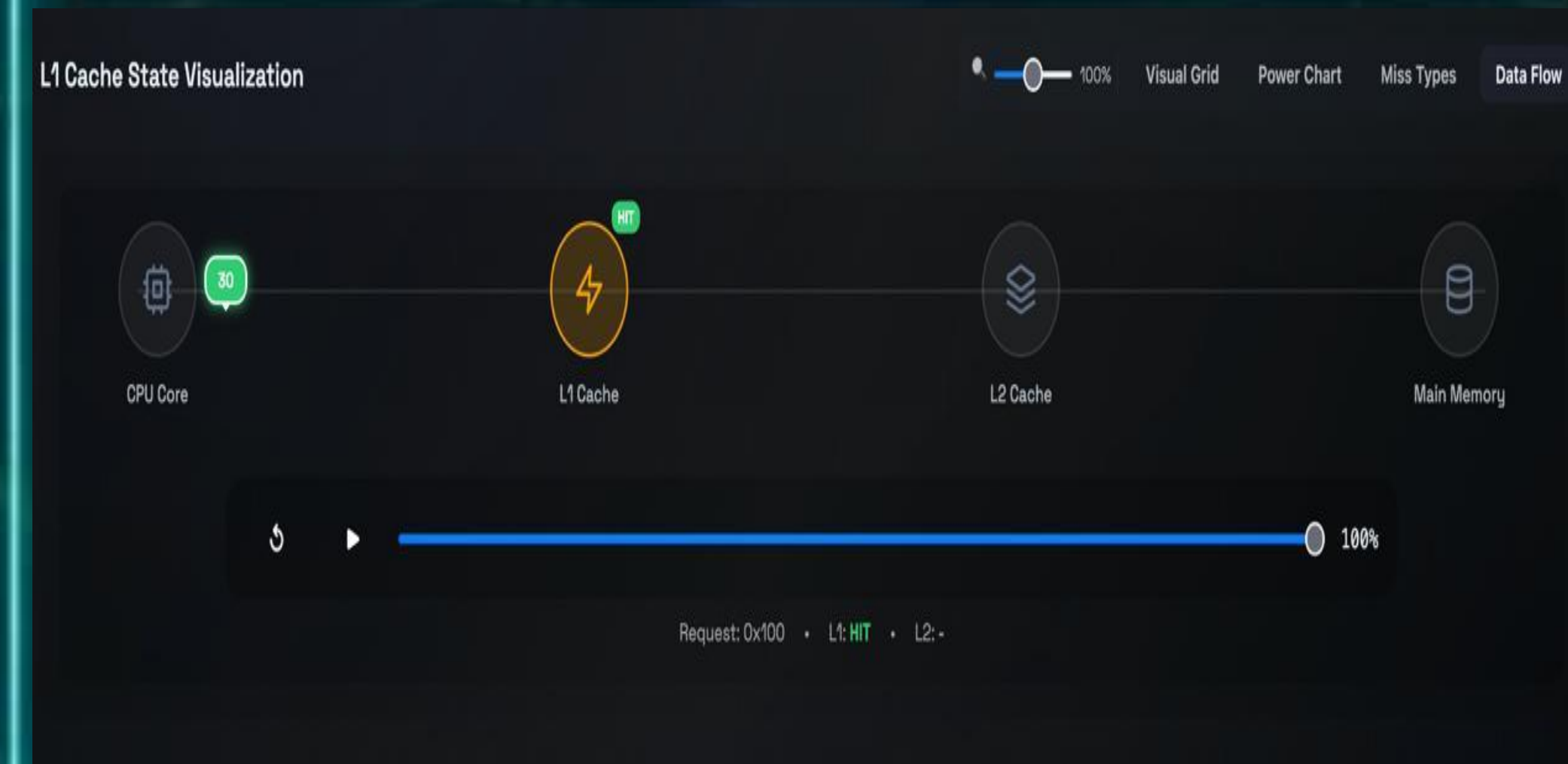
Multi-level Hierarchy Simulation



Multi-level Hierarchy Simulation

Simulates L1, L2, and RAM interactions with realistic latency.

Live Dataflow Animation



Live Dataflow Animation

Real-time animation showing the precise timeline of memory accesses.

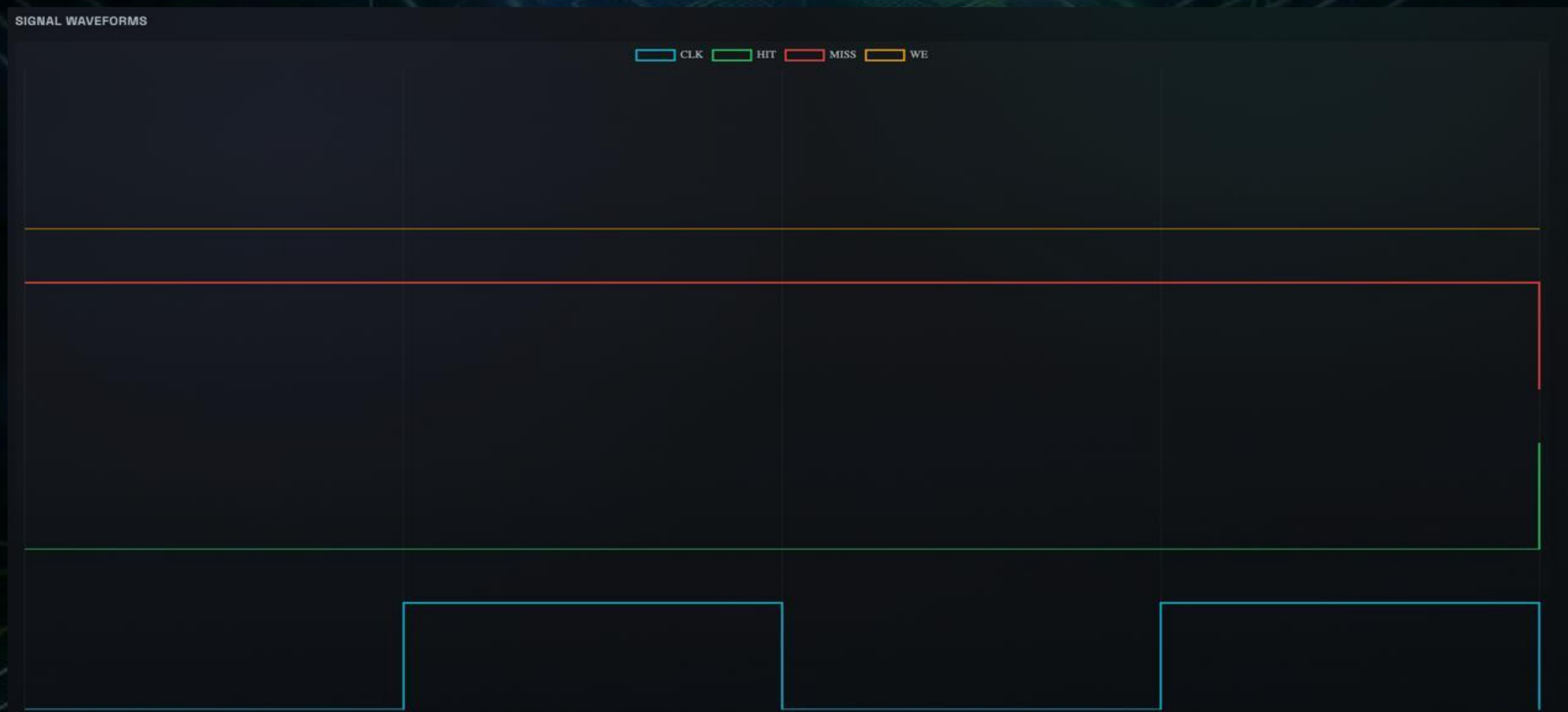
CPU Register View

A screenshot of the 'CPU Register View' interface. It displays a grid of registers, each with a label (e.g., x0, x1, x2, etc.) and a hexadecimal value. The register x10 is highlighted with a green border, showing the value 0x30. The interface also includes a tab for 'Register File (x0 - x31)'.

CPU Register View

Live view of CPU registers showing changing values inside the processor.

Power & Waveforms



Real-time power analysis of memory accesses.



Dynamic energy consumption graphs and estimations.



Cycle-accurate latency metrics for performance analysis.

The AI Tutor & Integration



Integrated AI Chatbot (BYO-Key)

Virtual professor explains misses and answers questions.



University Login Integration

Seamless login for persistence and progress tracking.



Gamified Learning

Engaging challenges and leaderboards for students.

Adoption Strategy

Milestone 1



Phase 1:

Hackathon Showcase

Free tier for immediate use and feedback.

Milestone 2



Phase 2:

University Pilot

Pilot with University Architecture courses.

Milestone 3



Phase 3:

Analytics Dashboard

Analytics for professors to track student progress.

Project CacheFlow: The Future of Architecture Education

The Technical Innovation



- **Full Hierarchy Simulation:** Visualizing the complete data path between L1, L2, and RAM (not just single-level).



- **Physics-Based Metrics:** Real-time Power Waveforms, energy consumption, and cycle-accurate latency.



- **Deep Inspection:** Live view of CPU Registers, Branch Prediction (1-bit/2-bit), and Dataflow animation.

The User Experience & Strategy



- **AI-Integrated Learning:** Integrated Chatbot (BYO-Key) acts as a personalized tutor for analyzing misses.



- **University-Ready:** Built-in SSO Login for student persistence and progress tracking.



- **Adoption Model:** Gamified challenges to ensure student engagement and easy professor integration.

▶ **Status:** Live Demo Available.

➔ **Goal:** Replacing static text tools with dynamic simulation.