UCD / College of Engineering and Architecture / Electronic Engineering /

Power Converter Design

Name: Tiarnach Ó Riada 16315466

I declare that all material in this assessment is my own work.

Signed By: Tiarnach Ó Riada **Date:** 9th December 2020

EEEN40310 Power Electronic Technology

Contents

1 Introduction

In this lab we designed a buck converter and a circuit to generate the switching voltage for it. The nominal specifications are given below in table 1.1.

Table 1.1: Specifications

V_{in}	$10\,\text{V} \pm 2\,\text{V}$
V_{out}	$5\,\text{V}$
I_{out}	$1\,\text{A}$
$I_{out,min}$	$0.2\,\text{A}$
$\Delta i_{L,max}$	$0.2I_{out} = 200\,\text{mA}$
ΔV_{out}	$0.02V_{out} = 50\,\text{mV}$

2 Converter Design Results

Table 2.2: Design Calculations

Quantity	Value	Assumptions and design comments
f_s	$100\,\text{kHz}$	
L	$83.2\,\mu\text{H}$	$L_{min} = \frac{V_{out}(1-D_{min})}{2f_s I_{out,min}} = 60\,\mu\text{H}$ where $D_{min} = \frac{V_{out}}{V_{in,max}\eta} = 0.5208 \therefore \eta = 0.8$. $83.2\,\mu\text{H}$ is the inductance of the inductor built during the lab.
C	$10\,\mu\text{F}$	$C_{min} = \frac{\Delta i_{L,max}}{8f_s \Delta V_{out}} = 3.6\,\mu\text{F}$. Allowing for a tolerance of 20%, the closest capacitor value available was $10\,\mu\text{F}$.

The switch resistance r_S and rise time t_r of the PMOS were taken as $0.1\,\Omega$ 55 ns from the datasheet and the forward voltage drop V_F and resistance r_d of the diode were 1.05 V and $0.06\,\Omega$. The capacitor esr r_C was taken as $60\,\text{m}\Omega$ from its datasheet. The inductor esr as measured once constructed was $0.02\,\Omega$.

Table 2.3: Efficiency Calculations

Conditions: $V_{in} = 10\,\text{V}$, $V_{out} = 5\,\text{V}$, $I_{out} = 1\,\text{A}$, $P_{out} = 5\,\text{W}$		
Component or Loss	Loss Equation	Value [W]
Switch Conduction	$r_S D I_{out}^2 \left(1 + \frac{1}{12}\left(\frac{\Delta i_L}{I_{out}}\right)^2\right)$	$0.0252\,\text{W}$
Switch Switching Loss	$2\frac{V_{in} I_{out}}{2}\frac{t_r}{T}$	$0.055\,\text{W}$
Diode Conduction	$r_S(1-D)\frac{I_{out}^2}{2}\left(1 + \frac{1}{12}\left(\frac{\Delta i_L}{I_{out}}\right)^2\right)$	$0.0302\,\text{W}$
Diode Forward voltage loss	$v_f\,(1-D)\,I_{out}$	$0.525\,\text{V}$
Inductor conduction loss	$r_L I_{out}^2 \left(1 + \frac{1}{12}\left(\frac{\Delta i_L}{I_{out}}\right)^2\right)$	$1.56\,\text{W}$
Capacitor conduction loss	$r_C \frac{\Delta i_L^2}{12}$	$0.45\,\text{mW}$
Losses	$\Sigma Losses$	$2.6454\,\text{W}$
Efficiency	$\frac{P_{out}}{P_{out}+P_{loss}}$	65.4%

3 Converter Simulation Results

Figure 1 gives the final converter circuit and fig. 2 the output voltage and current. The former has a dc value of 4.6875 V with a ripple of 50 mV and the latter a dc value of 997.34 mA with a ripple of 11 mA.

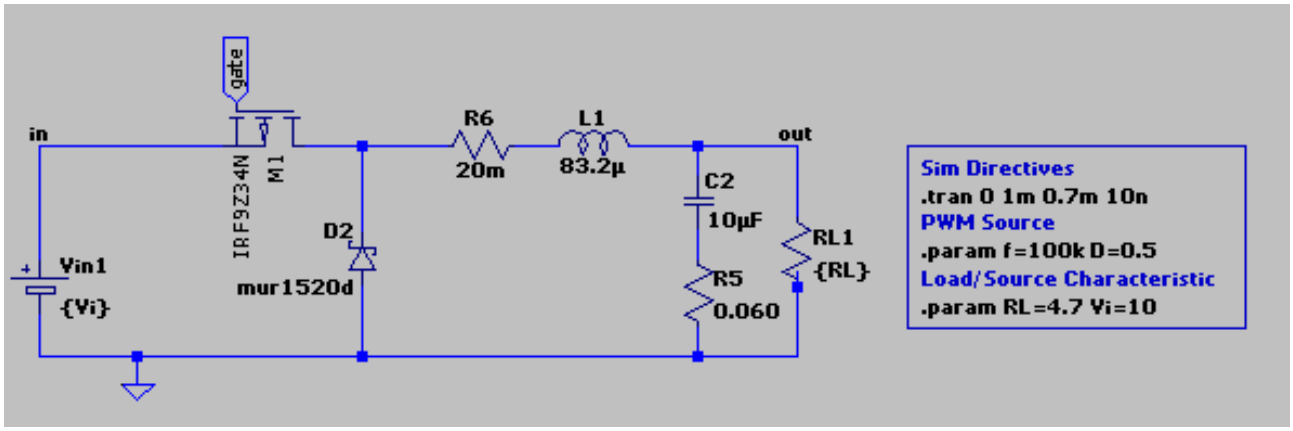

Figure 1: Converter circuit. `gate` is the PWM source.

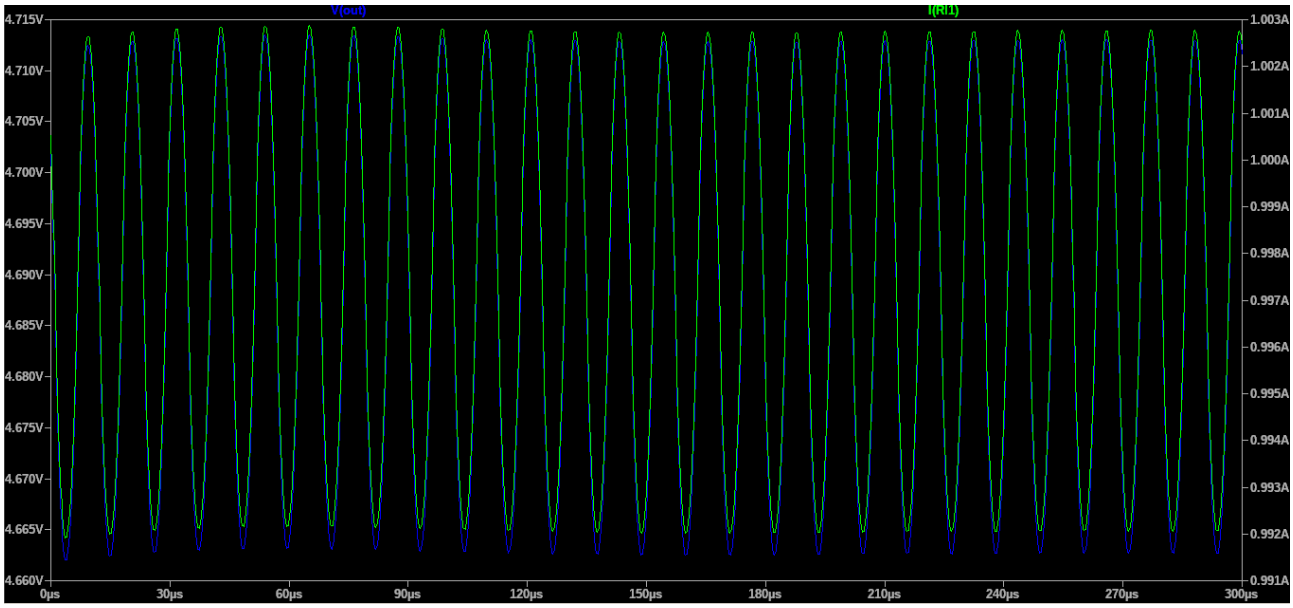

Figure 2: Converter output voltage and current

3.1 Questions

3.1.1 What is the minimum gate voltage that can be used to drive the high side switch?

The high side switch is a PMOS. For it not to be in cut-off, the gate voltage must be less than a threshold below the source voltage. Since the source voltage is at the input voltage, this means that the gate voltage must always be at least a threshold below the input voltage. The minimum gate voltage for which conduction is guaranteed is therefore $V_{in,max} + V_t = 12 - 2 = 10\,\text{V}$ ($V_t = 2\,\text{V}$ from datasheet).

3.1.2 What would be the implications for the required high side switch gate voltages of if an NMOS switch is used instead of an PMOS?

Since the gate voltage for the PMOS is lower than the input voltage used for the converter, a voltage divider can be used to drive it from the input voltage. An NMOS would require a gate voltage higher than the input and corresponding circuitry to increase the voltage.

3.1.3 In terms of how well the design meets the specifications, do the design calculations and results from the simulation agree?

Both the voltage and current ripples are within specifications.

3.1.4 What is the efficiency of the converter determined from the LTSpice simulation?

The power input to the converter is 7.4215 W from the input voltage and 7.3221 mW from the pwm source. 4.5469 W is dissipated in the load. This gives an efficiency of 61%.

3.1.5 Does this efficiency agree with the calculated efficiency? If not why not? What is different between the calculations and the simulation?

The measured efficiency is so similar to the calculated efficiency of 65% that it leads me to suspect some error in the calculations. The total simulated inductor loss was 39.649 mW rather than the calculated 1.56 W. This could indicate an error in calculations.

3.1.6 Under what conditions does the converter enter discontinuous conduction mode?

When the duty cycle is too high, the switching frequency is too low, or the output current is too low.

4 Initial Converter Test Results

Table 4.4: Inductor Design, build and test

Quantity	Value	Comments
Target Inductance Value	72 µH	Minimum inductance as previously calculated plus safety factor
Required number of turns	9	$N = ceiling\left\{\sqrt{\frac{L}{A_L}}\right\}$
Measured Inductance	83.2252 µH	
Actual number of turns	10	
Measured resistance (low frequency)	0.019 37 Ω	
Measured resistance (switching frequency)	0.02 Ω	

4.1 Initial Converter Test Results (driven by signal generator)

The output voltage for a load of 10 Ω is given in fig. 3. The converter was also tested with loads of 4.7 Ω and 1 Ω. We were unable to provide enough current for the circuit to work with the 1 Ω load.

The output voltages were 5.12 V for the 10 Ω load (current 0.512 A) and 4.73 V for the 4.7 Ω load (current 1 A).

The power input to the circuit was measured for the 4.7 Ω max current load by noting the current drawn from the power supply. This gave $P_{in} = 6.5\,\text{W}$, giving an efficiency of 74%.

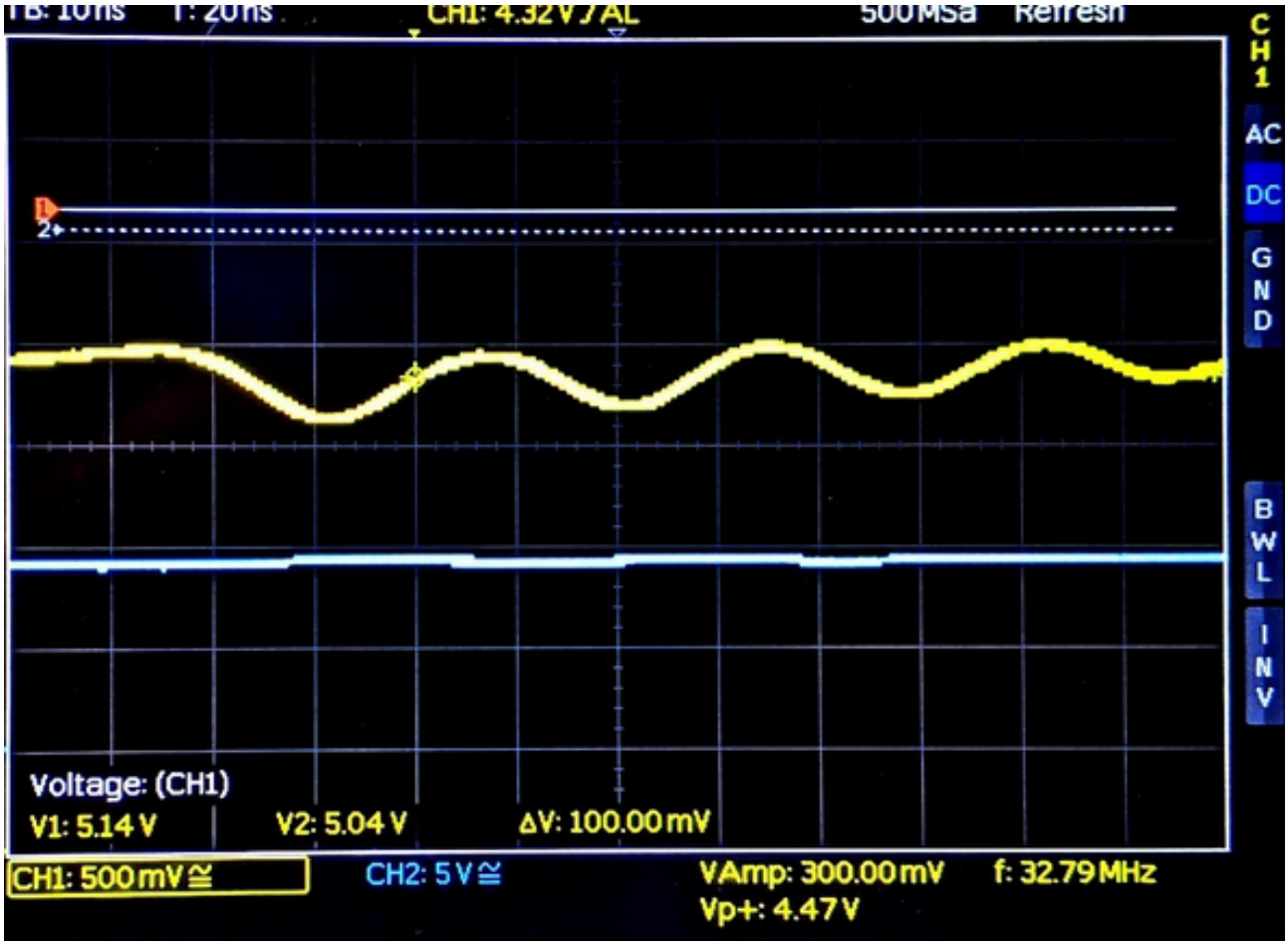

Figure 3: Converter output with ripple

4.1.1 How has the use of the signal generator (to drive the MOSFET) limited the tests which can be performed?

It can't emulate the power converter reacting to changes in the input voltage. It also can't vary the duty cycle, being fixed at 0.5.

4.1.2 Do the test results and the simulation results agree?

The following statements apply to the 4.7 Ω load circuit.

The efficiencies are different, with the physical circuit being 12 percentage points more efficient than the simulated circuit. I would have expected this to be the opposite, with the simulation being more efficient than reality. Perhaps the esrs are overestimated or the PMOS model is too lossy.

The simulated output voltage was 4.69 V whereas the tested voltage was measured at 4.73 V. These are rather close.

5 PWM Generation Design Results

Conditions: $+V_S = 0\,\text{V}$, $-V_S = 0\,\text{V}$, $V_{th-} = 0\,\text{V}$, $V_{th+} = 0\,\text{V}$		
Component	Equation	Value
R_2	eq. (1)	$8.2\,\text{k}\Omega$
R_1	eq. (1)	$2.2\,\text{k}\Omega$
R	eq. (2)	$560\,\Omega$
C	eq. (2)	$22\,\text{nF}$
$V_{ramp,p-p}$	$V_{ramp,p-p} < 4\,\text{V}$	$3.87\,\text{V}$
Reference voltage for required duty cycle		$1\,\text{V}$

The amplitude of the ramp voltage over the capacitor should be less than 4 Vp–p as the comparator has a limit to the input voltage it can withstand. This is achieved through selection of appropriate resistors in the voltage divider formed by R_1 and R_2.

$$V_{th} = 2\,\text{V} > \beta\,|V_{sat}| \qquad ,\beta = \frac{R_1}{R_1 + R_2}$$
$$\iff \frac{2}{|V_{sat}|} > \beta$$

Assuming the saturation voltage $|V_{sat}|$ of the op-amp is $\sim |V_s| - 1\,\text{V} = 9\,\text{V}$:

$$\frac{2}{9} \simeq 0.22 > \beta$$

To satisfy the above requirement, resistors were chosen as shown below. They were chosen of a magnitude such that the current through the voltage divider would be small; it is $\sim 190\,\mu\text{A}$ which is rather small compared to other currents in the circuit.

$$\beta = \frac{2.2\,\text{k}\Omega}{2.2\,\text{k}\Omega + 8.2\,\text{k}\Omega} \simeq 0.21 < 0.22 \tag{1}$$

Values for R and C derive from the following relation between the desired switching frequency, the RC time constant, and the voltage divider resistance ratio β. We chose a value for C first, of 22 nF, as there are less choices for capacitors available in the lab. The exact value of the capacitor was less important than it being the right magnitude not to require an inordinately large or small resistance.

$$f_s = \frac{1}{2RC\ln\left(\frac{1+\beta}{1-\beta}\right)} \tag{2}$$

6 PWM Circuit Simulation Results

Figure 4 gives the LTspice circuit for the PWM generator and fig. 5 gives its output and the ramp voltage over the capacitor.

The output voltage is not at the nominal frequency of 100kHz, but rather at 89.6 kHz.

V_C is 3.87 Vp–p, close to the design value and within the 4V limit.

6.1 PWM Generator Simulation Results

6.1.1 Explain the design basis for the choice of op-amp power supply voltages, +Vs and -Vs? What is the minimum value which could be used for these?

The op-amp power supply voltages must be large enough that the saturation voltage of the op-amp is enough to allow for the circuit to operate successfully. Given that we wanted to use the largest possible range of reference voltages, 4 Vp–p, the supply voltages would had have to have been greater than $\pm 2 + 1 = \pm 3V$. They would need to be greater than this however in order to use a resistive divider with reasonable resistances.

We chose 10 V because it was the nominal input voltage to the converter and having one input voltage level for the whole circuit would make supplying power much easier.

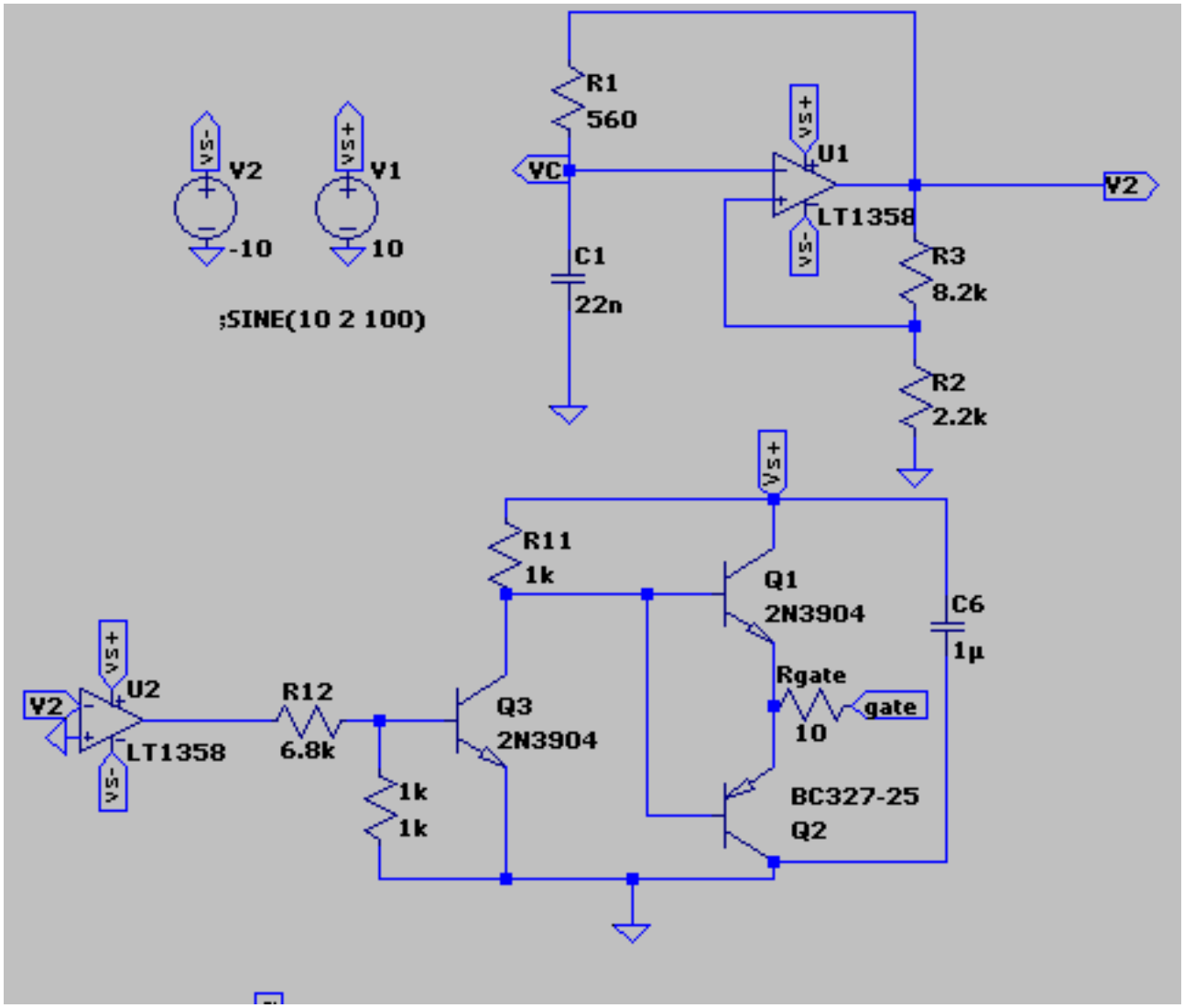

Figure 4: PWM Circuit

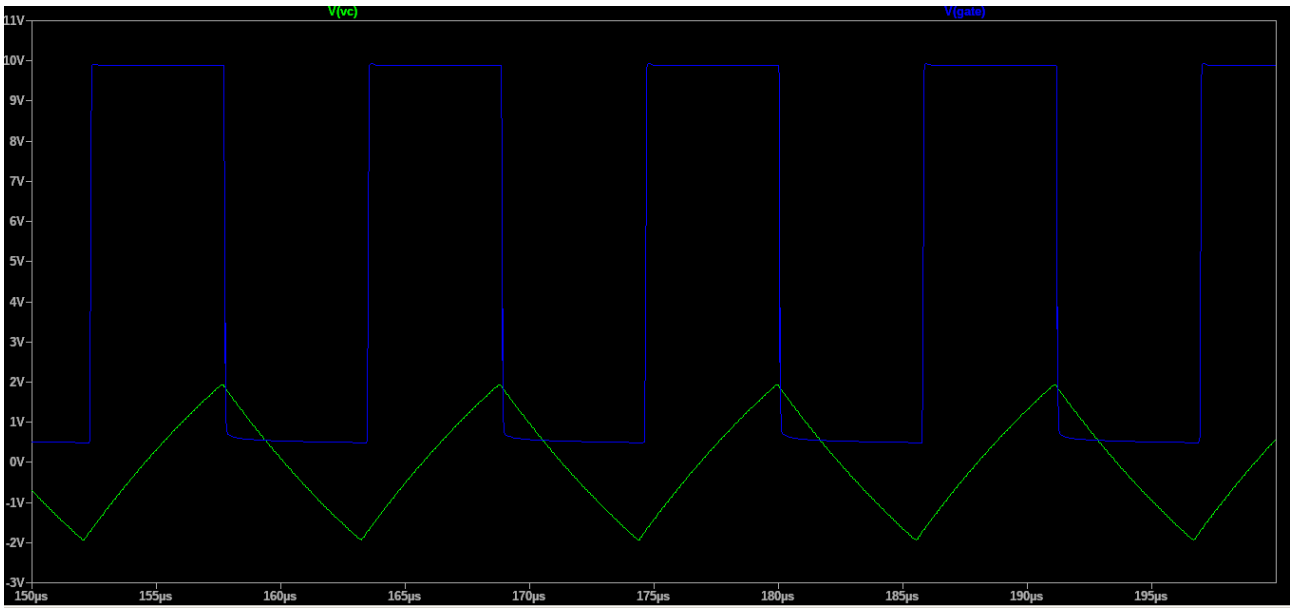

Figure 5: Output of PWM circuit

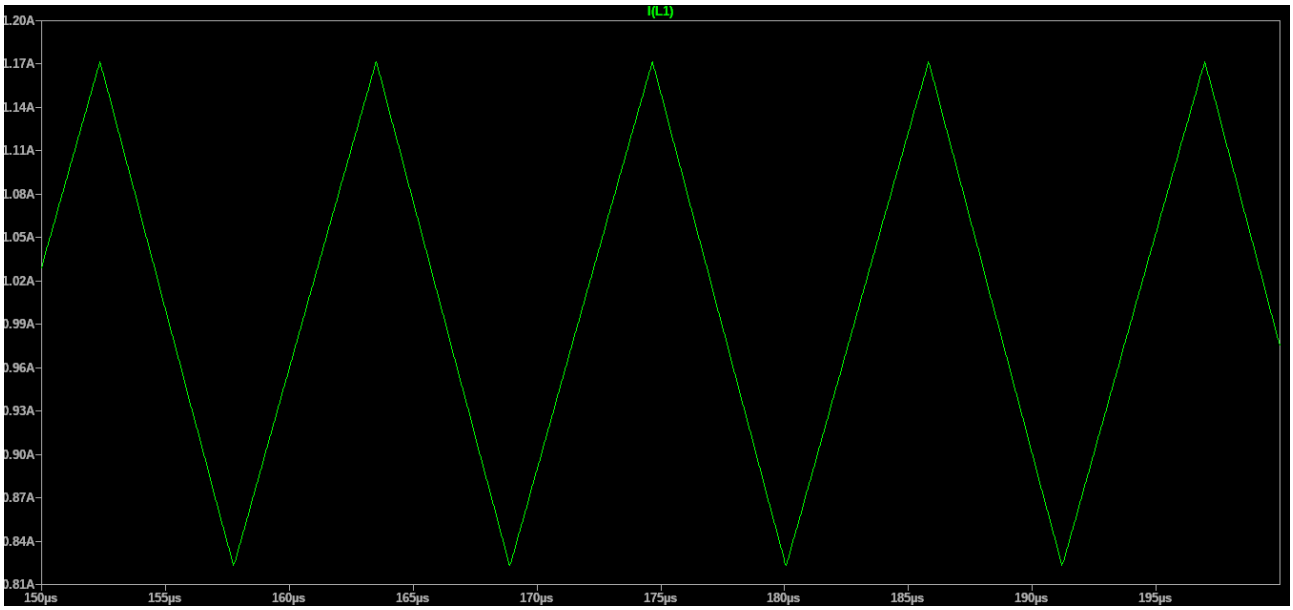

Figure 6: Inductor current

6.1.2 What is the power consumption of the PWM circuit? What is this power used for?

Table 6.5: Power Consumption

Component	Power Consumed W
PWM Power Supply	$-110.49 \times 10^{-3} + -171.74 \times 10^{-3} = -0.282\,23$
Converter Power Supply	-5.1519
Converter Output Voltage	4.6769

The power consumption of the PWM circuit is as given in table 6.5. This power is dissipated among the resistors, capacitors and MOSFETS, and is used to power the op amps.

6.1.3 What is the effect of the PWM circuit power consumption on the converter efficiency?

The power consumption of the PWM generator has a small impact on the overall efficiency. The total power supplied to the circuit is 0.282 23 W which will lower the overall converter efficiency: from 90.7% to 86.0%.

6.2 PWM Generator & Buck Converter Results

Figure 6 gives the inductor current and fig. 7 the output voltage and current for the combined circuit. The input voltage was 10V, the duty cycle was 0.5 and the load was 4.7 Ω.

The output voltage ripple is just over the specified value, 50.2 mV instead of 50 mV. The output current is 997.34 mA, nearly exactly the specified 1 A, and the output voltage is 4.6875 V.

6.2.1 What is the relationship between output voltage and reference voltage?

The output voltage and reference voltage appear to be related in a manner where the output voltage depends not only on the reference voltage but also on what direction the output voltage is travelling, similar to the current-voltage graph for a transformer.

6.2.2 Could the same PWM circuit be used to drive the converter at 10 times your design frequency? What might limit the maximum frequency of operation of this circuit?

The fall time of the circuit is ≈ 100 ns and the rise time is ≈ 90 ns. At a frequency of $f_s \times 10 = 1$ MHz, the rise and fall times of the circuit are about 10% the period of the converter. This would allow for only a reduced set of duty cycles if the RC product can be changed.

The maximum frequency of operation of this circuit could be limited by the slew rate of the op amps and the frequency at which the capacitors become inductive.

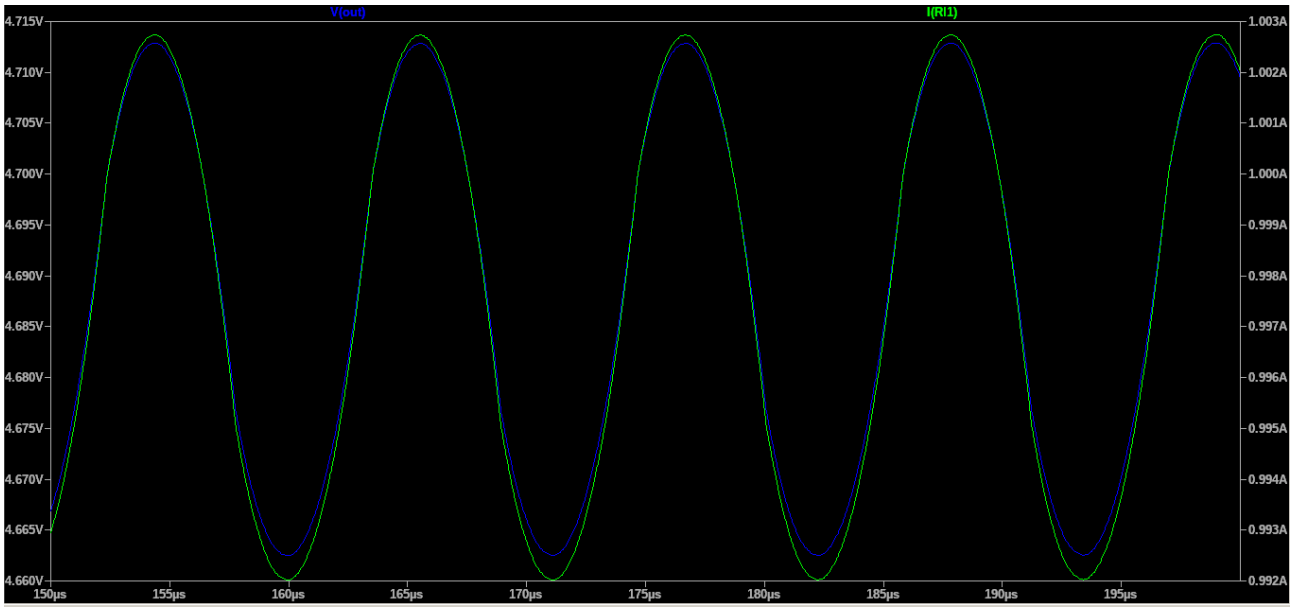

Figure 7: Output voltage and current for PWM and converter circuit

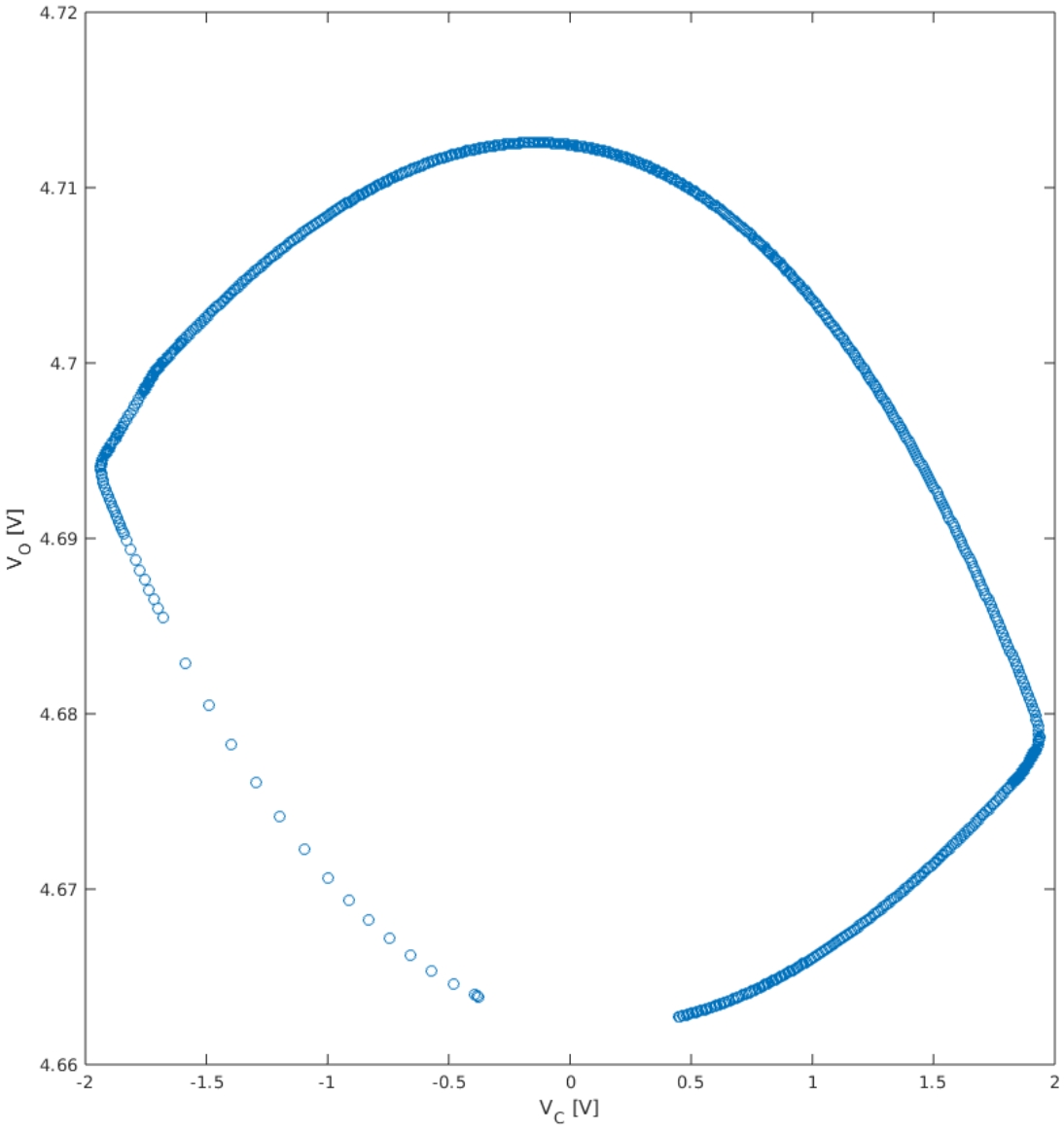

Figure 8: Graph of output voltage vs reference voltage for one switching cycle.

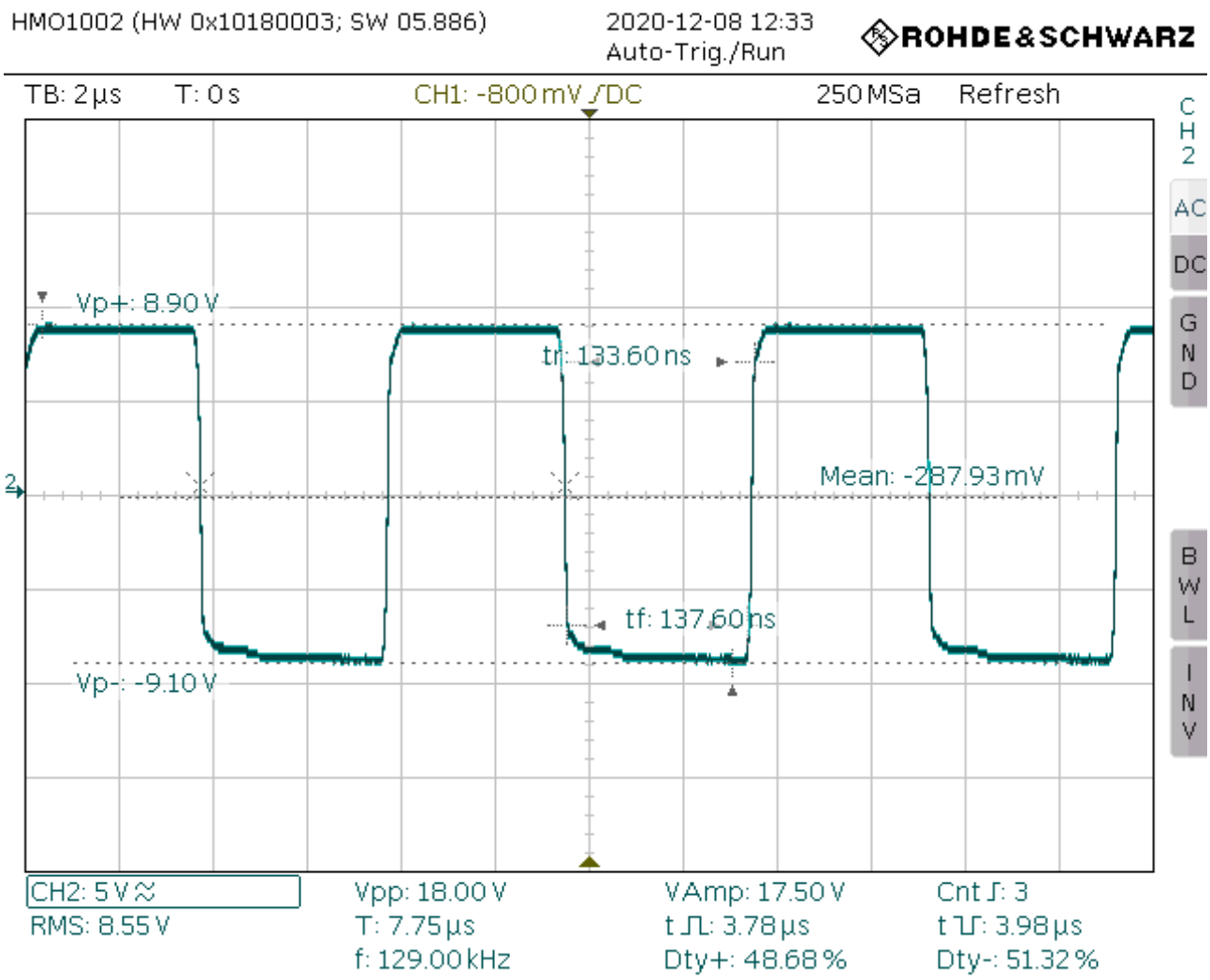

Figure 9: Output voltage of PWM circuit when disconnected from converter.

7 Test Results: PWM & Buck Converter

Figure 10 gives the converter and PWM output voltages or $R_L = 4.7\,\Omega$.

Figure 9 gives the PWM output voltage before connecting the two circuits. Note the lack of distortion.

7.1 Do the test results and the simulation results agree?

The switching frequency varied from 125 kHz to 135 kHz. It seemed to increase the longer we had the circuit on, possibly indicating some temperature dependency; this could also be due to one of us moving components on the breadboard and causing changes in capacitance. The initially high value for the switching frequency could be due to the choice of RC product initially. The simulation switching frequency was quite different, at 90 kHz, indicating that the fault might be elsewhere.

The output voltage was 4 V, four fifths of the specification. The simulated output voltage of 4.7 V is much closer to desired.

The large amount of distortion present in the converter output voltage could be caused by some feedback created when the two circuits were connected (fig. 9 shows the gate voltage before connection). This would have affected the reference input also, reducing the range of duty cycles available to the controller.

7.2 Provide a plot of converter output voltage vs. PWM reference voltage. Is this relationship as expected?

Figures 11 and 12 give the PWM and converter output voltages for the maximum and minimum duty cycles we achieved. There is not a great range of duty cycles due to distortion of the reference voltage. The duty cycle was adjusted by varying the reference voltage. This relationship is not what we had expected, we had expected a relatively linear relationship that would allow for a much wider range of duty cycles.

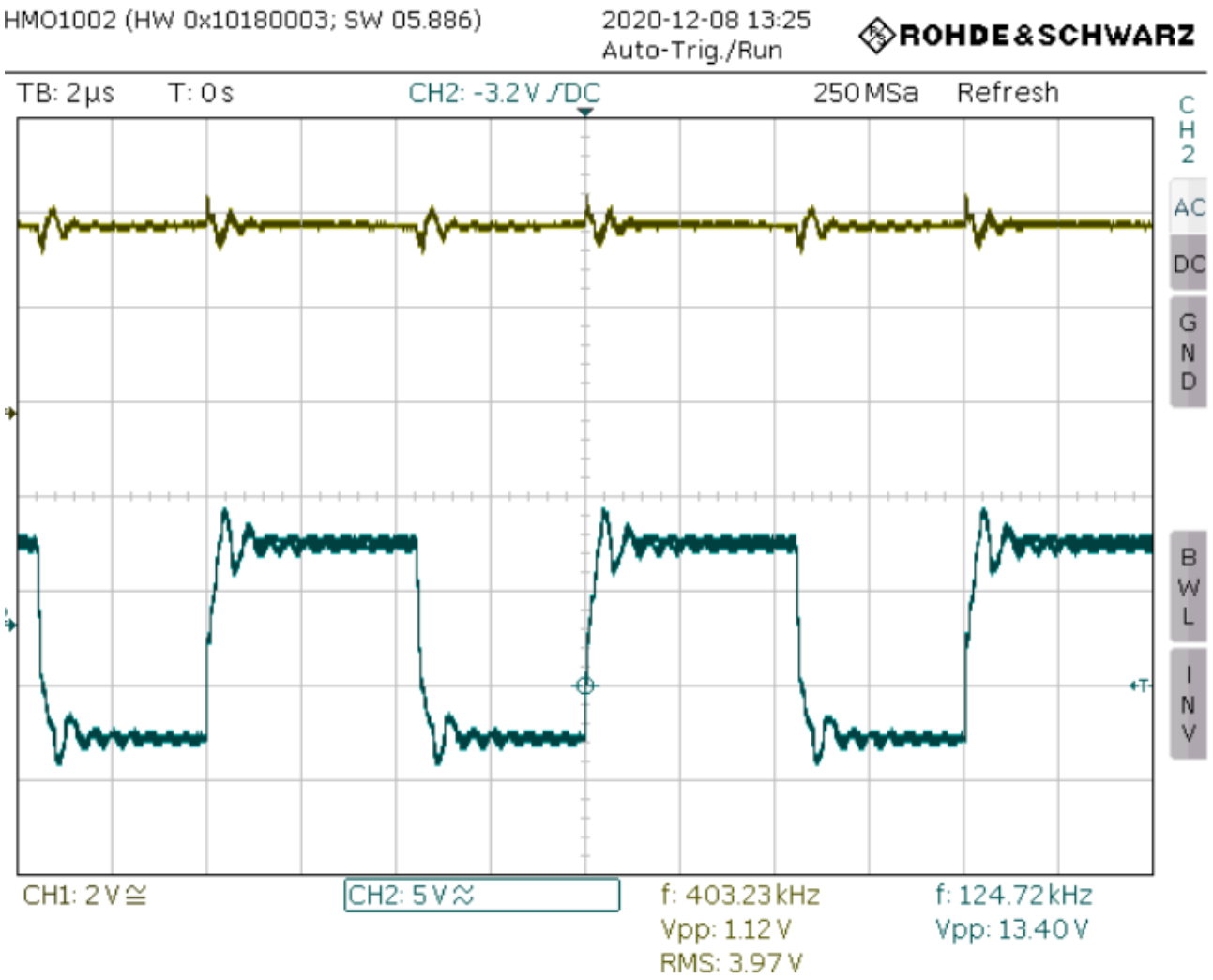

Figure 10: Converter output voltage (top) and PWM output voltage (bottom) for RL = 4.7 Ω.

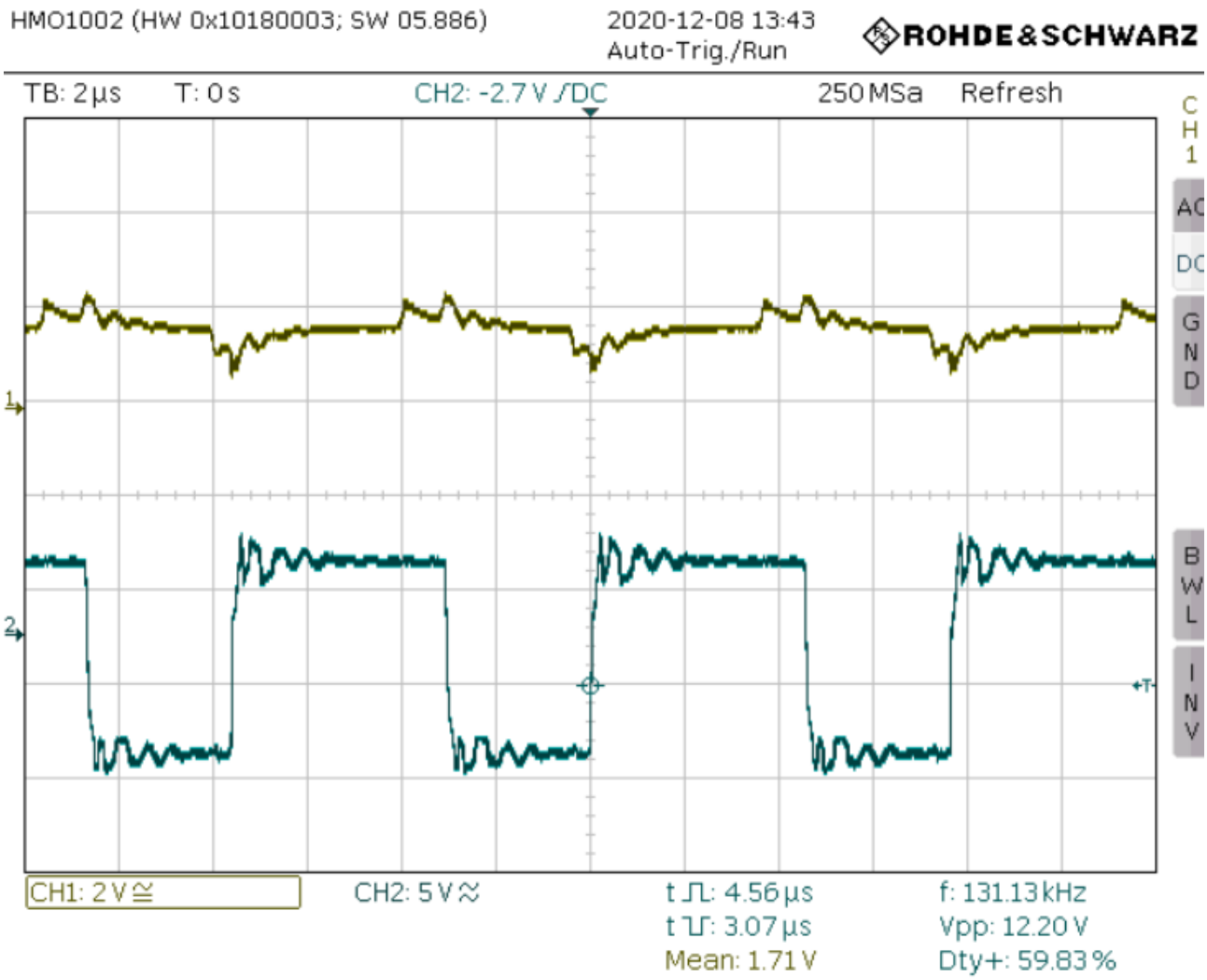

Figure 11: Maximum duty cycle

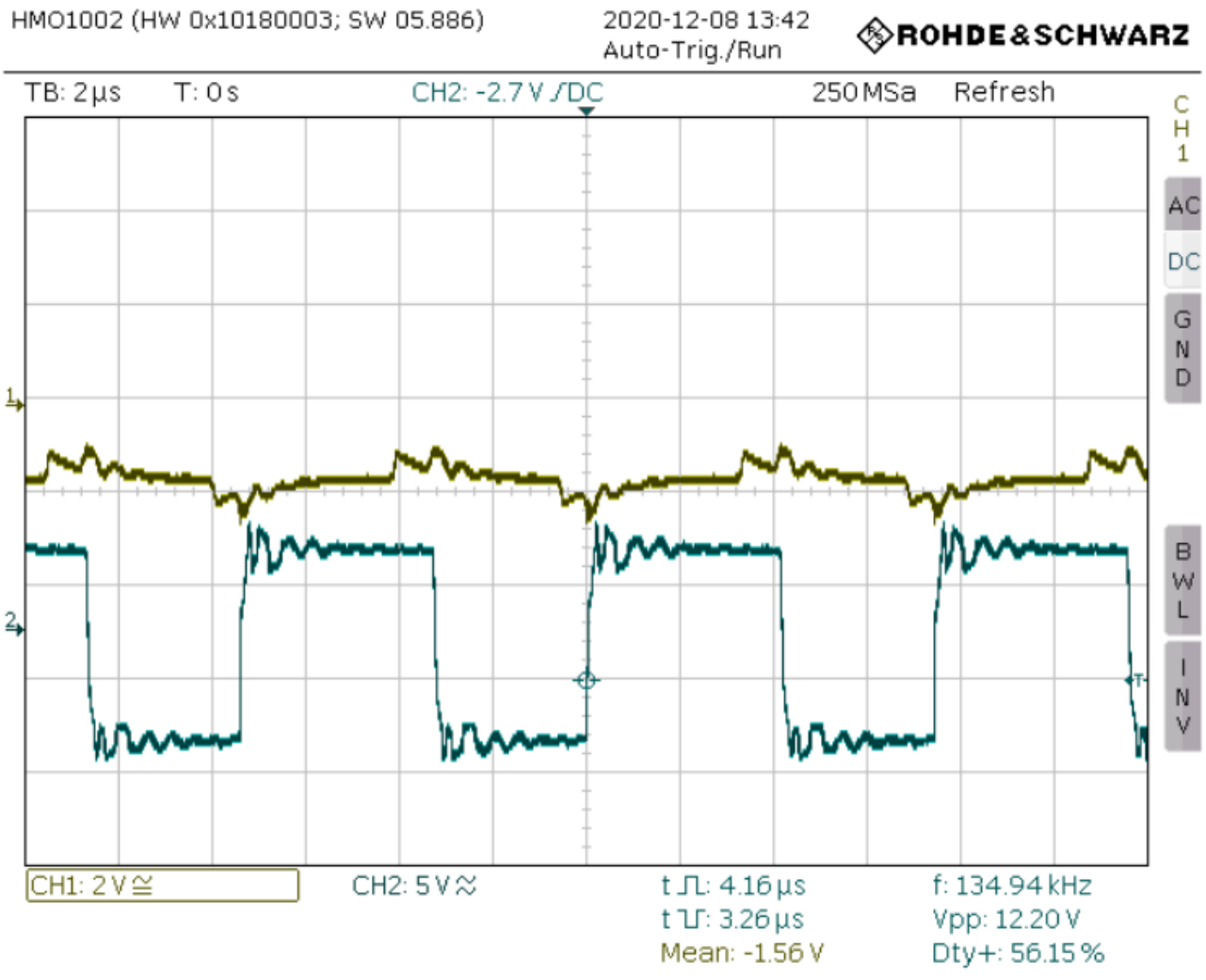

Figure 12: Minimum duty cycle

7.3 How does the measured efficiency compare with the simulated efficiency and calculated efficiency?

The efficiency of the circuit was calculated by measuring the current and voltage provided by the various supplies ($0.05\,\text{A} \cdot 10\,\text{V} + 0.05\,\text{A} \cdot 10\,\text{V} + 0.4\,\text{A} \cdot 10\,\text{V} = 5\,\text{W}$) and dividing the dissipated load power by it ($\frac{4^2}{4.7} = 3.4\,\text{W}$) giving an efficiency of 68%. This is somewhat less than the simulated value of 86%, but rather close to the calculated efficiency of 65%. Differences could be due to, among other factors, larger losses in the inductor due to the distortion.

8 Conclusions

In this lab we designed, simulated and built a buck converter and a PWM generator to operate the switch. At each stage of the process, errors appeared of varying magnitude, some of which were corrected, some of which were not.

I learned two things during this lab: firstly I learned that oscillations in an electrical circuit can produce an audible effect, which was cool, even though it sounded like something was about to explode; secondly I learned that sometimes one and one makes two but it's so distorted it looks like an eight.