UCD / College of Engineering and Architecture / Electronic Engineering /

Power Converter Design

Name: Tiarnach Ó Riada 16315466

I declare that all material in this assessment is my own work.

Signed By: Tiarnach Ó Riada **Date:** 9th December 2020

EEEN40310 Power Electronic Technology

Contents

1 Introduction

Table 1.1: Specifications

V_{in}	$10\,\mathrm{V} \pm 2\,\mathrm{V}$
V_out	$5\,\mathrm{V}$
I_{out}	$1\,\mathrm{A}$
$I_{out,min}$	$0.2\,\mathrm{A}$
$\Delta i_{L,max}$	$0.2I_{out} = 200\,\mathrm{mA}$
ΔV_{out}	$0.02V_{out} = 50\,\mathrm{mV}$

2 Converter Design Results

Table 2.2: Design Calculations

Quantity	Value	Assumptions and design comments
f_s	100 kHz	
L	83.2 µH	$L_{min} = \frac{V_{out}(1-D_{min})}{2f_s I_{out,min}} = 60\,\mu H$ where $D_{min} = \frac{V_{out}}{V_{in,max}\eta} = 0.5208 \because \eta = 0.8$. 83.2 µH is the inductance of the inductor built during the lab.
C	10 µF	$C_{min} = \frac{\Delta i_{L,max}}{8 f_s \Delta V_{out}}$

Table 2.3: Efficiency Calculations

Conditions: $V_{in} = 0\,V$, $V_{in} = 0\,V$, $I_{out} = 0\,A$, $P_{out} = 0\,W$		
Component or Loss	Loss Equation	Value [W]
Switch Conduction		
Switch Switching Loss		
Diode Conduction		
Diode Forward voltage loss		
Inductor conduction loss		
Capacitor conduction loss		
Efficiency		

3 Converter Simulation Results

In addition to presenting the simulation results include an answer to the following questions. In your report clearly indicate the question and the answer.

3.1 Questions

3.1.1 What is the minimum gate voltage that can be used to drive the high side switch?

3.1.2 What would be the implications for the required high side switch gate voltages of if a PMOS switch is used instead of an NMOS?

3.1.3 In terms of how well the design meets the specifications, do the design calculations and results from the simulation agree?

3.1.4 What is the efficiency of the converter determined from the LTSpice simulation?

3.1.5 Does this efficiency agree with the calculated efficiency? If not why not? What is different between the calculations and the simulation?

3.1.6 Under what conditions does the converter enter discontinuous conduction mode?

4 Initial Converter Test Results

4.1 Initial Converter Test Results (driven by signal generator)

4.1.1 How has the use of the signal generator (to drive the MOSFET) limited the tests which can be performed?

4.1.2 Do the test results and the simulation results agree?

Table 4.4: Inductor Design, build and test

Quantity	Value	Comments
Target Inductance Value	0 H	
Required number of turns	0	
Calculated Coil Resistance	0 Ω	
Measured Inductance	0 H	
Actual number of turns	0	
Measured resistance (low frequency)	0 Ω	
Measured resistance (switching frequency)	0 Ω	

5 PWM Generation Design Results

Conditions: $+V_S = 0\,\text{V}$, $-V_S = 0\,\text{V}$, $V_{th-} = 0\,\text{V}$, $V_{th+} = 0\,\text{V}$		
Component	Equation	Value
R_2	eq. (1)	$8.2\,\text{k}\Omega$
R_1	eq. (1)	$2.2\,\text{k}\Omega$
R	eq. (2)	$560\,\Omega$
C	eq. (2)	$22\,\text{nF}$
$V_{ramp,p-p}$	$V_{ramp,p-p} < 4\,\text{V}$	$3.87\,\text{V}$
Reference voltage for required duty cycle		$0\,\text{V}$

The amplitude of the ramp voltage over the capacitor should be less than 4 Vp–p as the comparator has a limit to the input voltage it can withstand. This is achieved through selection of appropriate resistors in the voltage divider formed by R_1 and R_2.

$$V_{th} = 2\,\text{V} > \beta\,|V_{sat}| \qquad ,\beta = \frac{R_1}{R_1 + R_2}$$
$$\iff \frac{2}{|V_{sat}|} > \beta$$

Assuming the saturation voltage $|V_{sat}|$ of the op-amp is $\sim |V_s| - 1\,\text{V} = 9\,\text{V}$:

$$\frac{2}{9} \simeq 0.22 > \beta$$

To satisfy the above requirement, resistors were chosen as shown below. They were chosen of a magnitude such that the current through the voltage divider would be small; it is $\sim 190\,\mu\text{A}$ which is rather small compared to other currents in the circuit.

$$\beta = \frac{2.2\,\text{k}\Omega}{2.2\,\text{k}\Omega + 8.2\,\text{k}\Omega} \simeq 0.21 < 0.22 \tag{1}$$

Values for R and C derive from the following relation between the desired switching frequency, the RC time constant, and the voltage divider resistance ratio β. We chose a value for C first, of 22 nF, as there are less choices for capacitors available in the lab. The exact value of the capacitor was less important than it being the right magnitude not to require an inordinately large or small resistance.

$$f_s = \frac{1}{2RC\ln\left(\frac{1+\beta}{1-\beta}\right)} \tag{2}$$

6 PWM Circuit Simulation Results

6.1 PWM Generator Simulation Results

6.1.1 Explain the design basis for the choice of op-amp power supply voltages, +Vs and -Vs? What is the minimum value which could be used for these?

6.1.2 What is the power consumption of the PWM circuit? What is this power used for?

Table 6.5: Power Consumption

Component	Power Consumed W
PWM Power Supply	$-110.49 \times 10^{-3} + -171.74 \times 10^{-3} = -0.282\,23$
Converter Power Supply	-5.0605
Converter Output Voltage	5.0701

The power consumption of the PWM circuit is as given in table 6.5

6.1.3 What is the effect of the PWM circuit power consumption on the converter efficiency?

6.2 PWM Generator & Buck Converter Results

6.2.1 What is the relationship between output voltage and reference voltage?

6.2.2 Could the same PWM circuit be used to drive the converter at 10 times your design frequency? What might limit the maximum frequency of operation of this circuit?

7 Test Results: PWM & Buck Converter

Include test results (e.g. oscilloscope traces) which show that the converter operates correctly and satisfies the specifications. The results from the tests should be compared to the simulation results. Note the earlier simulations results may have to be changed to match the actual test conditions.

In addition to presenting the test results include an answer to the following questions:

Do the test results and the simulation results agree? Comment on the results and especially any disagreement and the possible reasons for the disagreement.

Provide a plot of converter output voltage vs. PWM reference voltage. Is this relationship as expected? Comment and explain.

Measure the efficiency of the converter. How does the measured efficiency compare with the simulated efficiency and calculated efficiency? Comment and explain any differences.

8 Conclusions

For any technical report it is always good practice to provide a short conclusions section which might give a brief summary, and mention what have you learned.