UCD / College of Engineering and Architecture / Electronic Engineering /

Power Converter Design

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I declare that all material in this assessment is my own work.
Signed By: Tiarnach Ó Riada **Date:** 9th December 2020

EEEN40310 Power Electronic Technology

Contents

1 Introduction

Table 1.1: Specifications

V_{in}	$10\,\mathrm{V} \pm 2\,\mathrm{V}$
V_out	$5\,\mathrm{V}$
I_{out}	$1\,\mathrm{A}$
$I_{out,min}$	$0.2\,\mathrm{A}$
$\Delta i_{L,max}$	$0.2 I_{out} = 200\,\mathrm{mA}$
ΔV_{out}	$0.02 V_{out} = 50\,\mathrm{mV}$

2 PWM Generation Design Results

Conditions: $+V_S = 0\,\text{V}$, $-V_S = 0\,\text{V}$, $V_{th-} = 0\,\text{V}$, $V_{th+} = 0\,\text{V}$		
Component	Equation	Value
R_2	eq. (1)	$8.2\,\text{k}\Omega$
R_1	eq. (1)	$2.2\,\text{k}\Omega$
R	eq. (2)	$560\,\Omega$
C	eq. (2)	$22\,\text{nF}$
$V_{ramp,p-p}$	$V_{ramp,p-p} < 4\,\text{V}$	$3.87\,\text{V}$
Reference voltage for required duty cycle		$0\,\text{V}$

The amplitude of the ramp voltage over the capacitor should be less than 4 Vp–p as the comparator has a limit to the input voltage it can withstand. This is achieved through selection of appropriate resistors in the voltage divider formed by R_1 and R_2.

$$V_{th} = 2\,\text{V} > \beta\,|V_{sat}| \qquad ,\beta = \frac{R_1}{R_1 + R_2}$$
$$\iff \frac{2}{|V_{sat}|} > \beta$$

Assuming the saturation voltage $|V_{sat}|$ of the op-amp is $\sim |V_s| - 1\,\text{V}$:

$$\frac{2}{9} \simeq 0.22 > \beta$$

To satisfy the above requirement, resistors were chosen as shown below. They were chosen of a magnitude such that the current through the voltage divider would be small; it is $\sim 190\,\mu\text{A}$ which is rather small compared to other currents in the circuit.

$$\beta = \frac{2.2\,\text{k}\Omega}{2.2\,\text{k}\Omega + 8.2\,\text{k}\Omega} \simeq 0.21 < 0.22 \tag{1}$$

Values for R and C derive from the following relation between the desired switching frequency, the RC time constant, and the voltage divider resistance ratio β. We chose a value for C first, of 22 nF, as there are less choices for capacitors available in the lab. The exact value of the capacitor was less important than it being the right magnitude not to require an inordinately large or small resistance.

$$f_s = \frac{1}{2RC \ln\left(\frac{1+\beta}{1-\beta}\right)} \tag{2}$$

3 PWM Circuit Simulation Results

3.1 PWM Generator Simulation Results

3.1.1 Explain the design basis for the choice of op-amp power supply voltages, +Vs and -Vs? What is the minimum value which could be used for these?

3.1.2 What is the power consumption of the PWM circuit? What is this power used for?

3.1.3 What is the effect of the PWM circuit power consumption on the converter efficiency?

3.2 PWM Generator & Buck Converter Results

3.2.1 What is the relationship between output voltage and reference voltage?

3.2.2 Could the same PWM circuit be used to drive the converter at 10 times your design frequency? What might limit the maximum frequency of operation of this circuit?

4 Test Results: PWM & Buck Converter

Include test results (e.g. oscilloscope traces) which show that the converter operates correctly and satisfies the specifications. The results from the tests should be compared to the simulation results. Note the earlier simulations results may have to be changed to match the actual test conditions.

In addition to presenting the test results include an answer to the following questions:

Do the test results and the simulation results agree? Comment on the results and especially any disagreement and the possible reasons for the disagreement.

Provide a plot of converter output voltage vs. PWM reference voltage. Is this relationship as expected? Comment and explain.

Measure the efficiency of the converter. How does the measured efficiency compare with the simulated efficiency and calculated efficiency? Comment and explain any differences.

5 Conclusions

For any technical report it is always good practice to provide a short conclusions section which might give a brief summary, and mention what have you learned.