

Technical Session 3

The CLEARSY Safety Platform

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11th March 2025



Engineering and
Physical Sciences
Research Council

Agenda

- ▶ Introduction to proven software
 - ▶ Introduction to the CLEARY Safety Platform
- }
- Context
-
- ▶ Development process
 - ▶ Bits of B
- Architecture
-
- ▶ Using the modelling interface
- Some syntax elements to refer to
during exercises
- The different steps to use it

Introduction to Proven Software

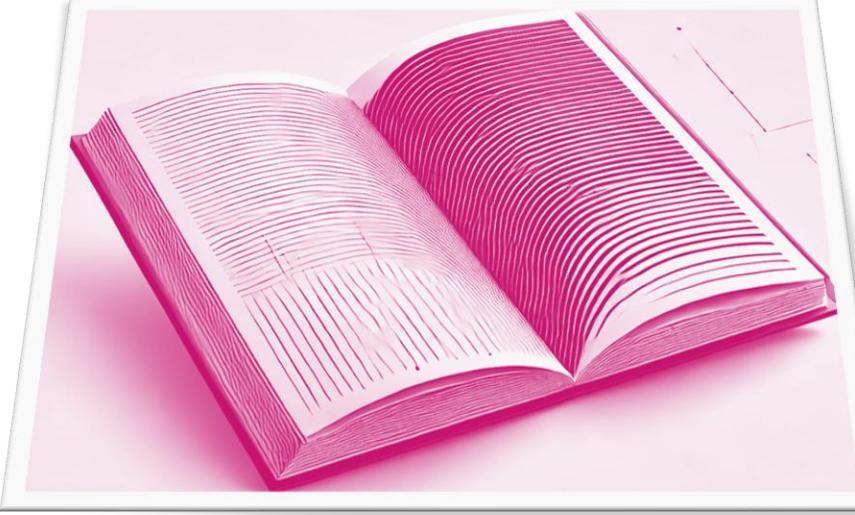


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Introduction to proven software: code manually produced and tested

requirements



code

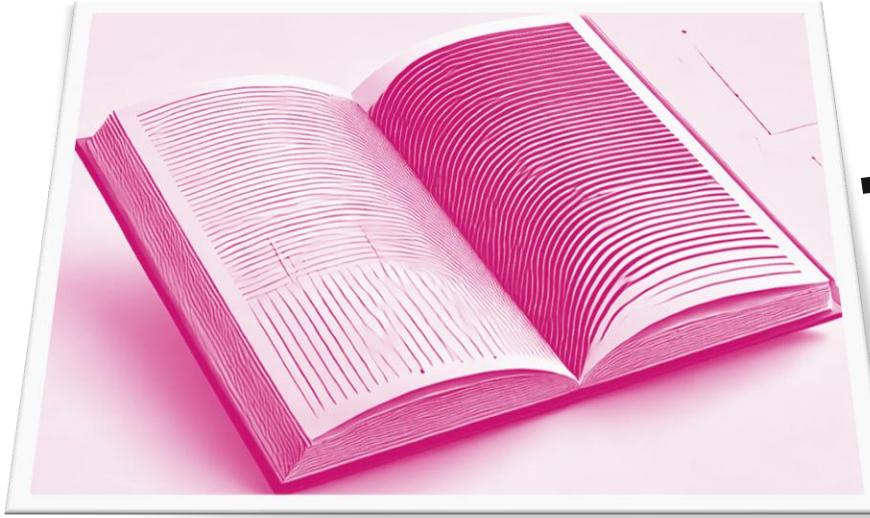


tests



Introduction to proven software: code manually produced and **formally verified**

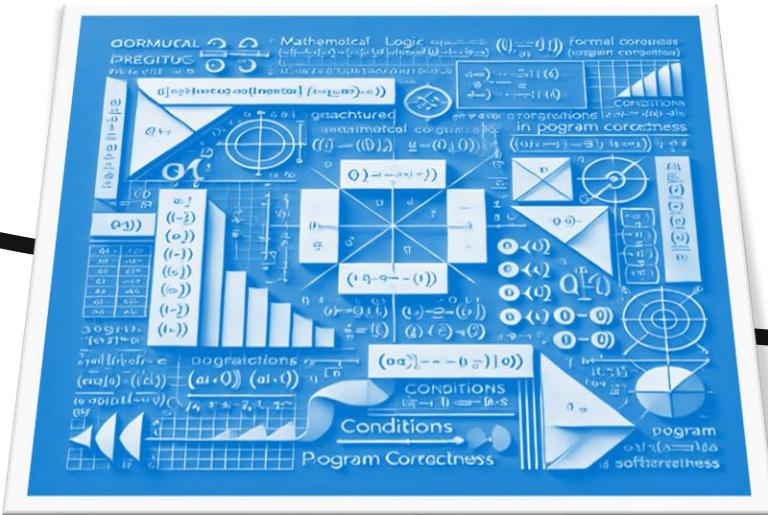
requirements



code

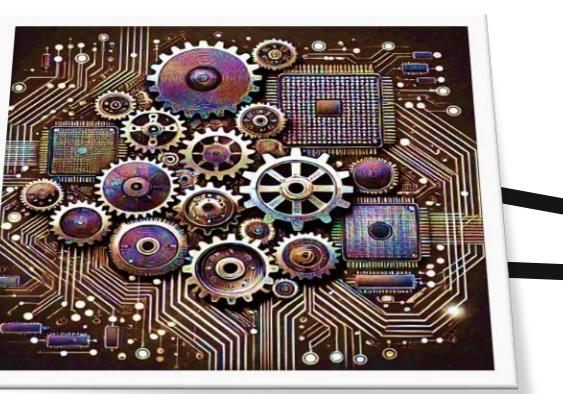


assertions

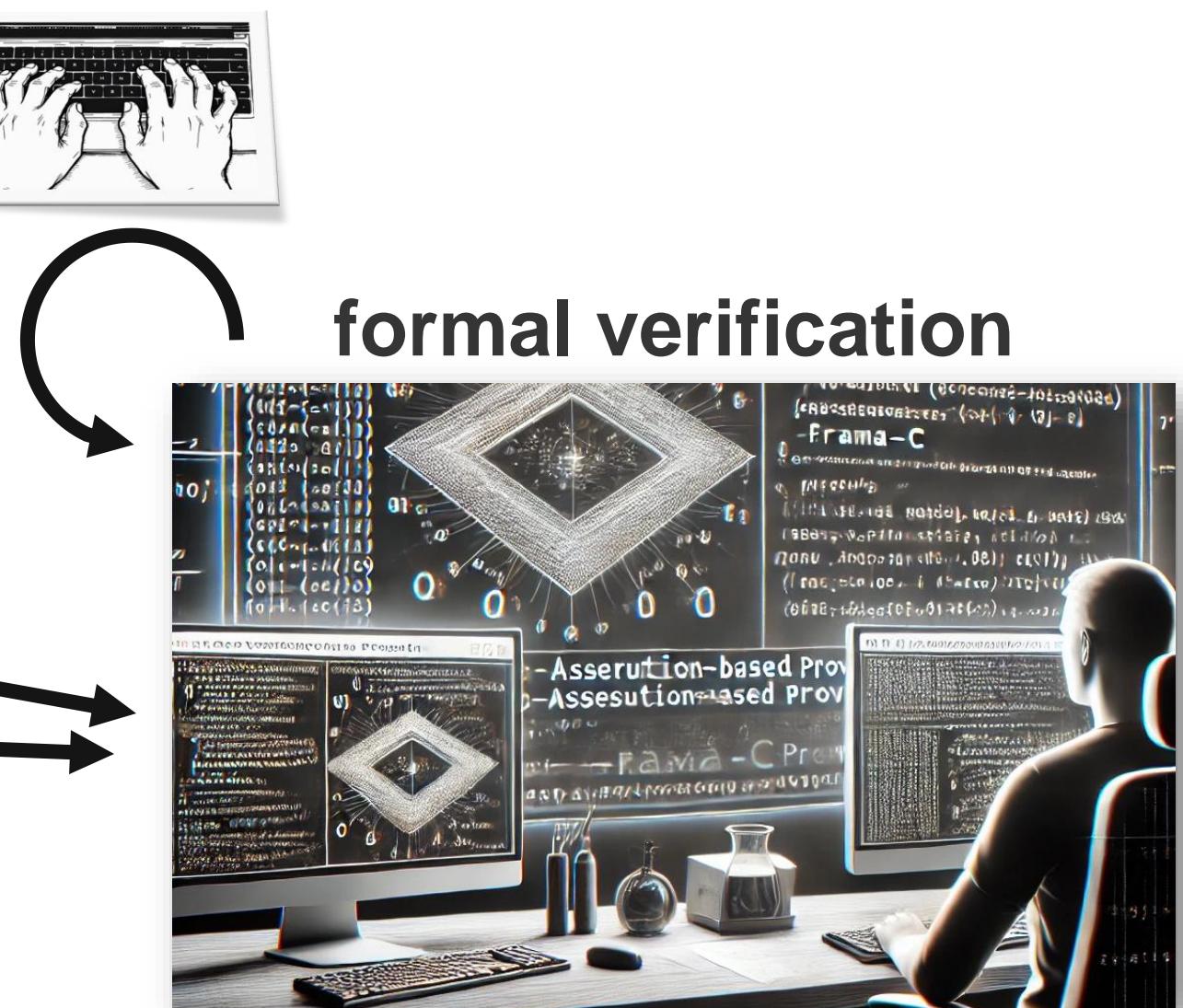


Assertions are mathematical predicates
for hypotheses and properties to verify

verifier

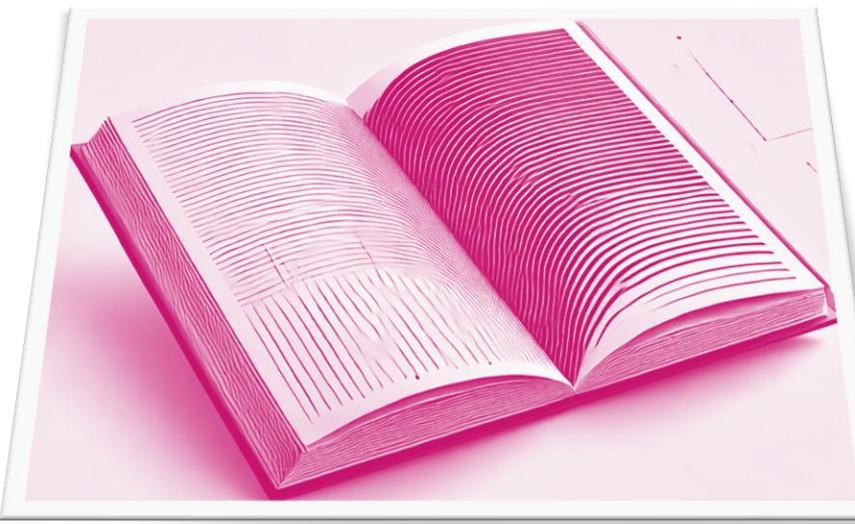


formal verification



Introduction to proven software: code formally specified and verified

requirements



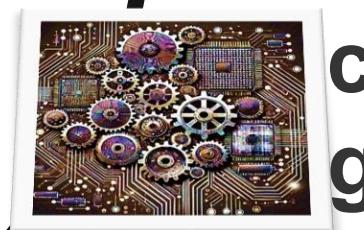
code



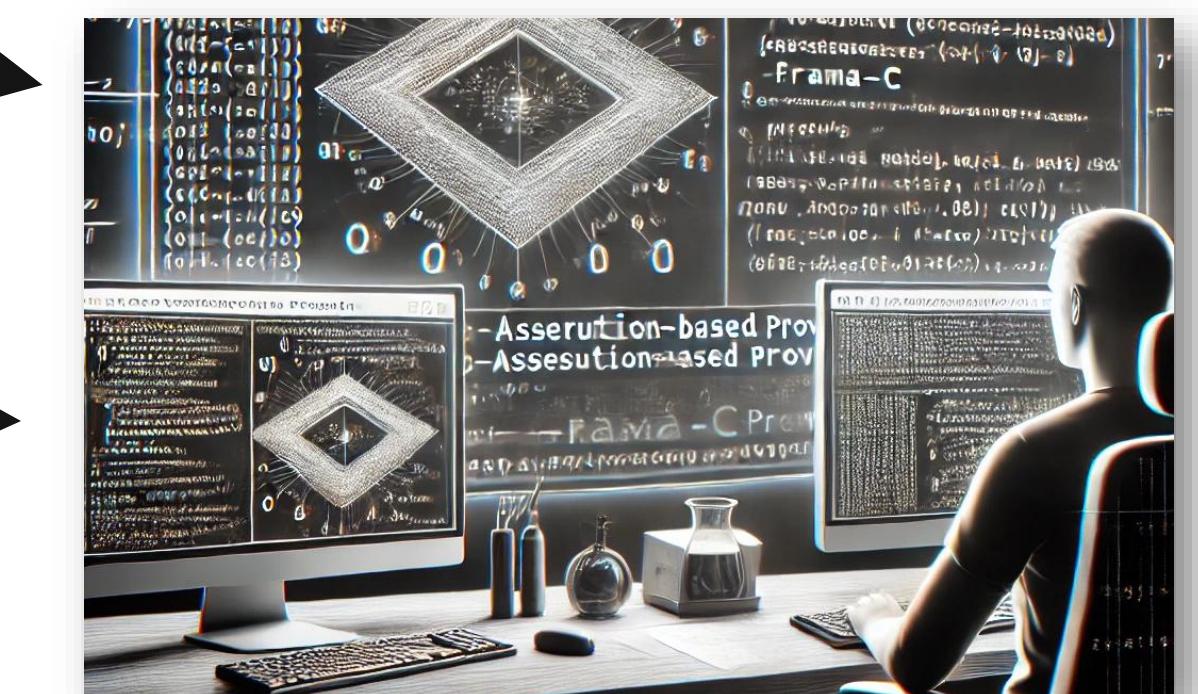
formal model



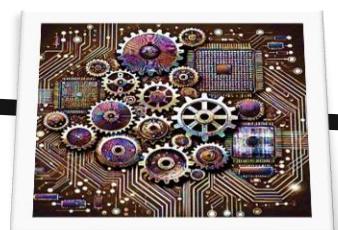
code generator



formal proof



prover



Formal model use mathematical notation
to specify and implement behaviour

Introduction to proven software: formal proof

Requirement

V1 is a variable of type Integer

Its initial value is 0

The function *increment* adds one to *V1*

Specification

```
MACHINE M0  
VARIABLES V1  
INVARIANT v1: NATURAL  
INITIALISATION V1 := 0  
OPERATIONS increment =  
BEGIN V1 := V1 + 1  
END  
END
```

•SPECIFICATION

•TYPING
NATURAL = INFINITE SET

•ASSIGNMENT

Introduction to proven software: formal proof

WHAT DO WE PROVE ?

PROOF STATUS

GREEN= ALL PROVED

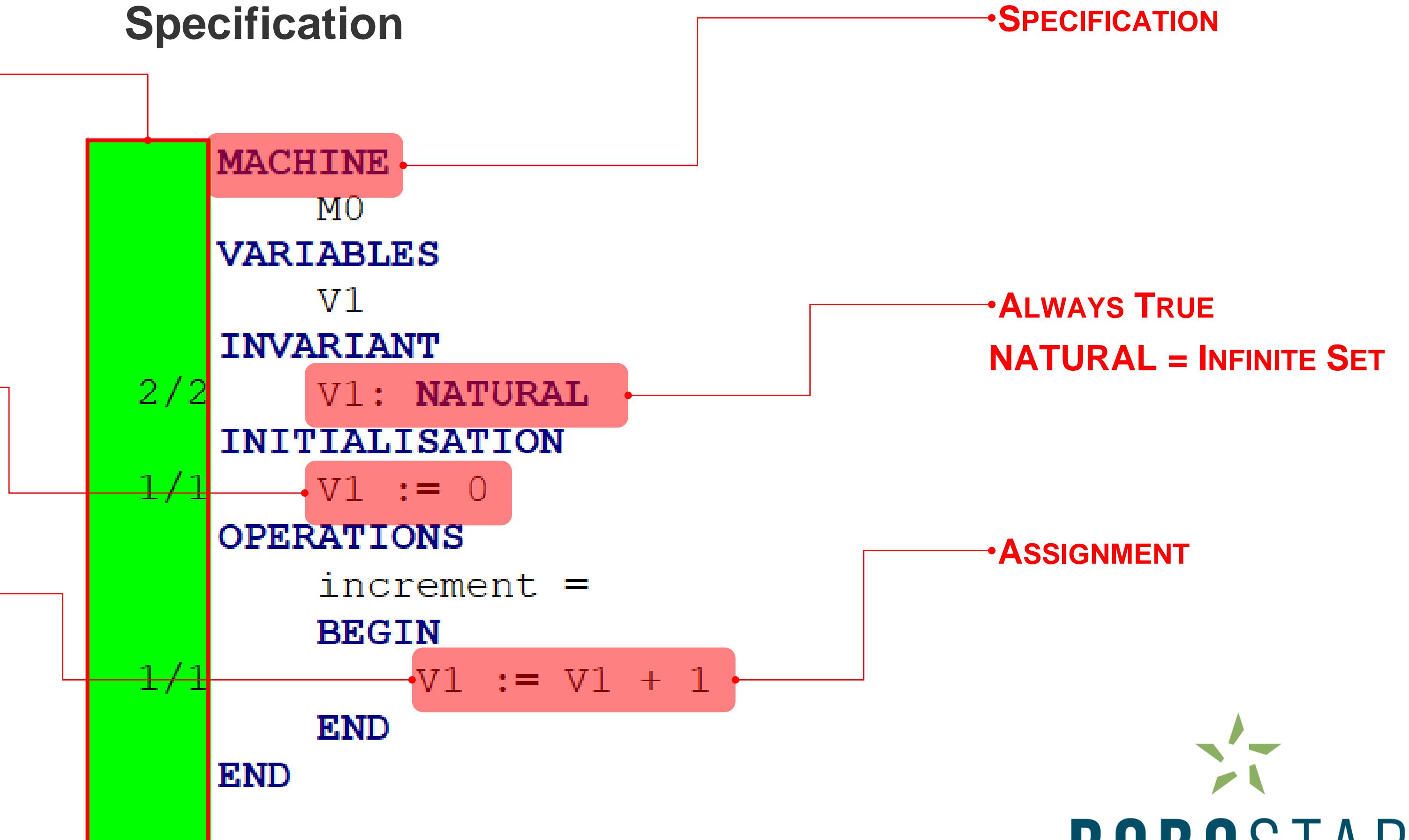
Invariant established

✓ IS 0 : NATURAL TRUE ?

Invariant preserved

✓ IF V1 : NATURAL THEN
IS V1 +1 : NATURAL ?

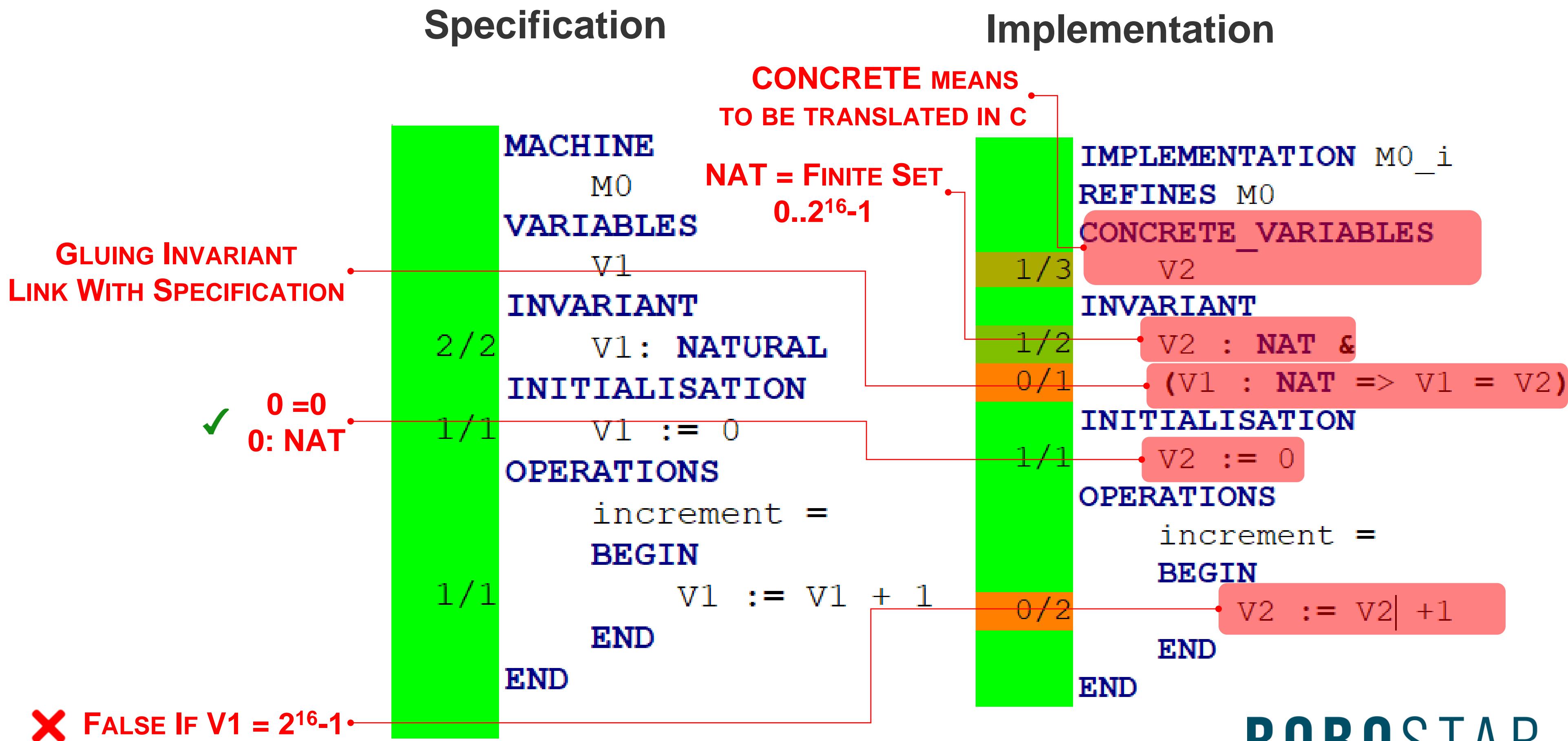
Specification



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Introduction to proven software: formal proof



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Implementation

IF GREEN, NO TESTING REQUIRED

PROOF STATUS
NOT GREEN = NOT PROVED AUTOMATICALLY.
EITHER WRONG OR NOT PROVABLE BY THE TOOL

```
IMPLEMENTATION M0_i
REFINES M0
CONCRETE_VARIABLES
    V2
INVARIANT
    V2 : NAT &
    (V1 : NAT => V1 = V2)
INITIALISATION
    V2 := 0
OPERATIONS
    increment =
BEGIN
    V2 := V2 + 1
END
```

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Introduction to proven software: formal proof

```
#include "M0.h"

/* Clause CONCRETE_CONSTANTS */
/* Basic constants */

/* Array and record constants */
/* Clause CONCRETE_VARIABLES */

static int32_t M0_V2;
/* Clause INITIALISATION */
void M0_INITIALISATION(void)
{
    M0_V2 = 0;
}

/* Clause OPERATIONS */

void M0_increment(void)
{
    M0_V2 = M0_V2+1;
}
```

CODE GENERATED

Implementation

IMPLEMENTATION M0_i
REFINES M0
CONCRETE_VARIABLES

1/3 V2

INARIANT

1/2 V2 : NAT &

0/1 (V1 : NAT => V1 = V2)

INITIALISATION

1/1 V2 := 0

OPERATIONS

increment =

BEGIN

0/2 V2 := V2 + 1

END

END

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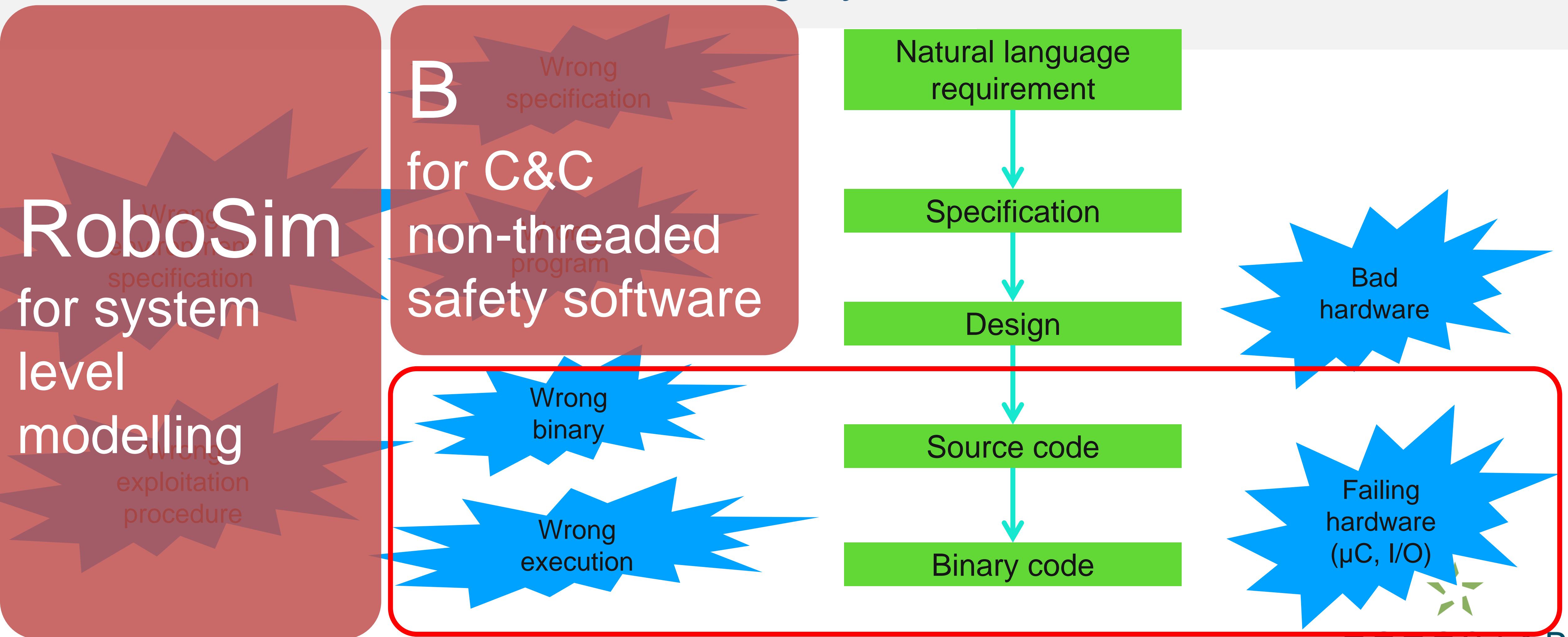
Introduction to the **CLEARSY Safety Platform**



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Formal Methods to Handle Failing Systems



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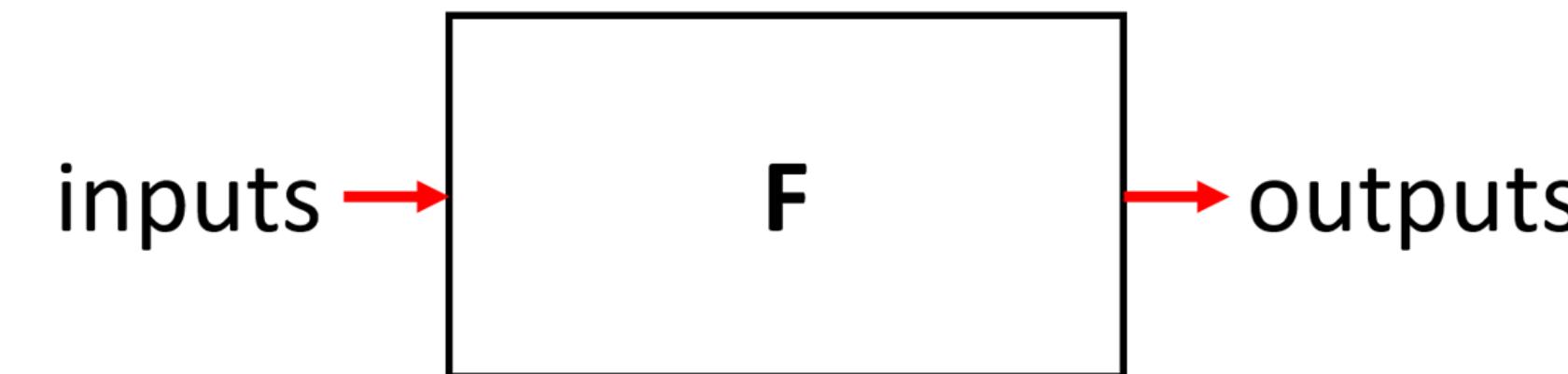
Introduction to the CLEARSY Safety Platform

Summary of
<https://youtu.be/A8uemvcclcU>

What a Safety Computer is

Safety computer

- $F == (\text{read inputs}, \text{compute}, \text{set outputs})^*$
- F could harm / kill people
- Ability to check if able to execute F properly



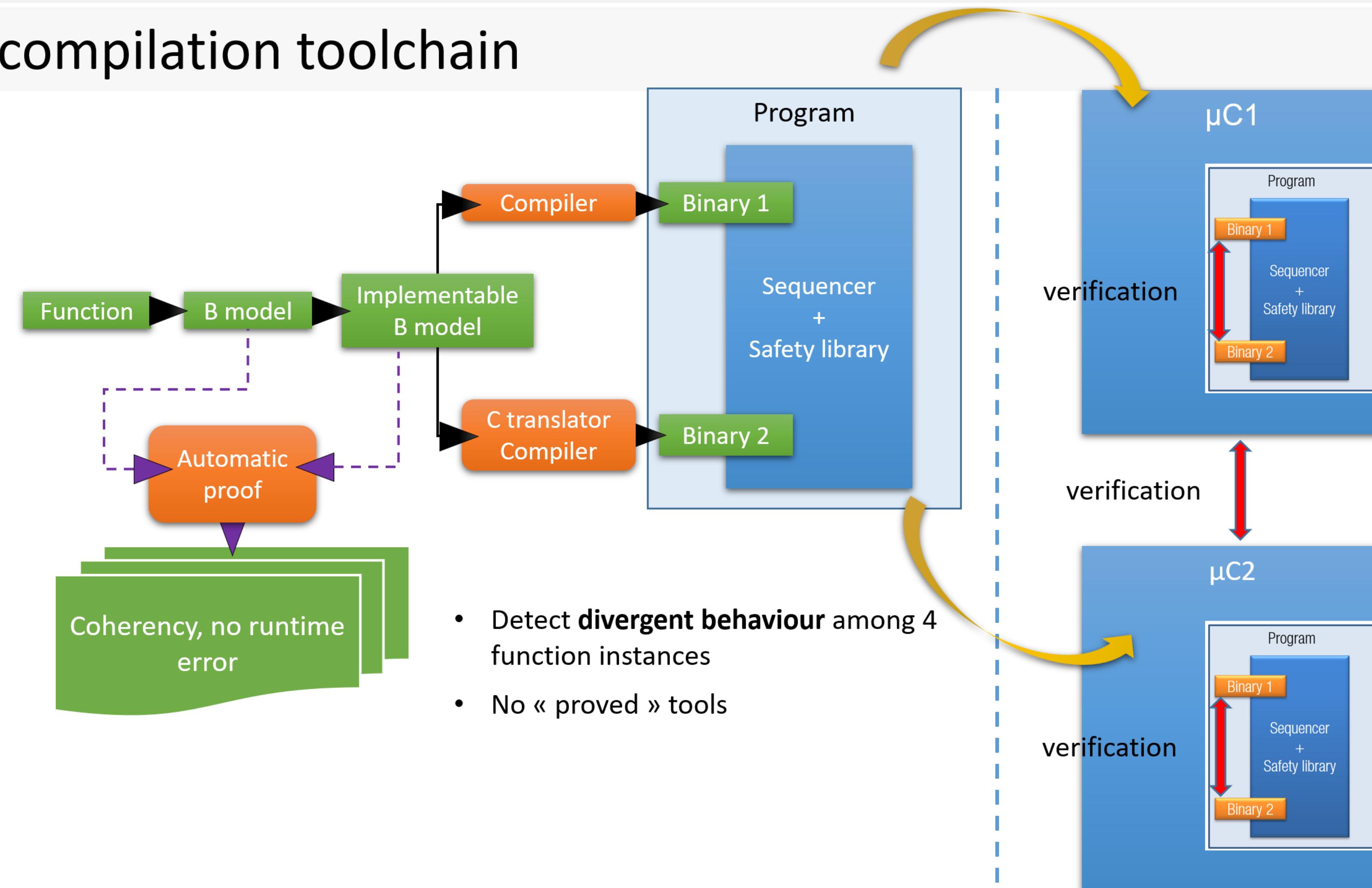
- F is not safe just because a safety computer is used
« execute the right F and execute the F right »

*: for space applications, could be a reset when computer hit by high energy particle

Introduction to the CLEARY Safety Platform

Summary of
<https://youtu.be/A8uemvcclcU>

Double compilation toolchain



Introduction to the CLEARSY Safety Platform

Summary of
<https://youtu.be/A8uemvcclcU>

Verification

- Starter kits for education:
 - Programmed with B
 - SK0 available since Q1 2019: 5 digital I/O
 - SK0 software simulator (no safety)



Handle failures:

- **Systematic** (buggy code generator and compiler, etc.)
- **Random** (memory corruption, failing transistor, degrading clock, etc.)

Safety is built-in, out of reach of the developer who cannot alter it

Introduction to the CLEARSY Safety Platform

Summary of
<https://youtu.be/A8uemvcclcU>

Summary

- CLEARSY Safety Platform
 - Safety computer
 - Execute 4 instances of the same function on 2 processors
 - Verify health regularly
 - Stop application execution and deactivate outputs if problem
 - IDE
 - Application developed with B formal language
 - Model mathematically proved



CLEARSY Safety Platform Programming Model

- ▶ The execution is cyclic
- ▶ The function is executed regularly as often as possible similar to arduino programming (`setup()`, `loop()`)
- ▶ No underlying operating system
- ▶ No `interrupt()`
- ▶ No predefined cycle time (if outputs are not set and cross read every **50ms**, board enters panic mode)
- ▶ No `delay()`
- ▶ Inputs are values captured at the beginning of a cycle (digital I/O)
- ▶ Outputs are maintained from one cycle to another (digital I/O)
- ▶ Project skeleton is generated from board description (I/O used, naming)
- ▶ Programming is specifying and implementing the function *user_logic*

```
init();  
while (1) {  
    instance1();  
    instance2();  
}
```



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CLEARSY Safety Platform Applications (Industrial Version)

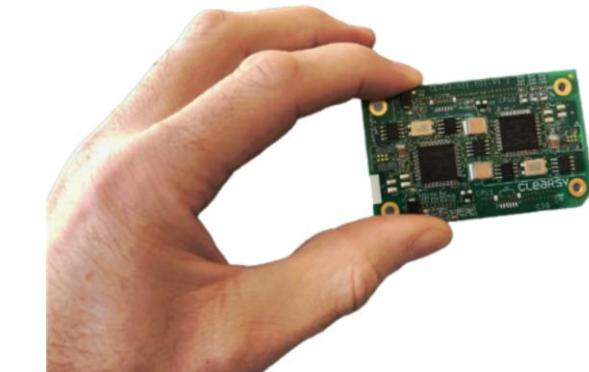
Platform Screen Doors Controller



São Paulo, Monorail line 15
Stockholm, City Line
Brisbane, Cross River Rail



SIL4 Certified



Design examination type certificate
Certificat de type par examen de la conception

N° 9594/0262 edition 2

Attributed to

Délivré à

CLEARSY

320 Av. Archimède - Pléiades III
F-13100 Aix-en-Provence

by

par

CERTIFER SA
18 Rue Edmond Membrey
F-59300 VALENCIENNES

Which certifies that the design of the following product:
Qui certifie que la conception du produit suivant :

GENERIC PRODUCT

CLEARSY SAFETY PLATFORM

BASELINE 1.0.2

Meets SIL4 requirements of the standards

Est conforme aux exigences SIL4 des normes

CENELEC EN 50126:2017, EN 50129:2018, EN 50128:2011

Autonomous Train Localization



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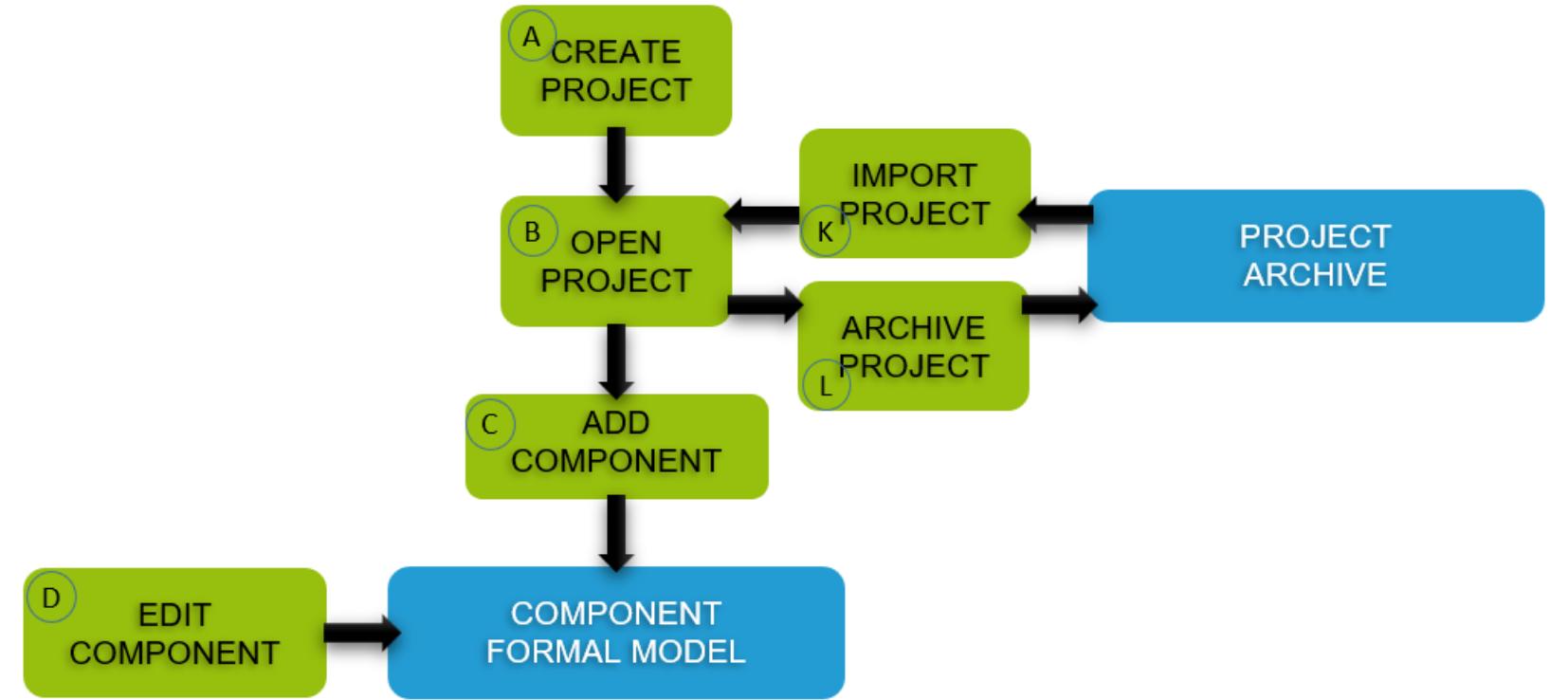
Development Process



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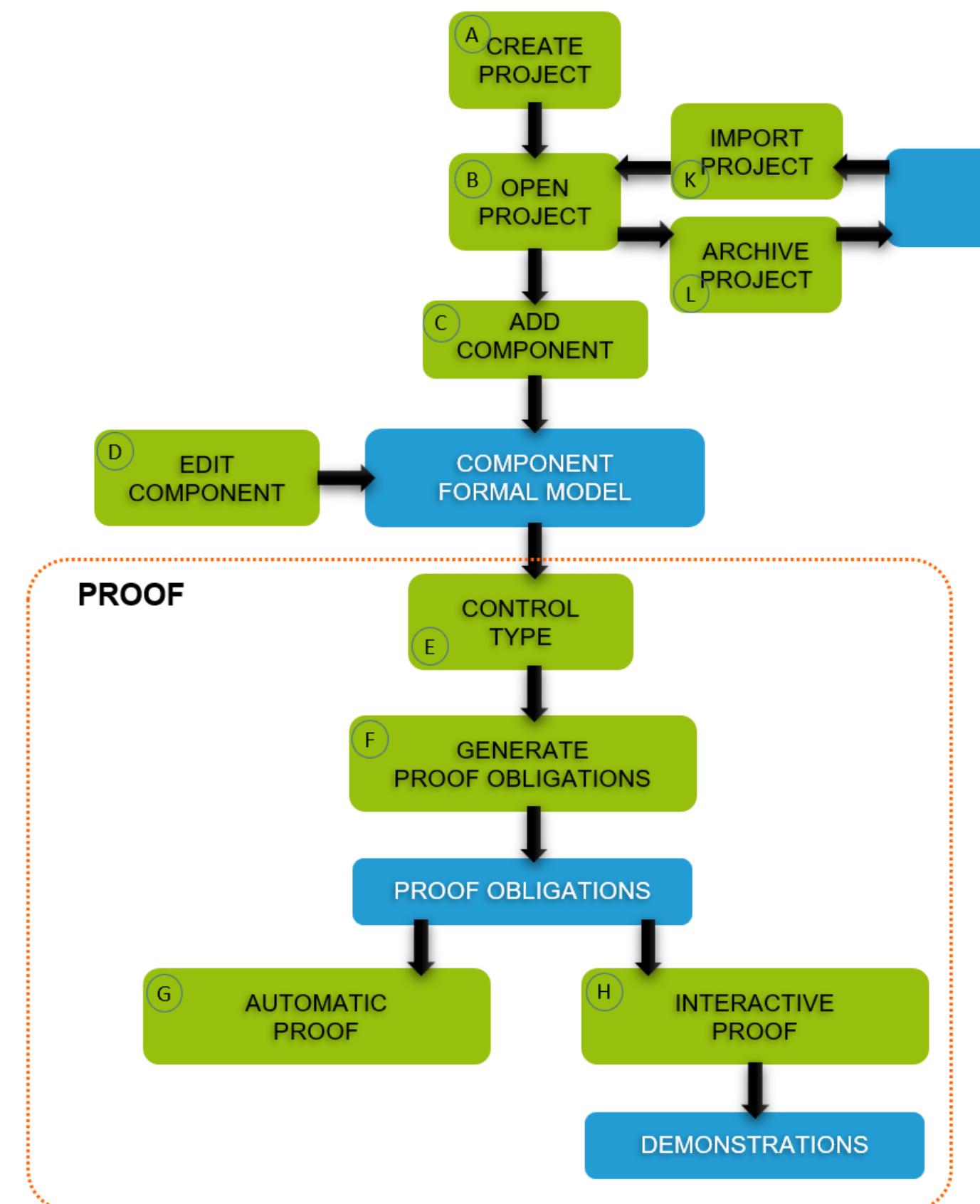
Development process



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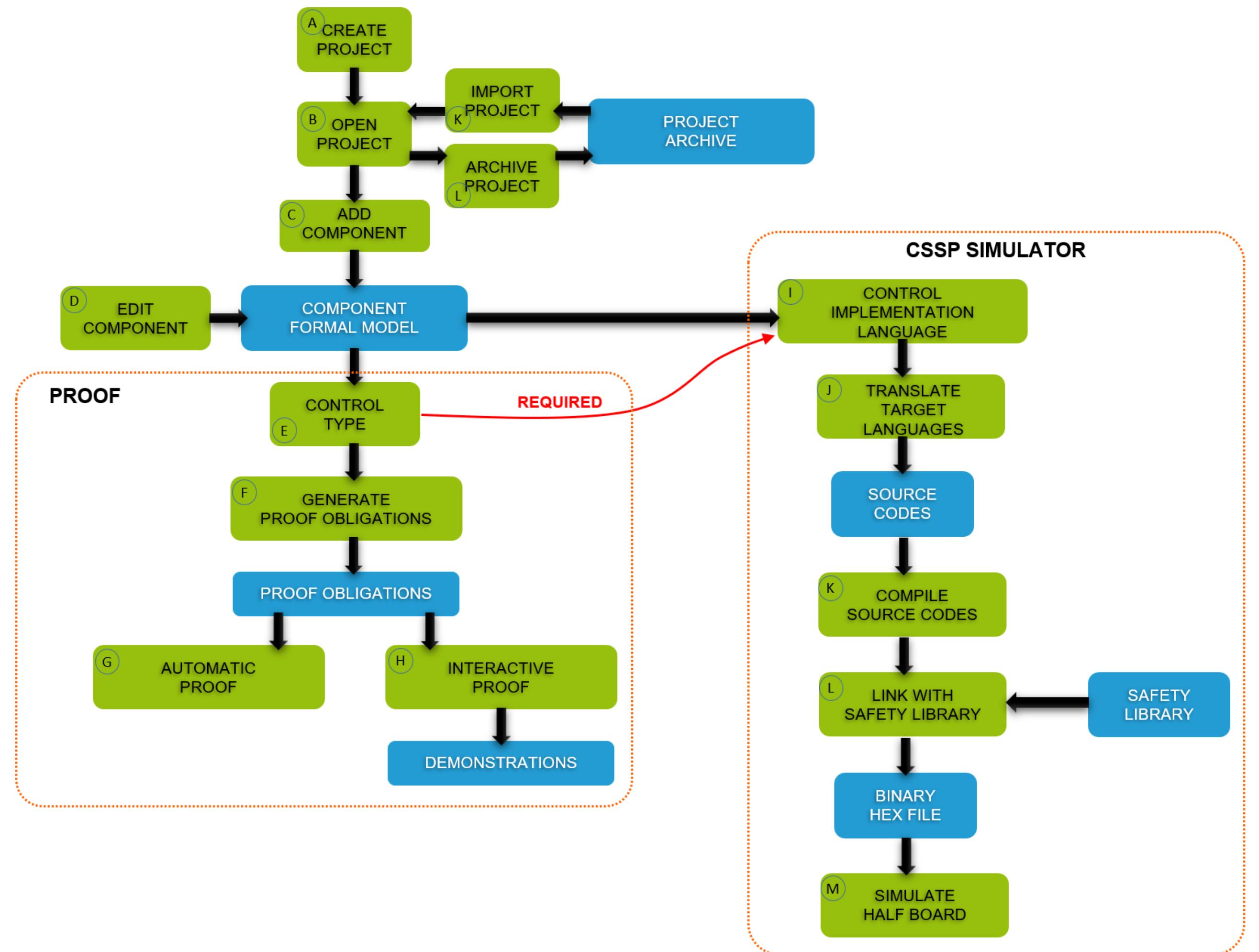
Development process



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Development process



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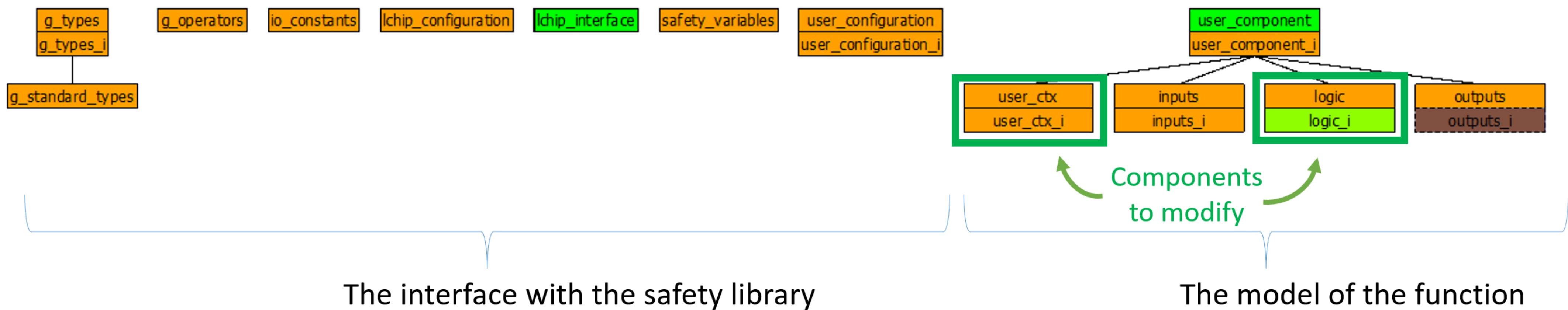
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CLEARSY Safety Platform Project

A CSSP project is a B project

- is generated automatically from board configuration (# IOs, naming)

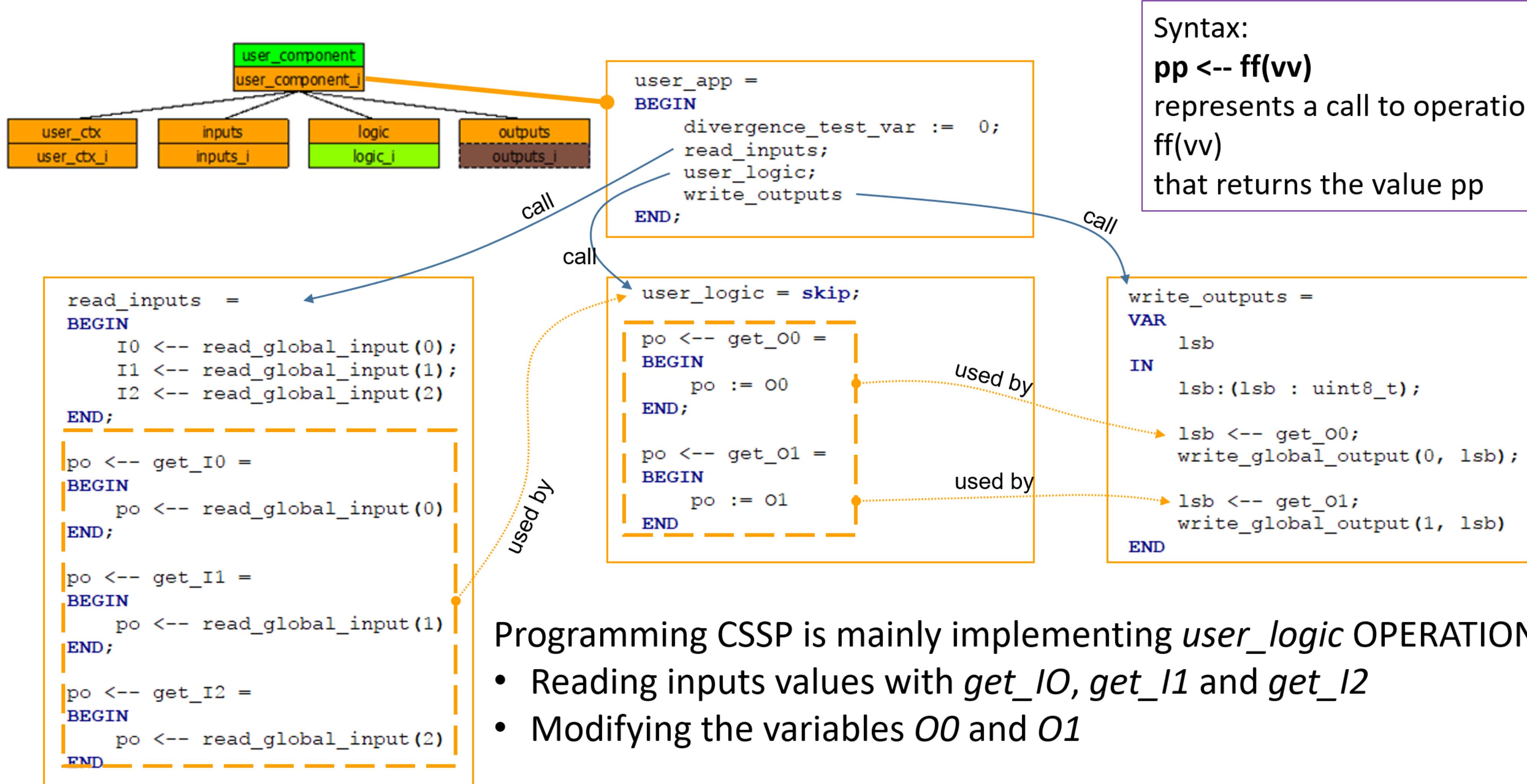
It contains



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Generated Models



Syntax:
pp <- ff(vv)
represents a call to operation
ff(vv)
that returns the value pp

Programming CSSP is mainly implementing `user_logic` OPERATION

- Reading inputs values with `get_I0`, `get_I1` and `get_I2`
- Modifying the variables `O0` and `O1`

Bits of B



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Bits of B : B Variables Declaration

specification

```
ABSTRACT_VARIABLES  
00,  
01
```

: means « belongs

```
INVARIANT  
00 : uint8_t &  
01 : uint8_t
```

|| means « in parallel », « at the
same time »

```
INITIALISATION  
00 :: uint8_t  
01 :: uint8_t
```

« Not deterministic »

:: means « any value within »

implementation

Mandatory
Contains variables that
will be verified

```
// pragma SAFETY_VARS
```

CONCRETE_VARIABLES
00,
01,
TIME_A,
STATUS

To appear in C code

Variables local to
implementation

```
INVARIANT  
00 : uint8_t &  
01 : uint8_t &  
TIME_A : uint32_t &  
STATUS : uint8_t
```

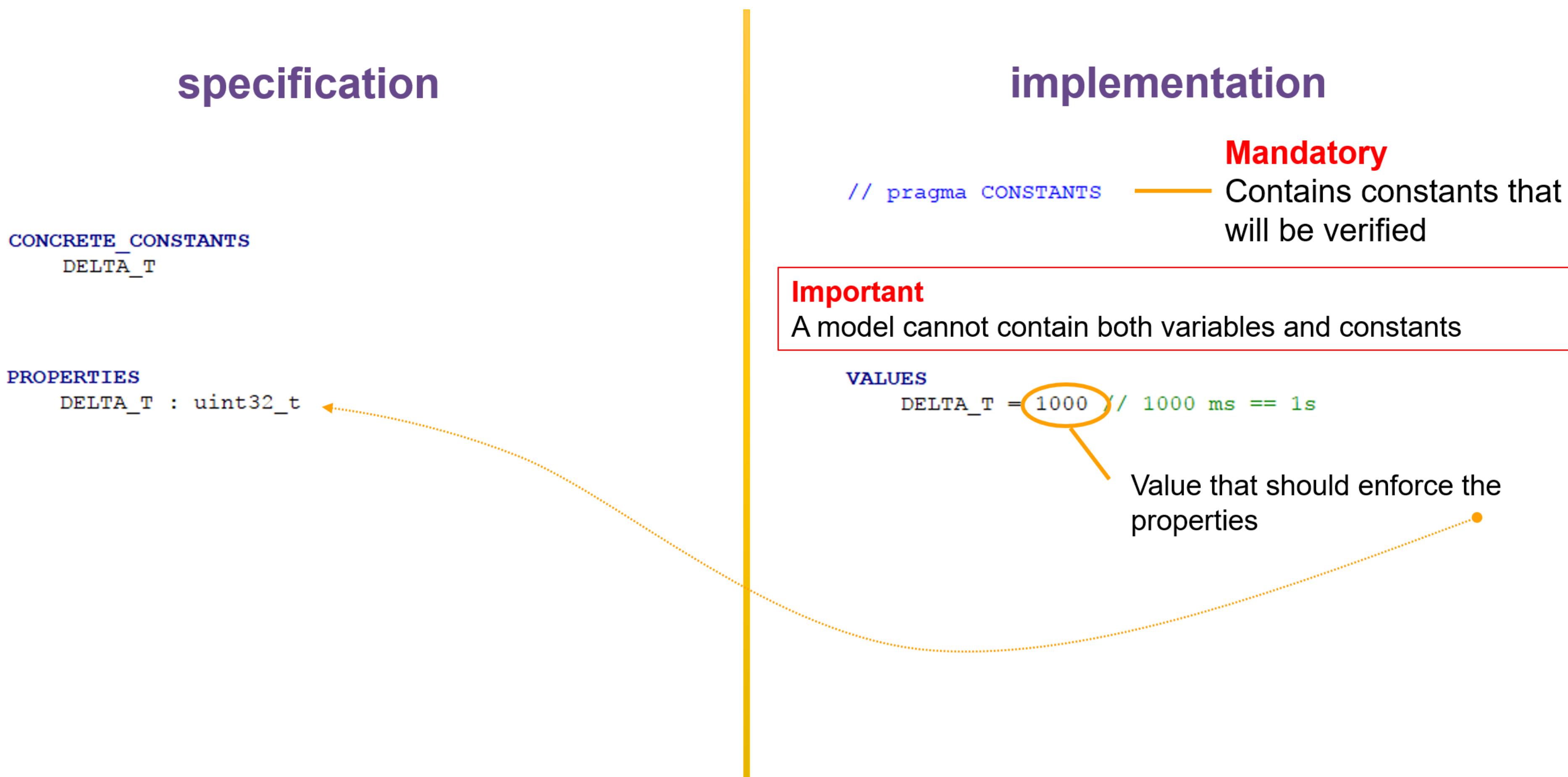
```
INITIALISATION  
00 := IO_OFF;  
01 := IO_OFF;  
TIME_A := 0;  
STATUS := SFALSE
```



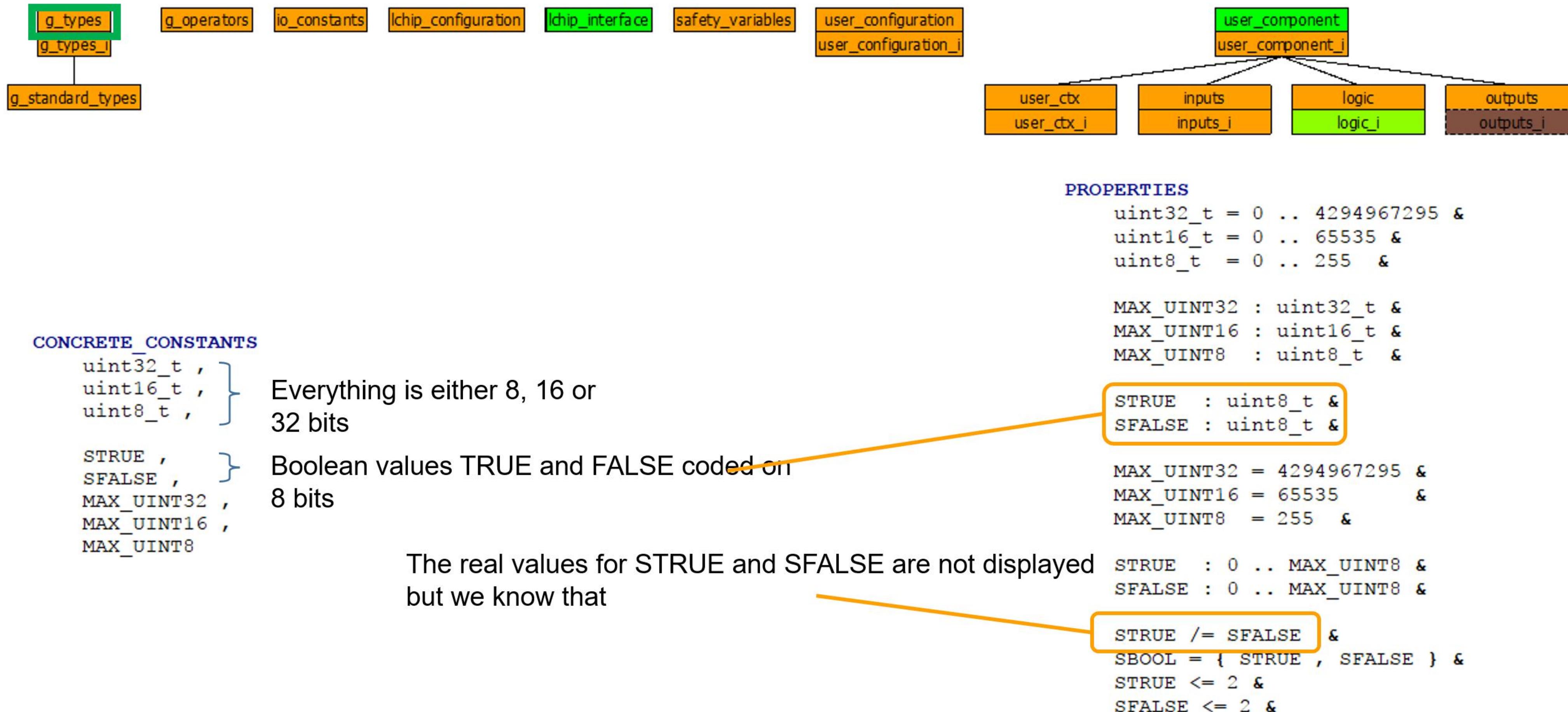
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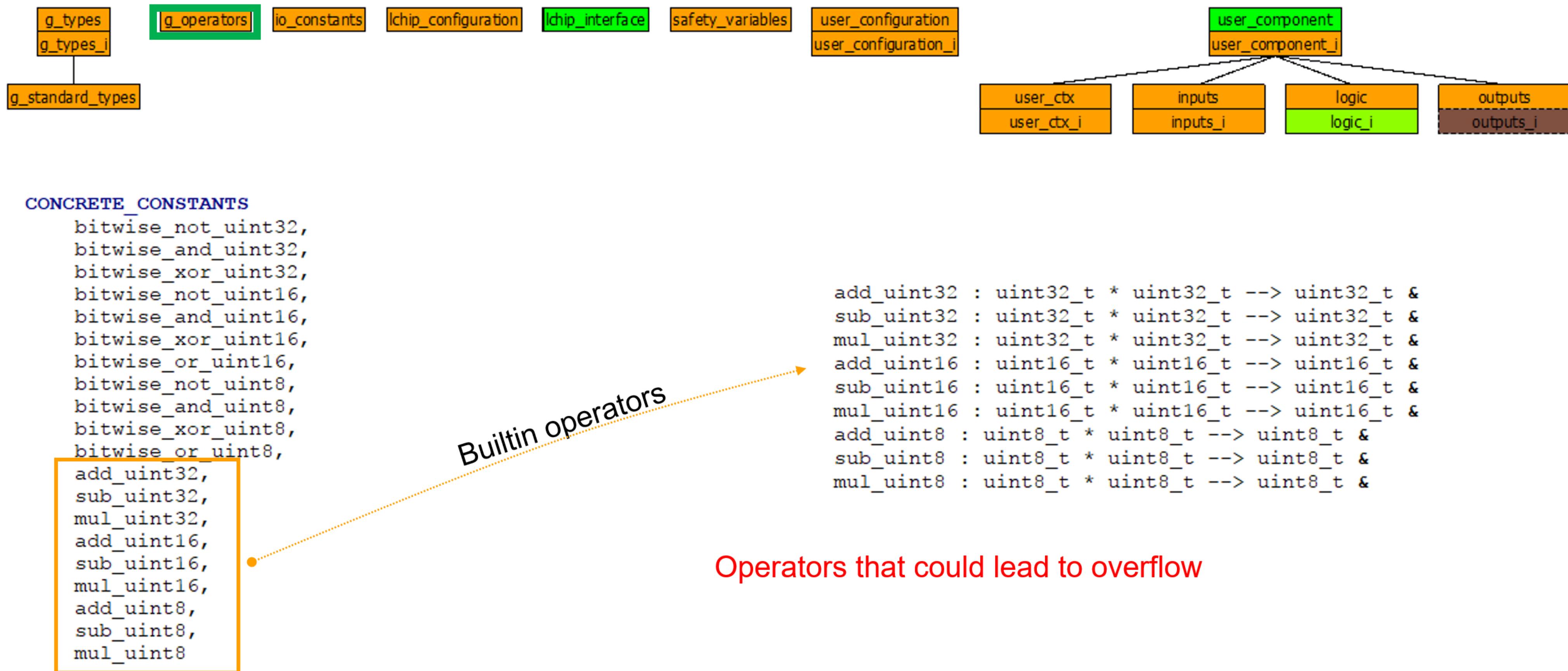
Bits of B : B Constants Declaration



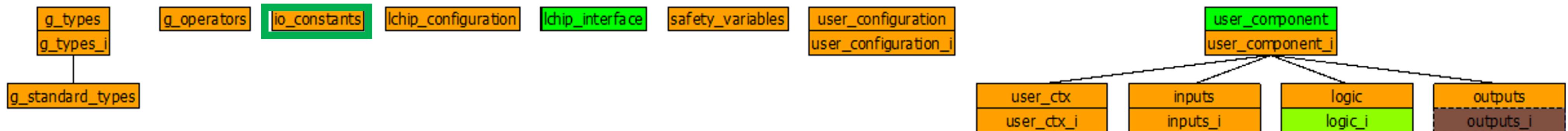
Bits of B : CLEARSY Safety Platform Supported Types



Bits of B : Unsigned INT Operators



Bits of B : Inputs/outputs



ABSTRACT_CONSTANTS
TIME,
IO_STATE

CONCRETE_CONSTANTS
IO_ON,
IO_OFF

PROPERTIES

```
TIME = uint32_t &
IO_STATE = uint8_t &

IO_ON : uint8_t &
IO_OFF : uint8_t &
IO_ON /= IO_OFF &
IO_ON : IO_STATE &
IO_OFF : IO_STATE
```

inputs and outputs state

values used by digital inputs and outputs

coded on 8 bits

Verification

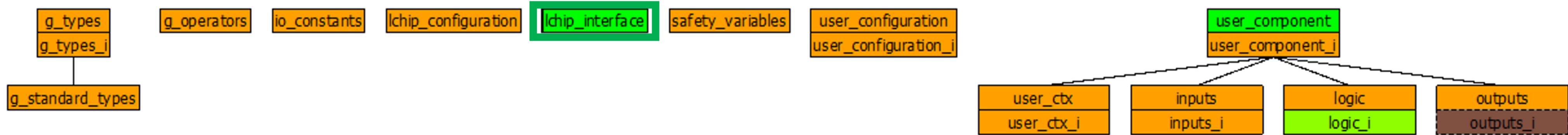
If a digital output is valued with a value different from `IO_ON` or `IO_OFF` then SK_0 stops in error mode



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Bits of B : Time



```
out <-- get_ms_tick =  
PRE  
    out : uint32_t  
THEN  
    out := ms_tick  
END
```

Returns the number of milliseconds elapsed since last reboot

Bits of B: B Operations

Operations are populated with substitutions

Available substitutions in specification are different from the ones available in implementation

specification

Express the properties that the variables comply with when the operation is completed independently from the algorithm implemented (*post-condition*)

WHY ?

TO AVOID PROVING COPY/PASTE

To simplify, always use « becomes such that substitutions »

```
user_logic =
  BEGIN
    oo, o1 : (
      oo : uint8_t &
      o1 : uint8_t &
      not(oo = o1) )
  END;
```

Typing (mandatory)
Constraints (optional)

Bits of B: Implementation

implementation

```
user_logic = skip; — do nothing
```

```
user_logic =
BEGIN
  o0 := IO_ON;
  o1 := IO_OFF
END;
```

```
user_logic =
BEGIN
  IF Var8 = 0 THEN
    o0 := IO_ON
  ELSE
    o1 := IO_ON
  END
END;
```

Important

Only single condition (no conjunction nor disjunction)
= < <= operators only

```
user_logic =
BEGIN
  VAR time_ IN
    time_ : (time_ : uint32_t);
    time_ <-- get_ms_tick;
  IF 2000 <= time_ THEN
    o1 := IO_ON
  END
END;
```

Local variables declaration
Operation call

Important

Local variables have to be typed first using
« becomes such that » substitution

Constraints on the language to simplify the compiler

Bits of B: user_logic without modification

specification

```
user_logic = skip;
```

skip means « do no alter the variables of the model »

```
MACHINE logic
  SEES g_types, g_operators, io_constants, lchip_interface
  ABSTRACT_VARIABLES o1, o2
  INVARIANT o1 : uint8_t & o2 : uint8_t
  INITIALISATION o1 :: uint8_t || o2 :: uint8_t
  OPERATIONS
    user_logic = skip;
    po <- get_o1 =
      PRE po : uint8_t
      THEN po := o1
      END;
    po <- get_o2 =
      PRE po : uint8_t
      THEN po := o2
      END
  END
```

implementation

```
user_logic = skip;
```

Minimum example:

- do nothing; outputs remain in their initial state (INITIALISATION)

```
IMPLEMENTATION logic_i
  REFINES logic
  SEES g_types, g_operators, io_constants, lchip_interface, inputs
  CONCRETE_VARIABLES o1, o2
  INVARIANT o1 : uint8_t & o2 : uint8_t
  INITIALISATION o1 := IO_OFF; o2 := IO_OFF
  OPERATIONS
    user_logic = skip;
    po <- get_o1 =
      BEGIN po := o1
      END;
    po <- get_o2 =
      BEGIN po := o2
      END
  END
```



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Bits of B: user_logic – examples of specification for a given implementation

specification

```
user_logic =
BEGIN
  o0 :: uint8_t ||  O0 and O1 belong to
  o1 :: uint8_t      their type
END
```



```
user_logic =      :( ) means « becomes such that »
BEGIN
  o0, o1 : (       O0 and O1 belong to
    o0 : uint8_t & their type
    o1 : uint8_t &
    not(o0 = o1)  and O0 is different from
  )
END
```



```
user_logic =
BEGIN
  o0 := IO_ON ||   Set O0 and reset O1
  o1 := IO_OFF
END
```

implementation

```
user_logic =
BEGIN
  o0 := IO_ON;    Set O0 then
  o1 := IO_OFF;  reset O1
END
```

« then » is related to the valuation of O0
regarding O1
O0 and O1 will be positioned at the same time
at the end of the cycle



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Using the Modelling Interface



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Using the modelling interface



- ▶ I_1, I_2, O_1, O_2 belongs to $\{IO_OFF, IO_ON\}$
- ▶ O_1 is IO_ON iff both I_1 and I_2 are IO_ON
- ▶ O_2 is the complement of O_1



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Using the modelling interface – minimum specification



- ▶ I1, I2, O1, O2 belongs to `{IO_OFF, IO_ON}` • is unsigned 8 bit integer enumeration
- ▶ O1 is IO_ON iff both I1 and I2 are IO_ON
- ▶ O2 is the complement of O1

```
user_logic =  
BEGIN  
    o1, o2: (  
        o1 : uint8_t &  
        o2 : uint8_t  
    )  
END;
```

}

- « 01, 02 become such that
- Type of O1 is unsigned 8 bit integer
 - Type of O2 is unsigned 8 bit integer »

Minimum specification : « 01 and 02 are modified in accordance with their type »

Using the modelling interface – more complete specification



- ▶ I1, I2, O1, O2 belongs to {IO_OFF, IO_ON}
- ▶ O1 is IO_ON iff both I1 and I2 are IO_ON
- ▶ O2 is the complement of O1

```
user_logic =  
BEGIN  
    o1, o2: (  
        o1 : uint8_t &  
        o2 : uint8_t &  
        (o1=IO_ON <=> (I1=IO_ON & I2=IO_ON)) &  
        not(o1 = o2)  
    )  
END
```



Using the modelling interface - implementation



Green means
« Implementation
Fully proved
Against
Specification »

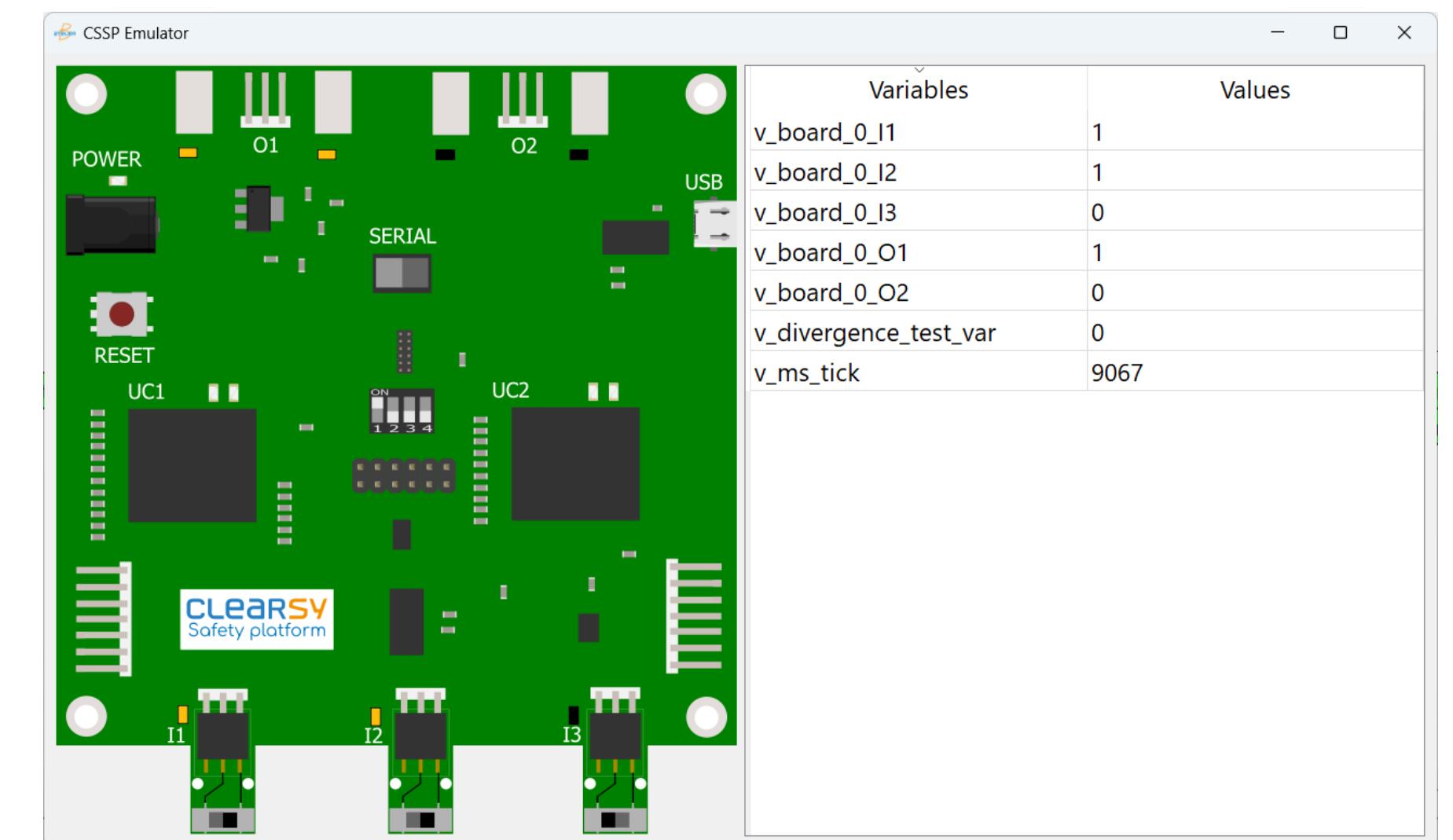
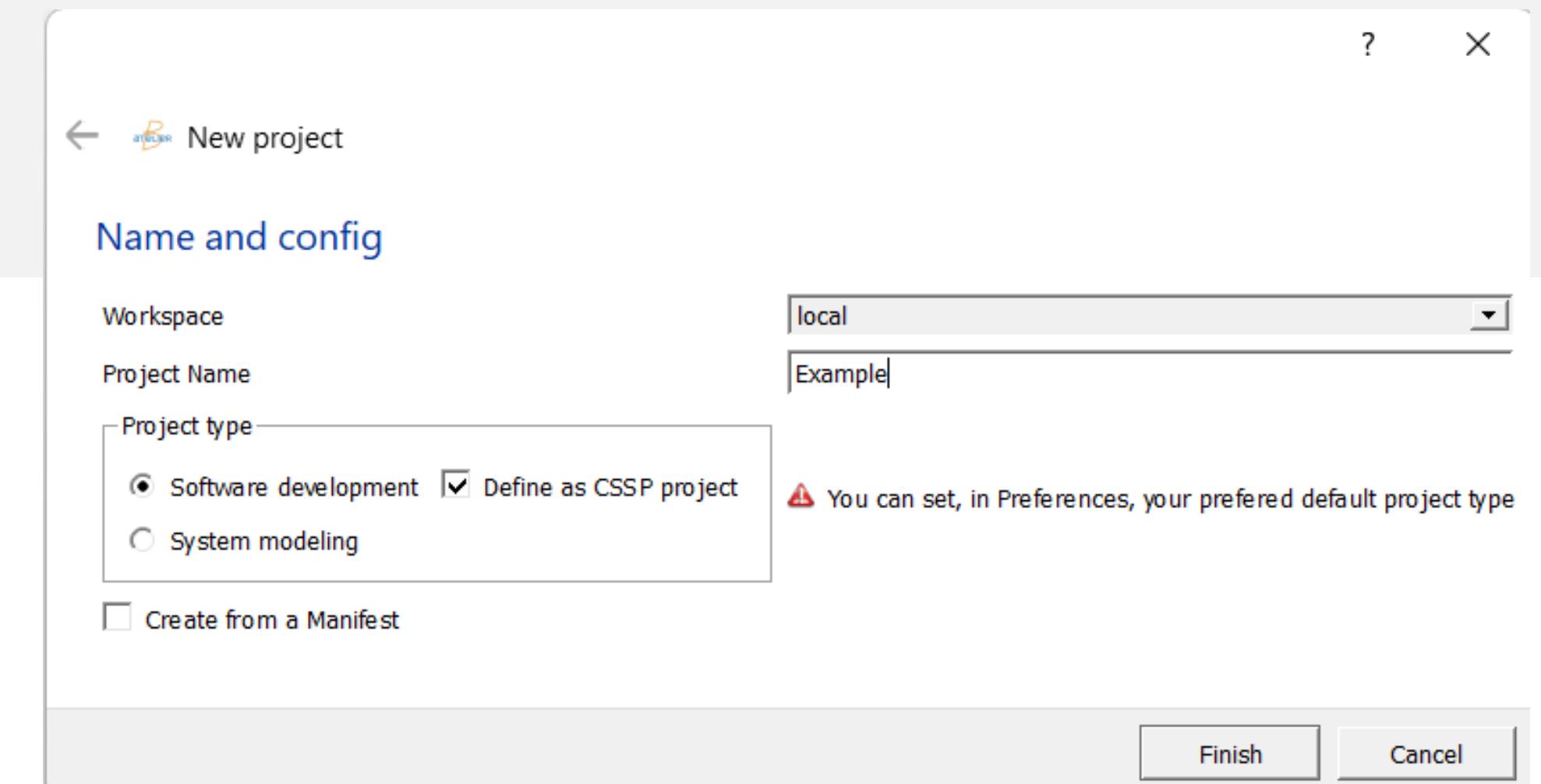
```
user_logic =
BEGIN
  VAR i1_, i2_ IN
    i1_ : (i1_ : uint8_t);
    i2_ : (i2_ : uint8_t);

    i1_ <- get_I1;
    i2_ <- get_I2; ] Get I1 and I2 values

    o1 := IO_OFF;
    o2 := IO_ON;
    IF i1_ = IO_ON THEN
      IF i2_ = IO_ON THEN
        o1 := IO_ON;
        o2 := IO_OFF
      END
    END
  END
END
```

Using the modelling interface

- Edit logic.mch
- Edit logic_i.imp
- Save to check if the model (Ctrl+S)
 - has a correct type
 - is proved
- Start the simulator (Ctrl+D)
 - Once the simulator has started, click on the inputs to observe the expected behaviour

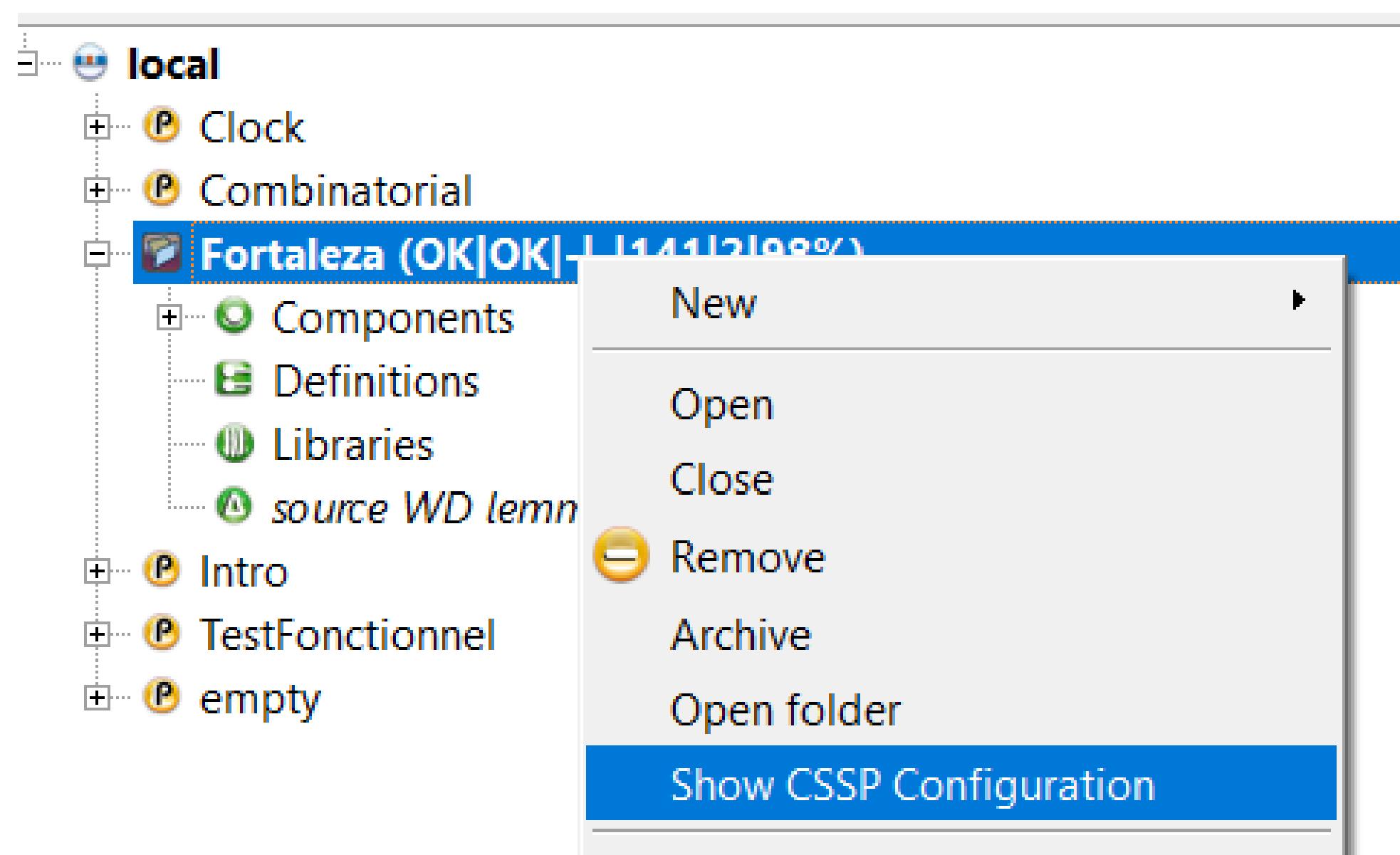


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Using the modelling interface – tip 1

- To know the name of your inputs and outputs,
- Select your project, right click, then
- Select “Show CSSP Configuration”



The screenshot shows the 'Boards and IO configuration' window. On the left, there is a preview of a green printed circuit board (PCB) labeled 'SK0' with three input pads labeled 'I1', 'I2', and 'I3' and two output pads labeled 'O1' and 'O2'. The main area is divided into 'Board properties' and 'Board ports' sections. In the 'Board properties' section, 'boardId' is set to 0, 'name' is 'Board_0', and 'secuid' is empty. 'Total inputs' is 3 and 'Total outputs' is 2. 'Jumper settings' are shown as four binary digits: off, off, on, on. The 'Board ports' section contains two tables: 'Inputs' and 'Outputs'. Both tables have columns 'Used' and 'Name'. The 'Inputs' table has three rows: I1 (Used checked, Name 'board_0_I1'), I2 (Used checked, Name 'board_0_I2'), and I3 (Used checked, Name 'board_0_I3'). The 'Outputs' table has two rows: O1 (Used checked, Name 'board_0_O1') and O2 (Used checked, Name 'board_0_O2'). Both the 'Inputs' and 'Outputs' tables are highlighted with a red border.

Using the modelling interface – tip 2

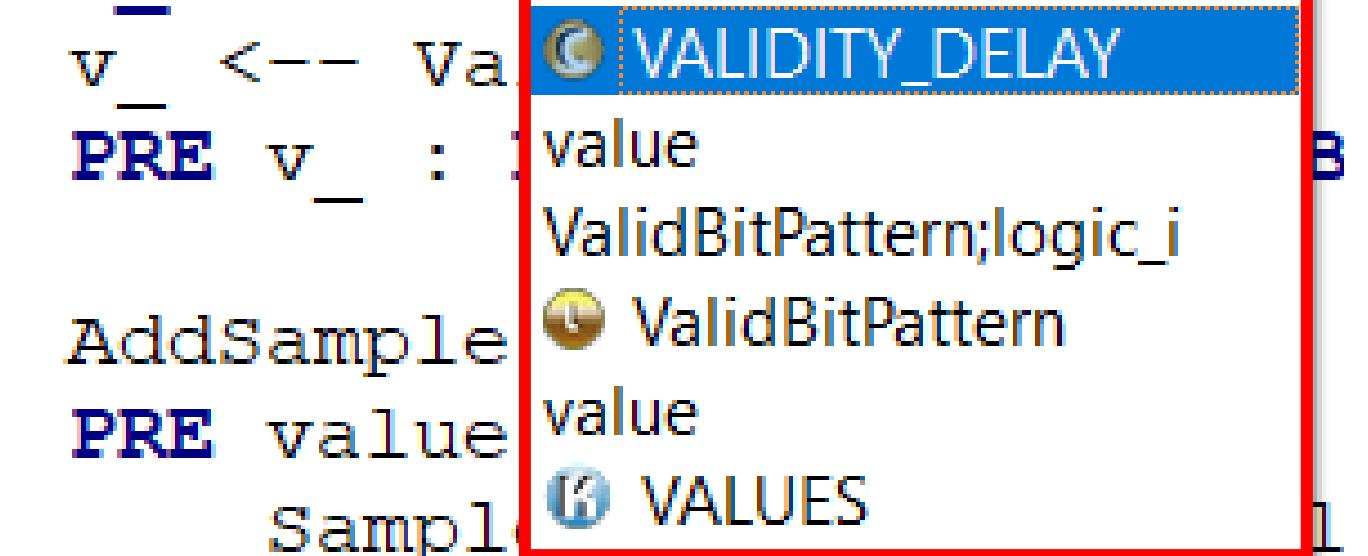
- To autocomplete your identifiers,
- Once they have been added to your model and model has been saved
- Type the first letters of your identifier
- Type Ctrl+<space>
- Use arrow keys to navigate the menu then hit <Enter>

INITIALISATION

```
board_0_01 := IO_OFF;
board_0_02 := IO_OFF;
SOM := SFALSE;
BatteryLow := SFALSE;
CommLinkOK := FALSE;
SamplesContain0 := FALSE;
SamplesContain1 := FALSE;
SamplesDeadline := VAL
```

LOCAL_OPERATION

```
v_ <-- Va value
PRE v_ : value
ValidBitPattern;logic_i
AddSample
PRE value
Sampling
```



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Next

Programming The CLEARY Safety Platform

Paulo Bezerra, Thierry Lecomte



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