

컴퓨터공학실험II

FPGA의 소개와 이해



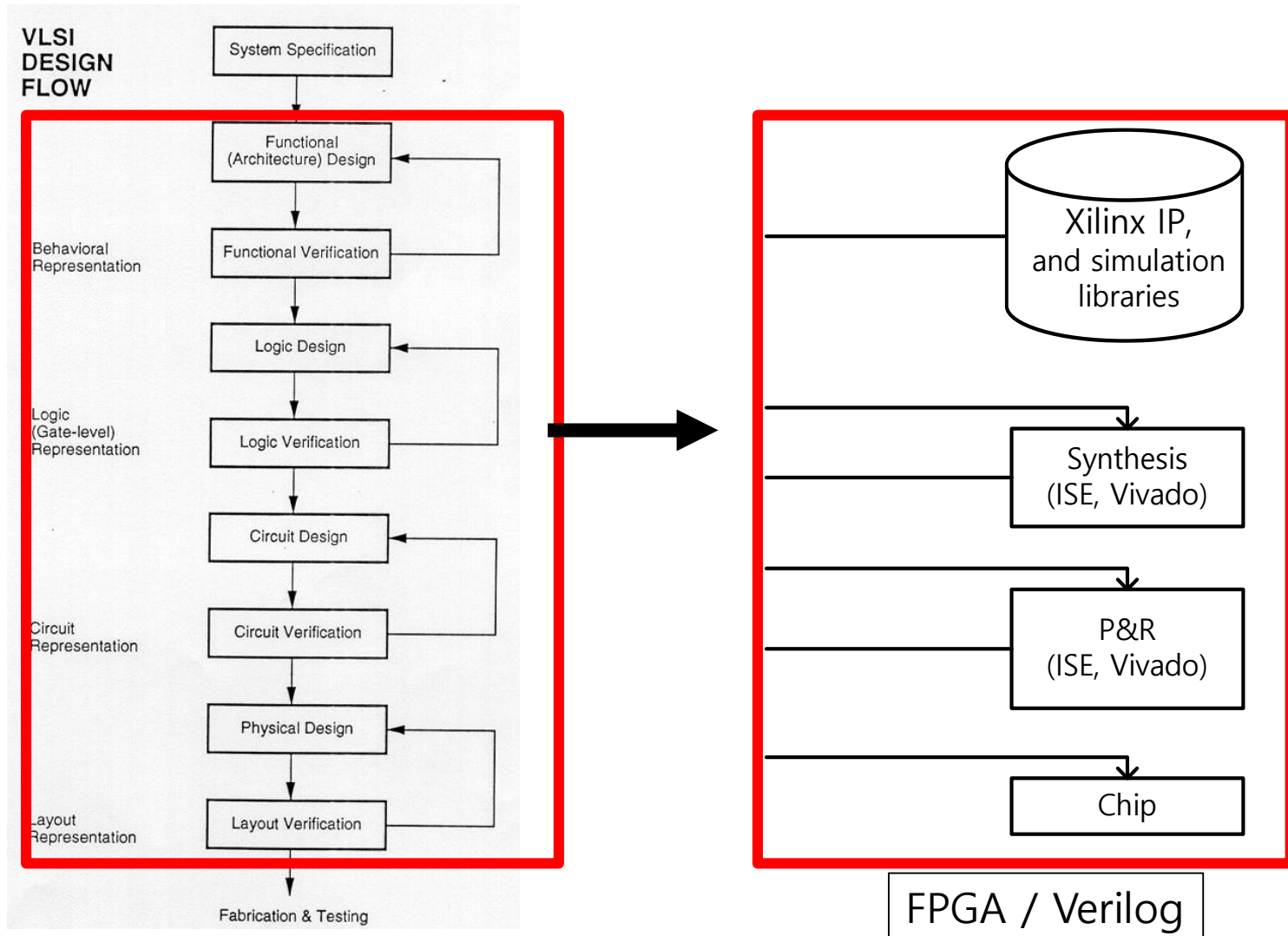
*Be as proud of Sogang
As Sogang is proud of you*

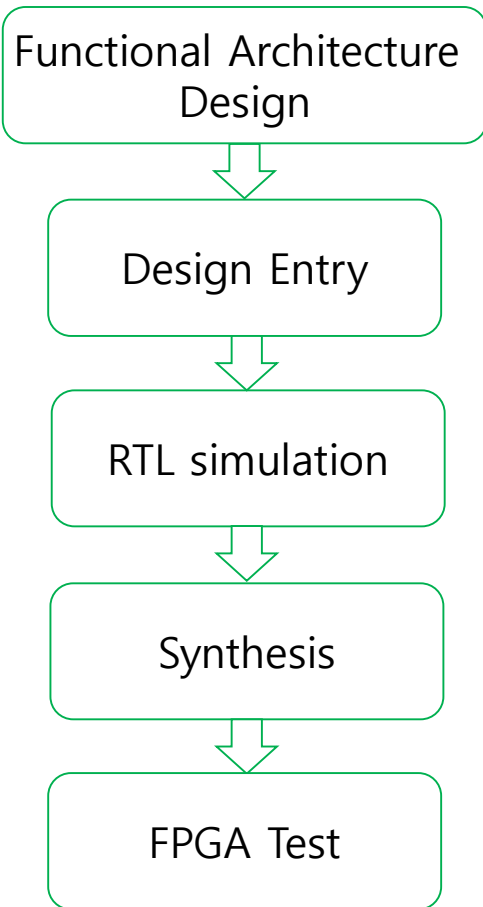
◆ FPGA(Field Programmable Gate Array)

- 이미 설계된 하드웨어를 반도체로 생산하기 직전 최종적으로 하드웨어의 동작 및 성능을 검증하기 위해 제작하는 중간 개발 물 형태의 집적 회로(IC)로, 프로그래밍을 할 수 있는 중간 형태의 비메모리 반도체의 한 종류입니다.
일반 반도체는 회로 변경과 프로그래밍이 불가능한 데 반해 프로그래밍이 가능합니다.
- 설계 가능 논리 소자는 AND, OR, XOR, NOT, 더 복잡한 디코더나 계산기능의 조합 기능같은 기본적인 논리 게이트의 기능을 복제하여 프로그래밍할 수 있으며,
대부분의 FPGA는 프로그래밍가능 논리 요소 에 간단한 플립플롭 이나, 메모리 블록으로 된 메모리 요소를 포함하고 있습니다.
- 활용 분야
 - 로봇제어(알파고)
 - 우주선, 인공위성 등

(압도적으로 빠른 하드웨어 프로그래밍을 요구로 하는 현장에서 주로 사용합니다.)

◆ 흐름도





◆ **Functional Architecture Design**

이론 및 스케메틱(schematic)을 통해서 디자인을 설계하는 단계.

◆ **Design Entry**

HDL(Hardware Description Language)로 설계하는 단계.

◆ **RTL simulation**

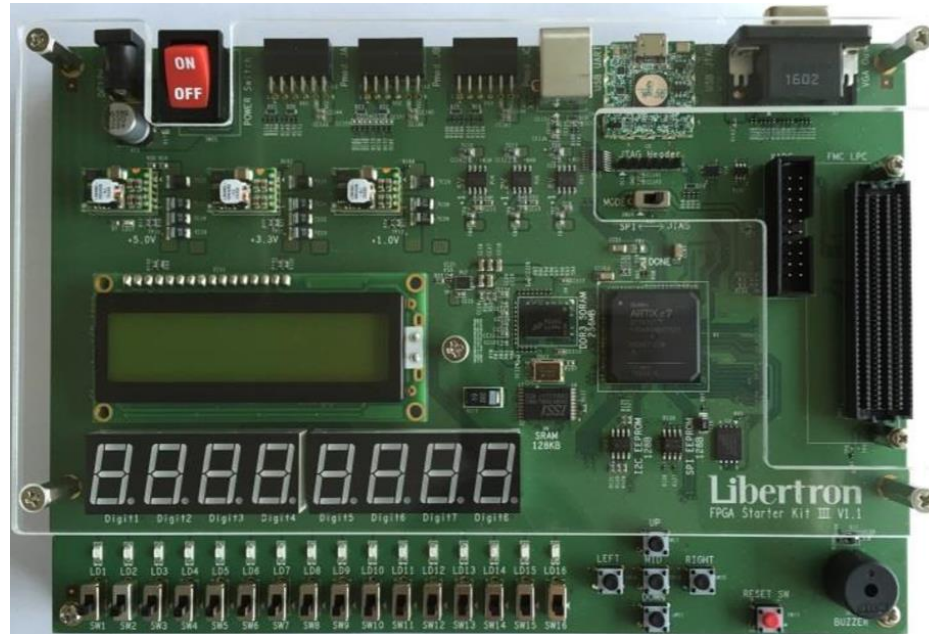
이전 과정인 design Entry에서 사용자가 구현한 것을 시뮬레이션으로 검증을 해보는 단계.

◆ **Synthesis**

합성과정은 유저가 구현한 High-Level한 디자인을 FPGA 보드가 이해 할 수 있는 Low Level로 바꿔주는 단계.

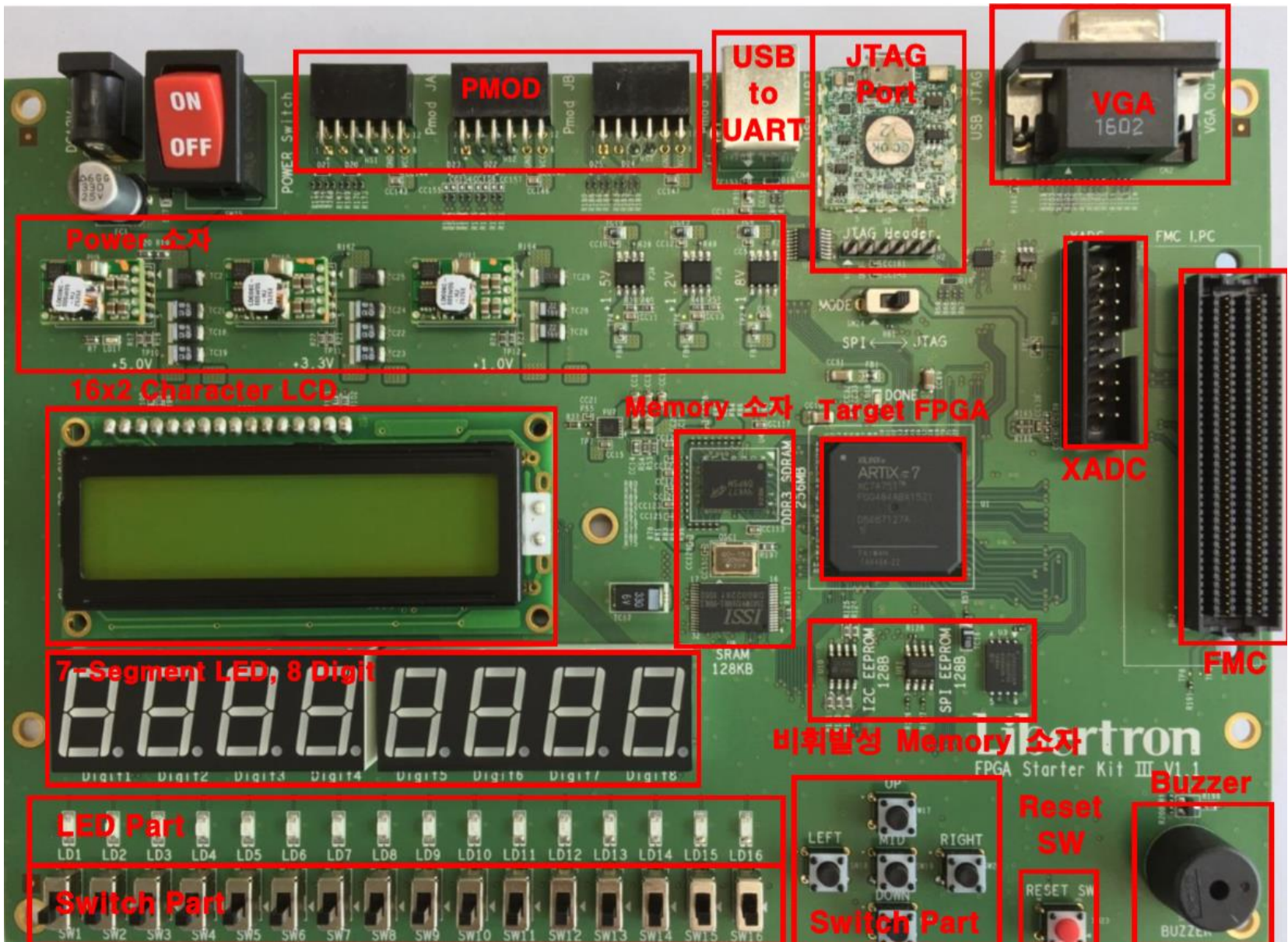
◆ **FPGA Test**

FPGA 보드를 통해 Test 해보는 단계.



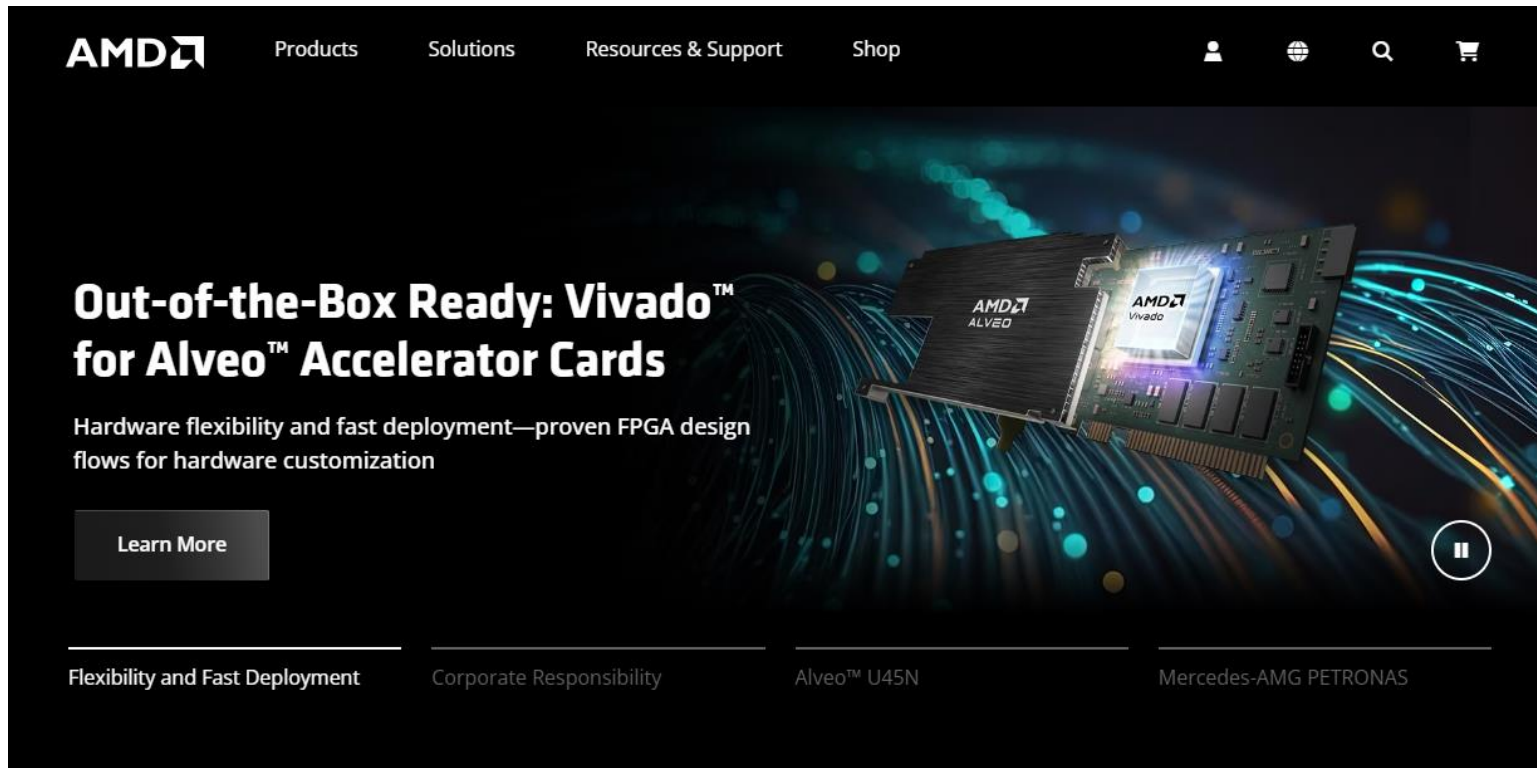
- ◆ 실험장비 : FPGA Starter Kit III Board
- ◆ S/W : Xilinx Vivado
- ◆ Language : Verilog

FPGA 장비 소개

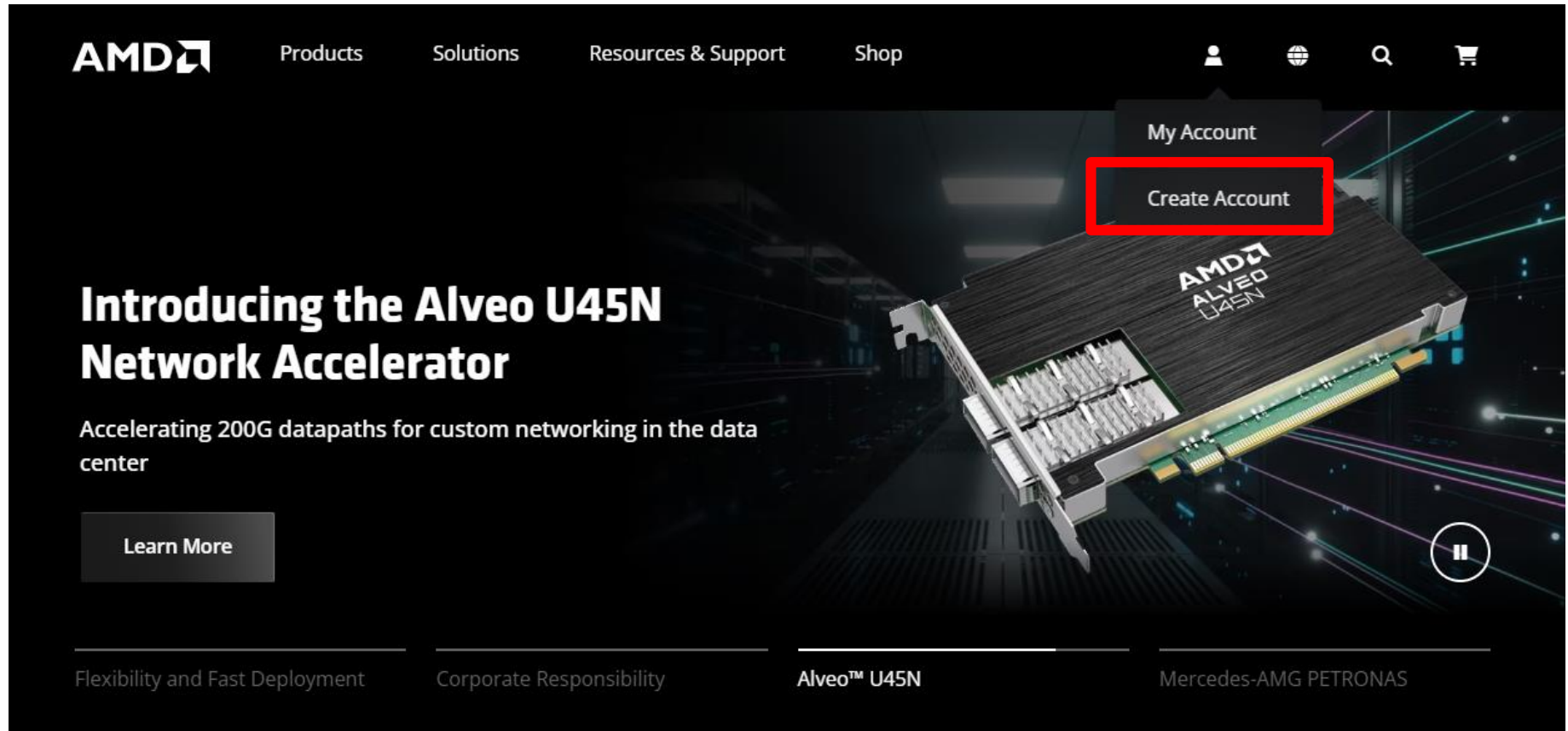


◆ Vivado 설치

<https://www.amd.com/en.html> 으로 접속합니다.



◆ Vivado 회원 등록



The image shows the AMD website's product page for the Alveo U45N Network Accelerator. The page has a dark background with a large image of the accelerator card. The AMD logo is in the top left. Navigation links include Products, Solutions, Resources & Support, and Shop. User account icons (person, globe, search, cart) are in the top right. A dropdown menu for the user icon shows 'My Account' and 'Create Account', with 'Create Account' highlighted by a red rectangle. The main heading is 'Introducing the Alveo U45N Network Accelerator', followed by the subtext 'Accelerating 200G datapaths for custom networking in the data center'. A 'Learn More' button is below. The footer contains four sections: 'Flexibility and Fast Deployment', 'Corporate Responsibility', 'Alveo™ U45N', and 'Mercedes-AMG PETRONAS'.

AMD Products Solutions Resources & Support Shop

My Account
Create Account

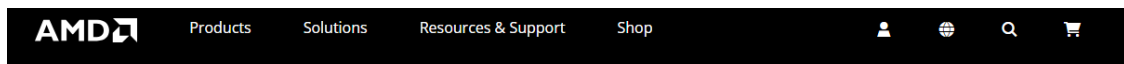
Introducing the Alveo U45N Network Accelerator

Accelerating 200G datapaths for custom networking in the data center

[Learn More](#)

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◆ Vivado 회원 등록



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To create an account, complete the form below.

An account activation message with an **Access Token** will be sent via e-mail to the address you specify below.

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Business users, please provide your company e-mail address for full access to licensing, support, and services. All other users, please use your personal e-mail address.

Preferred Language *

Location *

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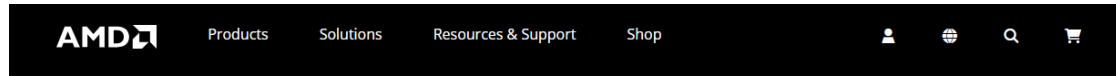

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Submit

①작성

②

◆ Vivado 회원 등록



Next Step - Activate Your Account

Please check your e-mail for your AMD account activation message.

To activate your account, enter the **Access Token** from the account activation e-mail message and create a password.

① 이전 페이지에서 입력한 이메일 확인

② 작성

③

Access Token *

yg9ResoaK2iRpDkHwO_T

Password *

Password Strength: Strong.


Must contain a minimum of 10 characters and a maximum of 72 characters

Must contain at least 1 lowercase letter, 1 uppercase letter, 1 number and 1 special character (eg: !@#\$%^&*+=)

Confirm Password *

Password match: Yes

✓ I'm not a robot



reCAPTCHA

Privacy - Terms

Activate Account

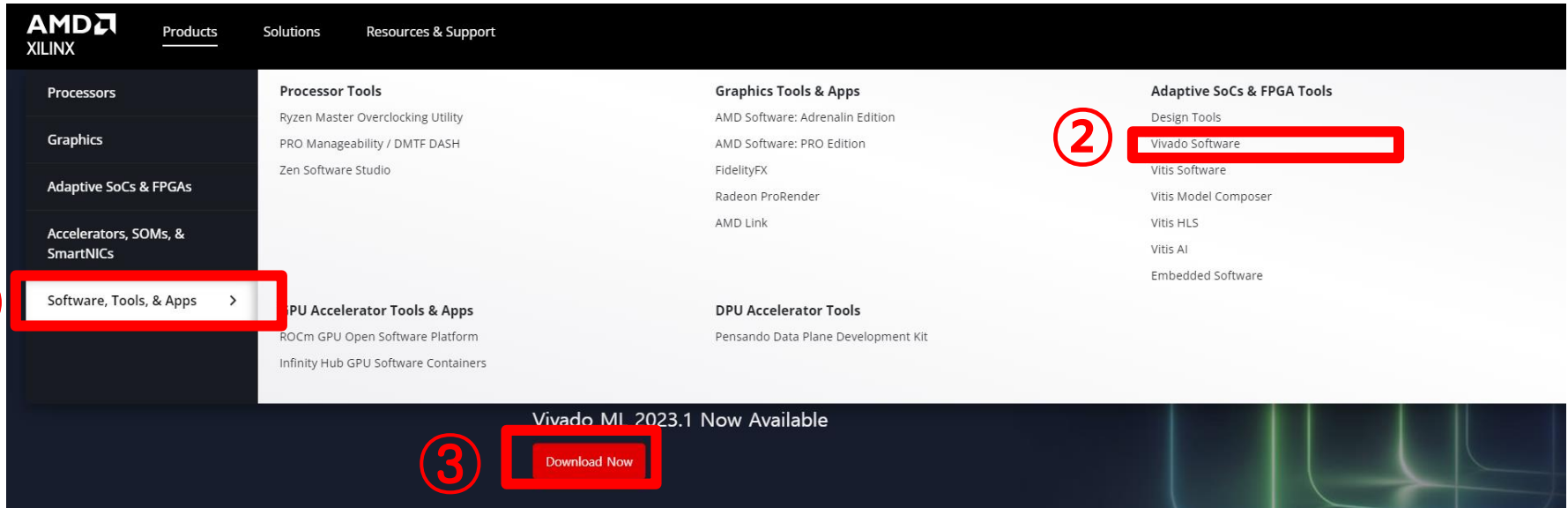
Resend Activation E-mail

Note: If you do not receive a confirmation e-mail within a few minutes please check your junk mail folder and add sender account.help@amd.com to your address book.

Department of Computer Science and Engineering, Sogang University

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◆ Vivado 설치



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- Design Tools
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 - Vitis Software
 - Vitis Model Composer
 - Vitis HLS
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Vivado ML 2023.1 Now Available

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Version

2023.1

2022.2

Vivado Archive

ISE Archive

CAE Vendor Libraries Archive

We strongly recommend using the latest releases available.

2021

2021.1
2021.2

2020

2020.3
2020.2
2020.1

2019

2019.2
2019.1

2018

2018.3
2018.2
2018.1

2017

2017.4
2017.3

1

2

◆ Vivado 설치

Vivado Design Suite - HLx Editions - 2017.3 Full Product Installation

Important

We strongly recommend to use the web installers as it reduces download time and saves significant disk space.

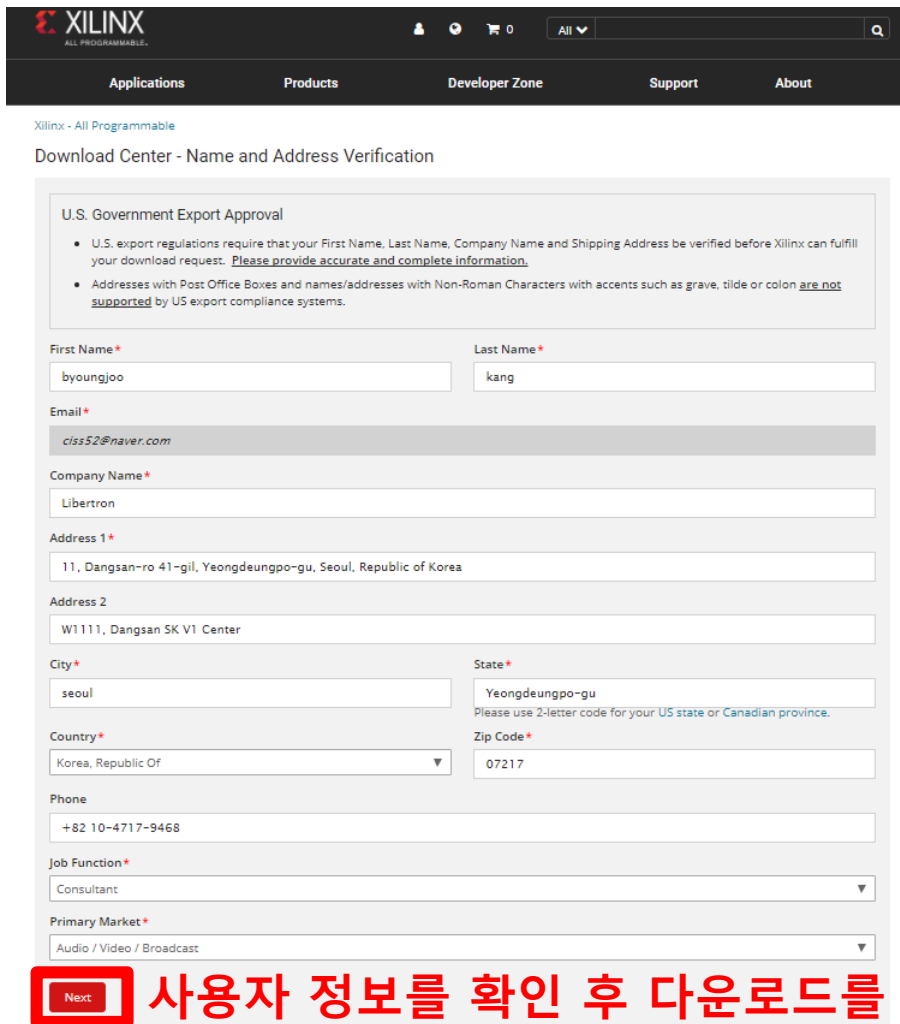
Please see [Installer Information](#) for details.

 [Vivado HLx 2017.3: All OS installer Single-File Download \(TAR/GZIP - 16.23 GB\)](#)

MD5 SUM Value : d443f58d703ff691cebc59c2173ae782

Download Includes	Vivado Design Suite HLx Editions (All Editions)
Download Type	Full Product Installation
Last Updated	Oct 9, 2017
Answers	2017.x - Vivado Known Issues
Documentation	2017.3 - Release Notes
Enablement	License Solution Center

◆ Vivado 설치



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Xilinx - All Programmable

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State *
Please use 2-letter code for your US state or Canadian province.

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Phone

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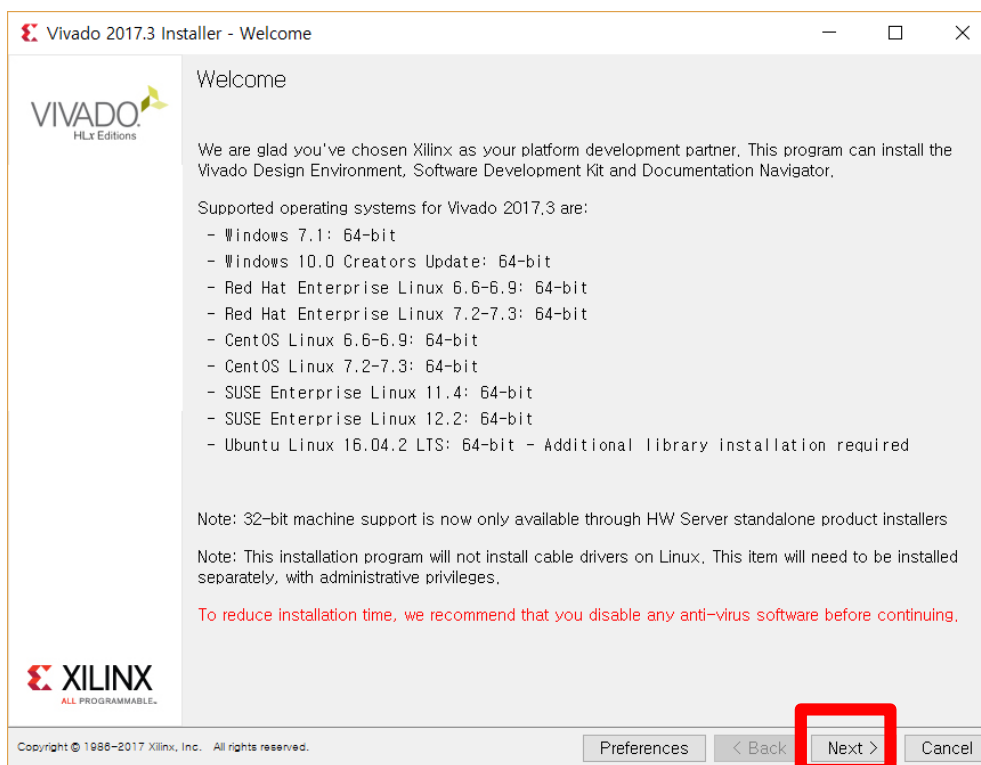
Primary Market *

Next 사용자 정보를 확인 후 다운로드를 시작합니다.

◆ Vivado 설치

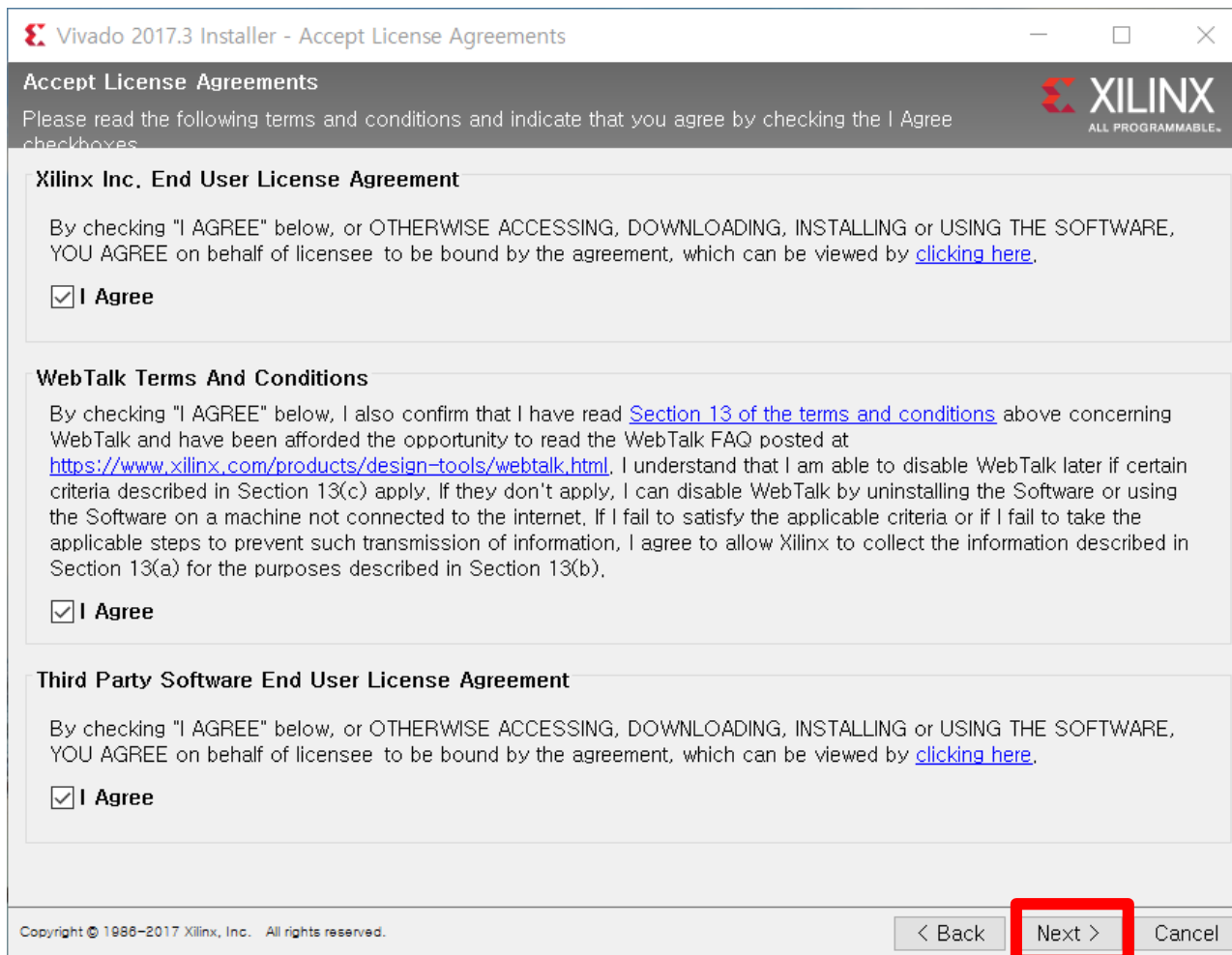


① 다운로드 완료된 파일을 압축 해제 후,
installer(xsetup.exe)를 시작합니다.



②

◆ Vivado 설치



Vivado 2017.3 Installer - Accept License Agreements

Accept License Agreements

Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.

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By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

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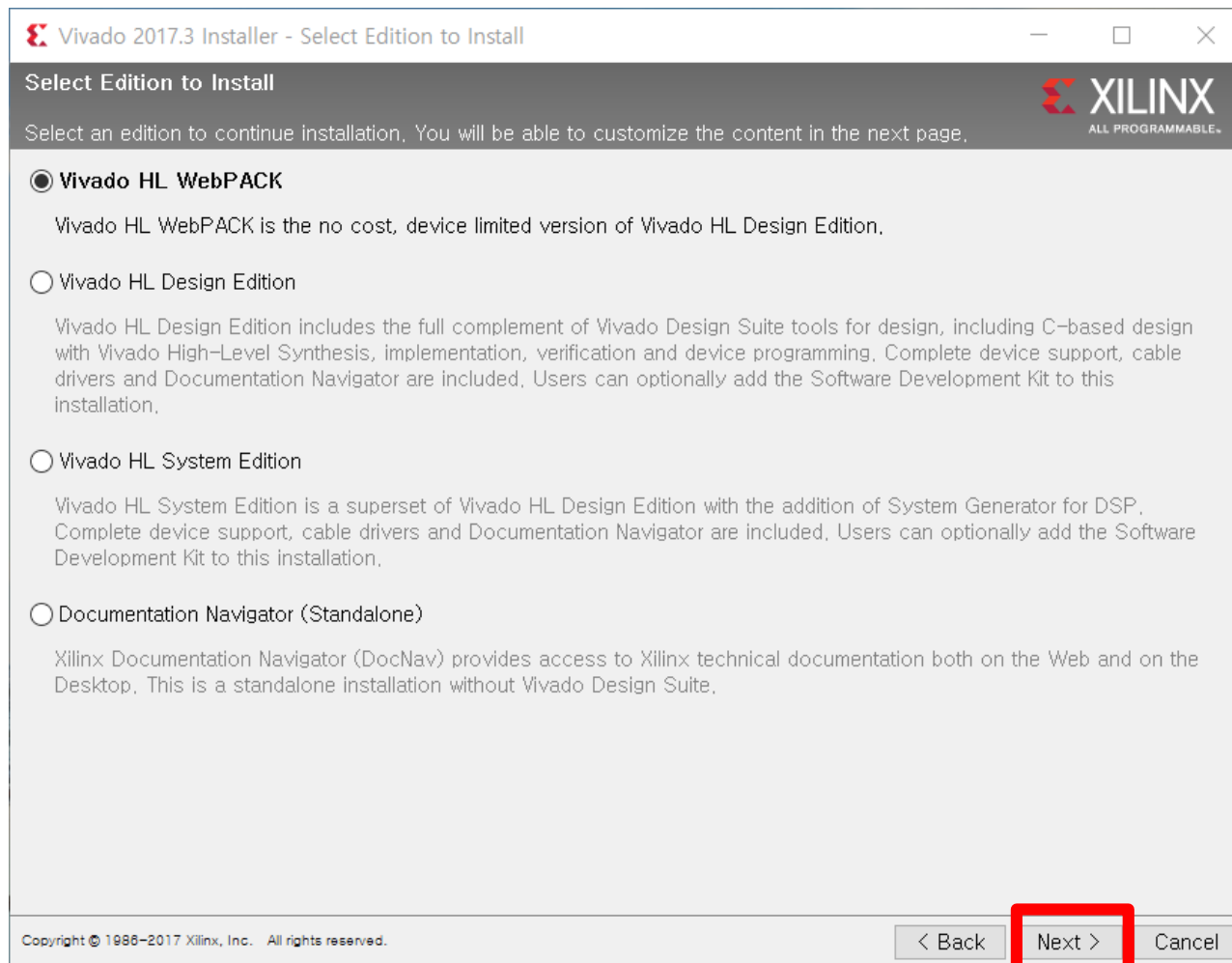
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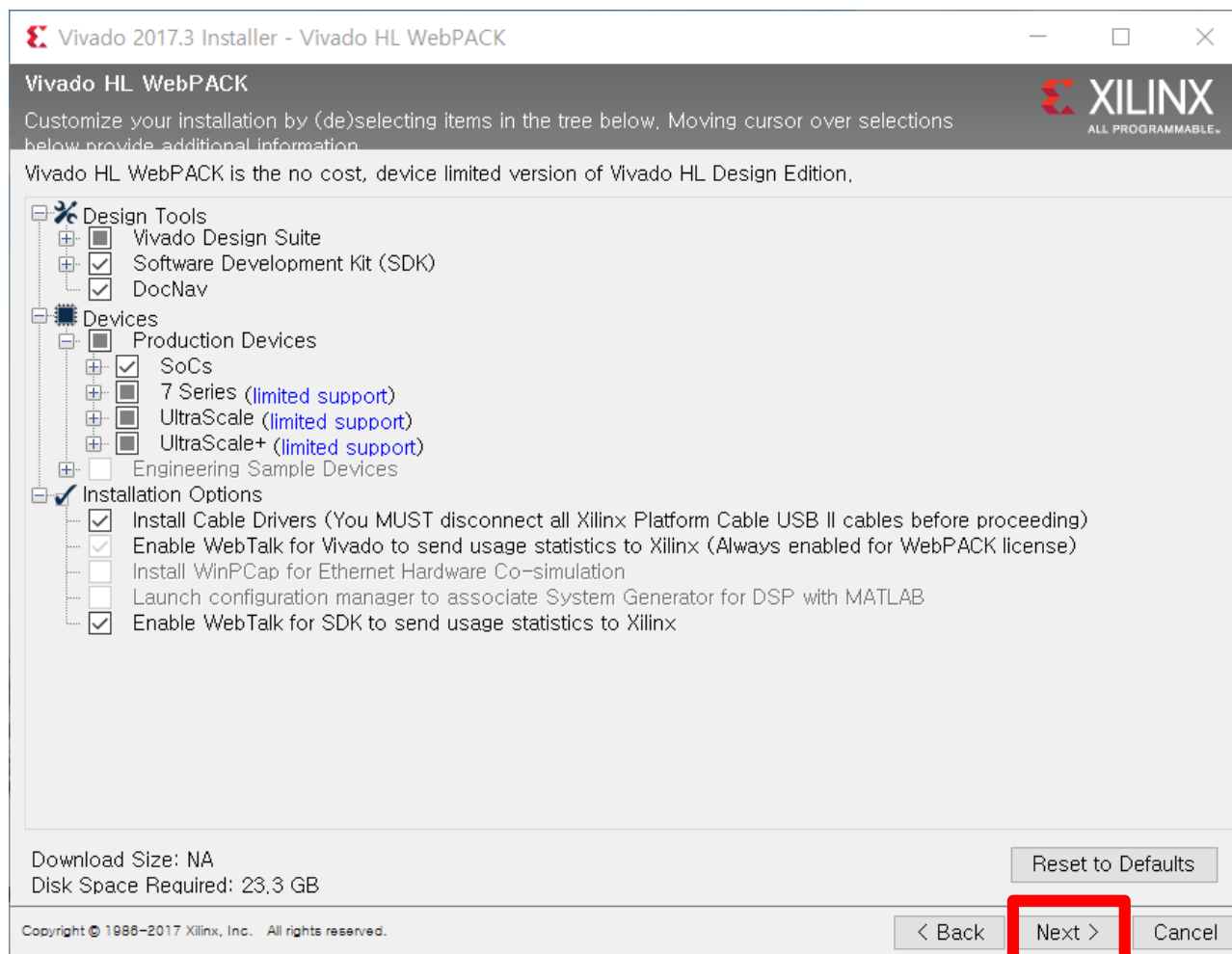
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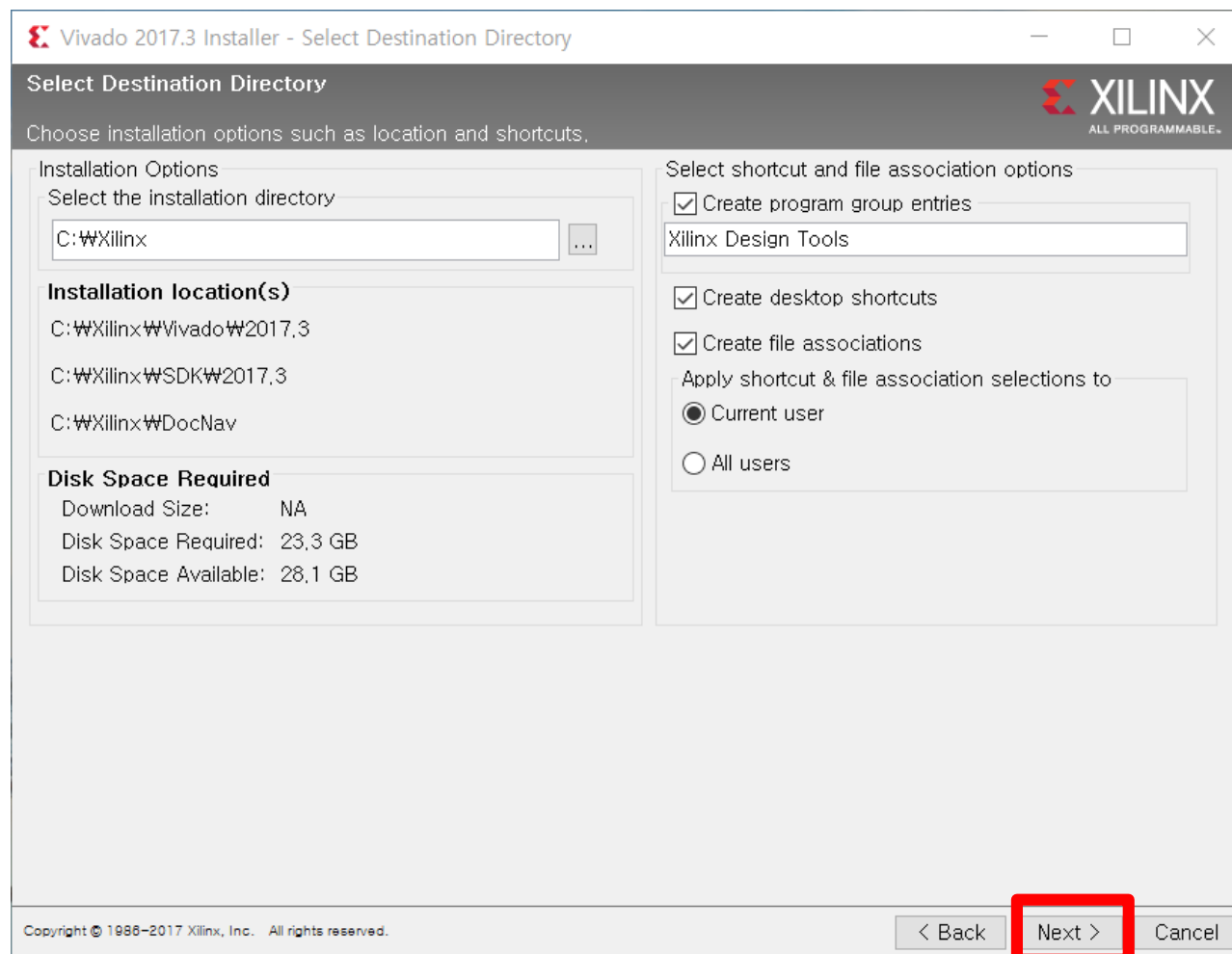
◆ Vivado 설치



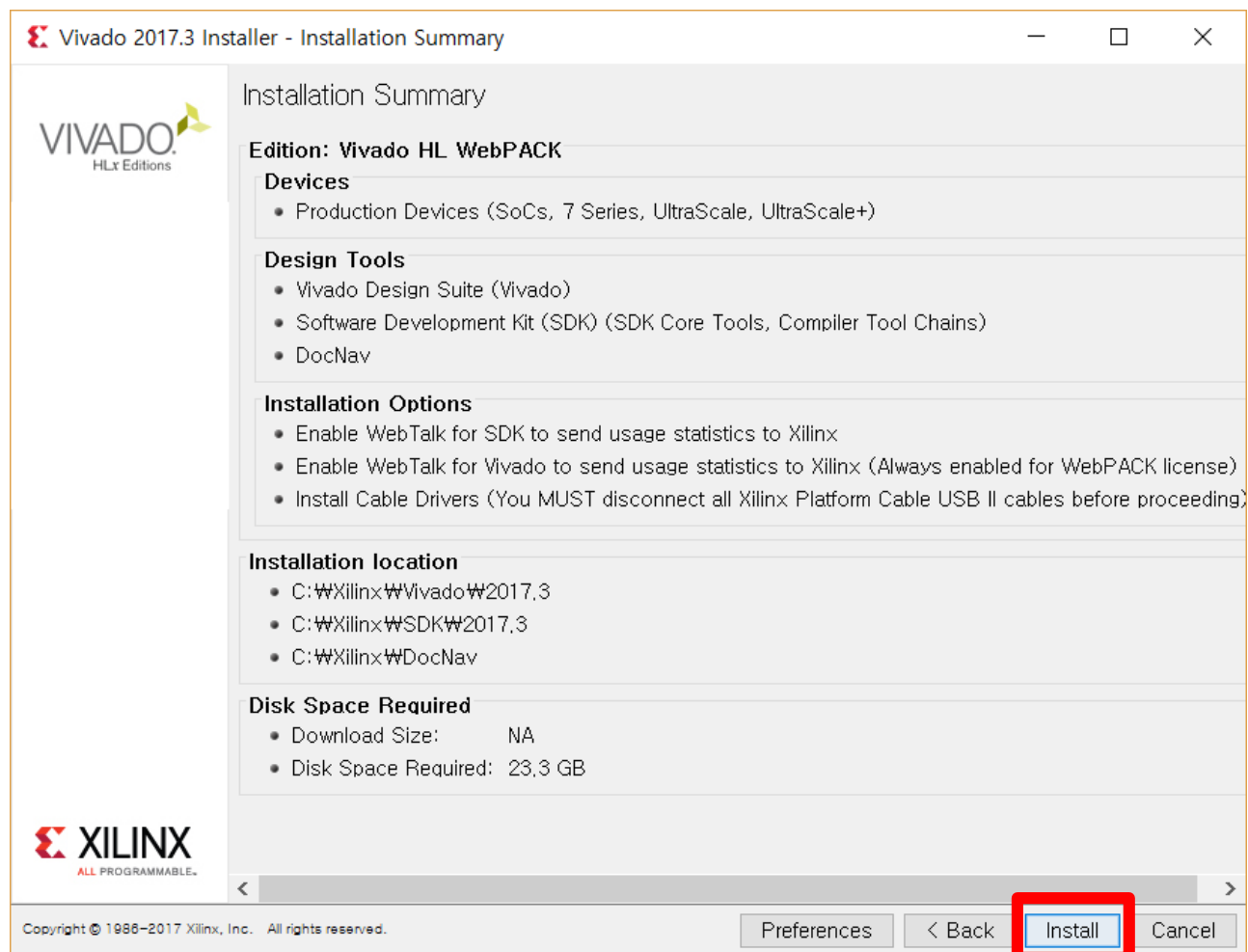
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◆ Vivado 설치



◆ Vivado 설치



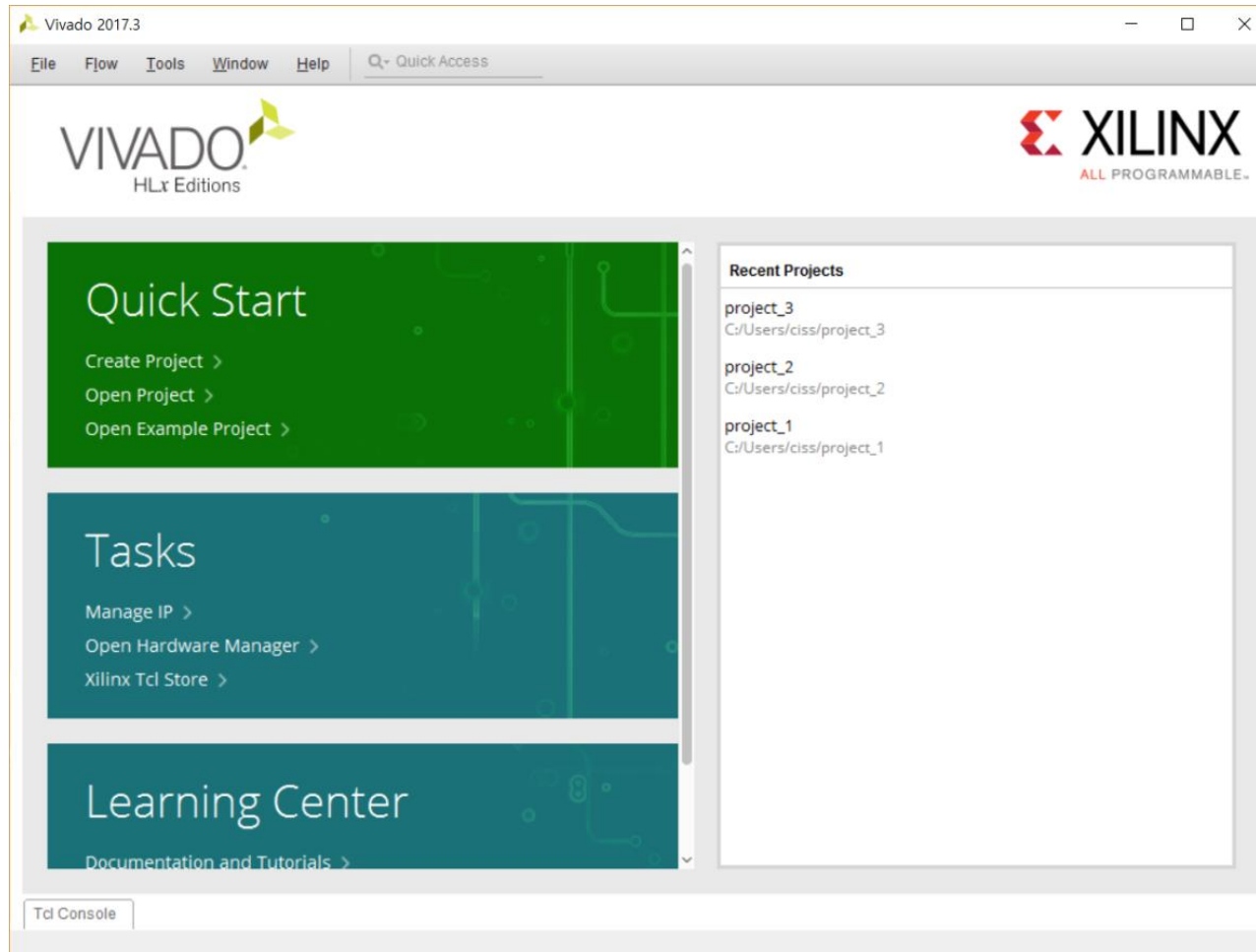
◆ Vivado 설치

파일 다운로드 및 설치가 시작됩니다.
수십분의 설치 진행후에 작업이 완료됩니다.



◆ Vivado 설치

정상적으로 설치가 완료되면 아래 와 같은
시작 화면을 보실 수 있습니다.



◆ Clock

Global Clock

Signal Name	FPGA Pin	I/O	Description
FPGA_CLK	R4	Input	FPGA Clock Input (100Mhz)

◆ Switch

Reset Switch

Signal Name	FPGA Pin	I/O	Description
FPGA_RSTB	U7	Input	FPGA Logic Reset Pin (Active 'L')

PUSH Switch

Signal Name	FPGA Pin	I/O	Description
PUSH_SW_UP	E21	Input	User Push Switch [4..0] (Active 'H')
PUSH_SW_LEFT	D21		
PUSH_SW_MID	G21		
PUSH_SW_RIGHT	G22		
PUSH_SW_DOWN	F21		

◆ Switch

DIP Switch

Signal Name	FPGA Pin	I/O	Description
DIP_SW<0>	J4	Input	User DIP Switch [15..0] (Active 'H')
DIP_SW<1>	L3		
DIP_SW<2>	K3		
DIP_SW<3>	M2		
DIP_SW<4>	K6		
DIP_SW<5>	J6		
DIP_SW<6>	L5		
DIP_SW<7>	L4		
DIP_SW<8>	Y16		
DIP_SW<9>	AA16		
DIP_SW<10>	AB16		
DIP_SW<11>	AB17		
DIP_SW<12>	AA13		
DIP_SW<13>	AB13		
DIP_SW<14>	AA15		
DIP_SW<15>	AB15		

◆ Display

Discrete LED

Signal Name	FPGA Pin	I/O	Description
LED<0>	F15	Output	User LED [15..0] (Active 'H')
LED<1>	F13		
LED<2>	F14		
LED<3>	F16		
LED<4>	E17		
LED<5>	C14		
LED<6>	C15		
LED<7>	E13		
LED<8>	AA10		
LED<9>	AA11		
LED<10>	V10		
LED<11>	W10		
LED<12>	Y11		
LED<13>	Y12		
LED<14>	W11		
LED<15>	W12		

◆ Display

7-Segment

Signal Name	FPGA Pin	I/O	Description
SEG_A	D20	Output	Segment [7..0] (Active 'H')
SEG_B	C20		
SEG_C	C22		
SEG_D	B22		
SEG_E	B21		
SEG_F	A21		
SEG_G	E22		
SEG_DP	D22		
DIGIT1	E14	Output	Digit [7..0] (Active 'H')
DIGIT2	E16		
DIGIT3	D16		
DIGIT4	D14		
DIGIT5	AB11		
DIGIT6	AB12		
DIGIT7	AA9		
DIGIT8	AB10		