Design of synchronous counter (0,1,2, ... 13,14,15,0,1,2 ...) (input X)

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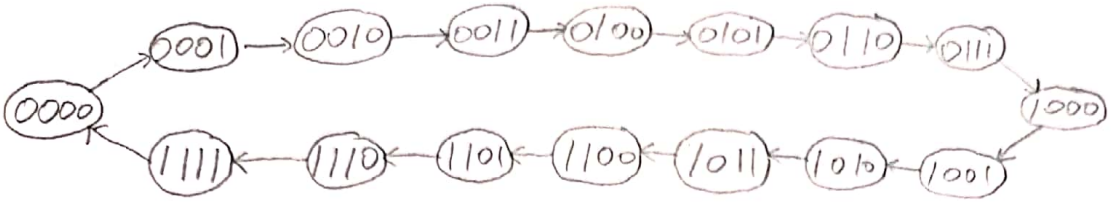
1. Using D-FF

① State diagram



② State table

D	C	B	A	D^*	C^*	B^*	A^*	Dd	Dc	Db	Da
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	1	1
1	0	1	1	1	1	0	0	1	1	0	0
1	1	0	0	1	1	0	1	1	1	0	1
1	1	0	1	1	1	1	0	1	1	1	0
1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	0	0	0	0	0	0	0	0

③ D-FF의 Excitation table

Q	Q^*	D
0	0	0
0	1	1
1	0	0
1	1	1

④ Karnaugh Map

• Dd

BA \ DC	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	1	0	1
10	0	0	1	1

$Dd = DC' + DB' + DA' + D'CBA$

• Dc

BA \ DC	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	0	1	1	0

$Dc = CB' + CA' + C'BA$

• Db

BA \ DC	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

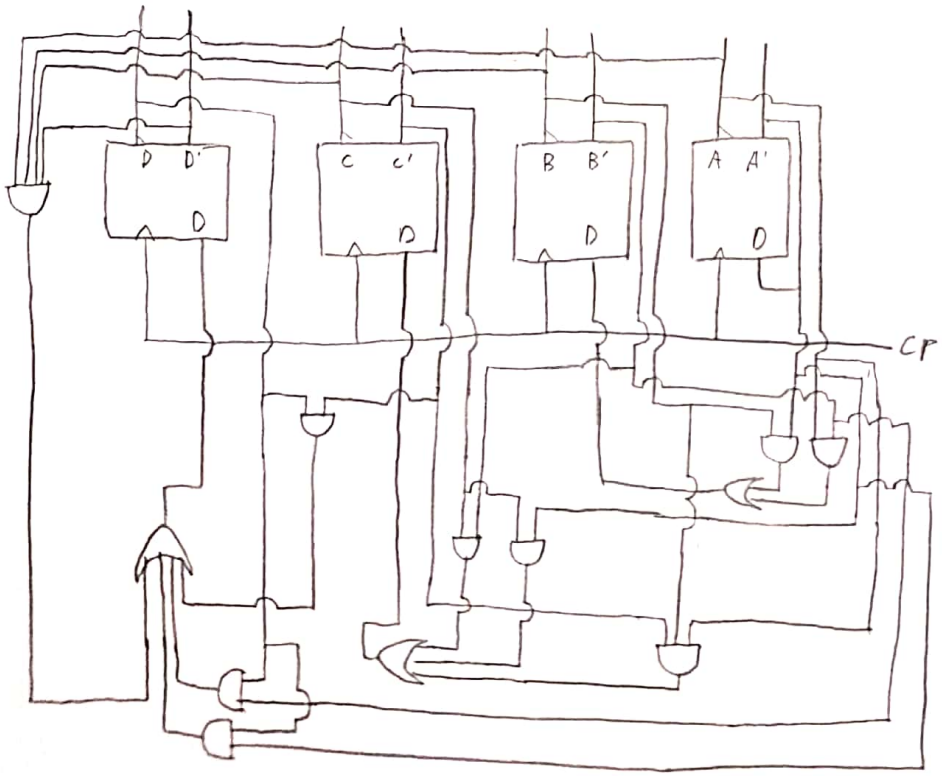
$Db = B'A + BA'$

• Da

BA \ DC	00	01	11	10
00	1	1	1	1
01	0	0	0	0
11	0	0	0	0
10	1	1	1	1

$Da = A'$

⑤ Circuit diagram



2. JK Flip Flop (state diagram 상태도)

① State table

D	C	B	A	D^*	C^*	B^*	A^*	J_DK_D	J_CK_C	J_BK_B	J_AK_A
0	0	0	0	0	0	0	1	0X	0X	0X	1X
0	0	0	1	0	0	1	0	0X	0X	1X	X1
0	0	1	0	0	0	1	1	0X	0X	X0	1X
0	0	1	1	0	1	0	0	0X	1X	X1	X1
0	1	0	0	0	1	0	1	0X	X0	0X	1X
0	1	0	1	0	1	1	0	0X	X0	1X	X1
0	1	1	0	0	1	1	1	0X	X0	X0	1X
0	1	1	1	1	0	0	0	1X	X1	X1	X1
1	0	0	0	1	0	0	1	X0	0X	0X	1X
1	0	0	1	1	0	1	0	X0	0X	1X	X1
1	0	1	0	1	0	1	1	X0	0X	X0	1X
1	0	1	1	1	1	0	0	X0	1X	X1	X1
1	1	0	0	1	1	0	1	X0	X0	0X	1X
1	1	0	1	1	1	1	0	X0	X0	1X	X1
1	1	1	0	1	1	1	1	X0	X0	X0	1X
1	1	1	1	0	0	0	0	X1	X1	X1	X1

② JK-FF Excitation Table

Q	Q^*	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

③ Karnaugh map

J_D

BA \ DC	00	01	11	10
00	0	0	X	X
01	0	0	X	X
11	0	1	X	X
10	0	0	X	X

$J_D = CBA$

K_D

BA \ DC	00	01	11	10
00	X	X	0	0
01	X	X	0	0
11	X	X	1	0
10	X	X	0	0

$K_D = CBA$

J_C

BA \ DC	00	01	11	10
00	0	X	X	0
01	0	X	X	0
11	1	X	X	1
10	0	X	X	0

$J_C = BA$

K_C

BA \ DC	00	01	11	10
00	X	0	0	X
01	X	0	0	X
11	X	1	1	X
10	X	0	0	X

$K_C = BA$

J_B

BA \ DC	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	X	X	X	X
10	X	X	X	X

$J_B = A$

K_B

BA \ DC	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	1	1	1	1
10	0	0	0	0

$K_B = A$

J_A

BA \ DC	00	01	11	10
00	1	1	1	1
01	X	X	X	X
11	X	X	X	X
10	1	1	1	1

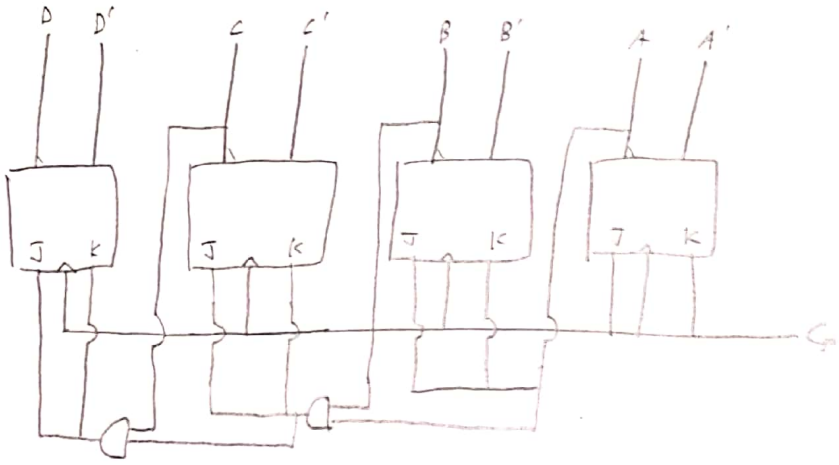
$J_A = 1$

K_A

BA \ DC	00	01	11	10
00	X	X	X	X
01	1	1	1	1
11	1	1	1	1
10	X	X	X	X

$K_A = 1$

(d) Circuit diagram



3. T Flip Flop (State diagram 생략)

① State table

D	C	B	A	D^*	C^*	B^*	A^*	T_D	T_C	T_B	T_A
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	1	0	1	0	0	0	1	1
1	0	1	0	1	0	1	1	0	0	0	1
1	0	1	1	1	1	0	0	0	1	1	1
1	1	0	0	1	1	0	1	0	0	0	1
1	1	0	1	1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1	0	0	0	1
1	1	1	1	0	0	0	0	1	1	1	1

② T-FF excitation table

D	D^*	T
0	0	0
0	1	1
1	0	1
1	1	0

③ Karnough map

T_D

BA \ DC	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	1	1	0
10	0	0	0	0

$T_D = CBA$

T_C

BA \ DC	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	0	0

$T_C = BA$

T_B

BA \ DC	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	1	1
10	0	0	0	0

$T_B = A$

T_A

BA \ DC	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$T_A = 1$

④ circuit diagram