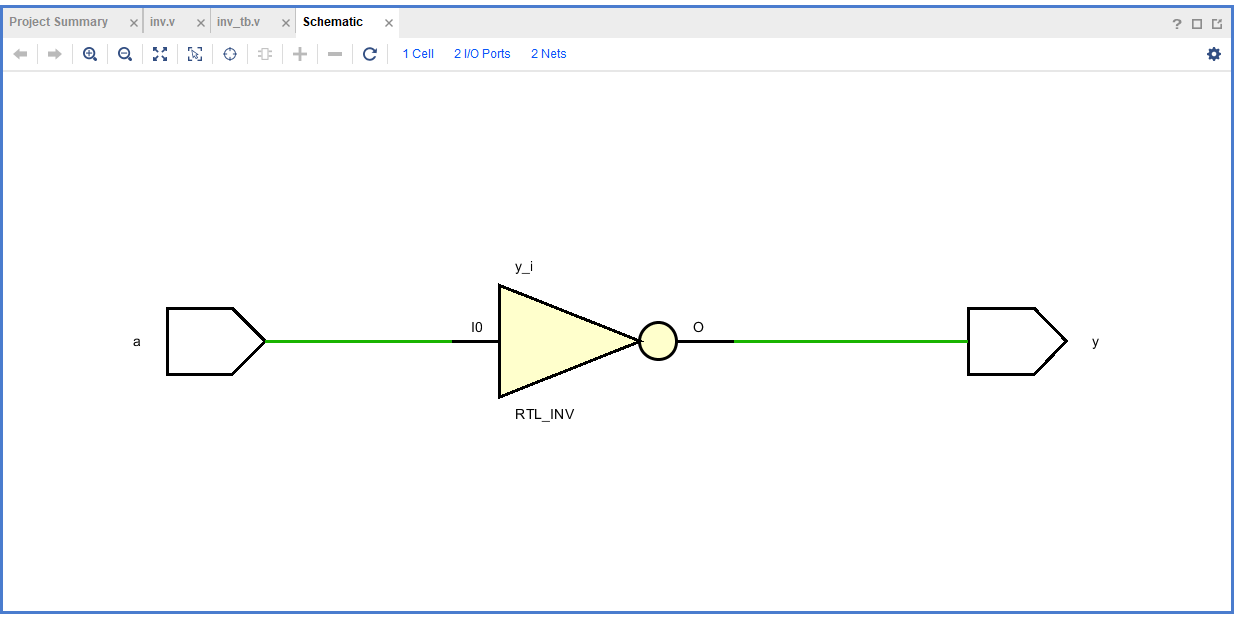
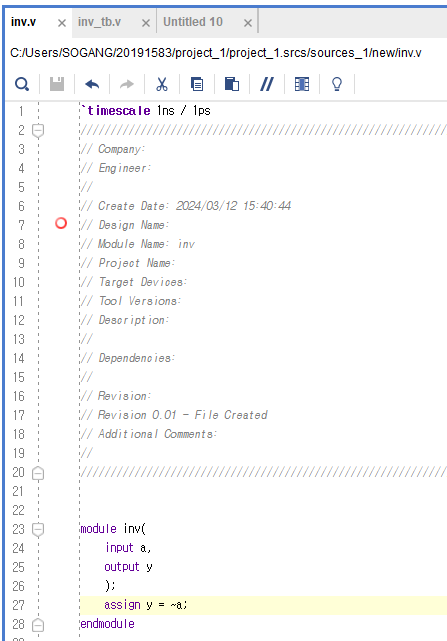
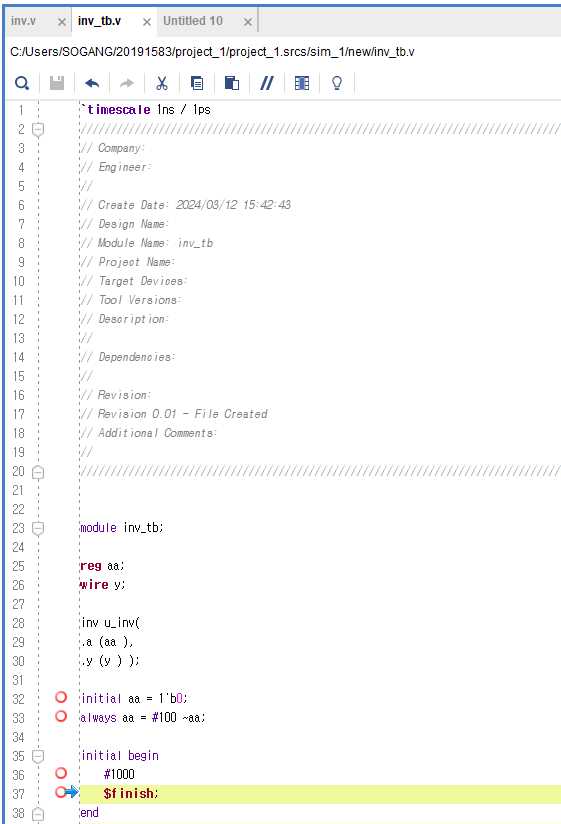
A번 문제



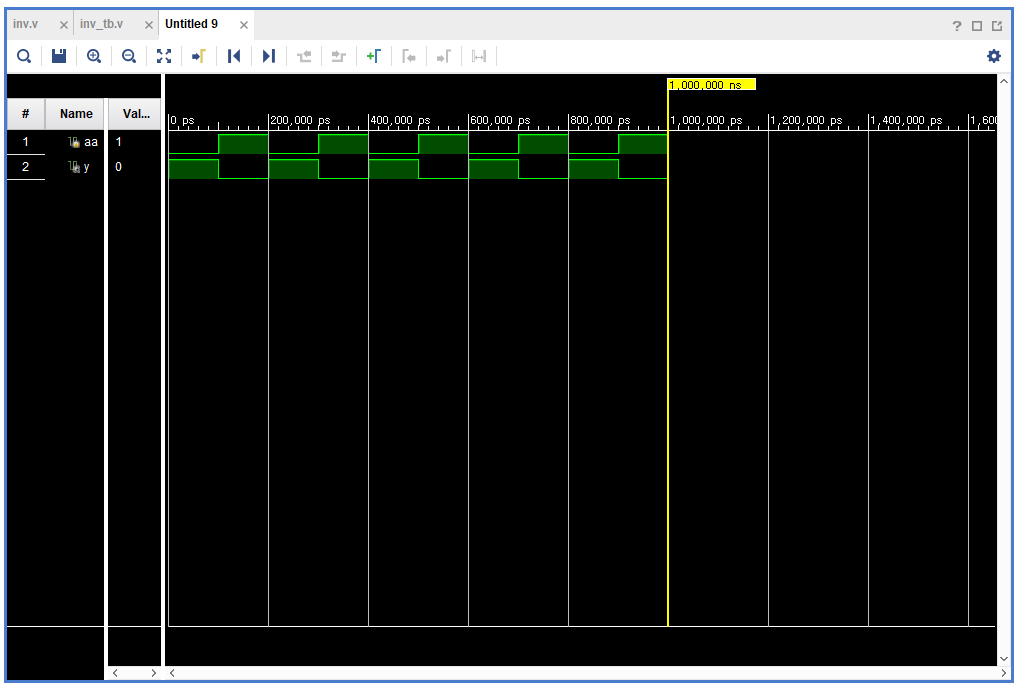
1. A의 Verilog file



1. A의 testbench file

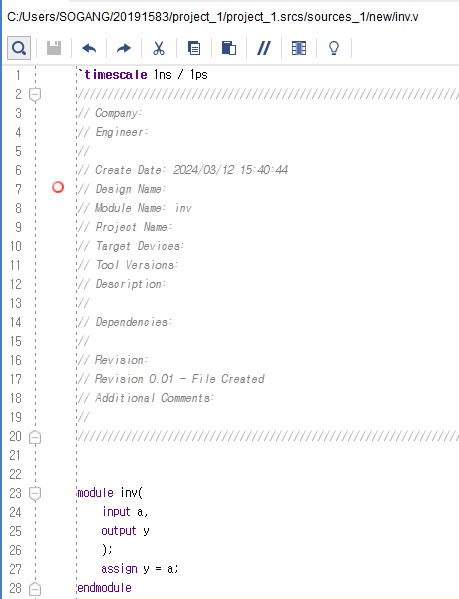


3) A의 simulation 결과

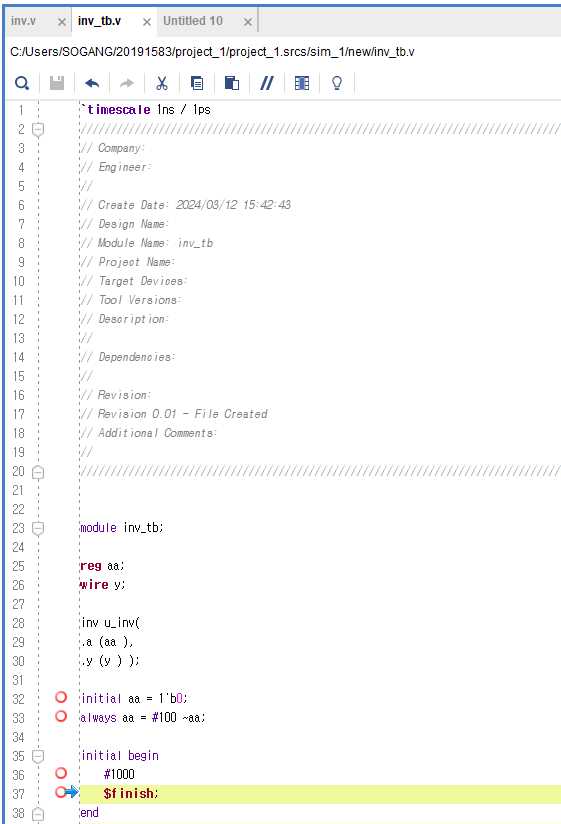


B번 문제

1. B의 Verilog file



1. B의 testbench file



1. B의 simulation 결과

