

# JIAYI (TRIS) TIAN

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## EDUCATION

### Nanjing University

School of Electronic Science and Engineering

Nanjing, China

Sept. 2019- Jul. 2023

- B.Eng., Major in VLSI Design & System Integration
- **Cumulative GPA: 4.51/5.0; Major GPA: 4.49/5.0 (Top 10% in the grade)**

## PREPRINTS

- **Jiayi Tian**, Chao Fang, Haonan Wang and Zhongfeng Wang. "BEBERT: Efficient and robust binary ensemble BERT." *IEEE Conference on Acoustics, Speech, and Signal Processing (ICASSP)*. 2023 [[under review](#)]

## RESEARCH EXPERIENCE

### Binary Quantization for Transformer-based Models Accelerator Design with Hardware Deployment

Member, ICAIS Lab, Nanjing University.

Nov. 2022- June. 2023

- Plan to use Python and Pytorch to perform full binarization in BERT and ViT with accuracy improvement.
- Plan to use Matlab to achieve important operations in binary BERTs for further hardware coding and then use Verilog to devise binary BERT operations in FPGA for efficient inference.
- Investigated literature on state-of-the-art binarization neural networks.
- Trying to use Python and Pytorch to accomplish an existing ensemble algorithm with the early-exit mechanism and apply it to binary BERT models for efficient and accurate inference design.

### Optimization for Phase Retrieval using DNN in Diffractive Neural Field

Sept. 2022- Mar. 2023

Independent project, Vision Lab, Nanjing University.

- Plan to use Python and Pytorch to improve the PSNR of phase retrieval using DNN in a diffractive neural field.
- Used Python and Pytorch to apply various mathematic operations in simple image reconstruction to check out the possible ones that harm the phase retrieval.
- Trying to use Python and Pytorch to optimize the parameter gradient to accelerate convergence and provide additional forward solutions to improve the performance.

### INT8 Quantization for BERT Accelerator Design with Hardware Deployment

Sept. 2021- Apr. 2023

Member, ICAIS Lab, Nanjing University.

- Used Python and Pytorch to perform INT8 quantization in BERT models and plan to deploy it in hardware.
- Used Matlab to achieve critical operations (Attention, Softmax. etc.) for further hardware coding.
- Trying to use Verilog to deploy INT8 BERT in FPGA for text classification.

### Low-bit Quantization for BERT Accelerator Design

Apr. 2021- Oct. 2022

Independent project, ICAIS Lab, Nanjing University.

- Used Python and Pytorch to perform low-bit quantization with ensemble methods in BERT models.
- Investigated literature on Transformer-based models and various model compression methods.
- Proposed Binary Ensemble BERT (BEBERT), a novel compression scheme to boost the efficiency and robustness of binary BERT, outperforming the existing binary models by **2%~4%** in accuracy, reducing variance by around **60%**, and achieves **2x** acceleration in the training process.
- Submitted the paper "BEBERT: Efficient and robust binary ensemble BERT" to ICASSP23.
- Participated in manuscripts reviewing work for TCAS-II.

## COURSE PROJECTS

### VLSI Design Experiment

Mar. 2022- Jun. 2022

Individual assignment, A (top 5%)

- Used Vivado and Cadence to devise efficient coding for computing one-dimension convolution.
- Proposed three optimization methods based on basic VLSI techniques, including pipeline, parallel, and transpose, to accelerate the convolution process and reduce the area.
- Wrote a report in 11 pages by Latex and got an A score (top 5%).

### Verilog Design Experiment

Mar. 2021- Jun. 2021

Member, A+

- Used Quartus and Intel Cyclone5 Series' FPGA to complete a VGA display clock on the monitor, which could set up time by typing on the keyboard.
- Analyzed the temporal logic of the VGA interface to achieve the correct time sequence and used RAM to store the address for the hands of the clock displayed on the screen.
- Wrote a report in 17 pages by Latex and got an A+ score.

## TECHNICAL SKILLS

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- Programming and HDL:  
Advanced in C/Matlab, Proficient in Verilog, Python/Pytorch, Familiar with C++
- Hardware design and simulation tools:  
Advanced in Vivado/Quartus/Modelsim, Altium Designer, and Multisim, Familiar with SPICE
- Languages: TOEFL 102; GRE V153+Q170+W3.5

## HONORS AND AWARDS

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- Excellent Volunteer Prize on the school's 120th anniversary, Sept. 2022 (<1%)
- Excellent Volunteer Prize, NJU, Dec. 2021 (<1%)
- Jinxiao Company Scholarship, Nov. 2021 (5%)
- People's Scholarship, The Academic Competition Award, Nov. 2021 (5%)
- National Undergraduate Electronic Design Contest, The 2nd Prize in Jiangsu Province, Nov. 2021 (30%)
- Excellent Department Director, Student Union in Sch of Elec Sci and Eng., NJU, Oct. 2021 (15%)
- People's Scholarship, The 2nd Prize in NJU, Nov. 2020 (10%)
- National Undergraduate Electronic Design Contest, The 2nd Prize in Jiangsu Province, Oct. 2020 (30%)
- Excellent Organization Award, Student Union in Sch of Elec Sci and Eng., NJU, Sept. 2020 (20%)

## EXTRA-CURRICULAR EXPERIENCE

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**Vice-chairman** Sept. 2021-Sept. 2022

*School Badminton Association, Nanjing University.*

- Organized large-scale sports events and contests in NJU; the number of participants is up to hundreds.

**Captain** Sept. 2021-Sept. 2022

*Women's Volleyball Team, Sch of Elec Sci and Eng.*

- Won the 4th prize in the 2019-2020 departmental contest and the 3rd prize in the 2020-2021 departmental contest.

**Department Director** Sept. 2020- Sept. 2021

*Organization Department, Student Union in Sch of Elec Sci and Eng.*

- Organized school social practice, volunteer work, and extracurricular activities.