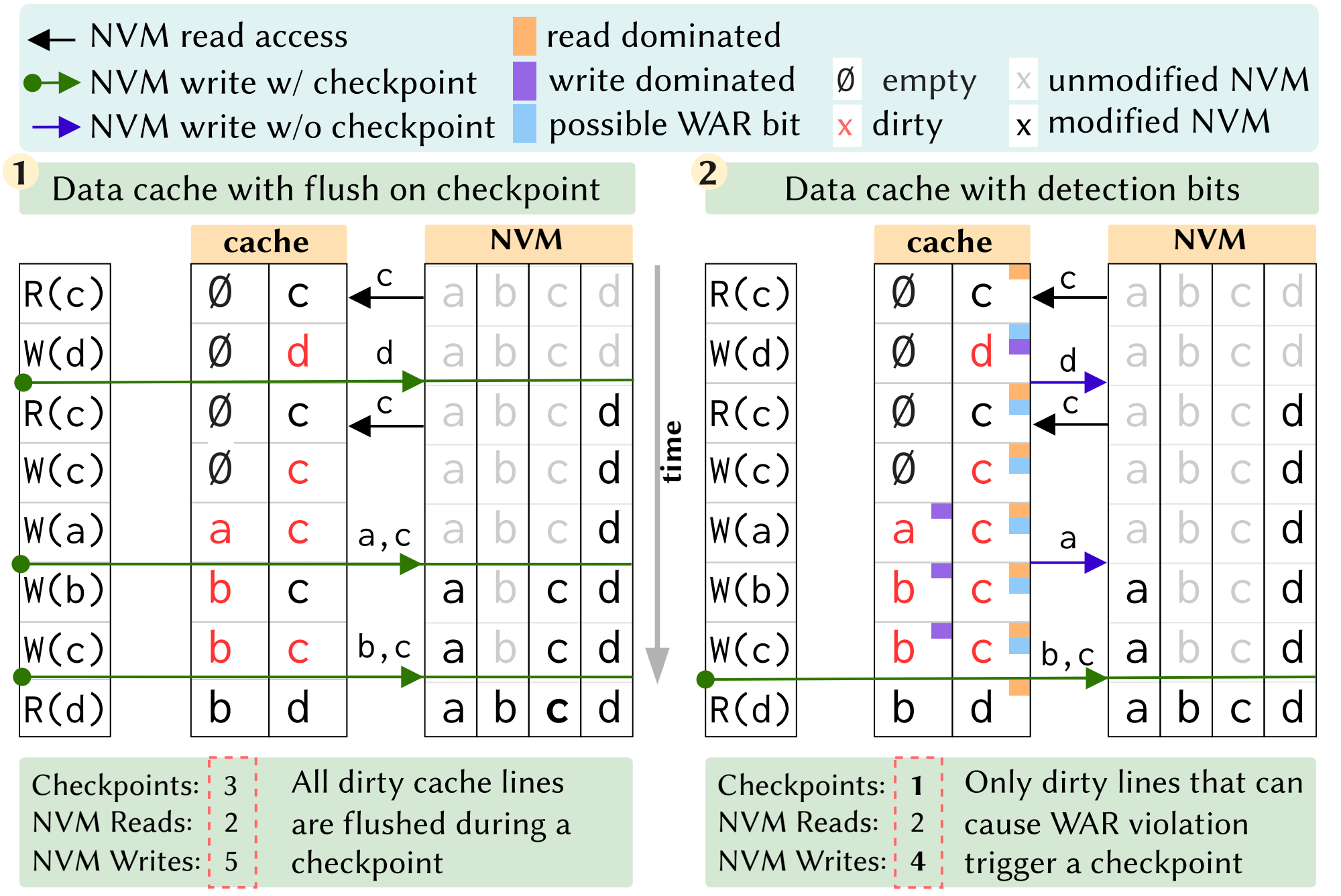
NVM read access
NVM write w/ checkpoint
NVM write w/o checkpoint
read dominated
write dominated
possible WAR bit
Ø empty
x dirty
x unmodified NVM
x modified NVM
1
Data cache with flush on checkpoint
cache
NVM
R(c)
W(d)
R(c)
W(c)
W(a)
W(b)
W(c)
R(d)
c
d
c
a, c
b, c
time
Checkpoints: 3
NVM Reads: 2
NVM Writes: 5
All dirty cache lines are flushed during a checkpoint
2
Data cache with detection bits
cache
NVM
R(c)
W(d)
R(c)
W(c)
W(a)
W(b)
W(c)
R(d)
c
d
c
a
b, c
Checkpoints: 1
NVM Reads: 2
NVM Writes: 4
Only dirty lines that can cause WAR violation trigger a checkpoint