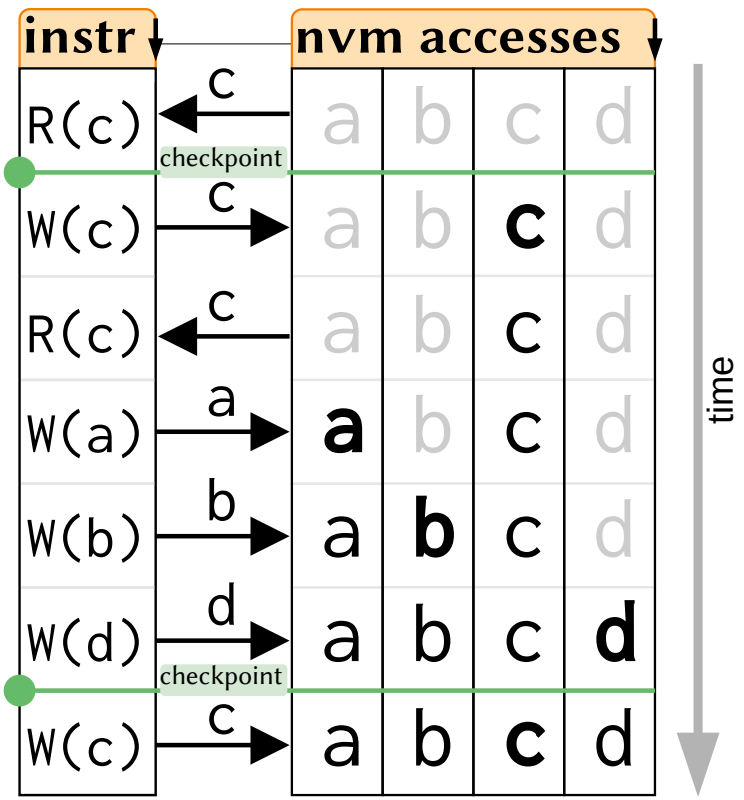
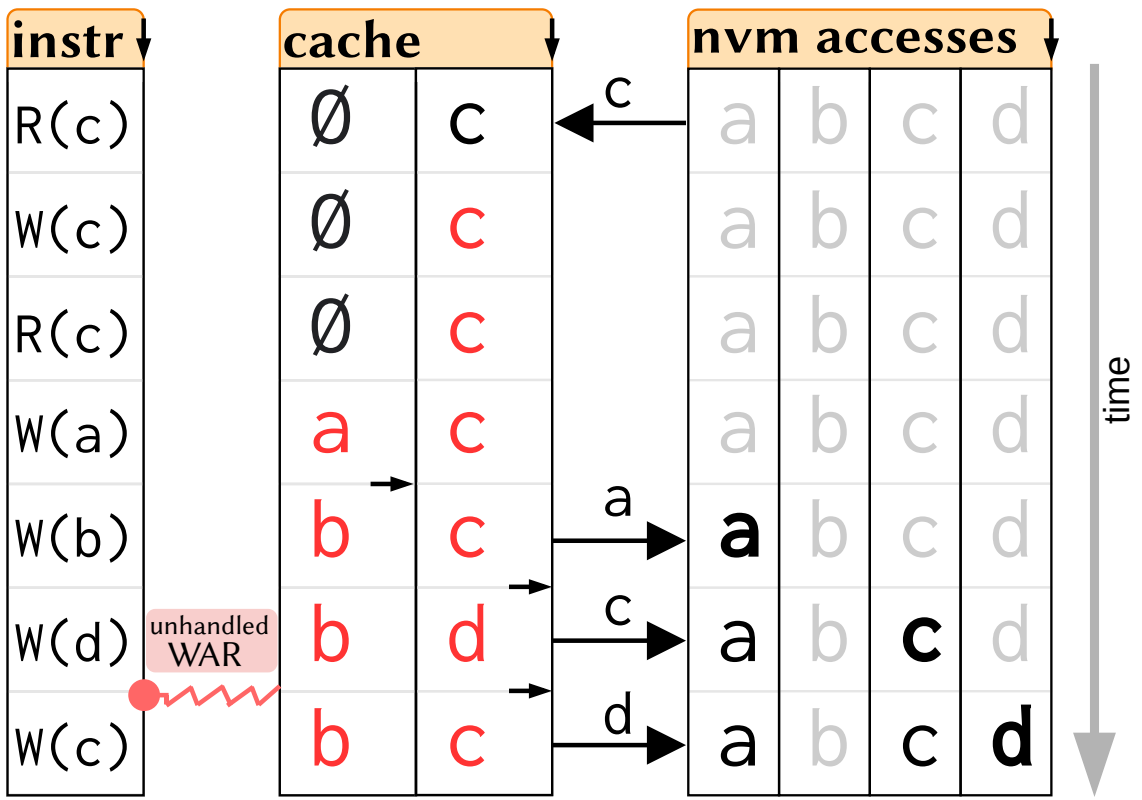
Traditional intermittent systems with no data cache



Checkpoints: 2
NVM Reads: 2
NVM Writes: 5

Checkpoint triggered by WAR violation

A naive intermittent system with a simple data cache but no additional support



Checkpoints: NA
NVM Reads: 1
NVM Writes: 3

WAR occurs when cache evicts 'c'. Without support, intermittent execution not possible