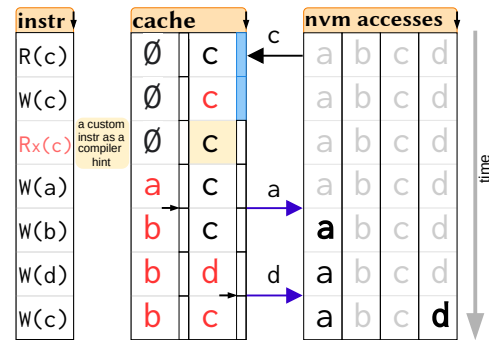
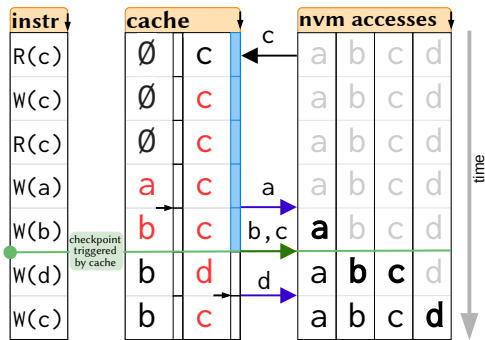
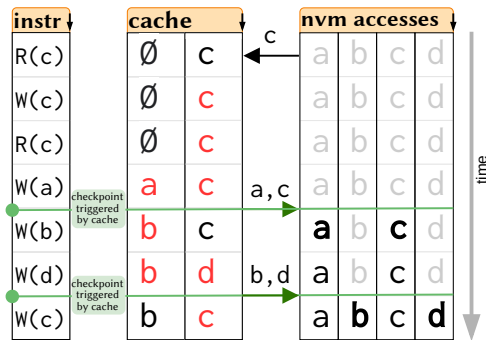


1 Data cache with flush on checkpoint

2 With possible WAR bit but no hints

3 With both possible WAR bit and hints



Checkpoints: 2
NVM Reads: 1
NVM Writes: 4

Checkpoints: 1
NVM Reads: 1
NVM Writes: 4

Checkpoints: 0
NVM Reads: 1
NVM Writes: 2

Number of checkpoints halved while NVM access remained the same

Completely removed checkpoints while NVM writes halved

Legend

← NVM read access

→ NVM write as part of checkpoint

→ NVM write on eviction without a checkpoint

a clean NVM mem

a NVM that is just written to

a dirty NVM mem

→ cache eviction

possible WAR bit

Rx(c) custom instr

a dirty cache

∅ empty cache

cache block marked clean