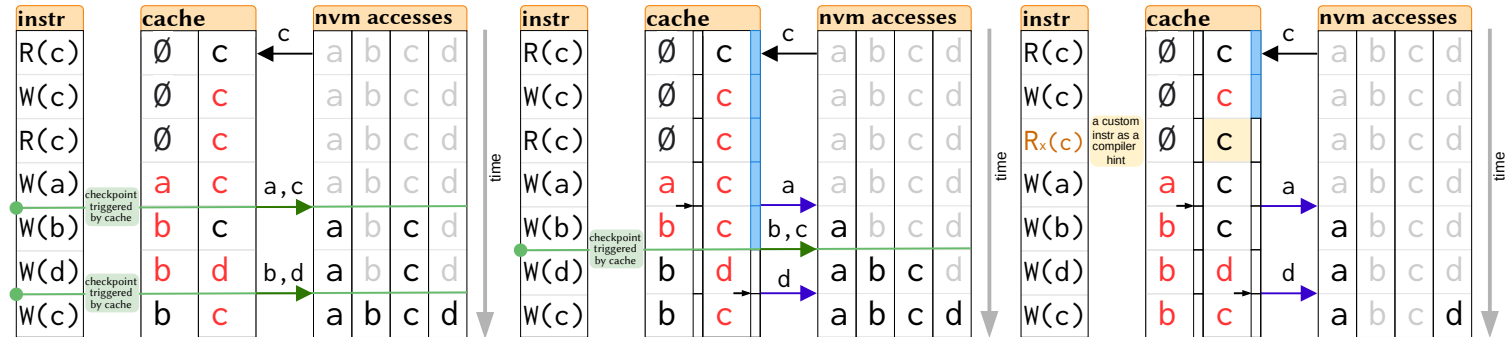


1 Data cache with flush on checkpoint

2 With possible WAR bit but no hints

3 With both possible WAR bit and hints



Checkpoints: 2
NVM Reads: 1
NVM Writes: 4

All dirty cache lines are flushed during a checkpoint

Checkpoints: 1
NVM Reads: 1
NVM Writes: 4

Only dirty lines that can cause WAR are flushed

Checkpoints: 0
NVM Reads: 1
NVM Writes: 2

Specific dirty lines are marked clean using compiler hints

Number of checkpoints halved while NVM access remained the same

Completely removed checkpoints while NVM writes halved

Legend

← NVM read access a clean NVM mem → cache eviction a dirty cache → NVM write w/ checkpoint cache block marked clean
 ● Checkpoint a dirty NVM mem possible WAR bit ∅ empty cache → NVM write w/o checkpoint R_x(c) custom instr