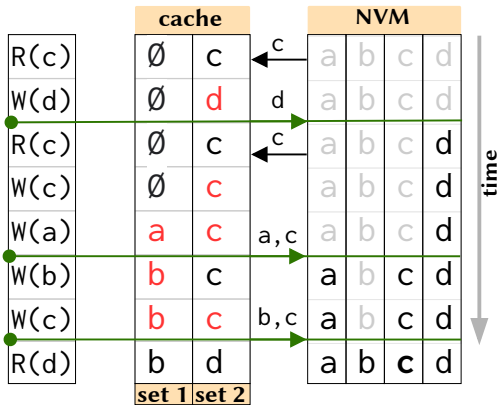


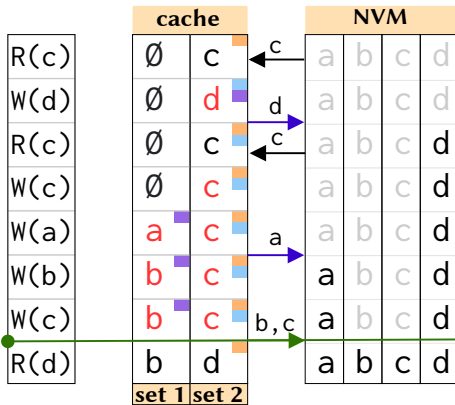
1 Data cache with flush on checkpoint



Checkpoints: 3
 NVM Reads: 2
 NVM Writes: 5

All dirty cache lines are flushed during a checkpoint

2 Data cache with detection bits



Checkpoints: 1
 NVM Reads: 2
 NVM Writes: 4

Only dirty lines that can cause WAR violation trigger a checkpoint