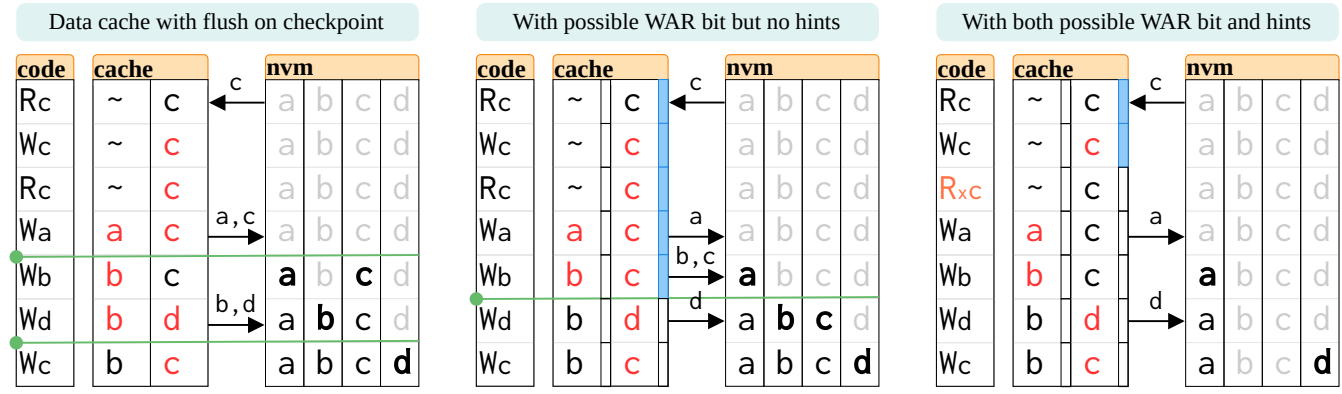
Data cache with flush on checkpoint
code
cache
nvm
Rc
Wc
Rc
Wa
Wb
Wd
Wc
~ c
~ c
~ c
a c
b c
b d
b c
a b c d
c
a, c
b, d
Checkpoints: 2
NVM Reads: 1
NVM Writes: 4
All dirty cache lines are flushed during a checkpoint
With possible WAR bit but no hints
Rc
Wc
Rc
Wa
Wb
Wd
Wc
a
b, c
d
Checkpoints: 1
NVM Reads: 1
NVM Writes: 4
Only the dirty lines that can cause WAR are flushed
With both possible WAR bit and hints
Rc
Wc
Rxc
Wa
Wb
Wd
Wc
a
d
Checkpoints: 0
NVM Reads: 1
NVM Writes: 2
Specific dirty lines are marked clean using compiler hints