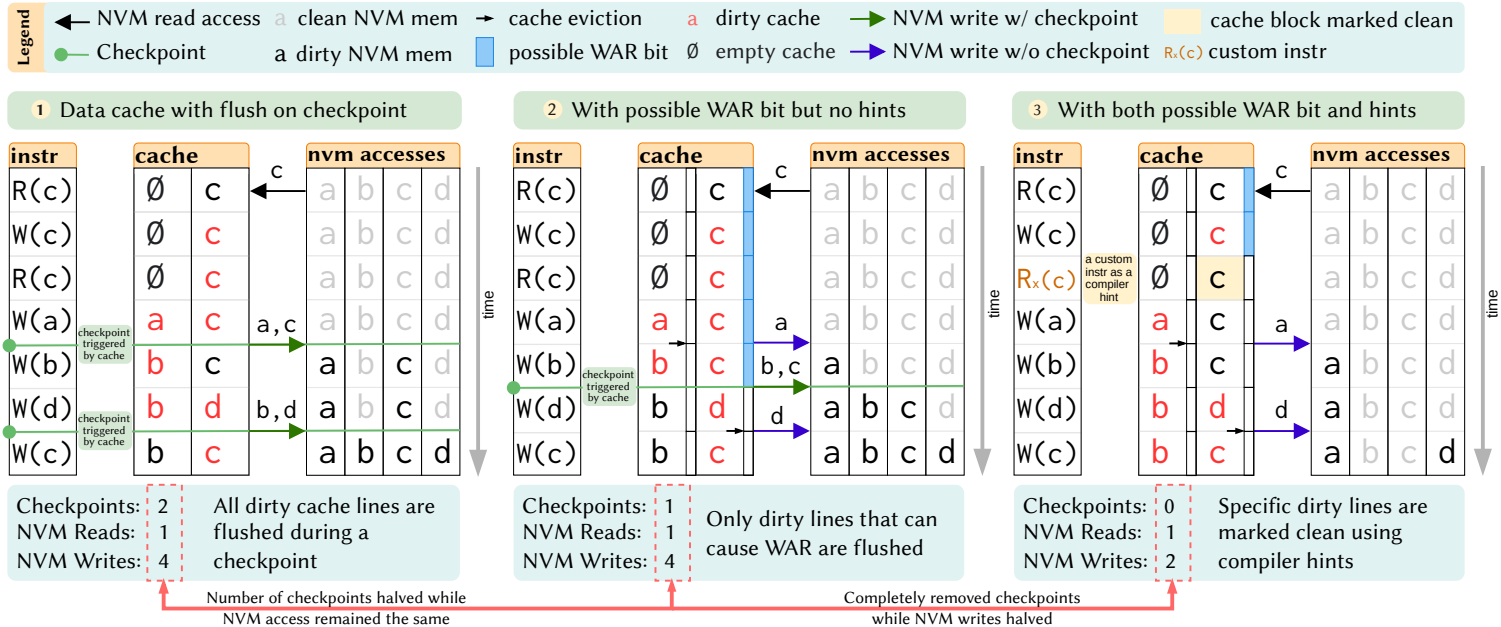
Legend
NVM read access
Checkpoint
clean NVM mem
dirty NVM mem
cache eviction
possible WAR bit
dirty cache
empty cache
NVM write w/ checkpoint
NVM write w/o checkpoint
cache block marked clean
custom instr
1 Data cache with flush on checkpoint
2 With possible WAR bit but no hints
3 With both possible WAR bit and hints
instr
cache
nvm accesses
time
checkpoint triggered by cache
a custom instr as a compiler hint
Checkpoints: 2
NVM Reads: 1
NVM Writes: 4
All dirty cache lines are flushed during a checkpoint
Checkpoints: 1
NVM Reads: 1
NVM Writes: 4
Only dirty lines that can cause WAR are flushed
Checkpoints: 0
NVM Reads: 1
NVM Writes: 2
Specific dirty lines are marked clean using compiler hints
Number of checkpoints halved while NVM access remained the same
Completely removed checkpoints while NVM writes halved