Mitigating Branch Predictor Latency with Hierarchical Design — an Analysis

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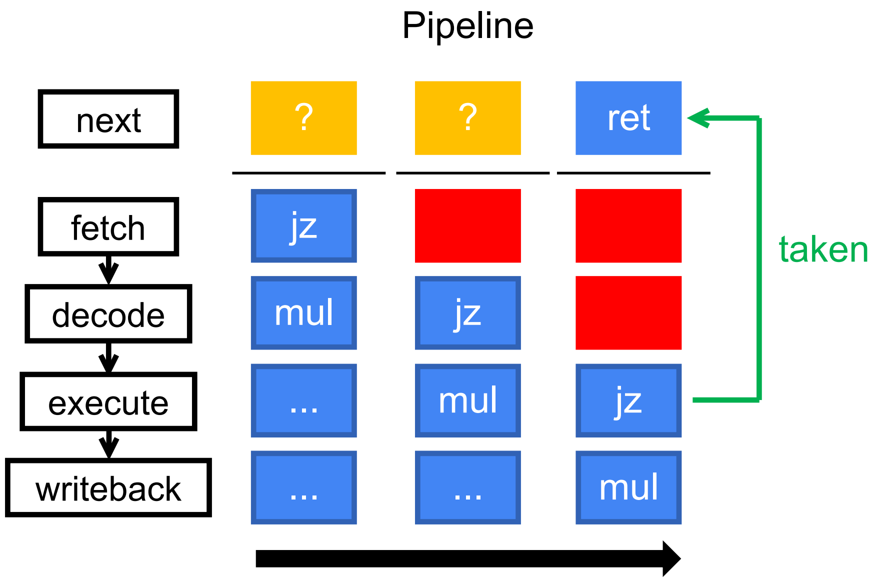
Branch prediction

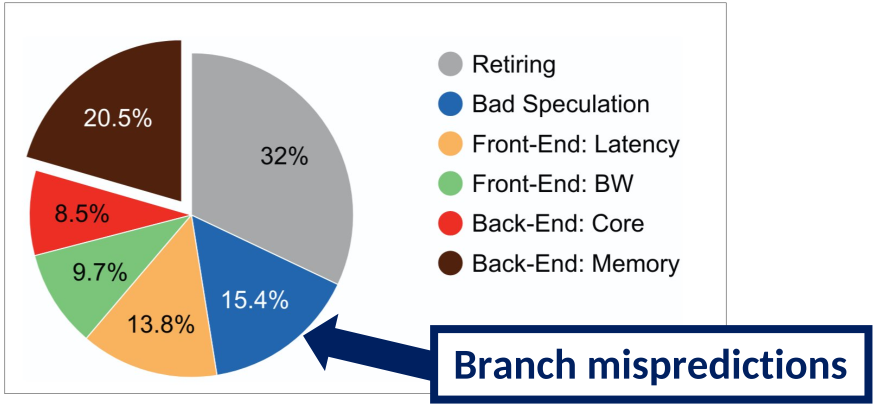


- Modern processors use **heavily pipelined** out-of-order execution [4]
- CPU cannot fetch the next instructions until branch direction is known

➡ **Branch prediction is required for effective pipelining**

Branch prediction

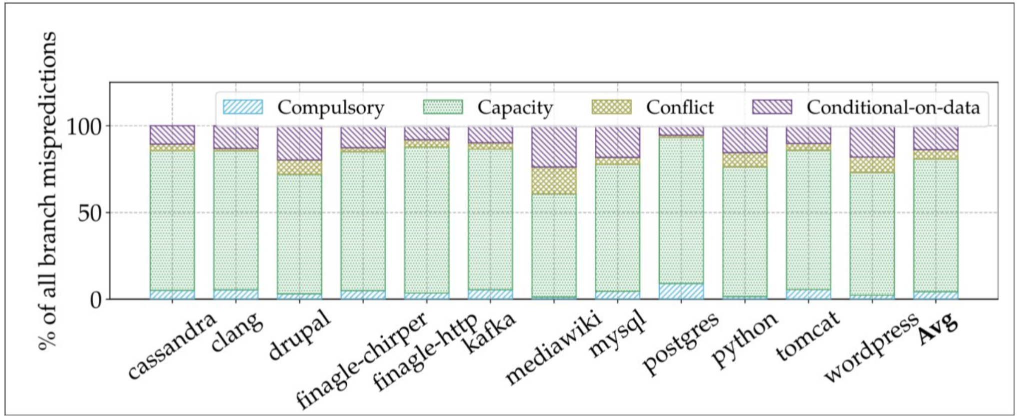
- Branch prediction is still a bottleneck in today’s processors:
  - Over 9% of cycles lost (avg) to mispredictions even on recent server processors [3]
  - 15.4% of pipeline slots wasted to branch mispredictions in Google’s datacenters [2]



Google; Top-down breakdown of search workload [2]

The capacity bottleneck

- The instruction footprint of datacenter workloads is growing [13]
- Branch predictors cannot keep up:
  - Over 75% of mispredictions in large server workloads are caused by a lack of storage capacity [14]

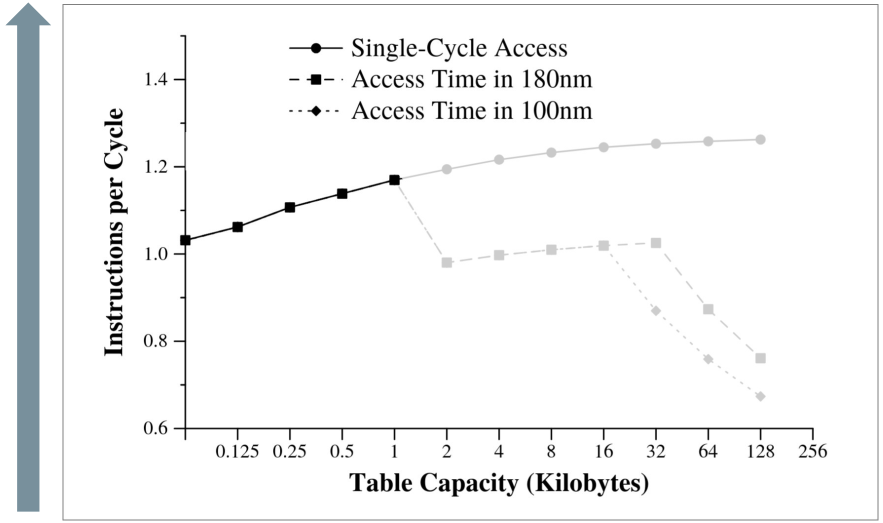


Whisper; Breakdown of branch mispredictions
Various server workloads [14]

➡ **Larger predictors needed to deal with growing branch working set**

Up-scaling alone is not the solution

Larger storage size ➡ Increased access latency



Theoretical improvement

With latency

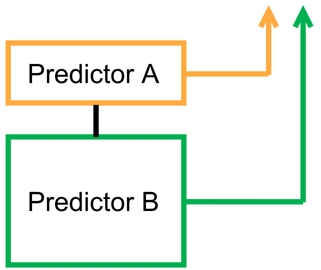
Jiménez et al; IPC vs table capacity, gshare predictor [8]

➡ Latency can be a performance limiter

Reduced latency with hierarchical designs

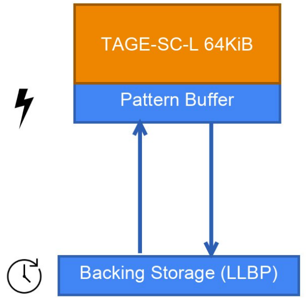
Overriding branch prediction

Commonly implemented in modern processors, **state-of-the-art**



The Last-Level Branch Predictor [3]

New design from MICRO '24

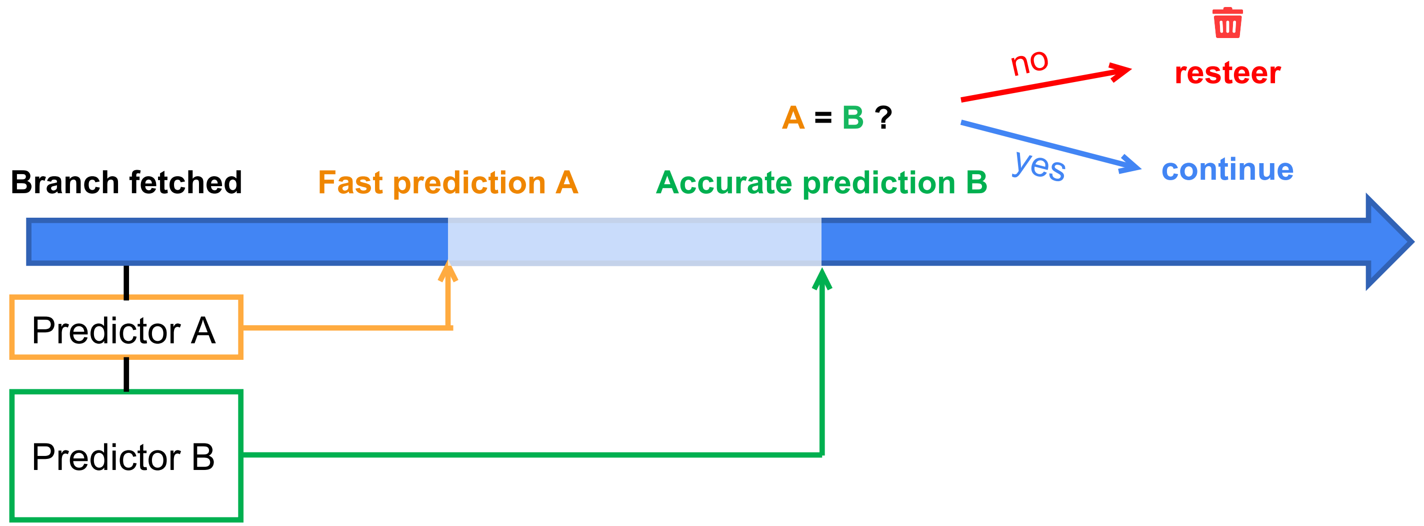


Overriding branch predictors

Two predictors:

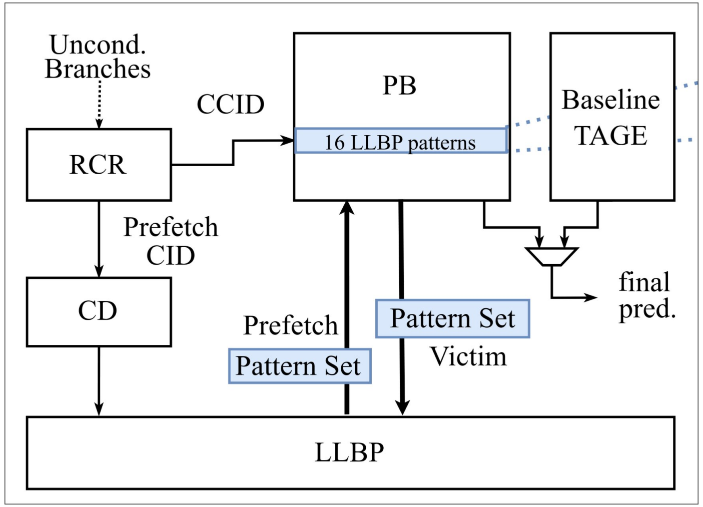
- Small, fast predictor A ➡ low latency
- Large, slow predictor B ➡ high accuracy

➡ **Hides long access latency of predictor B**

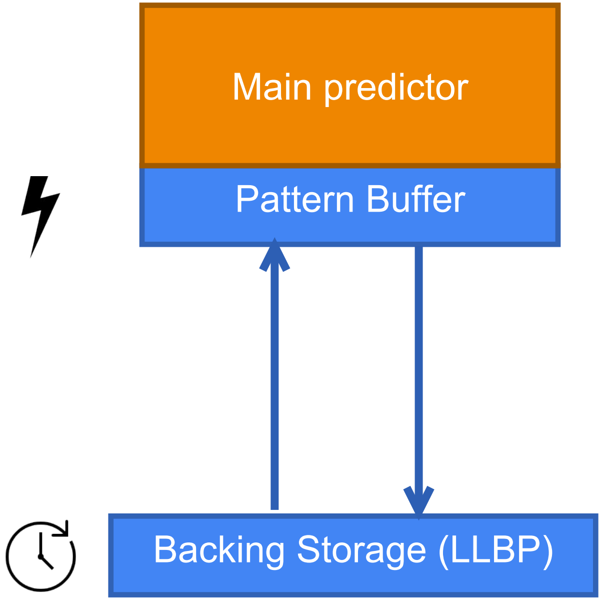


The Last-Level Branch Predictor (LLBP) [3]

- Extends a state-of-the-art TAGE-SC-L predictor
- Prefetching from backing storage ➡ **better accuracy — same latency**



Overview of LLBP from the paper [3]



Research gap & Problem statement

➡ **How effective are these approaches? Does predictor latency still have a large impact in modern processors?**

Problem Statement: Evaluating the impact of latency on state-of-the-art branch prediction and different latency mitigation schemes

Research Questions:

1. How large is the **impact of predictor latency** on performance?
2. Can **overriding prediction** reduce this penalty?
3. Is a recent approach, **The Last-Level Branch Predictor**, more effective?

The gem5 hardware simulator [9]

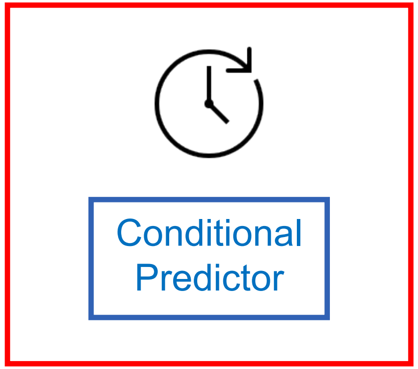
- Open-source execution-based hardware simulator (similar to hypervisor)
- Supports modeling a **detailed out-of-order CPU pipeline**

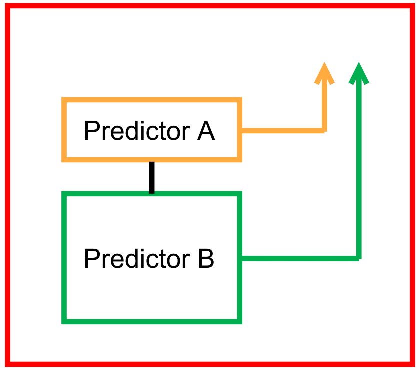
- False path execution is simulated, important for branch predictor evaluation
- **Models state-of-the-art decoupled frontend** [15]

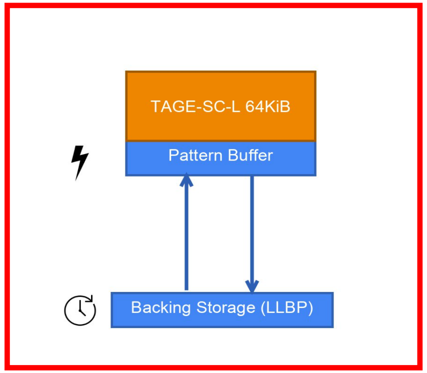
➡ **Allows for detailed evaluation of branch predictor behavior**

The missing link: Branch prediction in gem5

- gem5 is **missing features** for realistic branch prediction that are present in modern CPUs
- Most notably **latency modeling** and **overriding prediction** are not implemented, instead every prediction is available instantly







[1]

➡ **Need a framework for more realistic branch prediction simulation in gem5**

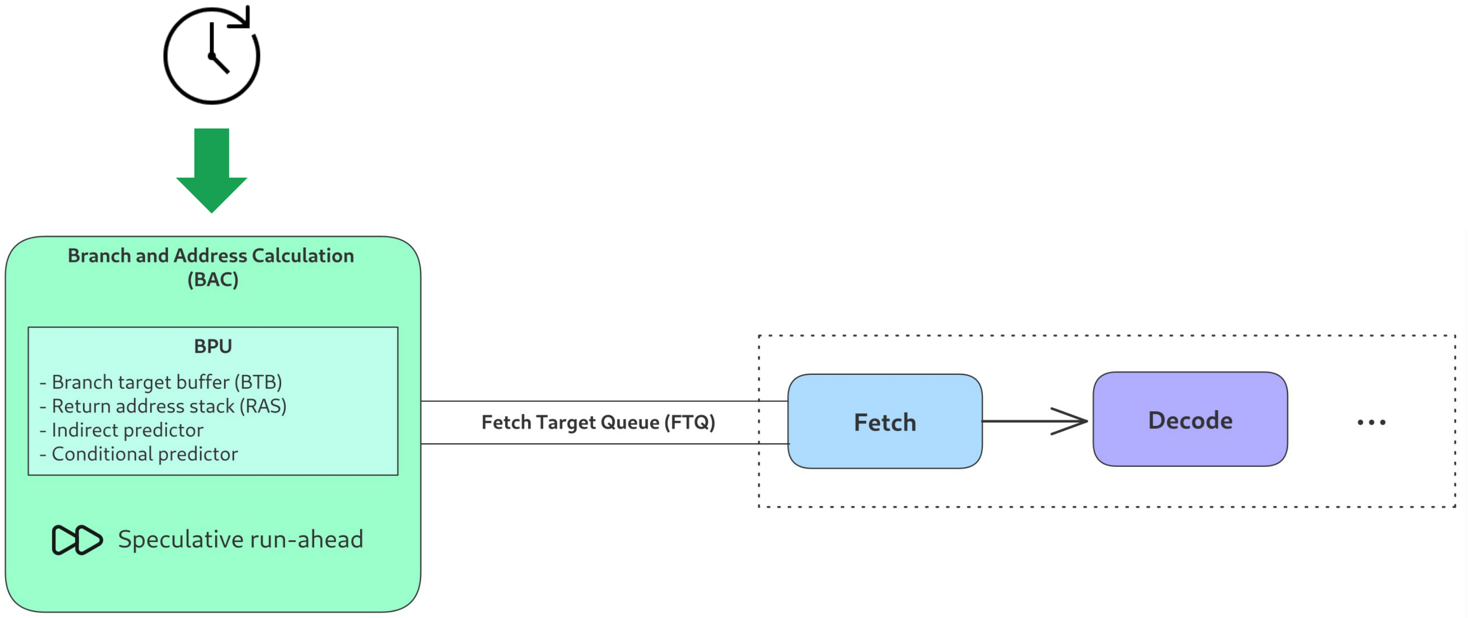
1 An initial prototype of LLBP for gem5 was implemented by the University of Wisconsin

Outline

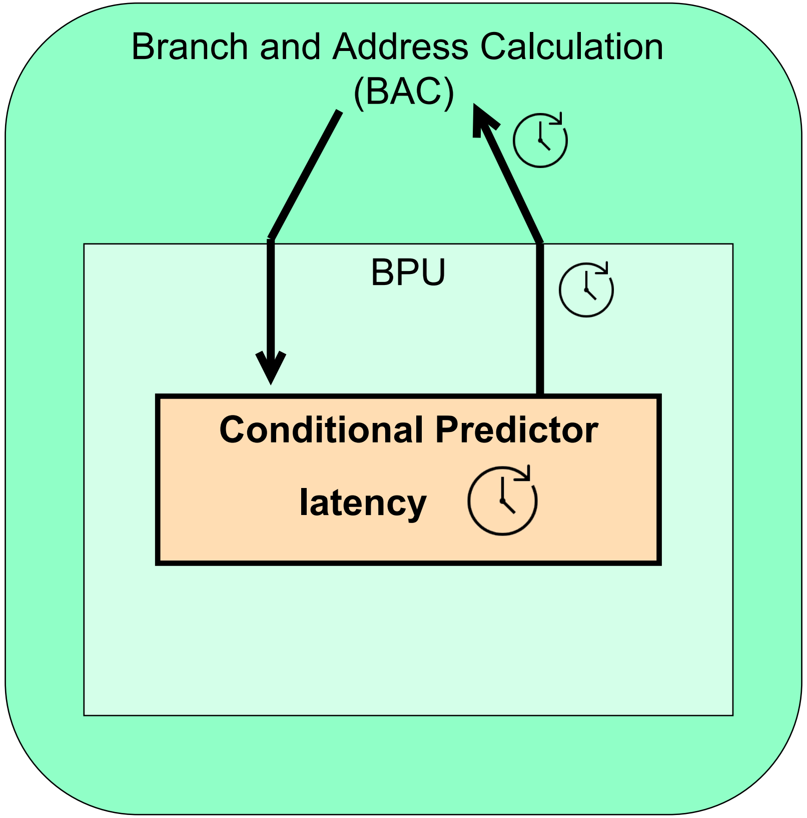
- ~~Motivation & Background~~
- Design
  - Modeling prediction latency in gem5
  - Overriding branch predictors
  - LLBP implementation
- Evaluation
- Conclusion

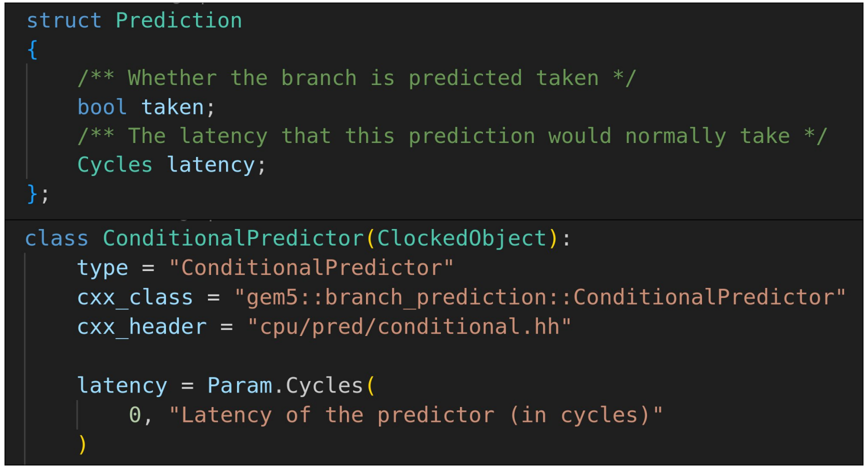
Modeling prediction latency in gem5

- Branch predictor is **decoupled from fetch**, runs ahead of instruction stream
- Predictor latency **only directly impacts the BAC stage**



Modeling prediction latency in gem5



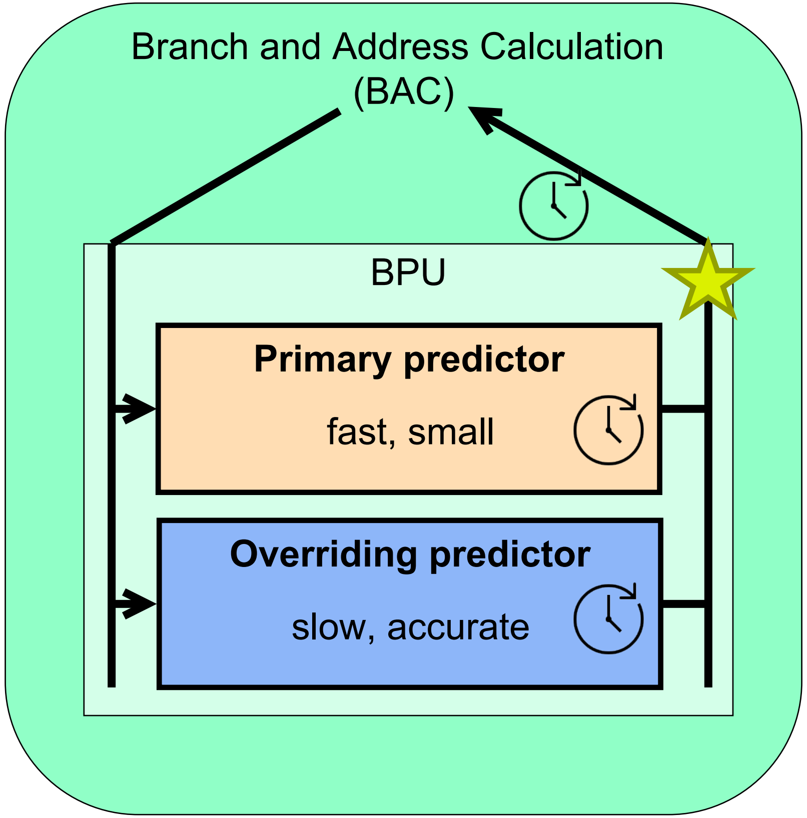


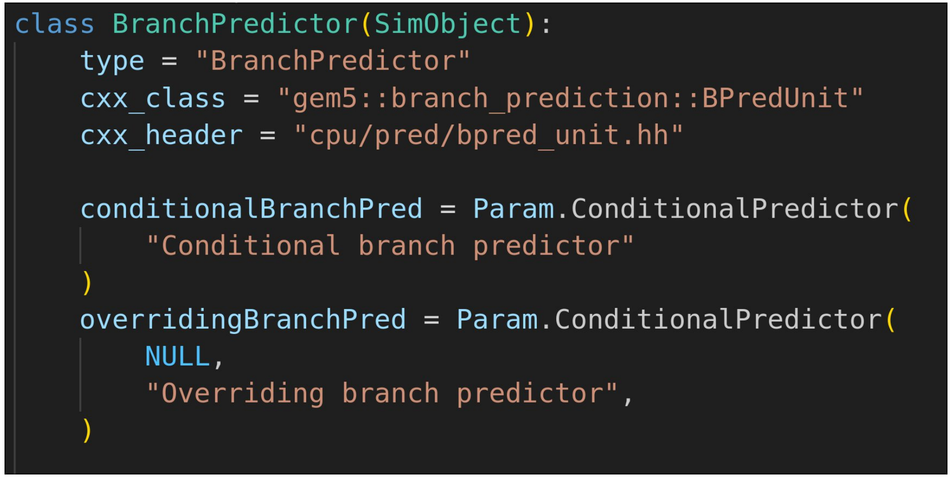
```
struct Prediction
{
    /** Whether the branch is predicted taken */
    bool taken;
    /** The latency that this prediction would normally take */
    Cycles latency;
};
```

```
class ConditionalPredictor(ClockedObject):
    type = "ConditionalPredictor"
    cxx_class = "gem5::branch_prediction::ConditionalPredictor"
    cxx_header = "cpu/pred/conditional.hh"

    latency = Param.Cycles(
        0, "Latency of the predictor (in cycles)"
    )
```

Overriding prediction in gem5

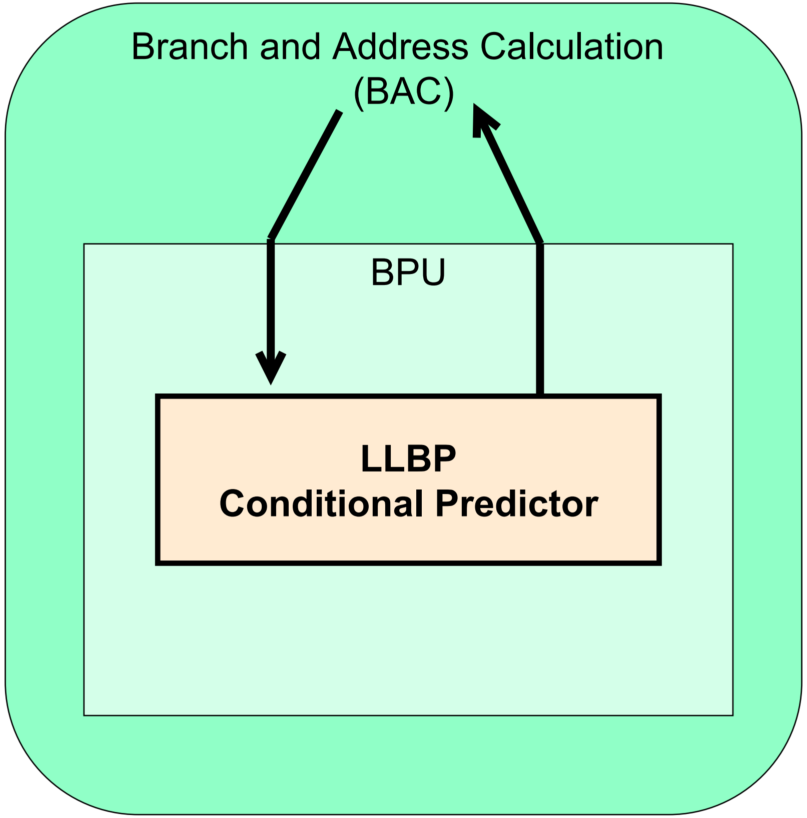


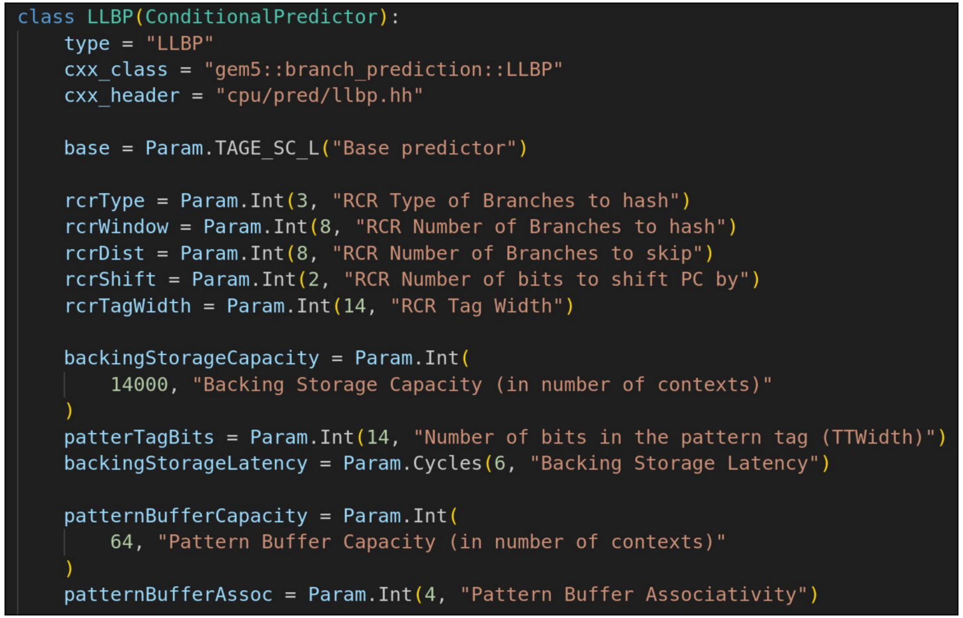


```
class BranchPredictor(SimObject):
    type = "BranchPredictor"
    cxx_class = "gem5::branch_prediction::BPredUnit"
    cxx_header = "cpu/pred/bpred_unit.hh"

    conditionalBranchPred = Param.ConditionalPredictor(
        "Conditional branch predictor"
    )
    overridingBranchPred = Param.ConditionalPredictor(
        NULL,
        "Overriding branch predictor",
    )
```

The Last Level Branch Predictor in gem5





```python
class LLBP(ConditionalPredictor):
    type = "LLBP"
    cxx_class = "gem5::branch_prediction::LLBP"
    cxx_header = "cpu/pred/llbp.hh"

    base = Param.TAGE_SC_L("Base predictor")

    rcrType = Param.Int(3, "RCR Type of Branches to hash")
    rcrWindow = Param.Int(8, "RCR Number of Branches to hash")
    rcrDist = Param.Int(8, "RCR Number of Branches to skip")
    rcrShift = Param.Int(2, "RCR Number of bits to shift PC by")
    rcrTagWidth = Param.Int(14, "RCR Tag Width")

    backingStorageCapacity = Param.Int(
        14000, "Backing Storage Capacity (in number of contexts)"
    )
    patterTagBits = Param.Int(14, "Number of bits in the pattern tag (TTWidth)")
    backingStorageLatency = Param.Cycles(6, "Backing Storage Latency")

    patternBufferCapacity = Param.Int(
        64, "Pattern Buffer Capacity (in number of contexts)"
    )
    patternBufferAssoc = Param.Int(4, "Pattern Buffer Associativity")
```

Outline

- ~~Motivation & Background~~
- ~~Design~~
- Evaluation
  - Parameters & Baseline
  - The impact of latency
  - Overriding branch prediction
  - The Last-Level Branch Predictor (LLBP)
- Conclusion

Configuration parameters for evaluation

- Base predictor: **TAGE-SC-L (state-of-the-art) with storage size from 64KiB - Infinite**

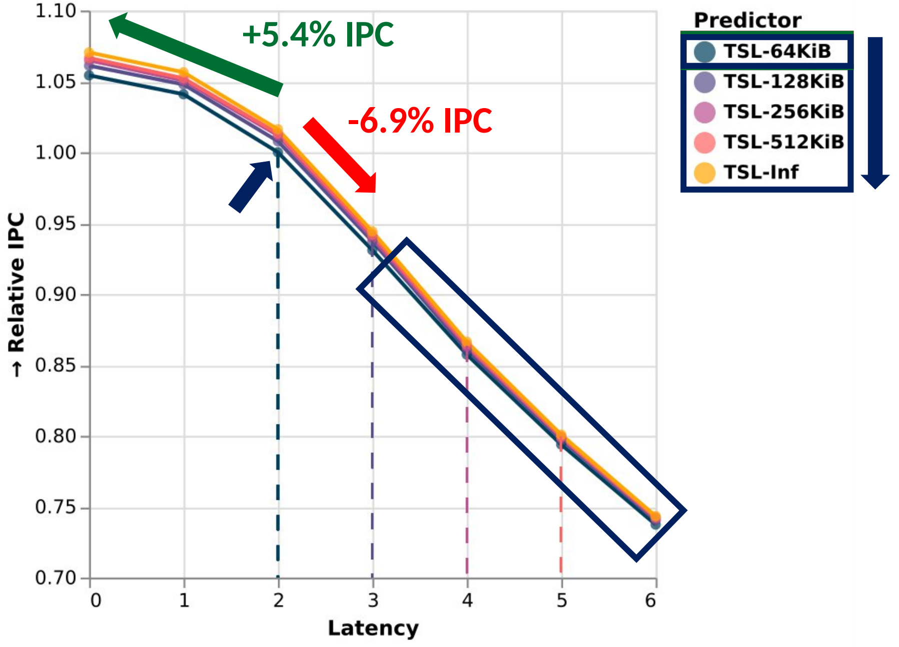
- Server workloads from the **Dacapo Benchmark Suite** [17] **and others** [16]
- **Warmup** for **100M** instructions, then **measuring** for **1B** instructions

- gem5 in **full system** mode on Arm ISA
- Simulated Processor: **O3 model** at 3GHz, 6-way OoO, 512 entry ROB
- Caches: 32KiB L1-I, 64KiB L1-D, 2MiB L2

RQ 1: The impact of latency

- **TAGE-SC-L (TSL)** with different sizes, latency sweep — **No latency mitigation**
  - **Baseline: TSL-64KiB with 2 cycles of latency**

IPC relative to TSL-64KiB with 2 cycles latency



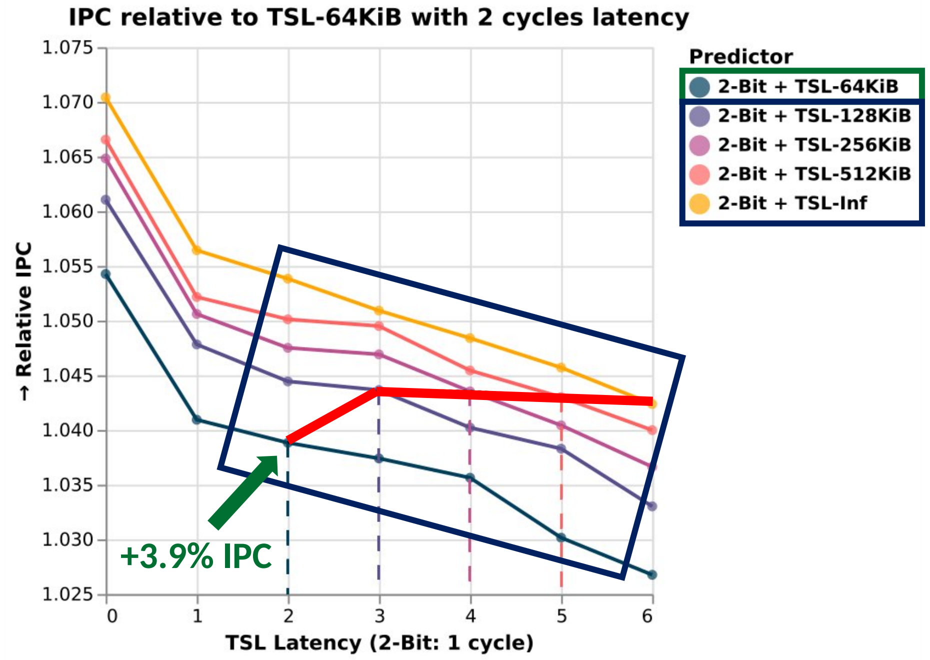
Latency has substantial performance impact

Eliminating latency can even benefit current predictor sizes of 64KiB

Increased storage capacity cannot offset latency — Mitigation is necessary

RQ 2: Overriding prediction

- **Small 2-bit predictor (fast) + TAGE-SC-L (accurate) — Overriding prediction**
    - **Fast predictor: 1 cycle of latency**



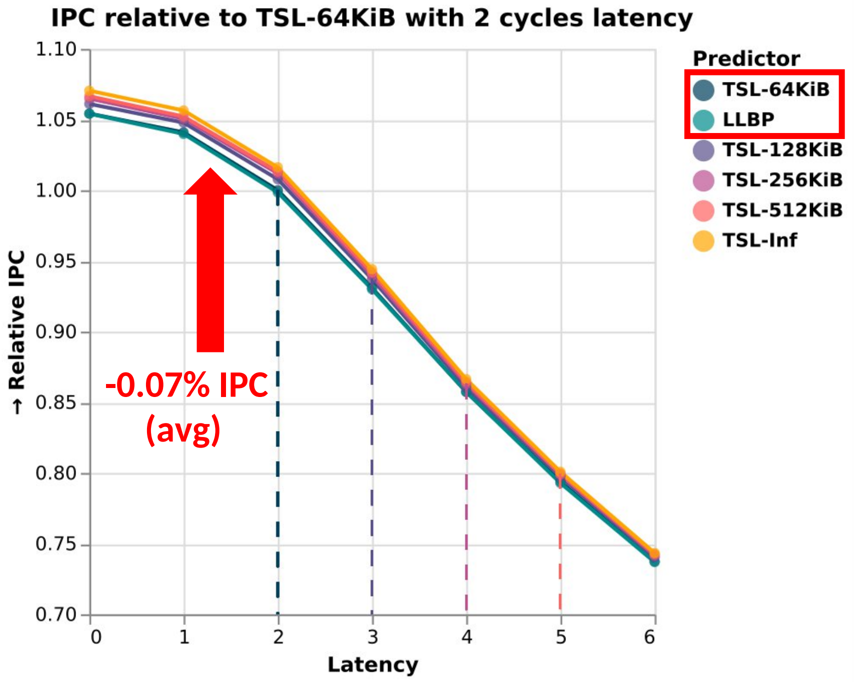
➡ **Overriding captures over 72% of the opportunity for latency elimination in the baseline predictor**

➡ **Increased storage capacity can now offset some latency**

➡ **Diminishing returns above 128KiB when assuming 2x storage = +1 cycle**

RQ 3: The Last-Level Branch Predictor (LLBP)

- **Pattern buffer + TSL-64KiB ("LLBP") – The Last-Level Branch Predictor**
  - **Same latency applied as unmodified TSL-64KiB**



➡ LLBP did not effectively mitigate latency

➡ Found an implementation bug near submission

Could not repeat the experiments due to time constraint

➡ Foundation for future work

Conclusion

1. How large is the impact of predictor latency on performance?

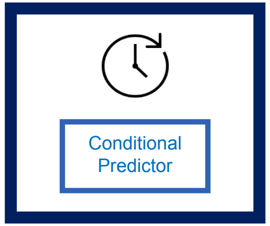
➡ Significant performance loss with state-of-the-art predictor up to 6.9% per cycle

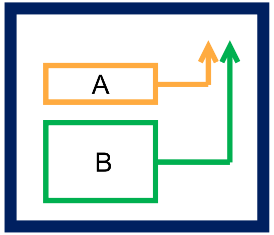
2. Can overriding prediction reduce this penalty?

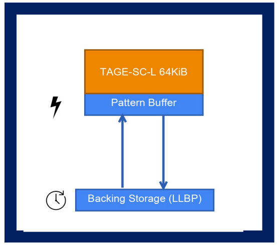
➡ Very effective, capturing over 72% of opportunity presented by reduced latency

3. Is a recent design, “The Last-Level Branch Predictor”, more effective?

➡ Performed worse than expected, implementation bug during evaluation







Contributions:

➡ Latency modeling framework for gem5 branch prediction

– Partially upstream, waiting for the decoupled frontend

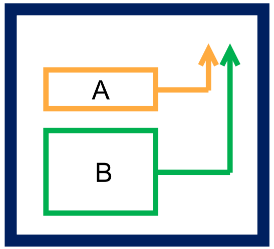
➡ Model of “The Last-Level Branch Predictor” for gem5

– Foundation for future research

Future work

➡ **Repeat the experiments of "The Last-Level Branch Predictor"**

➡ **Use the latency framework to research a <u>combined latency mitigation strategy</u>**



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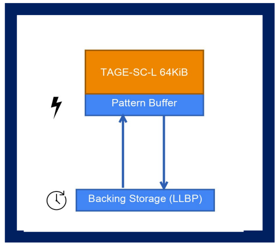

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