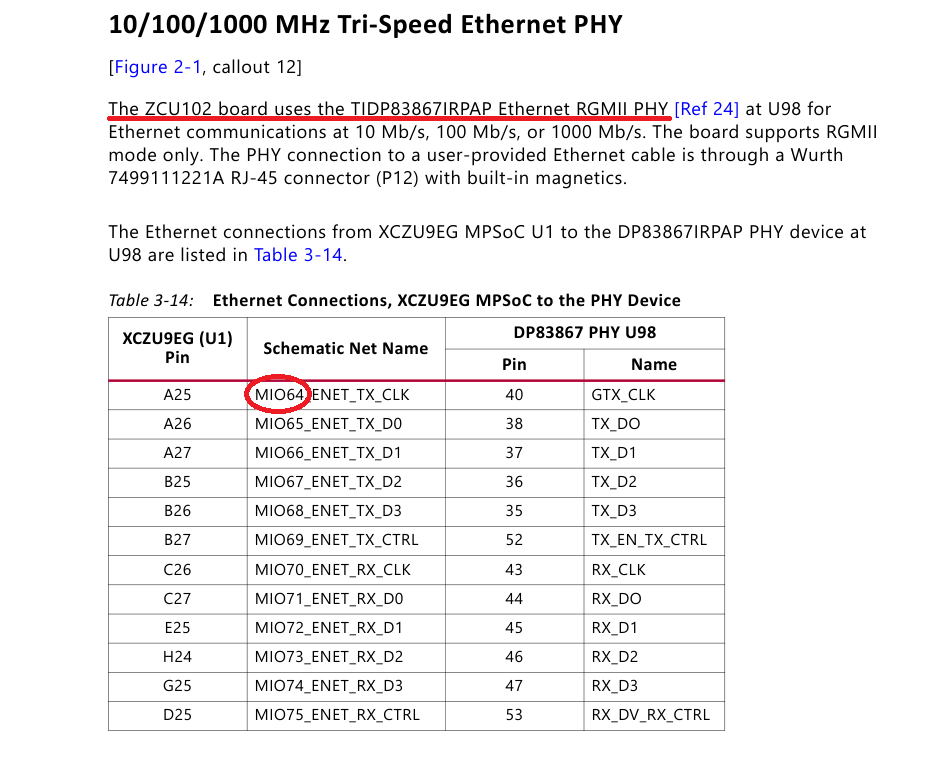
**How to use Ethernet in the FPGA Xilinx Zynq Ultrascale +**

**Kintex** is purely FPGA but **Zynq** combines an ARM processor (PS) with FPGA (PL).

In this board there is an Ethernet RGMII PHY:

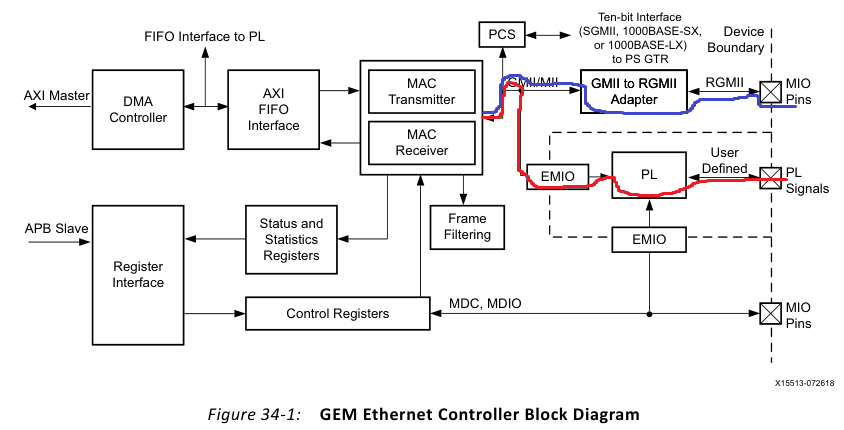


The Ethernet PHY is hardened to MIO pins, and the MIO pins cannot be accessed from the PL as Xilinx people confirms:

A screenshot of a computer

Description automatically generated  
  
As they say, it is possible to access some peripherals using EMIO (Extended Multiplexed I/O).

But, in case of the Ethernet, EMIO only can be used to connect PS GEM to the PL in order to implement an ethernet interface different from RGMII. Not possible to connect PL to MIO, only to PS GEM.



This is the generated interface when enabling EMIO:

A computer screen shot of a program

Description automatically generated

This interface is used to connect to another PHY (rxd is in and txd is out), **not** what we need.

System Viewpoint: PL don’t have access to MIO pins, only have access to some of the EMIO signals coming from PS GEM.

A diagram of a computer system

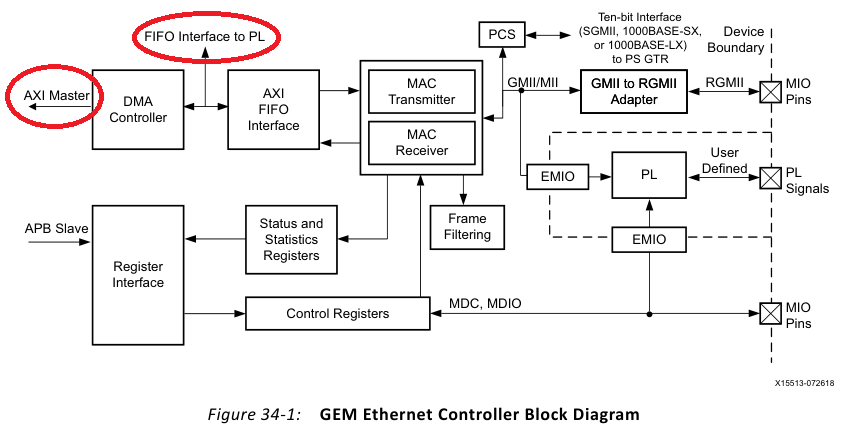
Description automatically generated

So, the only possibility to use ethernet from the PL on this board, is using the PS GEM instead of using Gaisler GEM.

A white background with black text

Description automatically generated

One way to work with PS GEM is using Rx and Tx FIFO, other way is to use DMA as a master on AXI:



This Stream FIFOs implement interfaces to PL, with the next interface:

A screen shot of a computer program

Description automatically generated

In the manual is explained in 36 pages how to manage the interface:  
A diagram of a timing criteria

Description automatically generated with medium confidence

I searched on internet some implementations for this interface and I only found on Github a module that convert the FIFO\_ENET3 interface into the AXI4-Stream interface.

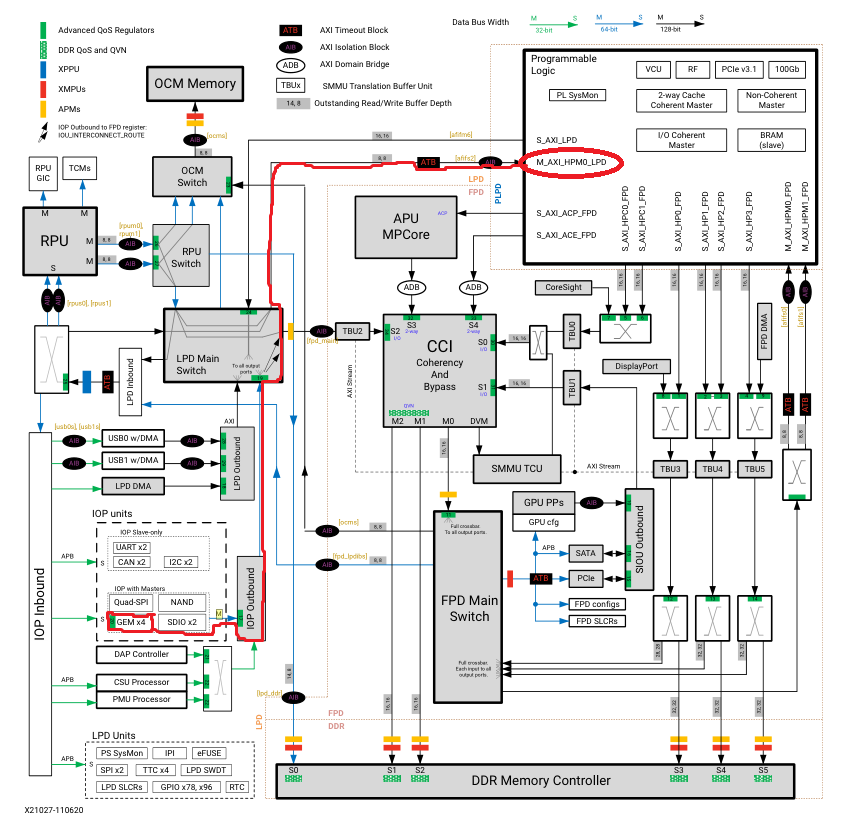
<https://github.com/diogo-marques/ORAN_FH_SW>

But, if using second option, we get directly an AXI interface to use in the PL:

A screen shot of a computer program

Description automatically generated

AXI Interconnect:



To integrate on the Noel-V system bus, AXI to AMBA conversor will be needed.