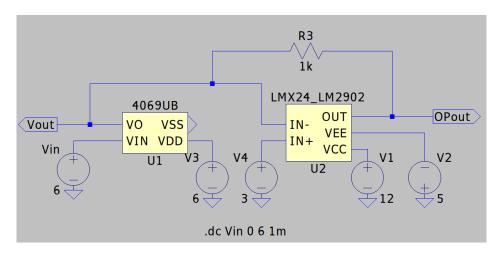
CMOS Inverter characteristics

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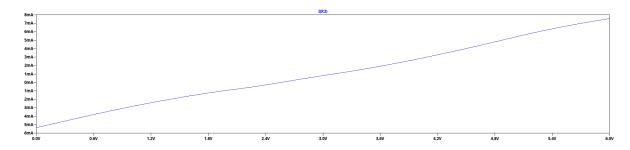
January 22, 2021

CMOS Inverter as Transconductor without ammeter

1. Testbench

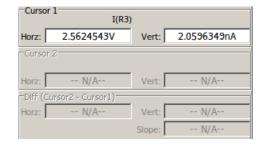


2. DC Sweep Analysis



3. What is self-bias Voltage(V_B) of the inverter?

At self bias it is known that I_{out} is 0.



Now solving these current equations

$$I_{out} = I_{SD_p} - I_{DS_n}$$

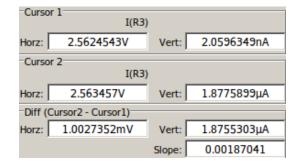
$$I_{out} = \frac{\beta_p}{2} (V_{SG} - |V_{TH_p}|)^2 (1 + \lambda_p V_{SD}) - \frac{\beta_n}{2} (V_{GS} - V_{TH_n})^2 (1 + \lambda_n V_{DS})$$

By using MOS parameters given in SPICE Model of CMOS Inverter we get, $0.0021(1+0.00187(6-V_{out}))(3.1-V_{in})^2 = 0.0029(1+0.00187(V_{out}))(V_{in}-2.1)^2$

Solving this equation at $V_{out} = V_{in} = V_B$ we get,

$$V_B \approx 2.56$$

4. Find the trans-conductance at V_B ?

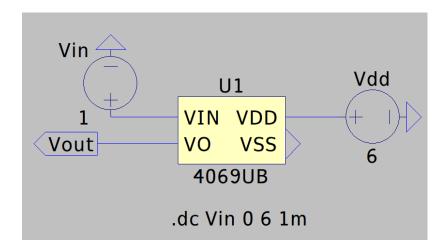


This is obtained by finding slope of DC sweep analysis of I_{out} and V_{in} at V_B .

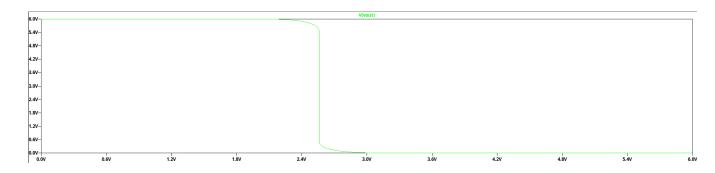
$$g_m|_{@V_B} = 0.00187041$$

2 V_{out} vs V_{in} of a CMOS Inverter

1. Testbench

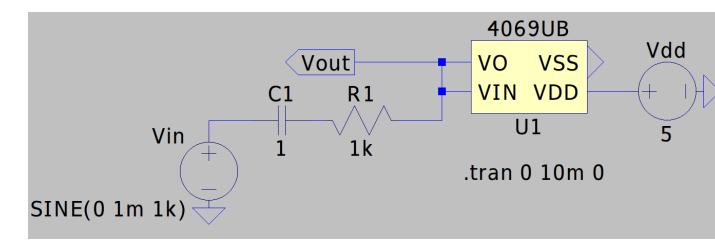


2. DC Sweep Analysis



3 Small-signal resistance of Self-biased inverter

1. Testbench

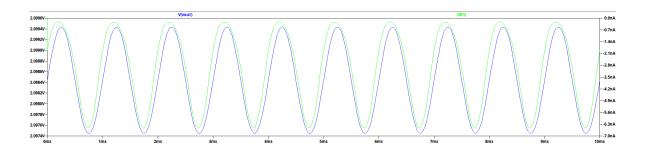


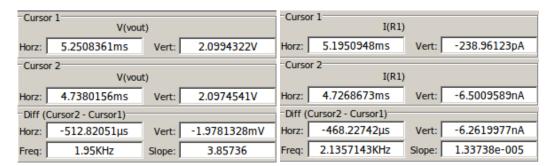
2. Analysis

3. Resistance

 $\frac{\Delta V_{in}}{\Delta I_{out}} = \text{Small-signal resistance}$ Thus at,

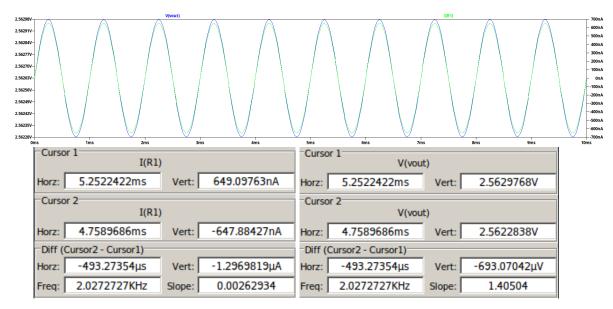
(a) Vdd = 5V





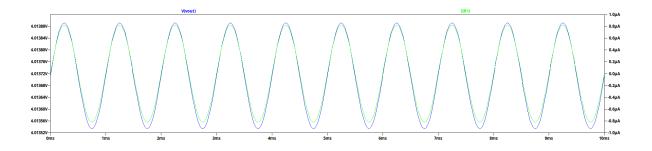
$$\frac{\Delta V_{in}}{\Delta I_{out}} = 315~\mathrm{K}\Omega$$

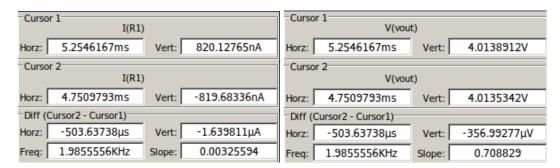
(b) Vdd = 6V



$$\frac{\Delta V_{in}}{\Delta I_{out}} = 534.405 \ \Omega$$

(c) Vdd = 9V





$$\frac{\Delta V_{in}}{\Delta I_{out}} = 217.703607 \text{ K}\Omega$$

4. Theoretical

Since our small-signal model for CMOS inverter is 2 port network. Thus trans-resistor is 1/gm. Now we can treat this Input resistance.

Thus at Vdd = 6V we found gm = 0.00187041 implies $R_{in} = 534.6421 \Omega$. Now similarly we can find transconductance for Vdd 5V and 9V and take its reciprocal for its Input resistance.

5. Abnormality

Observe that for Vdd=5V the transconductance is very very low it is to the order 10^{-6} .

We can also explain this phenomenon with respective to region also usually. There are 5 regions in CMOS Inverter.

- (a) NMOS:OFF & PMOS:LINEAR
- (b) **NMOS**:SATURATION & **PMOS**:LINEAR
- (c) NMOS:SATURATION & PMOS:SATURATION
- (d) NMOS:LINEAR & PMOS:SATURATION
- (e) **NMOS**:LINEAR & **PMOS**:OFF

So when NMOS turns from OFF to SATURATION even PMOS goes from Saturation to OFF at the same instant that is $V_{in} = V_{TH_n}$ or $Vdd - V_{TH_p}$. And even this saturation regions for respective MOSs doesn't last long just 1mV for each.

Thus we cannot find any point where both MOSs are in saturation. Now this proves that this **CMOS** Inverter at Vdd = 5V cannot be used as Trans-conductor.

Now because of its very short period for Saturation regions for each MOS. The current won't be drawn except around 2.1V with 1mV band.

Thus when Vdd=5V this is the best conditions for Digital Logic operations because of it very low power dissipation.

4 Find gm, ro of self-biased inverter. V_T , β of NMOS and PMOS

1. g_{m}

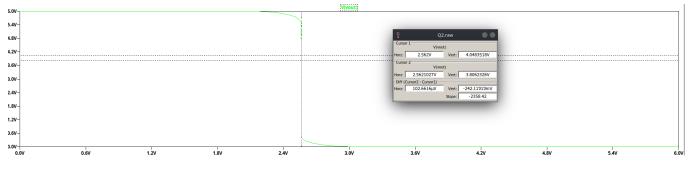
This transconductance of self-biased can be found with Circuit 1, By measuring slope of I_{out} and V_{in} near vicinity of $V_B(2.56\text{V})$.

$$g_m|_{@V_B} = 0.00187041$$

2. **ro**

Now since at self-bias voltage the whole CMOS inverter setup behaves as transconductor and can be modeled as VCCS with ro in parallel

Now we find that drop across V_{out} is $-g_m roV_{in}$. Thus this shows that $\frac{V_{out}}{V_{in}} = -g_m ro$ near V_B Now using Circuit given in Q2 finding slope at V_B we get,



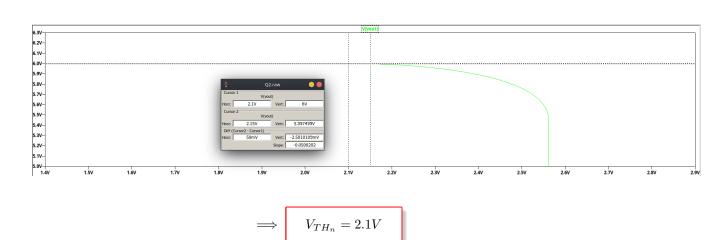
$$\frac{V_{out}}{V_{in}} = -g_m ro = -2358.42$$

$$\implies ro = 1.2609 M\Omega$$

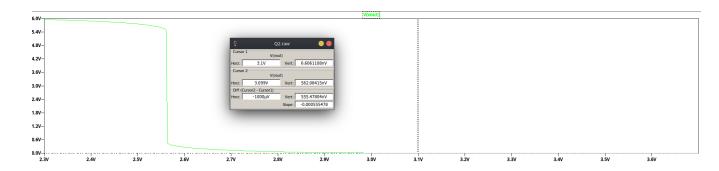
3. V_{TH_p} and V_{TH_n}

As mentioned earlier there exists 5 regions in CMOS inverter DC analysis.

As V_{in} gradually increases there exits a point where it crosses Threshold voltage of NMOS which makes its to switch to saturation from cut-off region. At this point CMOS draws current from the supply making V_{out} to drop from Vdd(6V). In order to find V_{TH_n} we need to find the point where V_{out} starts reducing.



Similarly for PMOS it turns off at $Vdd - V_{TH_p}$ because V_{SG} becomes less that $|V_{TH_p}|$ at this point further.



$$Vdd - |V_{TH_p}| = 3.1V$$

$$\implies V_{TH_p} = -2.9V$$

4. β_n and β_p

We found out self-bias voltage V_B at the point where I_{out} is zero. Using this condition writing current equations,

$$I_{out} = \frac{\beta_p}{2} (V_{SG} - |V_{TH_p}|)^2 (1 + \lambda_p V_{SD}) - \frac{\beta_n}{2} (V_{GS} - V_{TH_n})^2 (1 + \lambda_n V_{DS})$$

Since we are performing large signal analysis thus we can neglect channel-length modulation parameter

$$\frac{\beta_p}{2}(V_{SG} - |V_{TH_p}|)^2 = \frac{\beta_n}{2}(V_{GS} - V_{TH_n})^2$$

$$\frac{\beta_p}{2}(Vdd - V_B - |V_{TH_p}|)^2 = \frac{\beta_n}{2}(V_B - V_{TH_n})^2$$

$$\frac{\beta_p}{2}(6 - 2.562 - 2.9)^2 = \frac{\beta_n}{2}(2.562 - 2.1)^2$$

$$\beta_n = 1.356065\beta_n$$

We also found out gm which is $\frac{\Delta I_{out}}{\Delta V_{in}}$,

$$\frac{\Delta I_{out}}{\Delta V_{in}} = -(\beta_p (Vdd - V_B - |V_{TH_p}|) + \beta_n (V_B - V_{TH_n}))$$

$$\implies 0.0018741 = \beta_p (0.538) + \beta_n (0.462)$$

$$\implies \beta_p = 0.00218, \beta_n = 0.00161$$