

# FPGA LAB ASSIGNMENT 1

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## Problem

Obtain the minimal form for the following Boolean expression using Karnaugh's Map.

$$H(P, Q, R, S) = \sum(0, 1, 2, 3, 5, 7, 8, 9, 10, 14, 15)$$

## Solution

After simplification of the above truth table in Karnaugh's map, we get

$$H = Q'S' + Q'R' + P'S + PQR$$

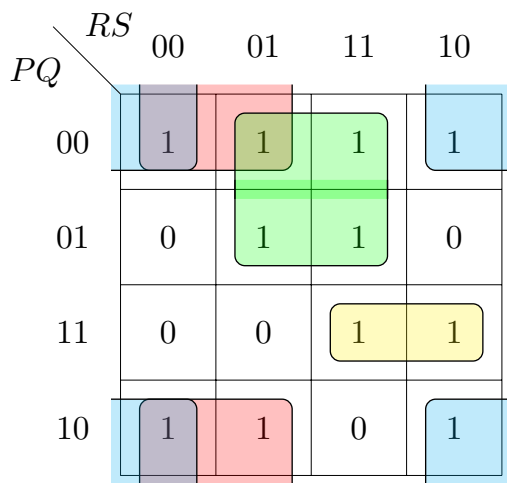
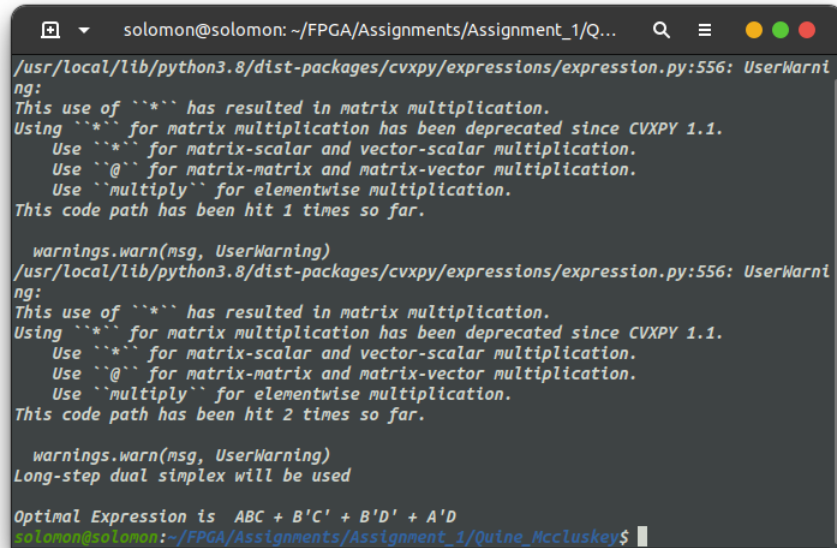


Figure 1: K-Map for  $H$ .

## Optimality verification

To verify the optimality of above result, The prime implicants were given to *Quine-McCluskey* algorithm implemented [here](#). This was implemented using *cvxpy*.



```
solomon@solomon: ~/FPGA/Assignments/Assignment_1/Q...
/usr/local/lib/python3.8/dist-packages/cvxpy/expressions/expression.py:556: UserWarning:
This use of '*' has resulted in matrix multiplication.
Using '*' for matrix multiplication has been deprecated since CVXPY 1.1.
    Use '*' for matrix-scalar and vector-scalar multiplication.
    Use '@' for matrix-matrix and matrix-vector multiplication.
    Use 'multiply' for elementwise multiplication.
This code path has been hit 1 times so far.

warnings.warn(msg, UserWarning)
/usr/local/lib/python3.8/dist-packages/cvxpy/expressions/expression.py:556: UserWarning:
This use of '*' has resulted in matrix multiplication.
Using '*' for matrix multiplication has been deprecated since CVXPY 1.1.
    Use '*' for matrix-scalar and vector-scalar multiplication.
    Use '@' for matrix-matrix and matrix-vector multiplication.
    Use 'multiply' for elementwise multiplication.
This code path has been hit 2 times so far.

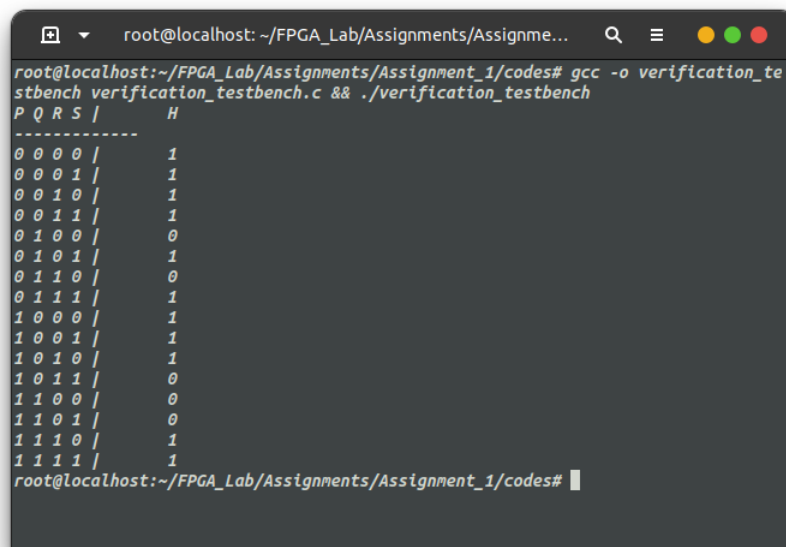
warnings.warn(msg, UserWarning)
Long-step dual simplex will be used

Optimal Expression is ABC + B'C' + B'D' + A'D
solomon@solomon:~/FPGA/Assignments/Assignment_1/Quine_Mccluskey$
```

NOTE:- Here A, B, C, and D corresponds to P, Q, R, and S respectively.

## Boolean expression verification

A [testbench](#) was created to verify the correctness of the obtained boolean expression.



```
root@localhost: ~/FPGA_Lab/Assignments/Assignme...
root@localhost:~/FPGA_Lab/Assignments/Assignment_1/codes# gcc -o verification_te
stbench verification_testbench.c && ./verification_testbench
P Q R S | H
-----
0 0 0 0 | 1
0 0 0 1 | 1
0 0 1 0 | 1
0 0 1 1 | 1
0 1 0 0 | 0
0 1 0 1 | 1
0 1 1 0 | 0
0 1 1 1 | 1
1 0 0 0 | 1
1 0 0 1 | 1
1 0 1 0 | 1
1 0 1 1 | 0
1 1 0 0 | 0
1 1 0 1 | 0
1 1 1 0 | 1
1 1 1 1 | 1
root@localhost:~/FPGA_Lab/Assignments/Assignment_1/codes#
```