

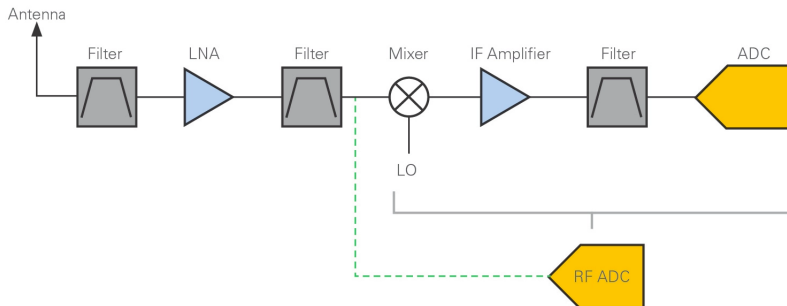
ADCs for Direct RF Sampling

Tadipatri Uday Kiran Reddy - EE19BTECH11038

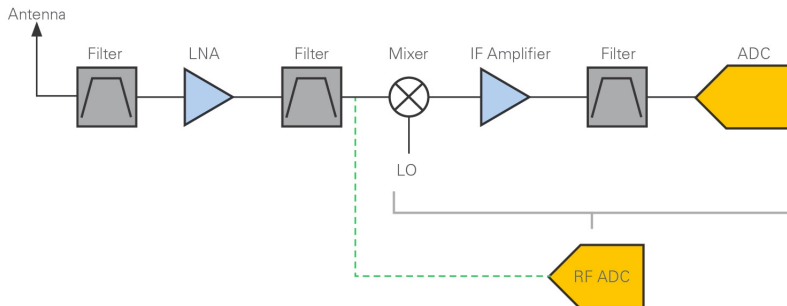
IIT Hyderabad

May 20, 2022

Introduction

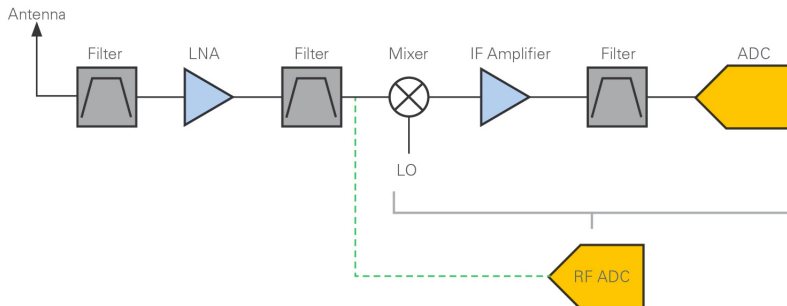


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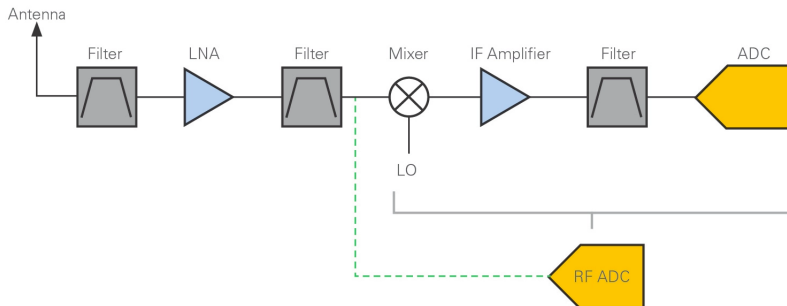
- ADC architecture for sampling at RF with low power and area.

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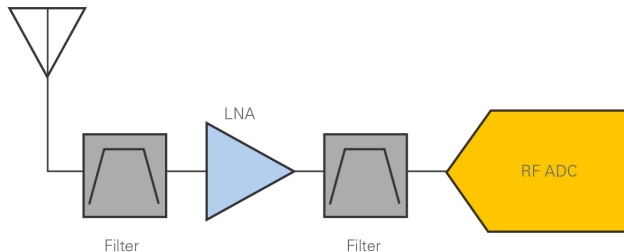
- ADC architecture for sampling at RF with low power and area.
- High sampling rate with relatively slow circuits, *Time-Interleaved ADC*.

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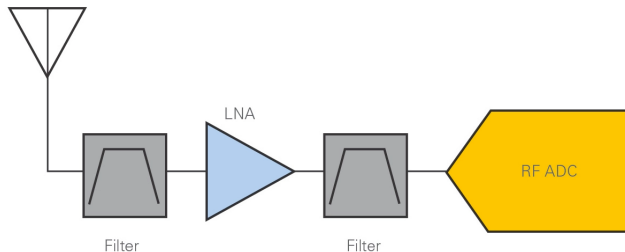
- ADC architecture for sampling at RF with low power and area.
- High sampling rate with relatively slow circuits, *Time-Interleaved ADC*.
- Minimize quantisation and noise error.

Motivation for RF sampling



- Simpler hardware design due to elimination of analog frequency conversion.

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- Exploit the computing power of DSPs.

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- Sample the input signal at reconstructable rate and then Quantize.

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- Nyquist-rate Converters, double the input bandwidth.

$$SQNR = 6.02ENOB + 1.76dB$$

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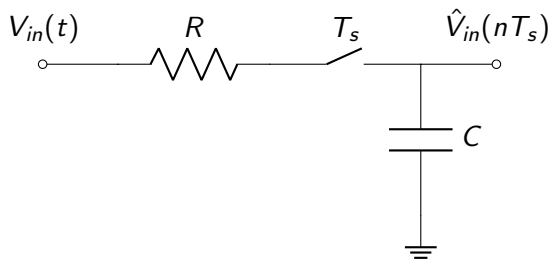
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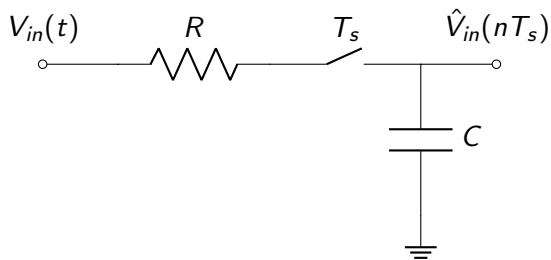
- Oversampled Converters, very high sampling rate, $OSR = \frac{f_s}{2f_B}$

$$SQNR = 6.02ENOB + 1.76 + 10\log(OSR)dB$$

Limitations of S/H Circuit

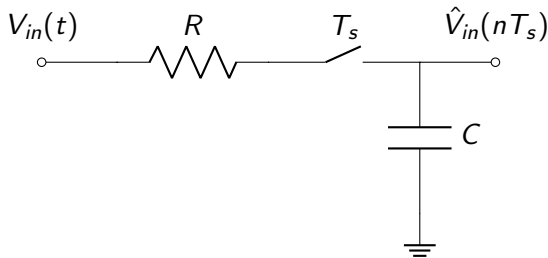


Limitations of S/H Circuit



$$\frac{1}{RC} \gg f_{in}$$

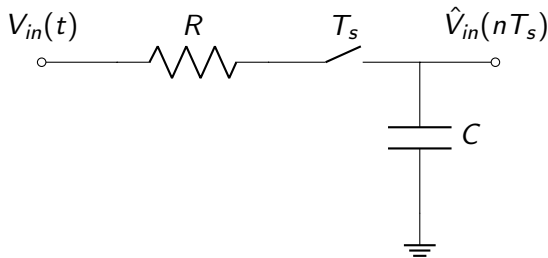
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- Difficult to construct S/H circuit with very high tracking BW.

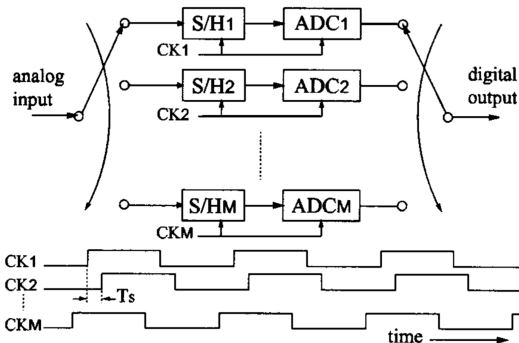
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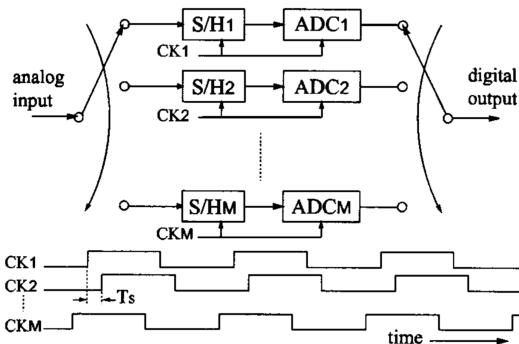
- Difficult to construct S/H circuit with very high tracking BW.
- Due to Low pass nature RF signal will attenuate.

Time-Interleaved ADC¹



¹N. Kurosawa *et al.*, "Explicit analysis of channel mismatch effects in time-interleaved ADC systems," in IEEE Transactions on Circuits and Systems I: Fundamental Theory

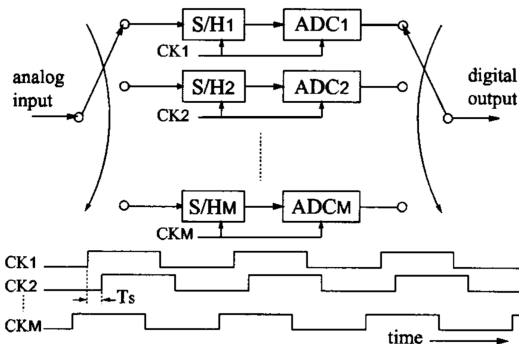
Time-Interleaved ADC¹



- Required clock, $f_{clk} = f_s/M$

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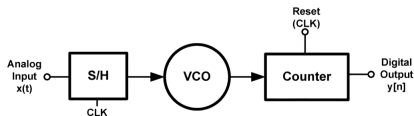
Time-Interleaved ADC¹



- Required clock, $f_{clk} = f_s/M$
- Phase difference, $\phi_i = \frac{2\pi(i-1)}{M}$

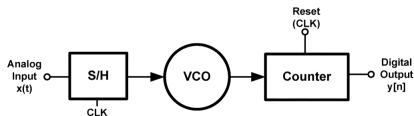
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Analysis of ADC based on VCO ²



²Y. Yoon *et al.*, "A Time-Based Bandpass ADC Using Time-Interleaved Voltage-Controlled Oscillators," in IEEE Transactions on Circuits and Systems I: Regular Papers

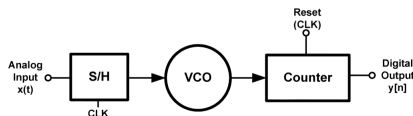
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- VCO translates the input voltage to phase.

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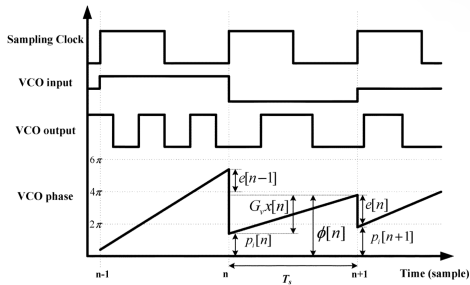


- VCO translates the input voltage to phase.
- Counter, counts the number of rising/falling edges.

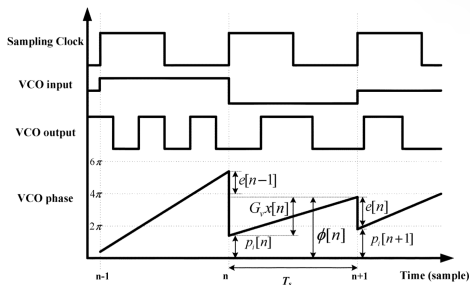
$$\phi[n] = \int_{nT_s}^{(n+1)T_s} K_v x[n] dt + p_i[n] = G_v x[n] + e[n-1]$$

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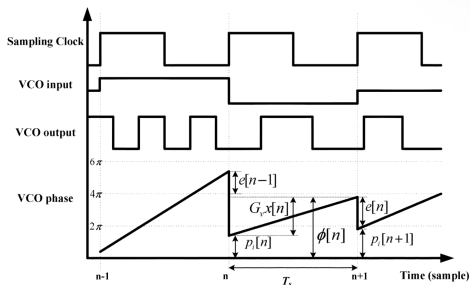


$$y[n] = \frac{1}{2\pi}(\phi[n] - e[n]) = \frac{1}{2\pi}(G_v x[n] + e[n-1] - e[n])$$

$$Y(z) = \frac{1}{2\pi}(G_v X(z) + (z^{-1} - 1)E(z))$$

$$NTF(z) = \frac{1}{2\pi}(z^{-1} - 1) \implies |NTF(e^{j\omega})| = |2\sin(\omega/2)|$$

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- First order high-pass filter.

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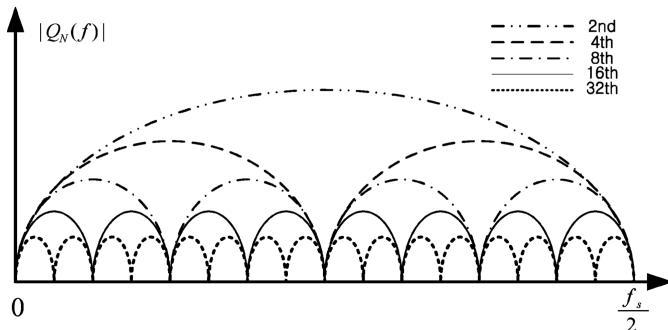
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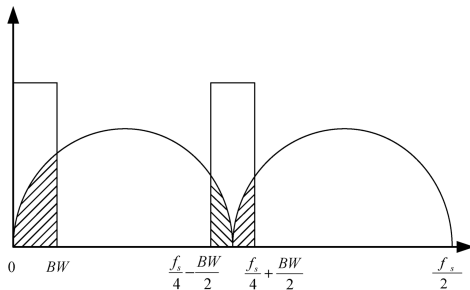
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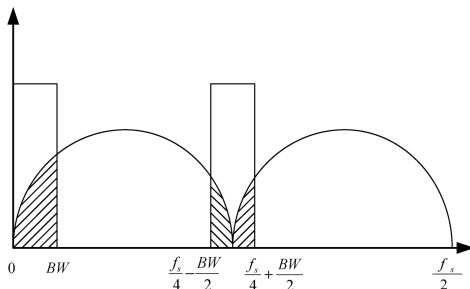
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Which Zero to center at?



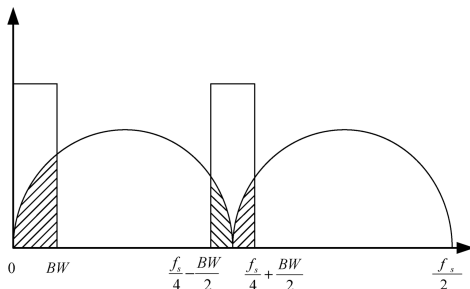
Which Zero to center at?



- At $\omega = 0$ or π ,

$$SQNR = 6.02ENOB - 3.41 + 30\log(OSR)dB$$

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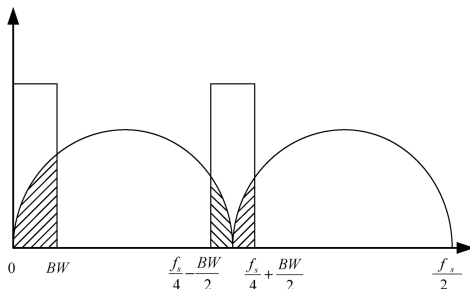
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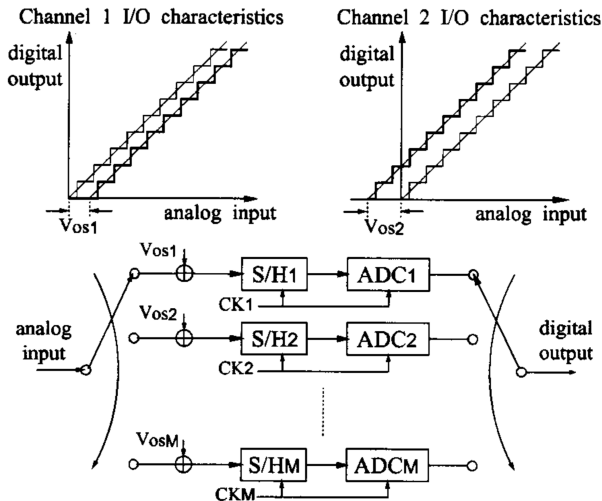
$$SQNR = 6.02ENOB - 3.41 + 6.02 + 30\log(OSR)dB$$

Increase of 6.02dB is equivalent to increase in 1-bit precision of ADC!!

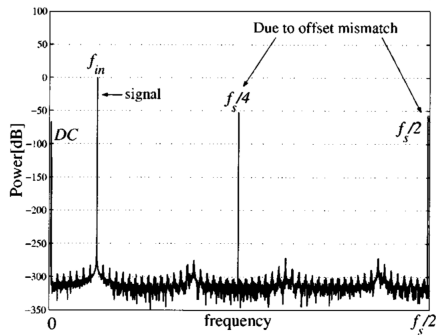
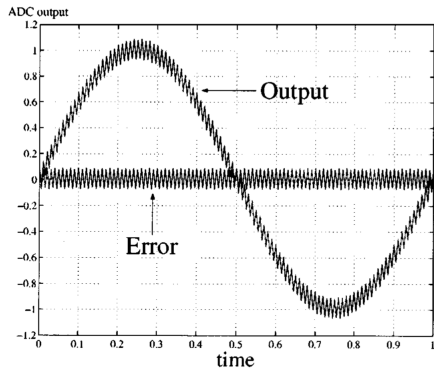
Non-idealities

- DC offset
- Gain mismatch
- Clock Jitter/Skew
- Bandwidth mismatch
- Non-linearity in VCO

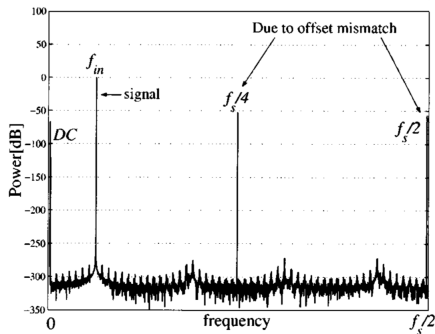
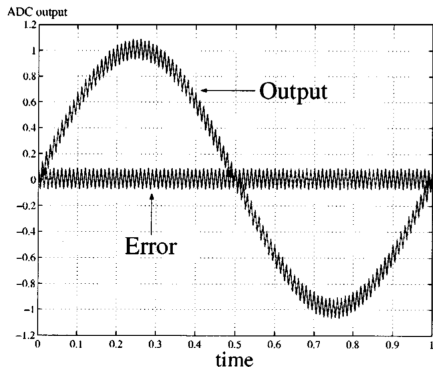
DC offset



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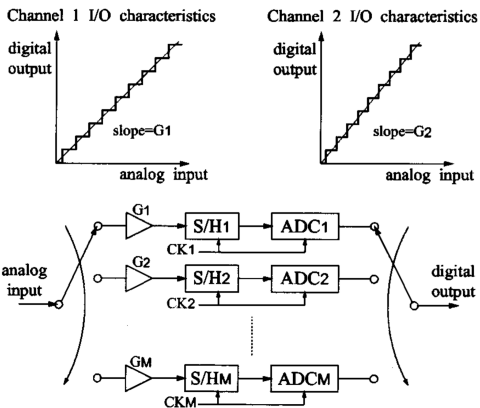


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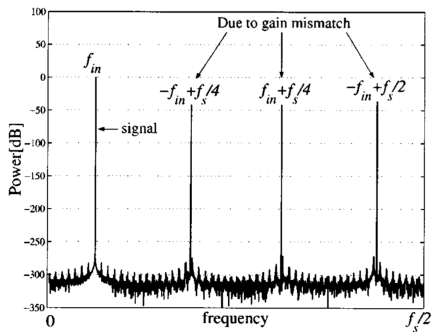
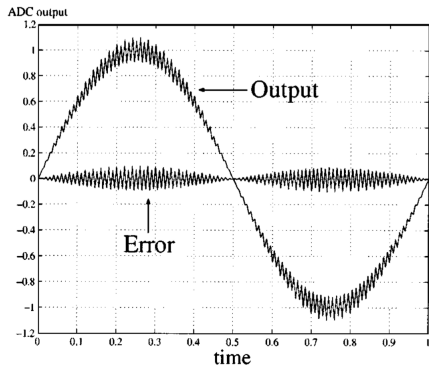


- We can see that dc offset periodicity \Rightarrow peaks at $\frac{k}{M} f_s$

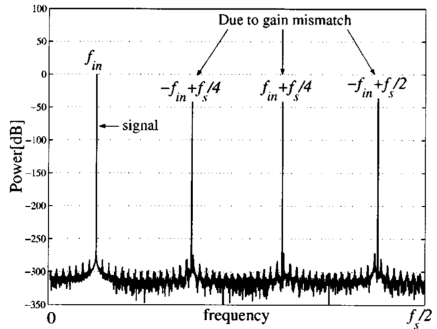
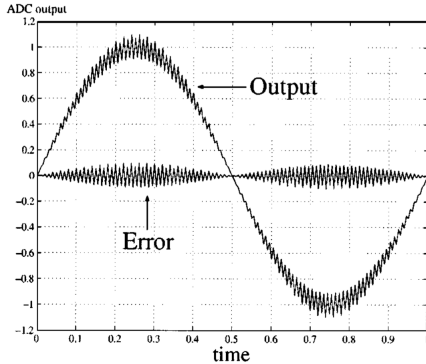
Gain mismatch



Gain mismatch

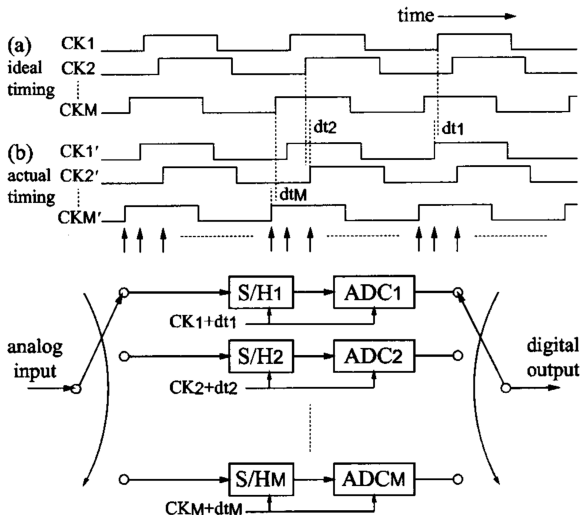


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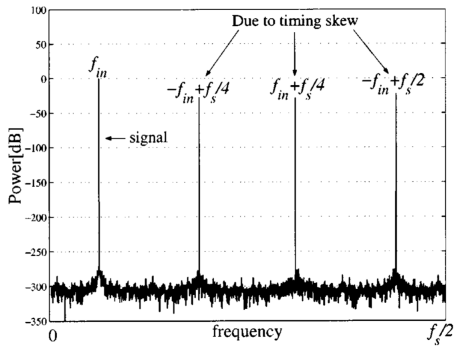
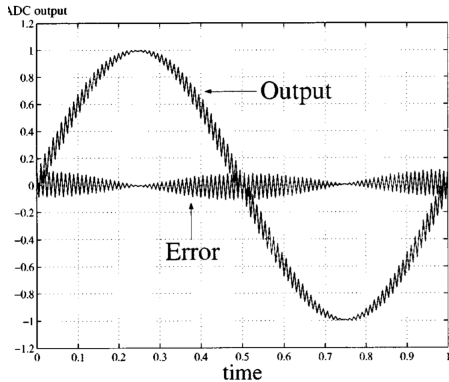


- Gain mismatch can be looked as A.M \Rightarrow peaks at $\pm f_{in} + \frac{k}{M} f_s$
- Error at higher amplitude is more.

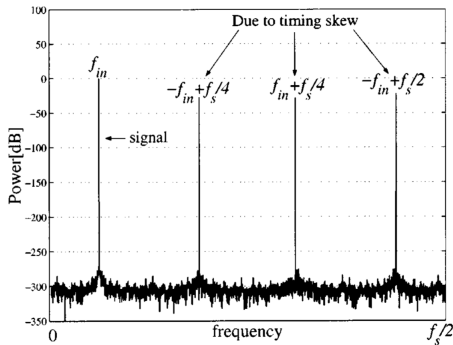
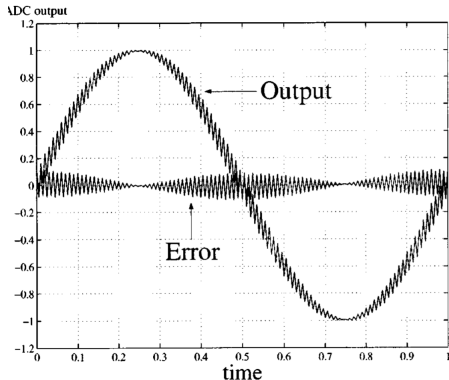
Clock jitter



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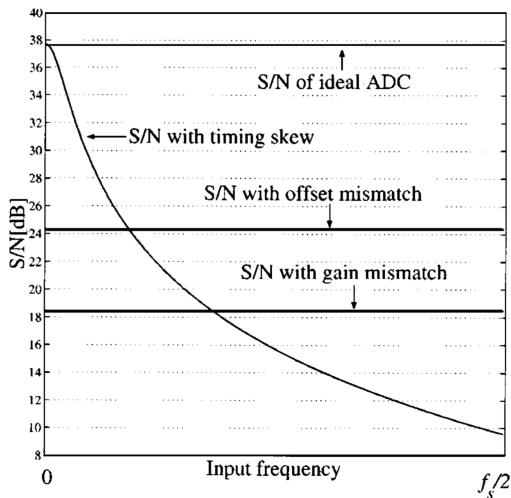


Clock jitter



- Clock skew behaves like P.M \implies peaks at $\pm f_{in} + \frac{k}{M} f_s$.
- Error is high at places where slew rate is more.

SNR comparisons



References

- N. Kurosawa *et al.*, "Explicit analysis of channel mismatch effects in time-interleaved ADC systems," in IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications.
- Y. Yoon *et al.*, "A Time-Based Bandpass ADC Using Time-Interleaved Voltage-Controlled Oscillators," in IEEE Transactions on Circuits and Systems I: Regular Papers
- Joonhee Lee *et al.*, "A 1.8 to 2.4-GHz 20mW digital-intensive RF sampling receiver with a noise-canceling bandpass low-noise amplifier in 90nm CMOS," 2010 IEEE Radio Frequency Integrated Circuits Symposium.
- Advantages of Direct RF Sampling Architectures, by www.ni.com

Thank You