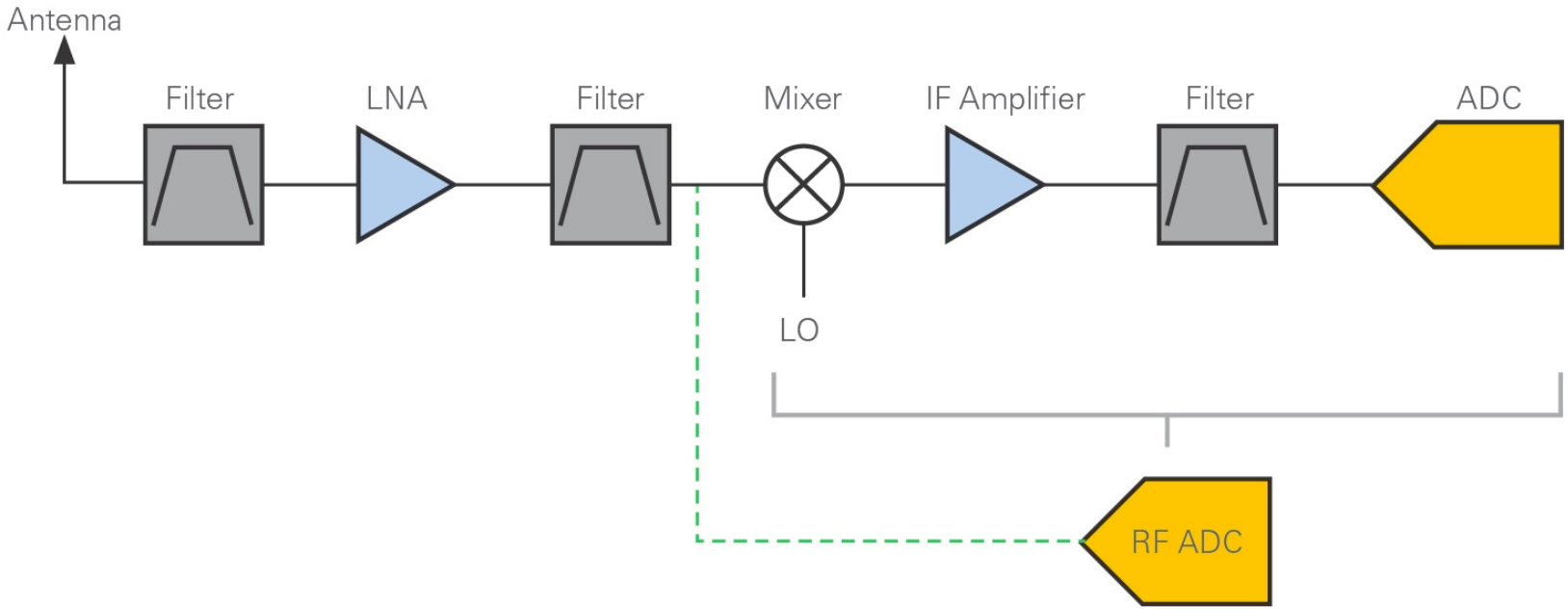
ADCs for Direct RF Sampling

Tadipatri Uday Kiran Reddy - EE19BTECH11038

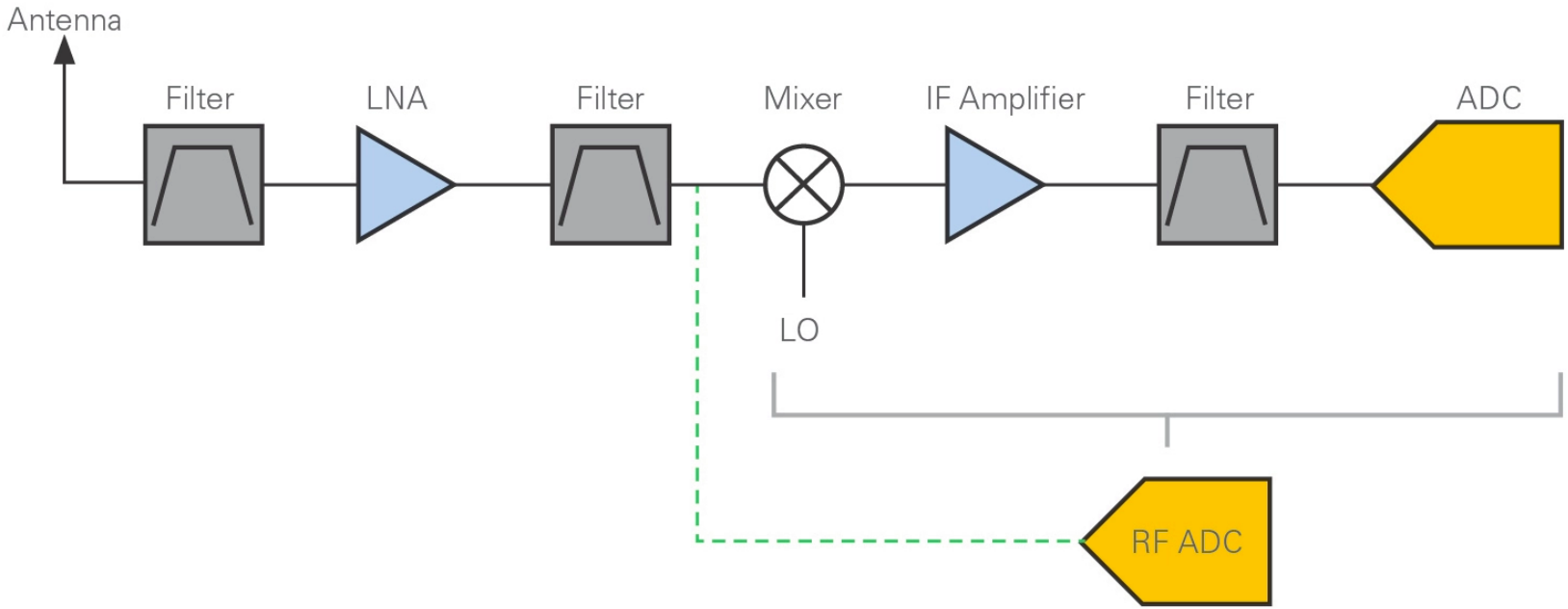
IIT Hyderabad

ICWC Presentation

Introduction

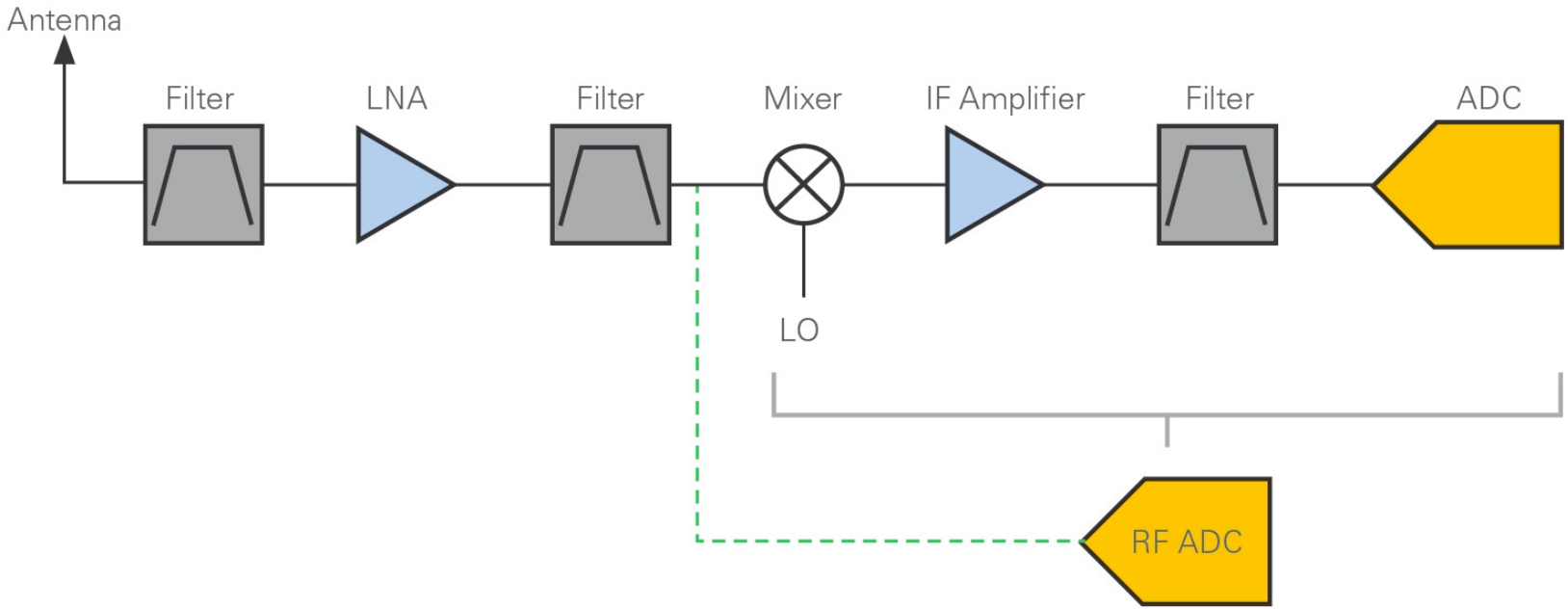


Introduction



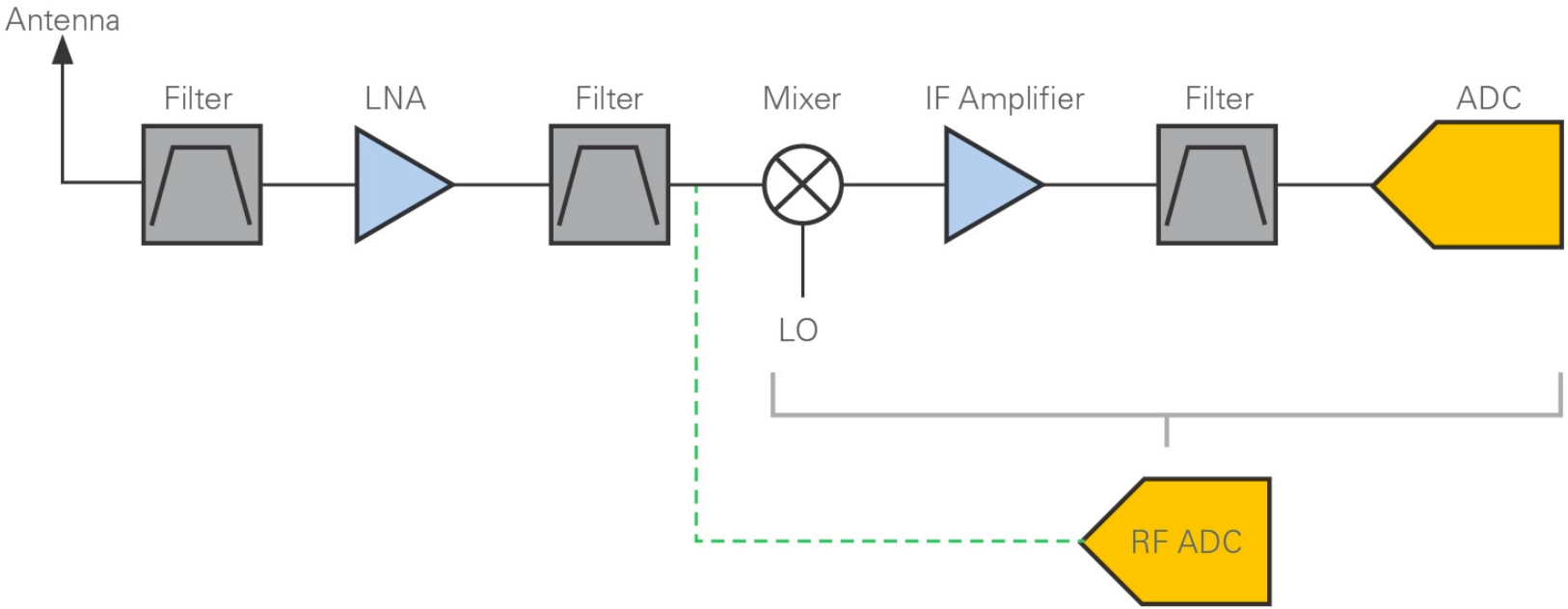
- ADC architecture for sampling at RF with low power and area.

Introduction



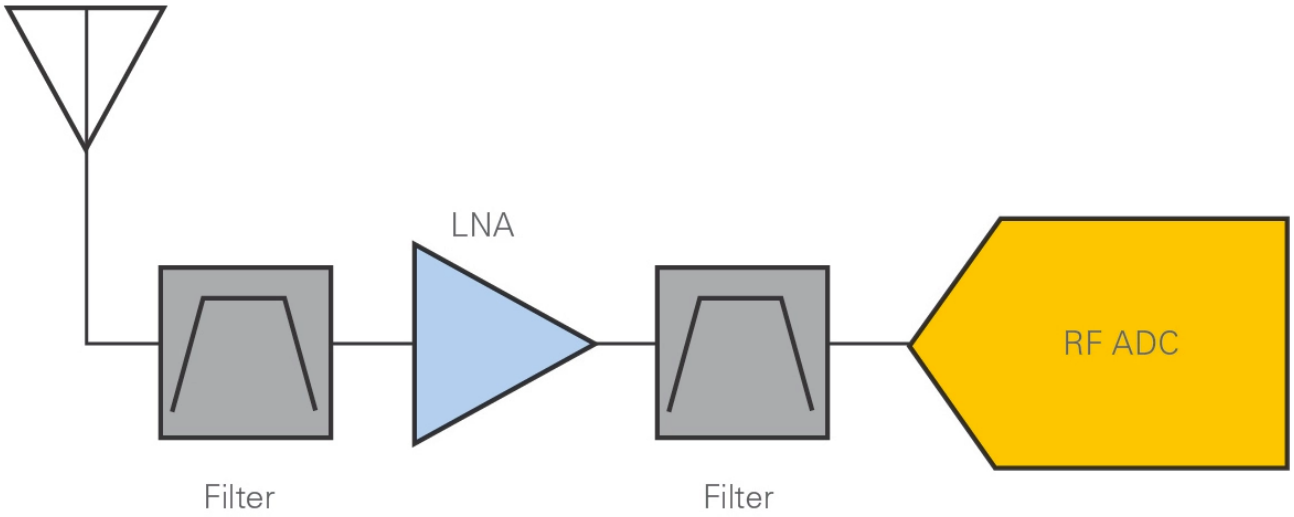
- ADC architecture for sampling at RF with low power and area.
- High sampling rate with relatively slow circuits with more bandwidth, *Time-Interleaved ADC*.

Introduction



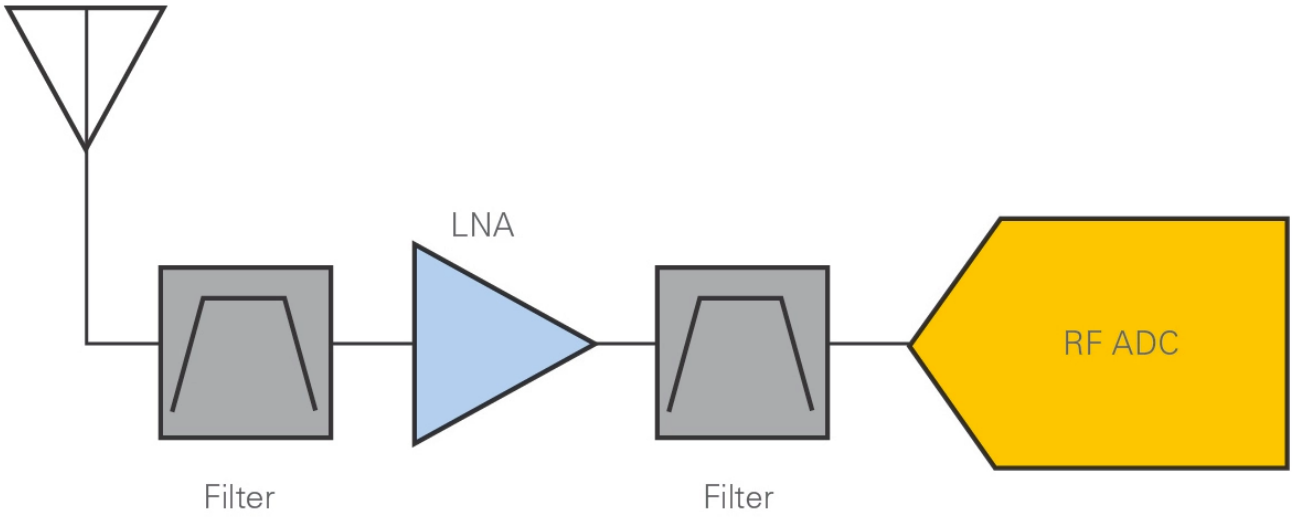
- ADC architecture for sampling at RF with low power and area.
- High sampling rate with relatively slow circuits with more bandwidth, *Time-Interleaved ADC*.
- Minimize quantisation and noise error.

Motivation for RF sampling



- Simpler hardware design due to elimination of analog frequency conversion.

Motivation for RF sampling



- Simpler hardware design due to elimination of analog frequency conversion.
- Exploit the computing power of DSPs.

Analog-to-Digital Converters

- Sample the input signal at reconstructable rate and then Quantize.

Analog-to-Digital Converters

- Sample the input signal at reconstructable rate and then Quantize.

Types of converters,

Analog-to-Digital Converters

- Sample the input signal at reconstructable rate and then Quantize.

Types of converters,

Analog-to-Digital Converters

- Sample the input signal at reconstructable rate and then Quantize.

Types of converters,

- Nyquist-rate Converters, double the input bandwidth.

$$SQNR = 6.02ENOB + 1.76dB$$

Analog-to-Digital Converters

- Sample the input signal at reconstructable rate and then Quantize.

Types of converters,

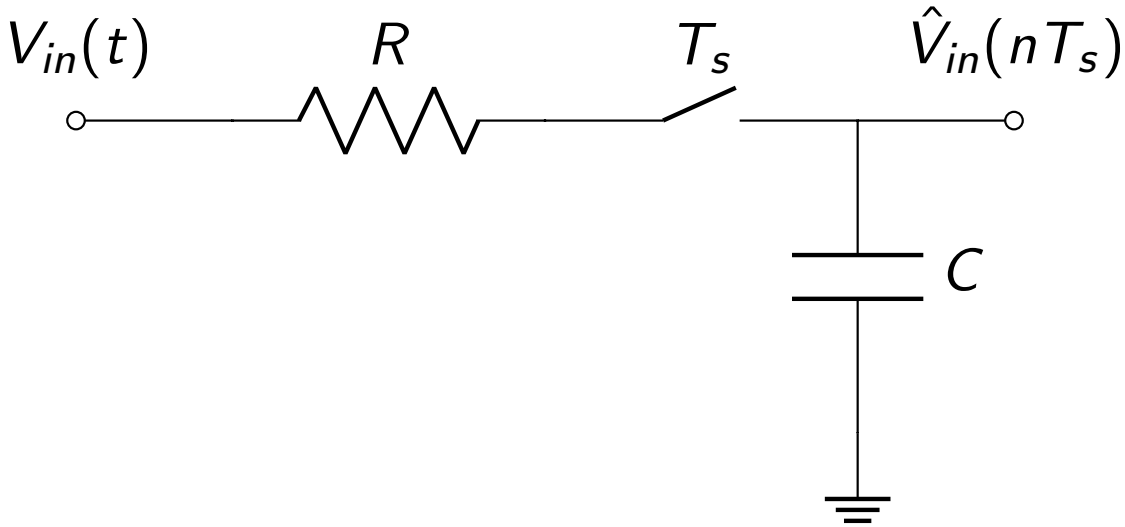
- Nyquist-rate Converters, double the input bandwidth.

$$SQNR = 6.02ENOB + 1.76dB$$

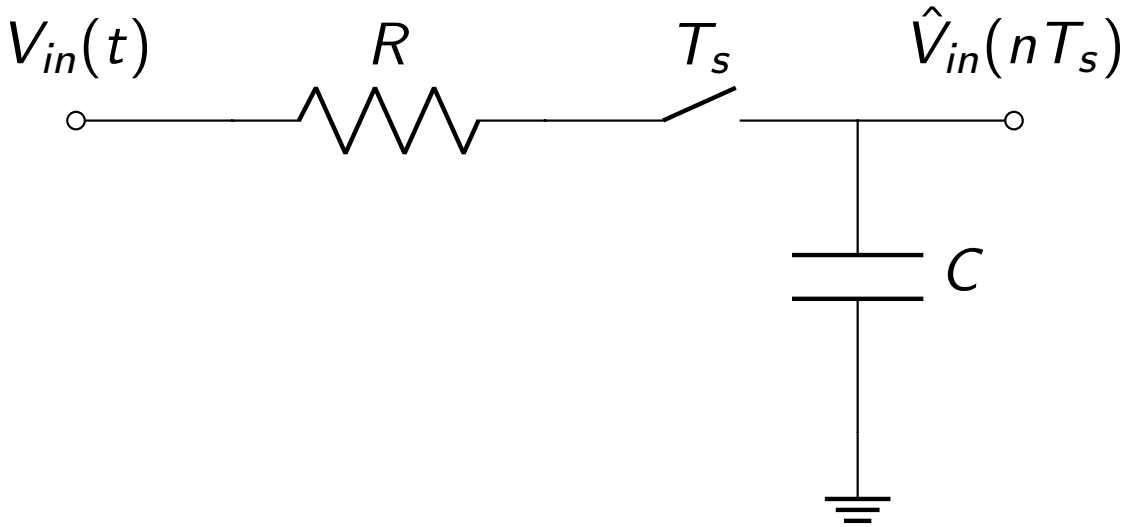
- Oversampled Converters, very high sampling rate, $OSR = \frac{f_s}{2f_B}$

$$SQNR = 6.02ENOB + 1.76 + 10log(OSR)dB$$

Limitations of S/H Circuit

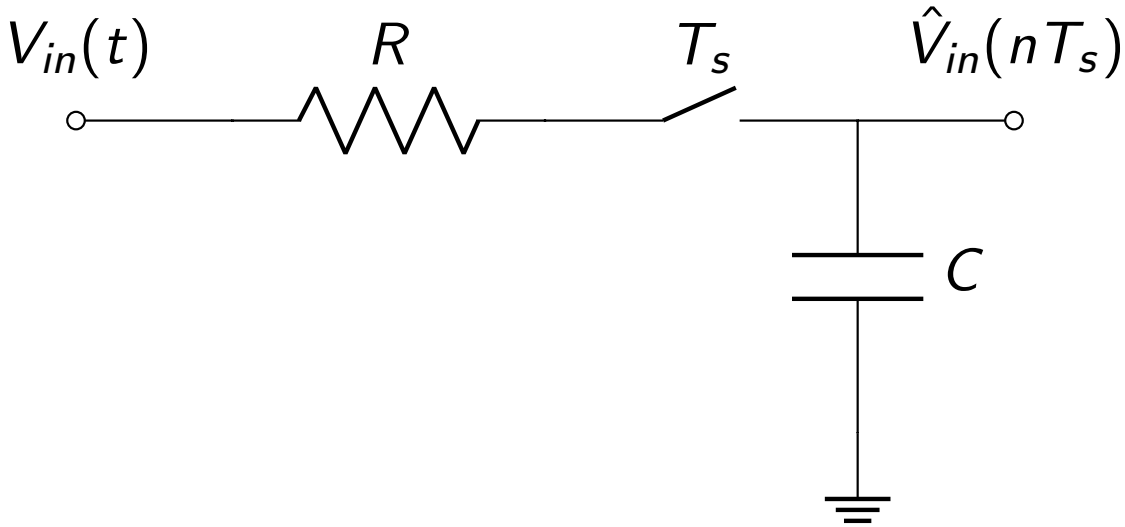


Limitations of S/H Circuit



$$\frac{1}{RC} >> f_{in}$$

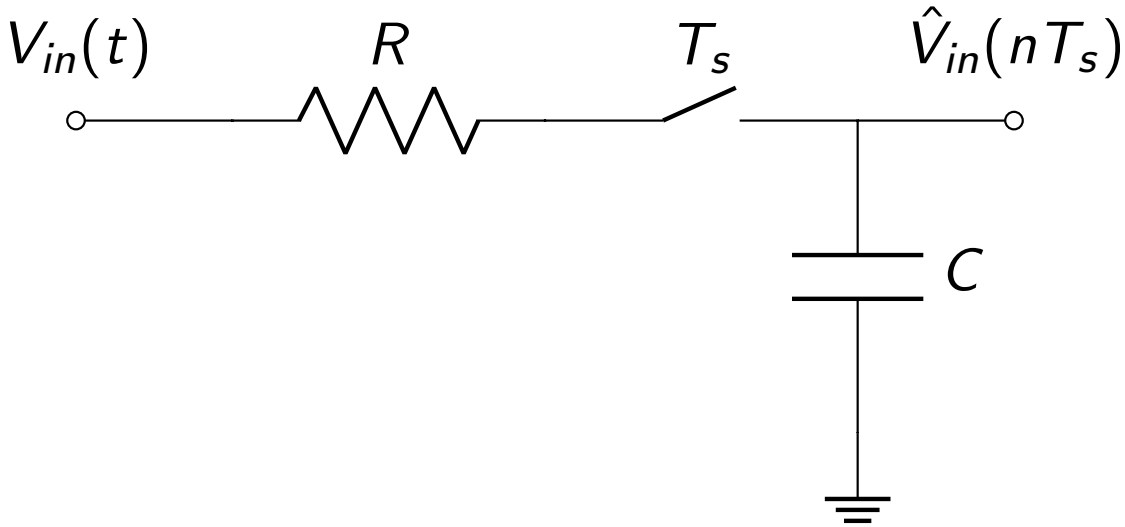
Limitations of S/H Circuit



$$\frac{1}{RC} >> f_{in}$$

- Difficult to construct S/H circuit with very high tracking BW.

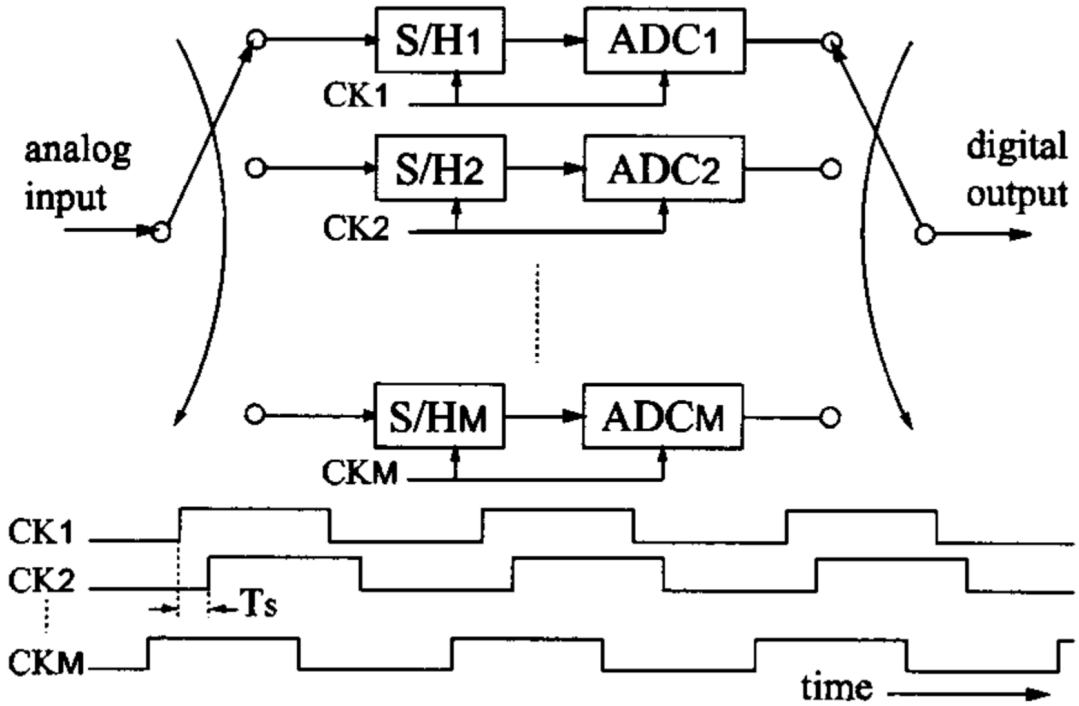
Limitations of S/H Circuit



$$\frac{1}{RC} >> f_{in}$$

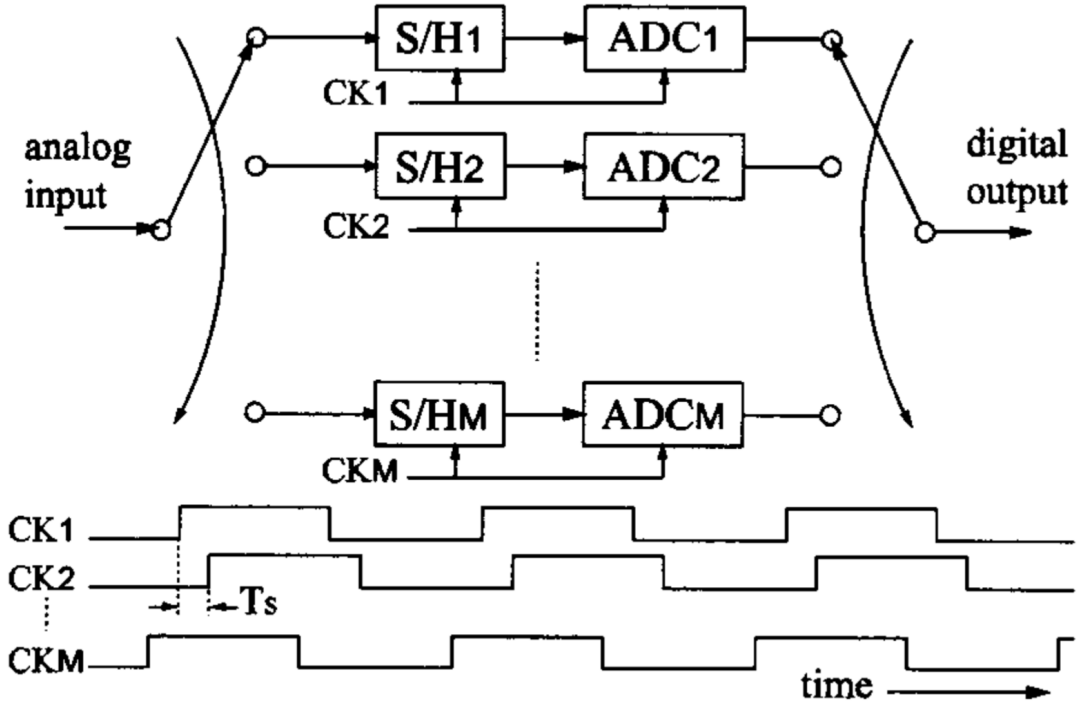
- Difficult to construct S/H circuit with very high tracking BW.
- Due to Low pass nature RF signal will attenuate.

Time-Interleaved ADC[1]



[1]N. Kurosawa *et al.*, "Explicit analysis of channel mismatch effects in time-interleaved ADC systems," in IEEE Transactions on Circuits and Systems I: Fundamental Theory

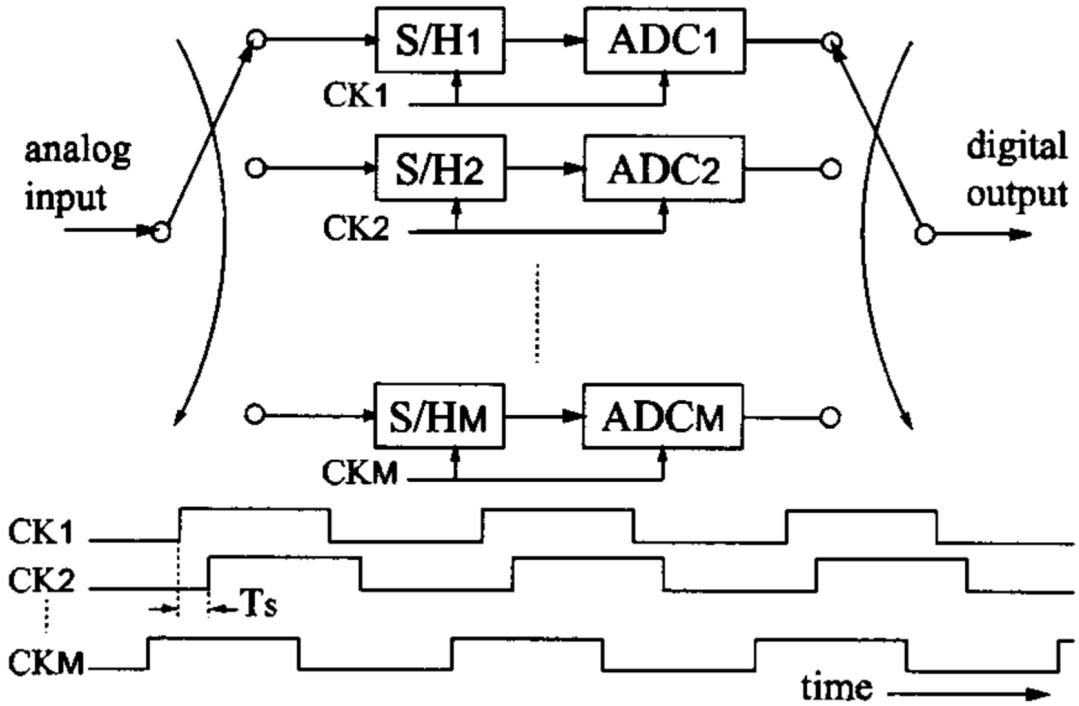
Time-Interleaved ADC[1]



- Required clock, $f_{clk} = f_s/M$

[1] N. Kurosawa *et al.*, "Explicit analysis of channel mismatch effects in time-interleaved ADC systems," in IEEE Transactions on Circuits and Systems I: Fundamental Theory

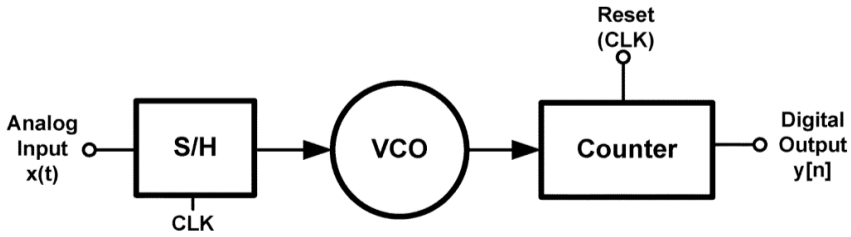
Time-Interleaved ADC[1]



- Required clock, $f_{clk} = f_s/M$
- Phase difference, $\phi_i = \frac{2\pi(i-1)}{M}$

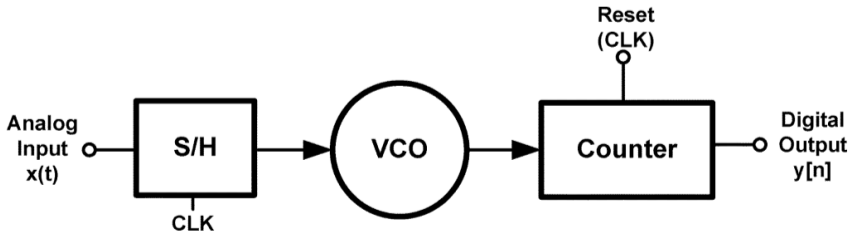
[1]N. Kurosawa *et al.*, "Explicit analysis of channel mismatch effects in time-interleaved ADC systems," in IEEE Transactions on Circuits and Systems I: Fundamental Theory

Analysis of ADC based on VCO [2]



[2] Y. Yoon *et al.*, "A Time-Based Bandpass ADC Using Time-Interleaved Voltage-Controlled Oscillators," in IEEE Transactions on Circuits and Systems I: Regular Papers

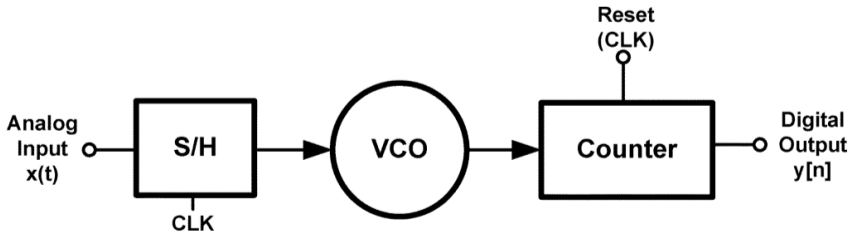
Analysis of ADC based on VCO [2]



- VCO translates the input voltage to phase.

[2] Y. Yoon *et al.*, "A Time-Based Bandpass ADC Using Time-Interleaved Voltage-Controlled Oscillators," in IEEE Transactions on Circuits and Systems I: Regular Papers

Analysis of ADC based on VCO [2]

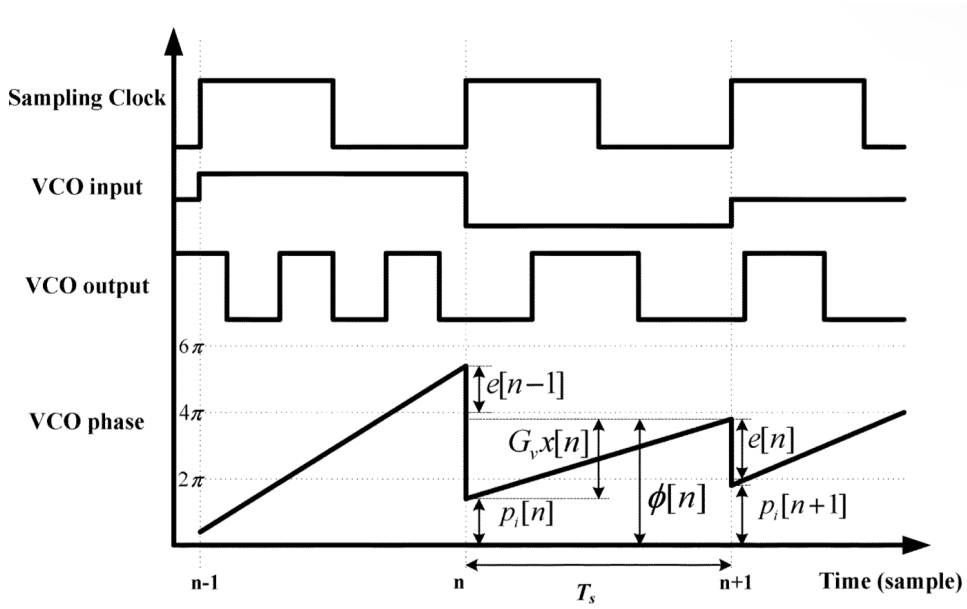


- VCO translates the input voltage to phase.
- Counter, counts the number of rasing/falling edges.

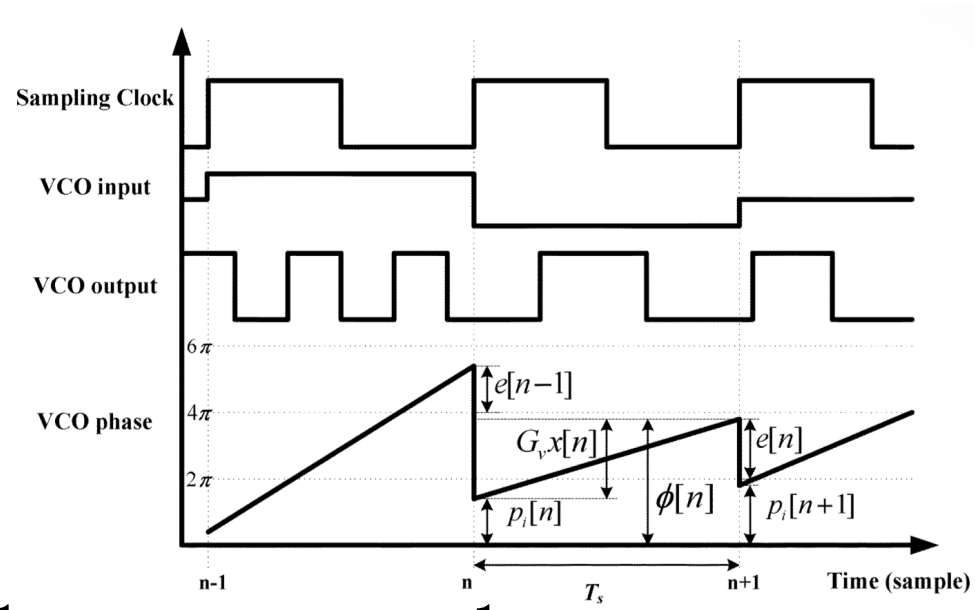
$$\phi[n] = \int_{nT_s}^{(n+1)T_s} K_v x[n]dt + p_i[n] = G_v x[n] + e[n-1]$$

[2] Y. Yoon *et al.*, "A Time-Based Bandpass ADC Using Time-Interleaved Voltage-Controlled Oscillators," in IEEE Transactions on Circuits and Systems I: Regular Papers

Analysis of ADC based on VCO



Analysis of ADC based on VCO

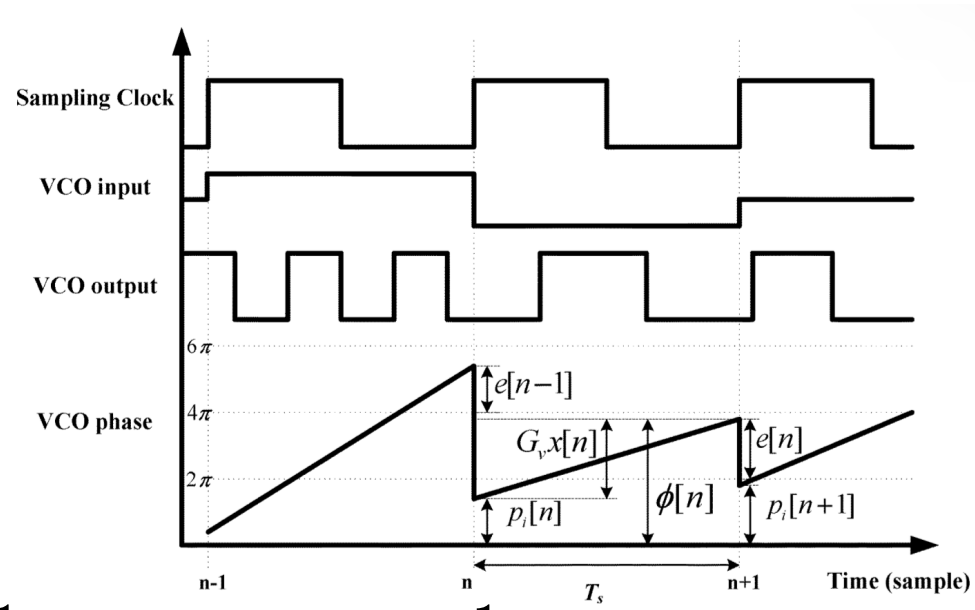


$$y[n] = \frac{1}{2\pi}(\phi[n] - e[n]) = \frac{1}{2\pi}(G_v x[n] + e[n-1] - e[n])$$

$$Y(z) = \frac{1}{2\pi}(G_v X(z) + (z^{-1} - 1)E(z))$$

$$NTF(z) = \frac{1}{2\pi}(z^{-1} - 1) \implies |NTF(e^{j\omega})| = |2sin(\omega/2)|$$

Analysis of ADC based on VCO



$$y[n] = \frac{1}{2\pi}(\phi[n] - e[n]) = \frac{1}{2\pi}(G_v x[n] + e[n-1] - e[n])$$

$$Y(z) = \frac{1}{2\pi}(G_v X(z) + (z^{-1} - 1)E(z))$$

$$NTF(z) = \frac{1}{2\pi}(z^{-1} - 1) \implies |NTF(e^{j\omega})| = |2sin(\omega/2)|$$

- First order high-pass filter.

Extension for N-th order ADC

$$NTF(z) = \frac{1}{2\pi}(z^{-N} - 1)$$

Extension for N-th order ADC

$$NTF(z) = \frac{1}{2\pi}(z^{-N} - 1)$$

- Zeros will occur when $z = 1^{1/N} \implies \omega_k = \frac{2\pi(k-1)}{N}$.

Extension for N-th order ADC

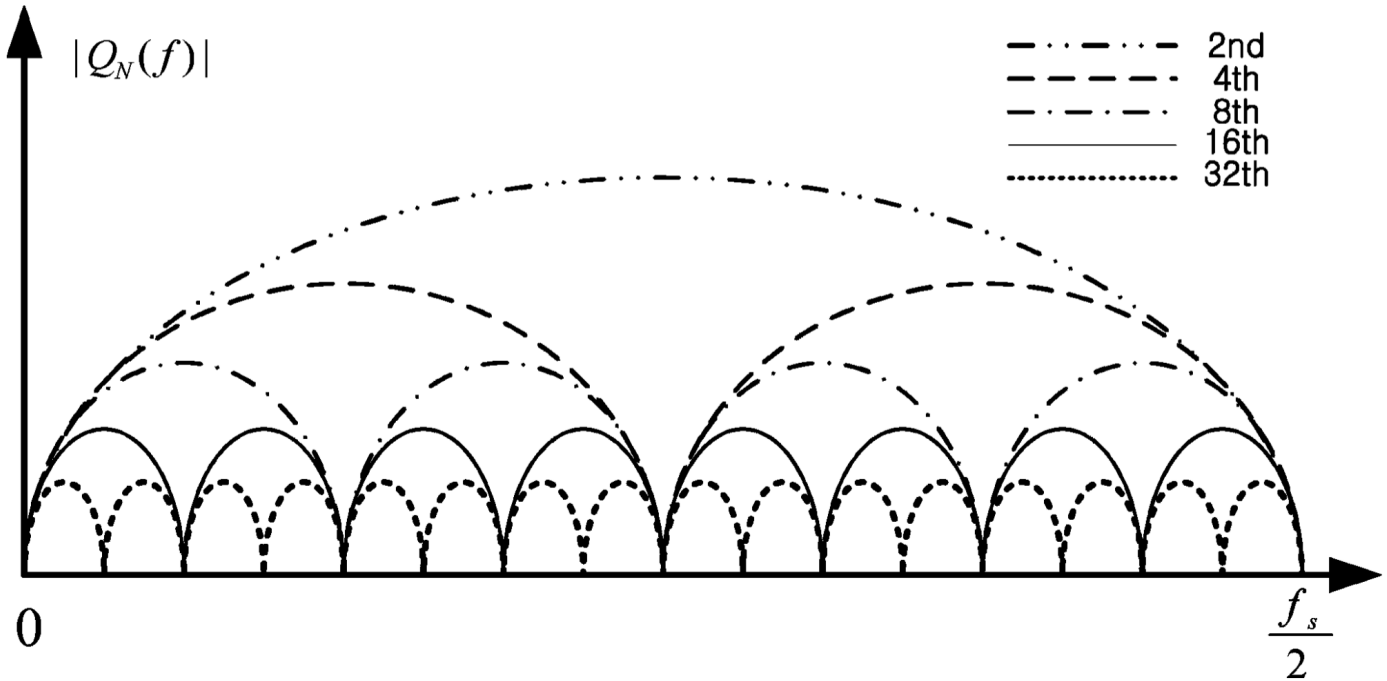
$$NTF(z) = \frac{1}{2\pi}(z^{-N} - 1)$$

- Zeros will occur when $z = 1^{1/N} \implies \omega_k = \frac{2\pi(k-1)}{N}$.
- We will try to center our signal frequency at these zeros.

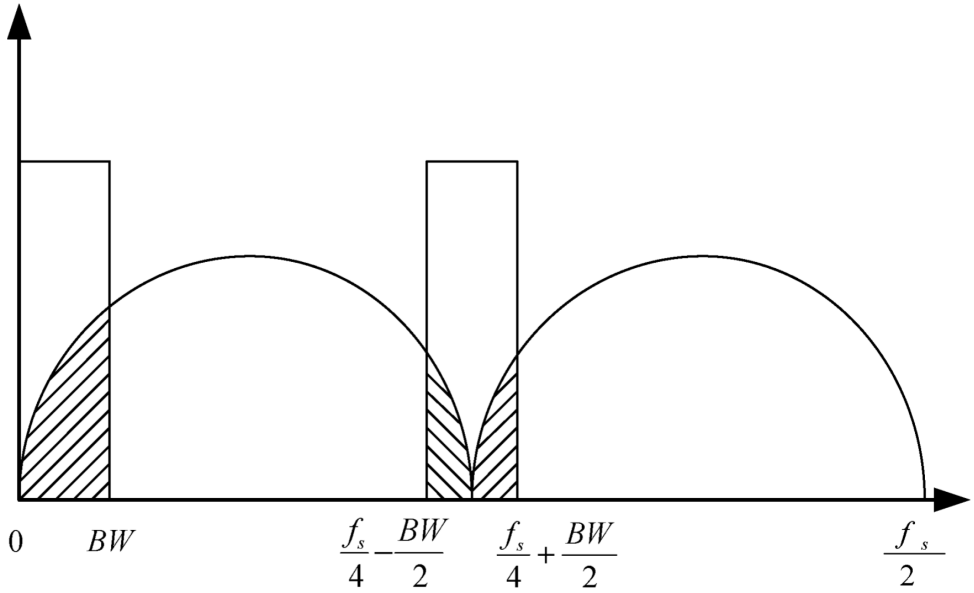
Extension for N-th order ADC

$$NTF(z) = \frac{1}{2\pi}(z^{-N} - 1)$$

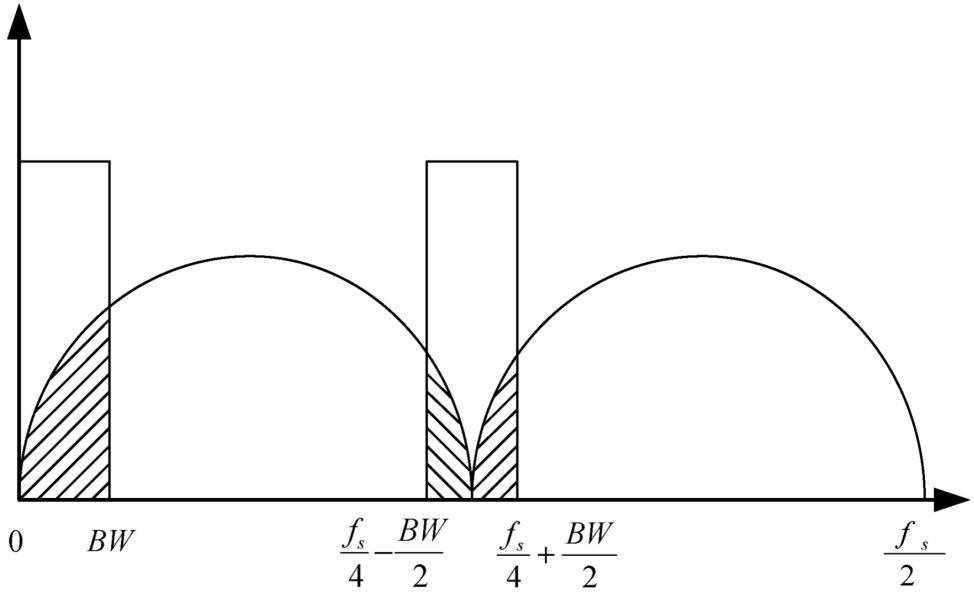
- Zeros will occur when $z = 1^{1/N} \implies \omega_k = \frac{2\pi(k-1)}{N}$.
- We will try to center our signal frequency at these zeros.



Where do we center our signal?



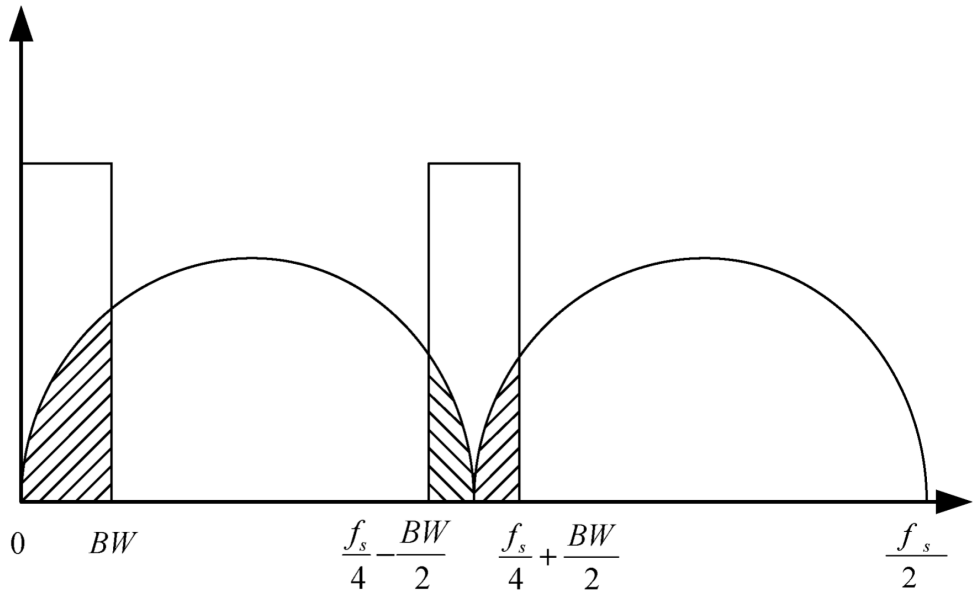
Where do we center our signal?



- As low pass signal,

$$SQNR = 6.02ENOB - 3.41 + 30log(OSR)dB$$

Where do we center our signal?



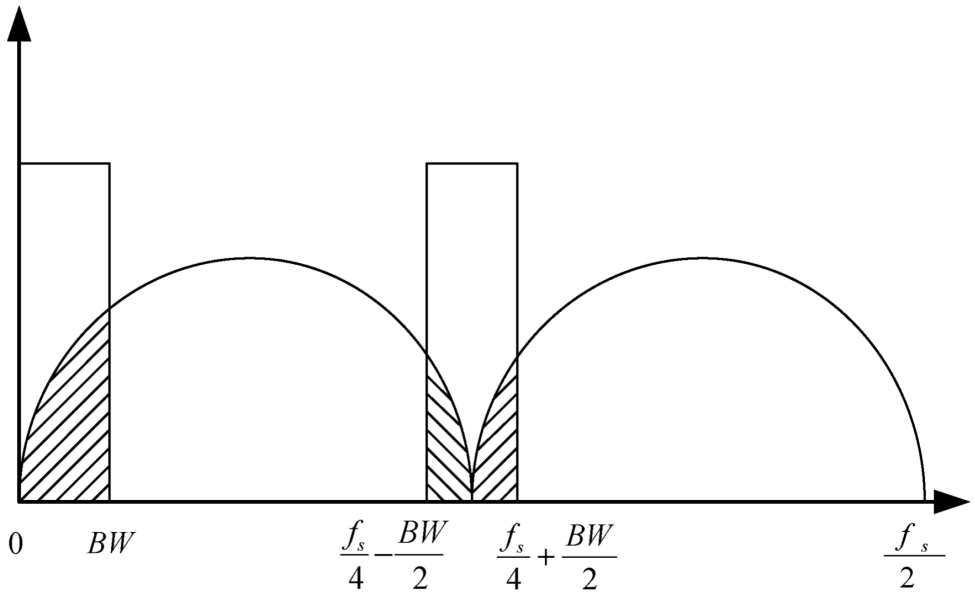
- As low pass signal,

$$SQNR = 6.02ENOB - 3.41 + 30log(OSR)dB$$

- At zeroes,

$$SQNR = 6.02ENOB - 3.41 + 6.02 + 30log(OSR)dB$$

Where do we center our signal?



- As low pass signal,

$$SQNR = 6.02ENOB - 3.41 + 30log(OSR)dB$$

- At zeroes,

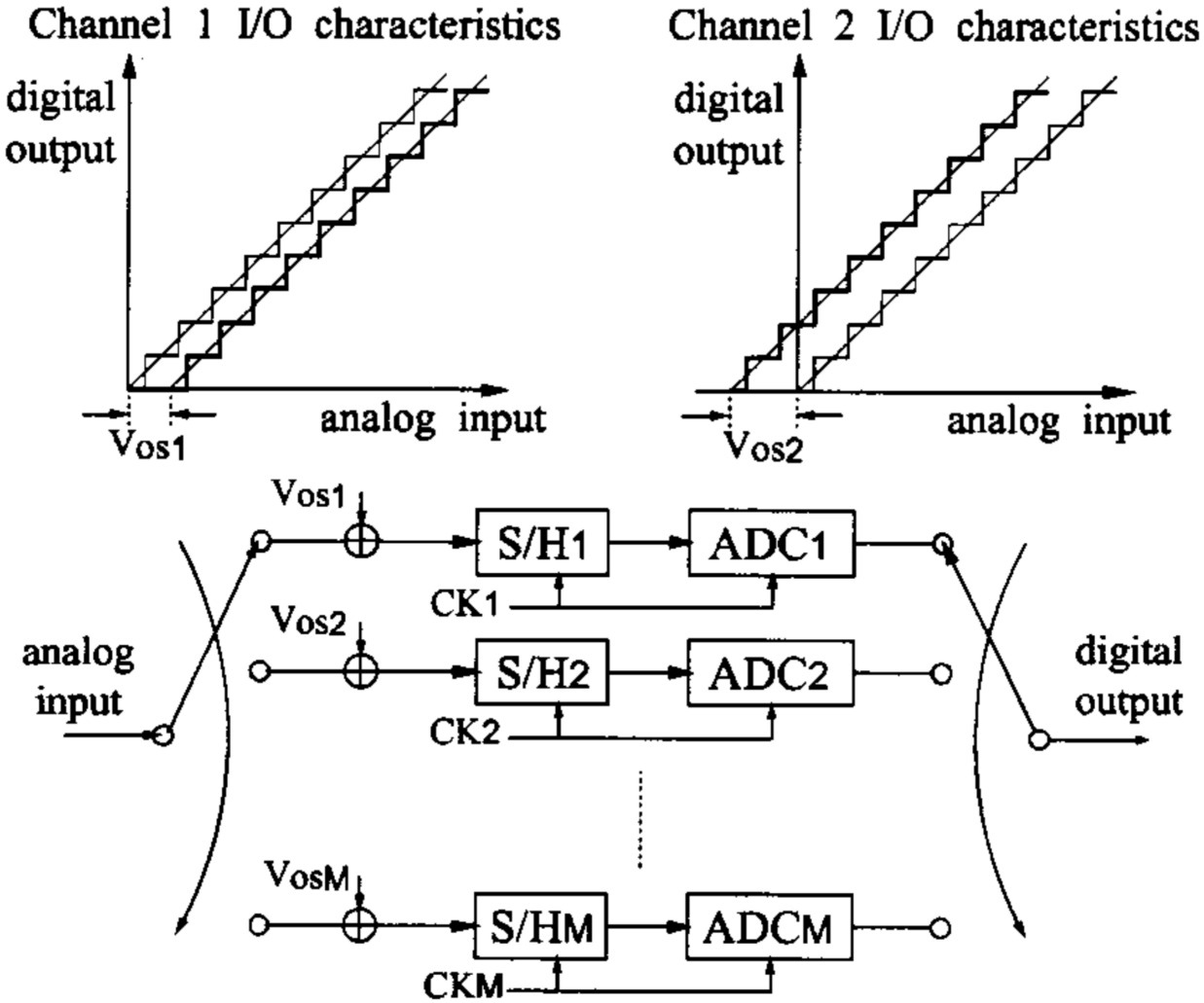
$$SQNR = 6.02ENOB - 3.41 + 6.02 + 30log(OSR)dB$$

Increase of 6.02dB is equivalent to increase in 1-bit precision of ADC!!

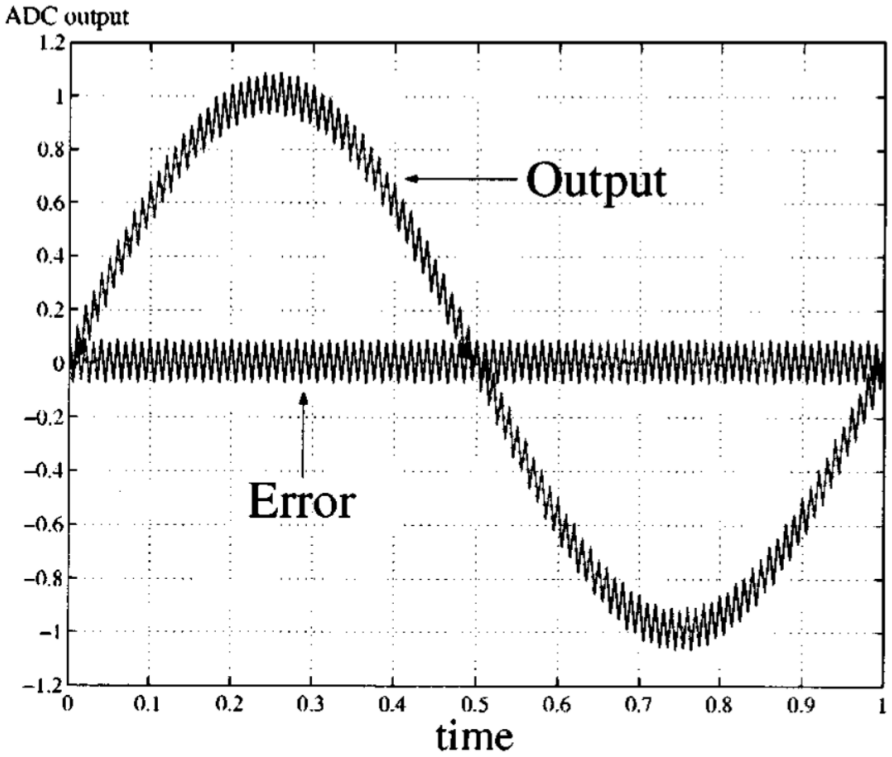
Non-idealities

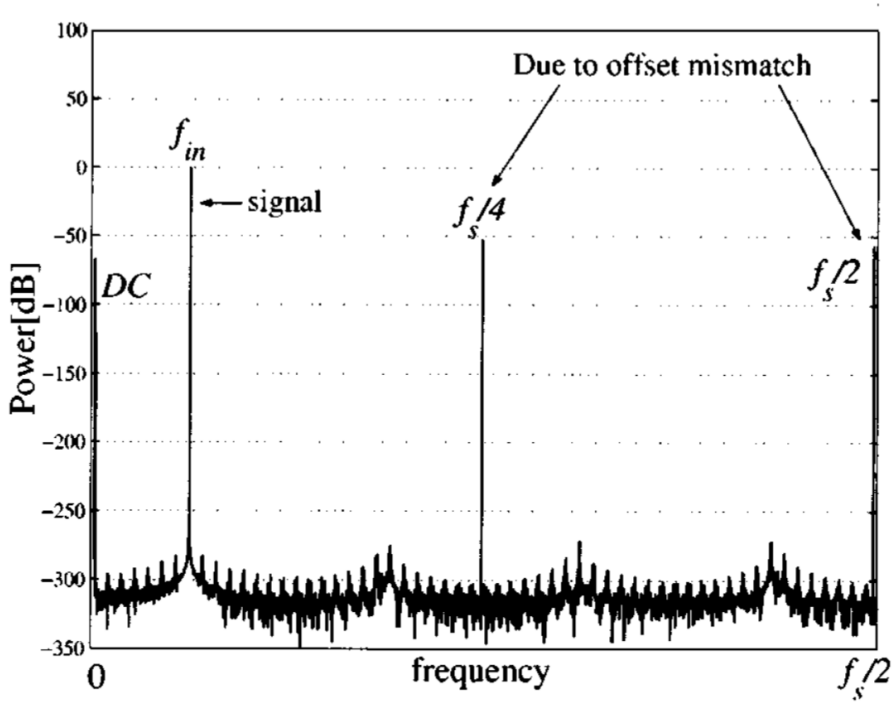
- DC offset
- Gain mismatch
- Clock Jitter/Skew
- Bandwidth mismatch
- Non-linearity in VCO

DC offset

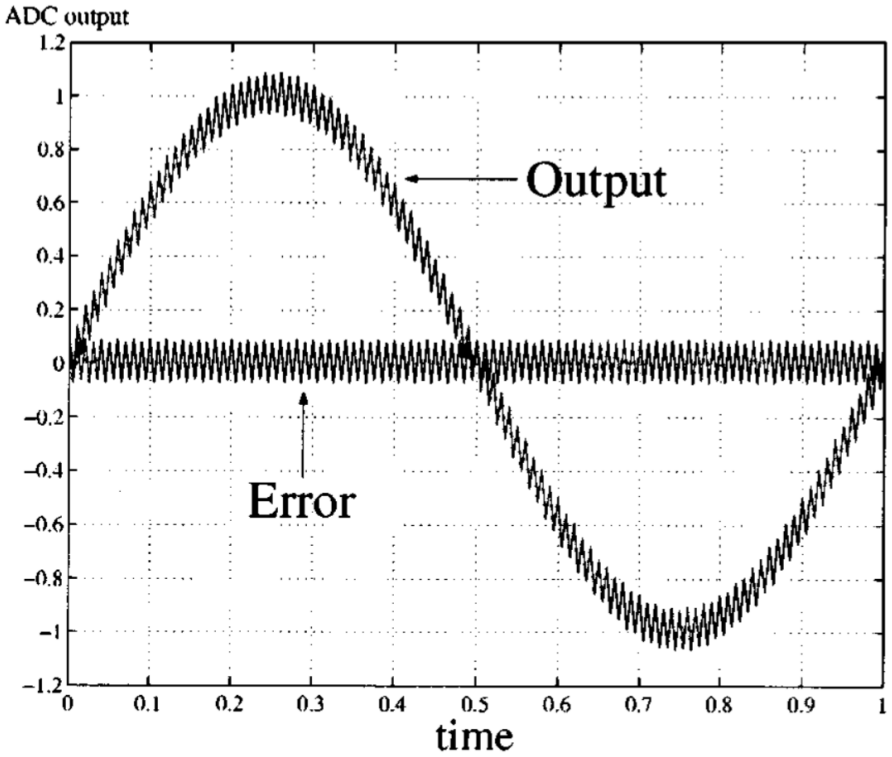

Channel 1 I/O characteristics
digital output
analog input
Vos1
Channel 2 I/O characteristics
digital output
analog input
Vos2
Vos1
S/H1
ADC1
CK1
Vos2
S/H2
ADC2
CK2
analog input
digital output
VosM
S/HM
ADCM
CKM

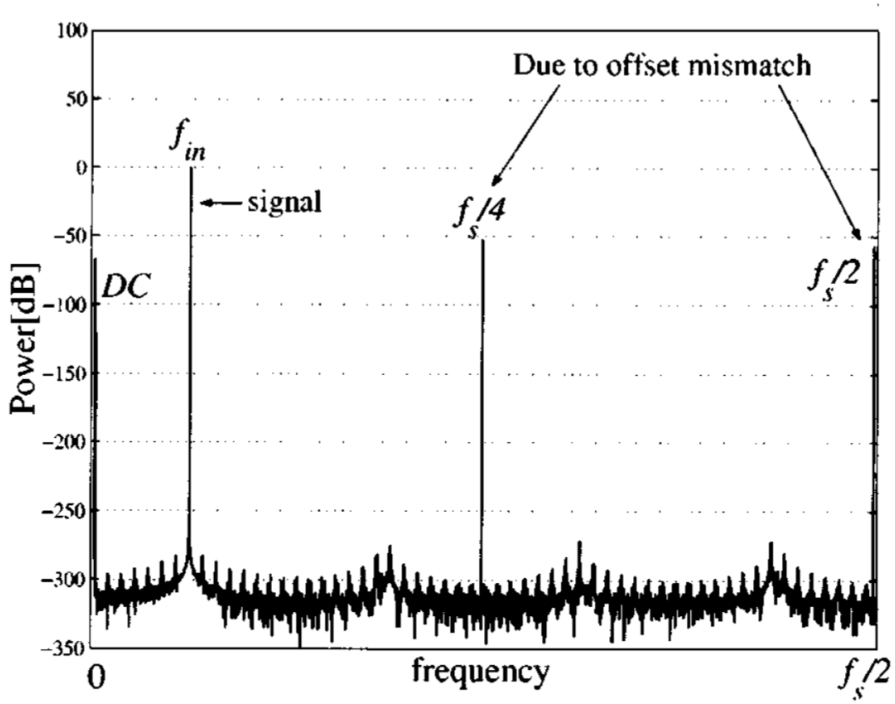
DC offset


ADC output
Output
Error
time


Due to offset mismatch
f_{in}
signal
$f_s/4$
DC
$f_s/2$
Power[dB]
0
frequency
$f_s/2$

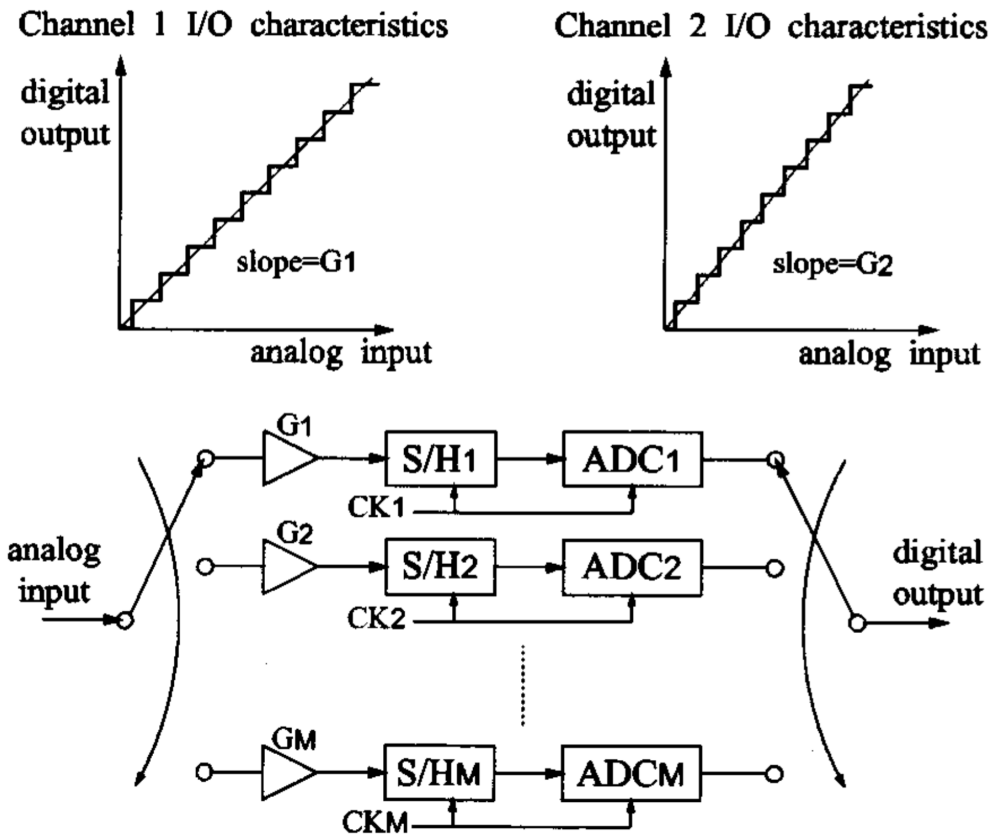
DC offset



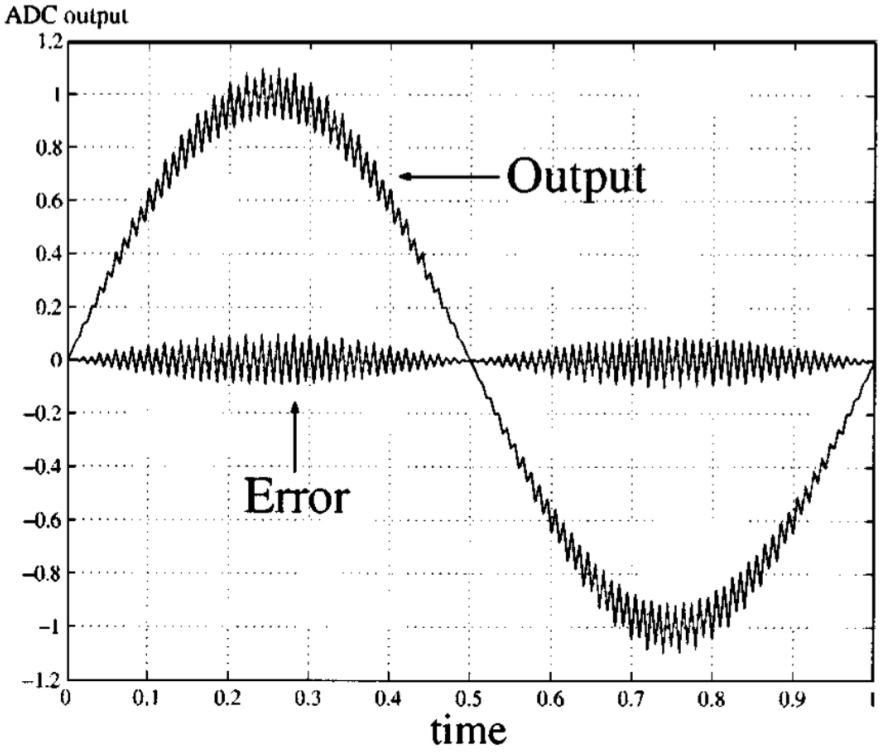


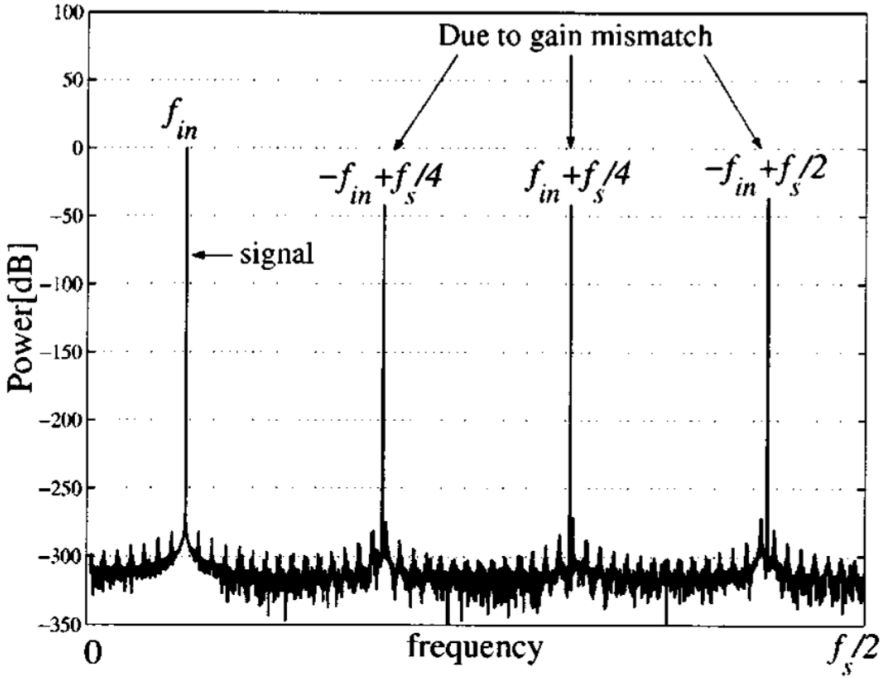
- We can see that dc offset periodicity $\Longrightarrow$ peaks at $\frac{k}{M} f_s$

Gain mismatch

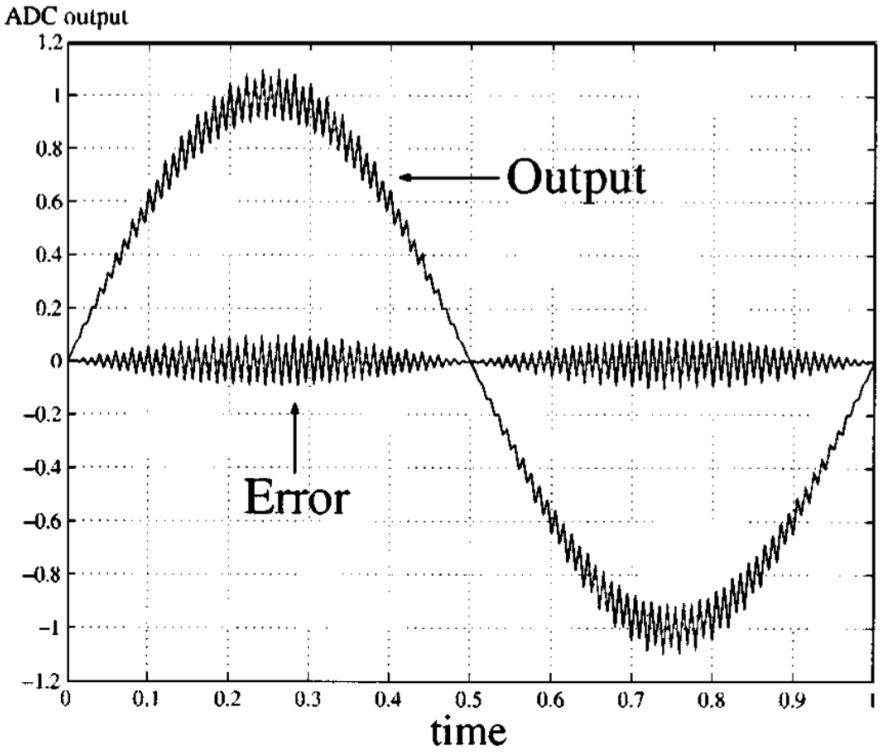


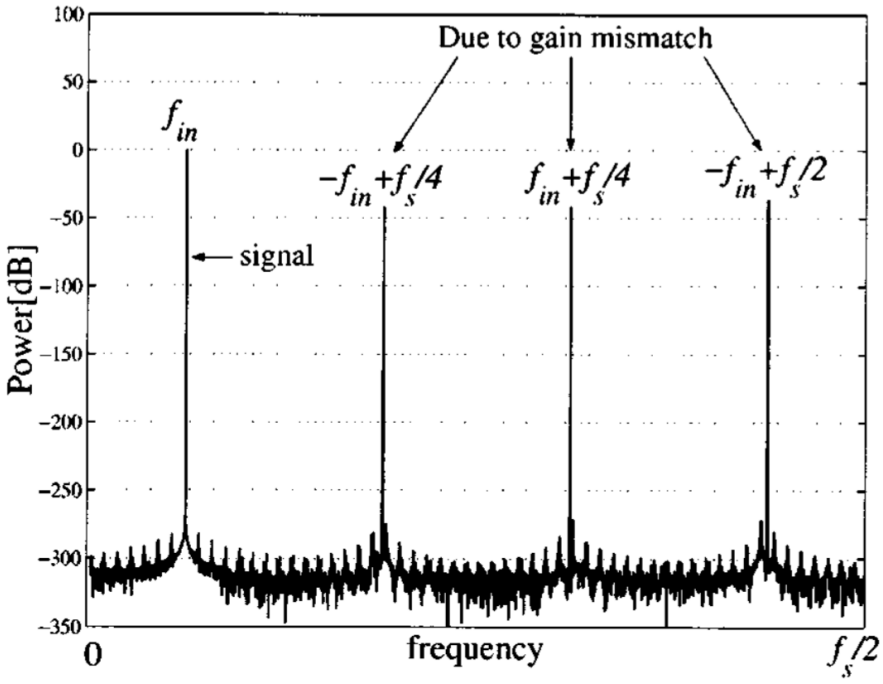
Gain mismatch





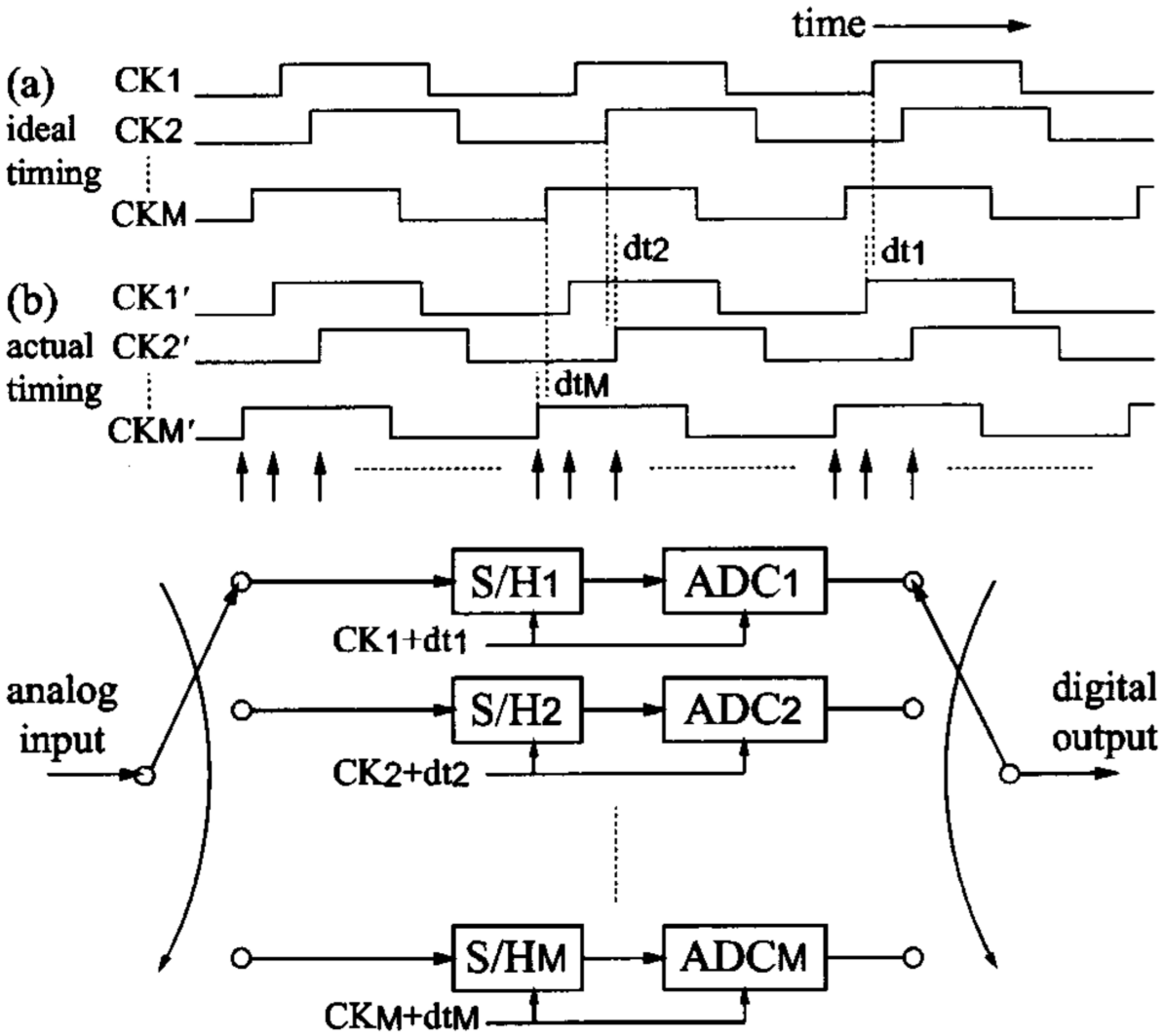
Gain mismatch



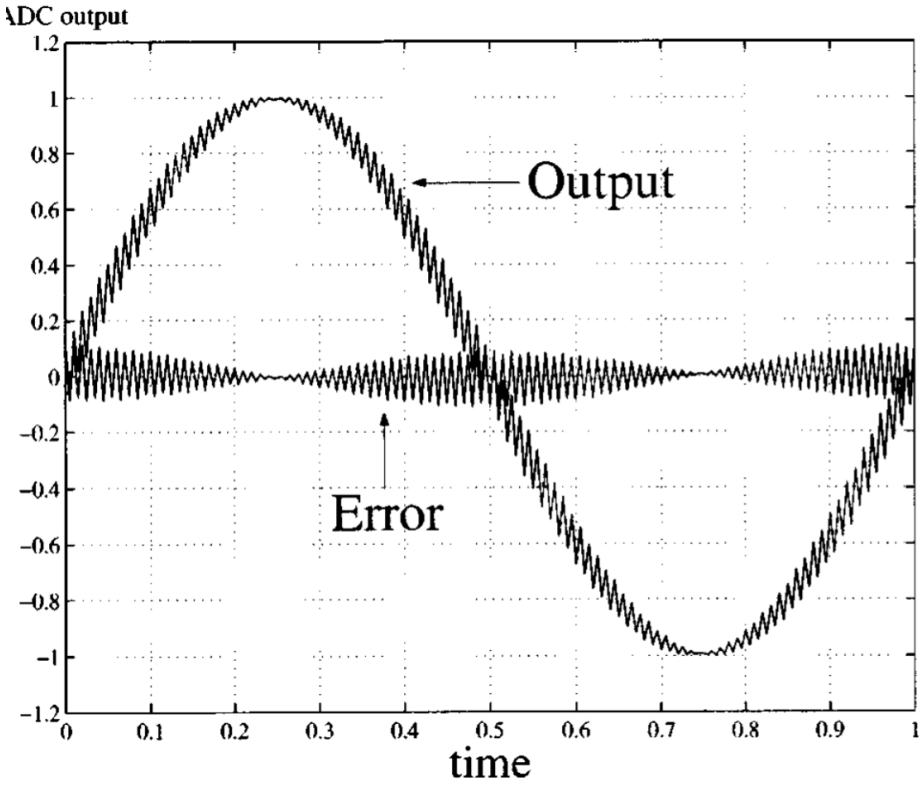


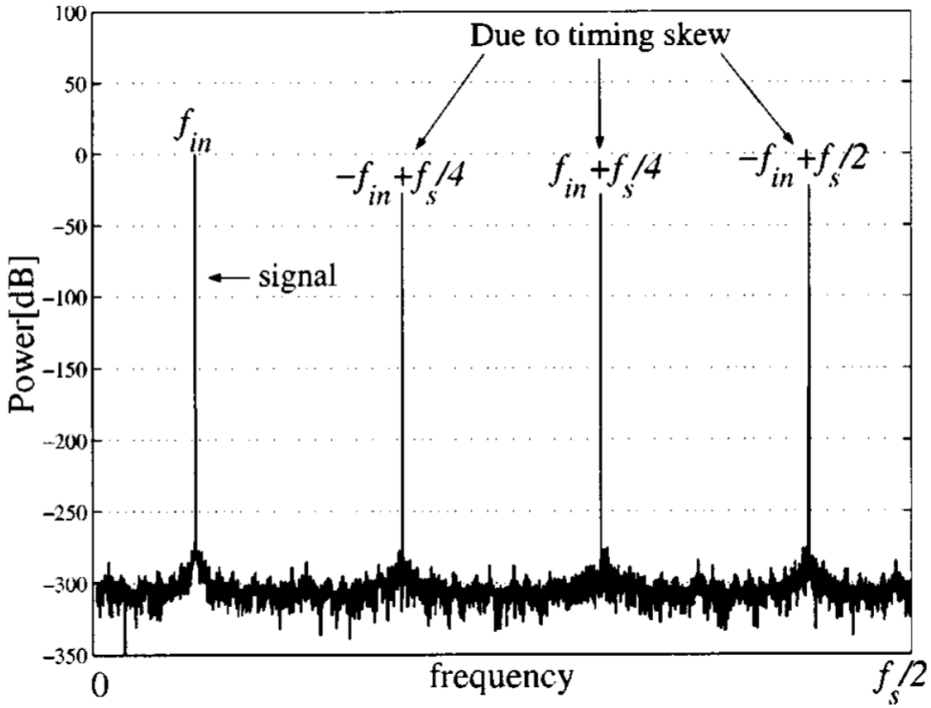
- Gain mismatch can be looked as A.M $\Longrightarrow$ peaks at $\pm f_{in} + \frac{k}{M} f_s$
- Error at higher amplitude is more.

Clock jitter

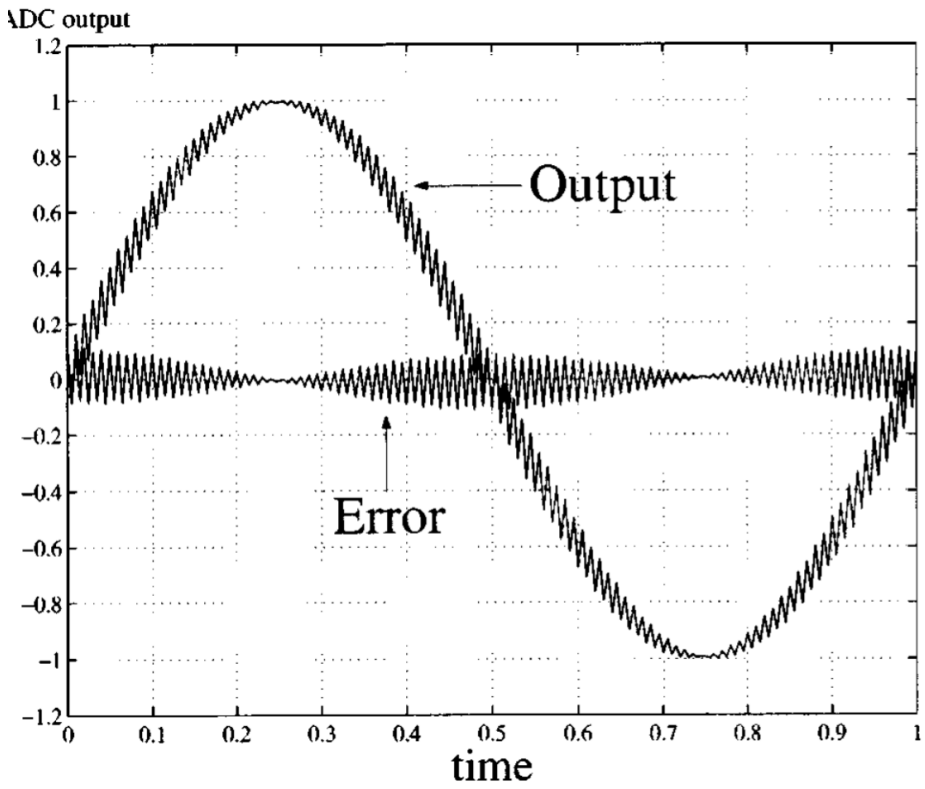


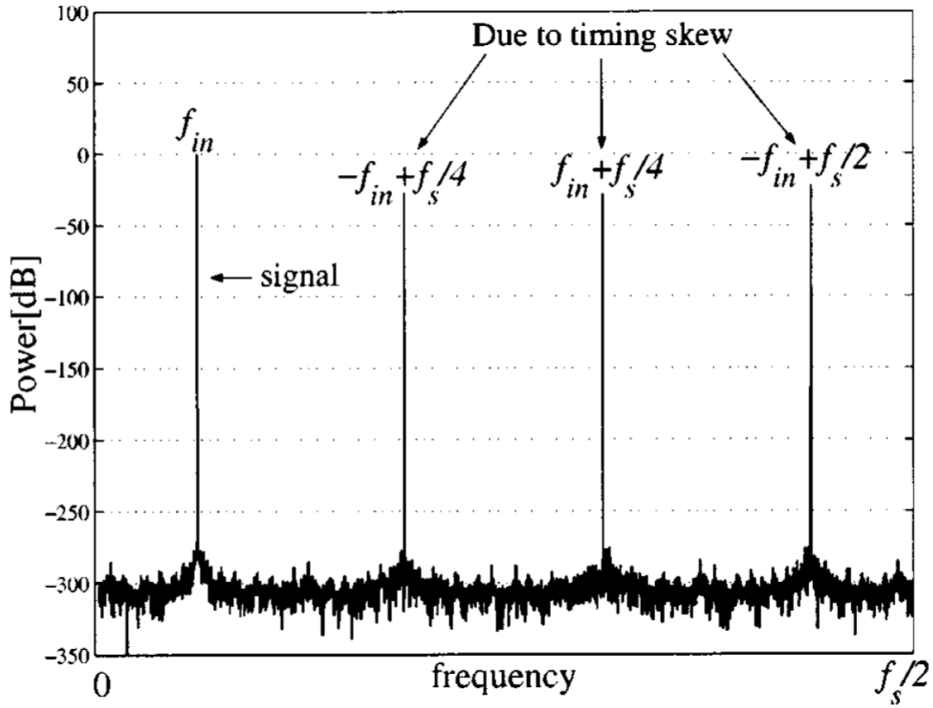
Clock jitter





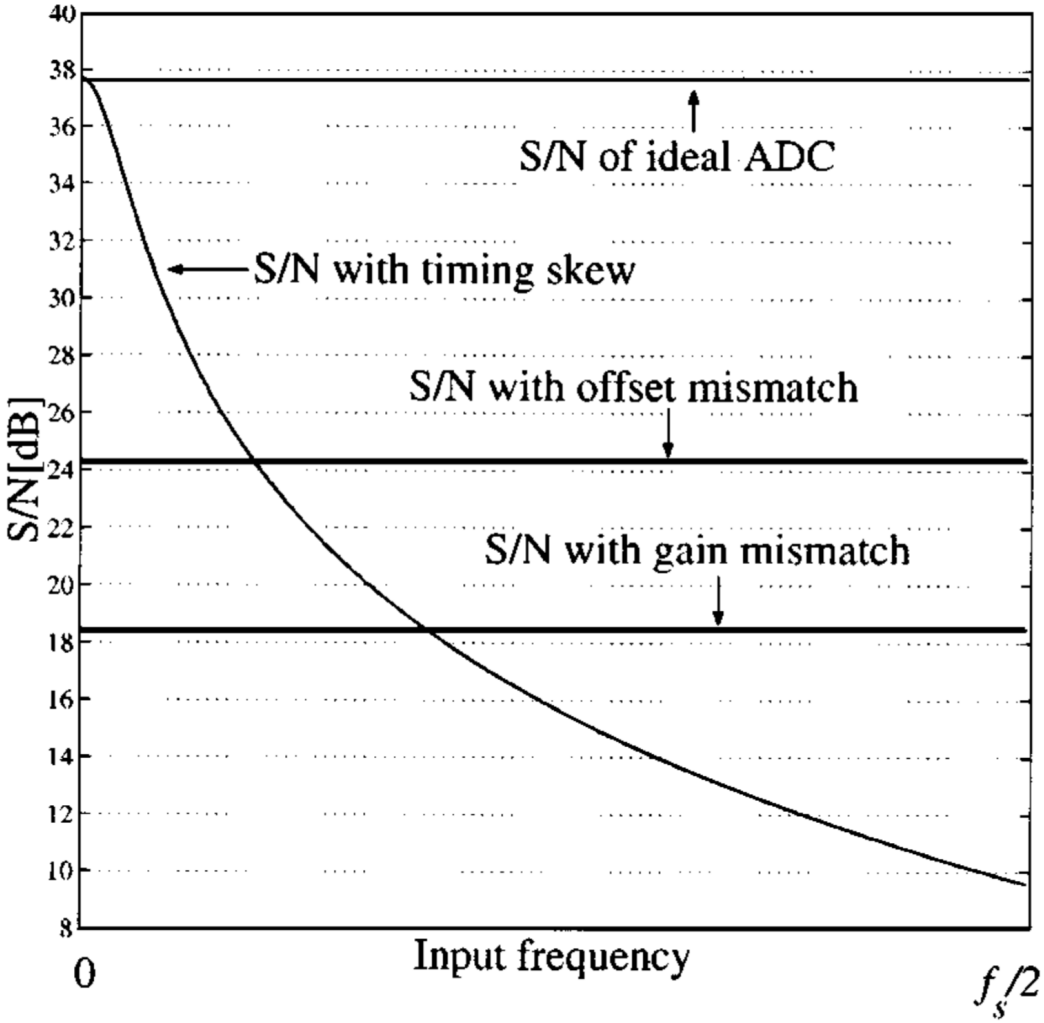
Clock jitter





- Clock skew behaves like P.M $\implies$ peaks at $\pm f_{in} + \frac{k}{M} f_s$.
- Error is high at places where slew rate is more.

SNR comparisions



Area comparisions

Metrics	3x ADS7056	THS1408
Resolution	14-bit	14-bit
Sampling rate	7.5 MSPS	**8 MSPS**
SQNR (dB)	**73**	72
Power consumption (mW)	**17.5**	270
Package area (mm^2)	**6.75**	81

DataSheet by TI

References

- N. Kurosawa *et al.*, "Explicit analysis of channel mismatch effects in time-interleaved ADC systems," in IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications.
- Y. Yoon *et al.*, "A Time-Based Bandpass ADC Using Time-Interleaved Voltage-Controlled Oscillators," in IEEE Transactions on Circuits and Systems I: Regular Papers
- Joonhee Lee *et al.*, "A 1.8 to 2.4-GHz 20mW digital-intensive RF sampling receiver with a noise-canceling bandpass low-noise amplifier in 90nm CMOS," 2010 IEEE Radio Frequency Integrated Circuits Symposium.
- Advantages of Direct RF Sampling Architectures, by www.ni.com

Thank You