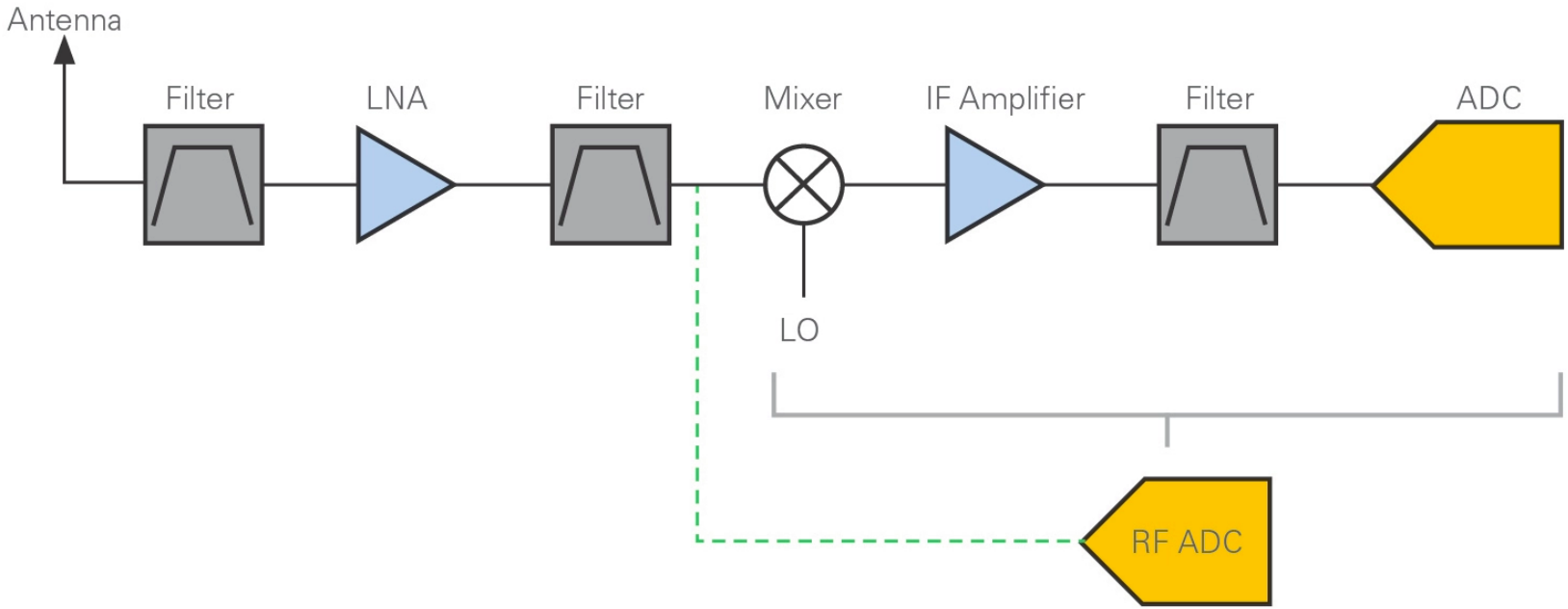
ADCs for Direct RF Sampling

Tadipatri Uday Kiran Reddy - EE19BTECH11038

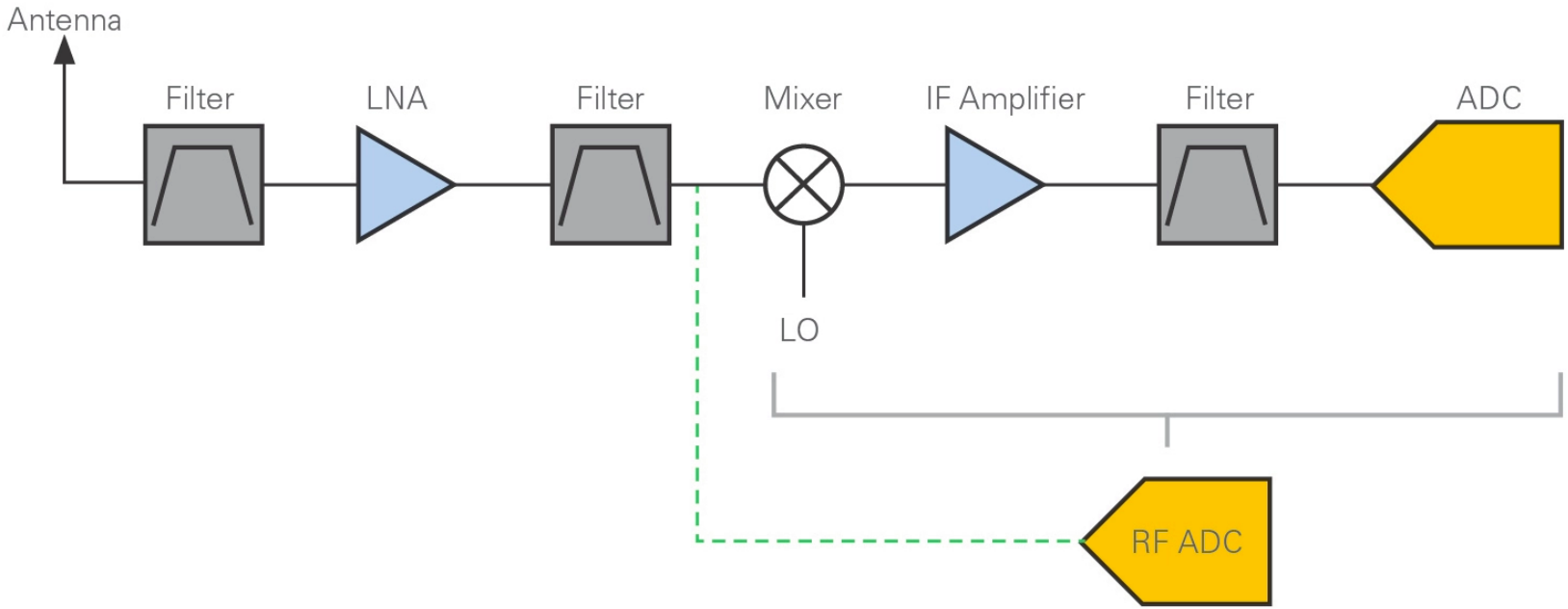
IIT Hyderabad

May 19, 2022

Introduction

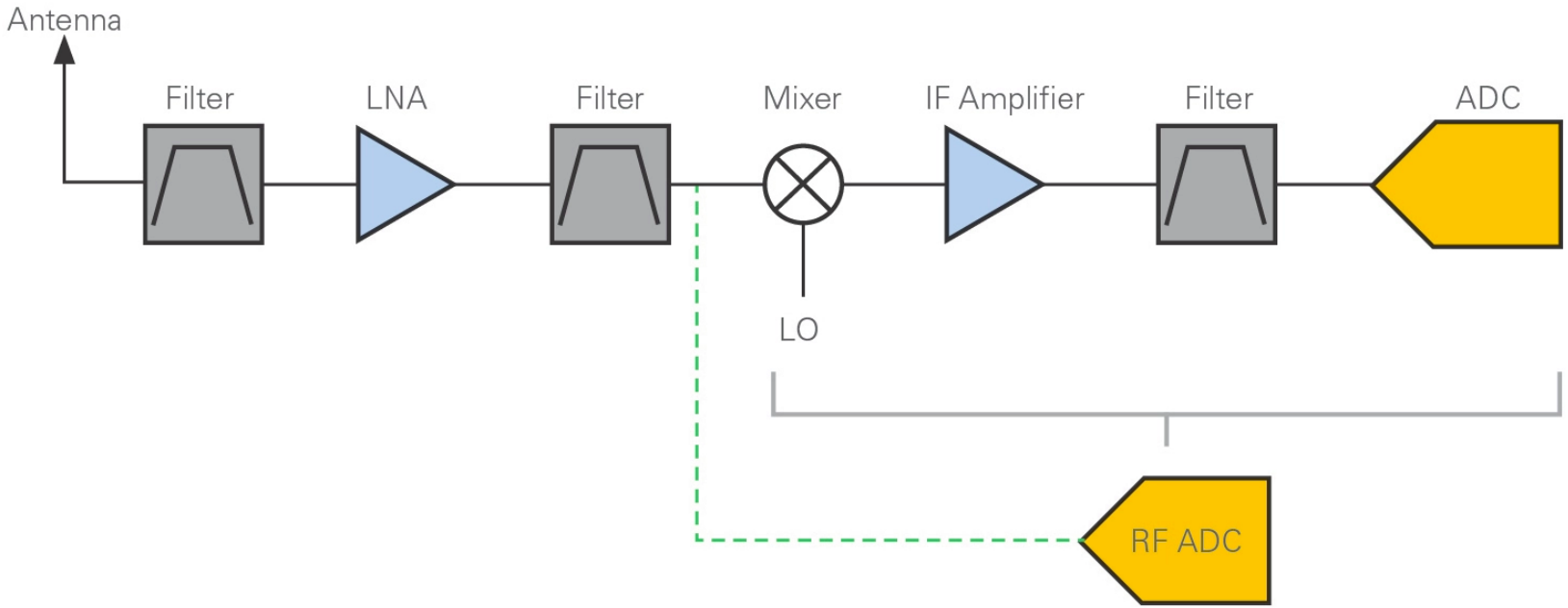


Introduction



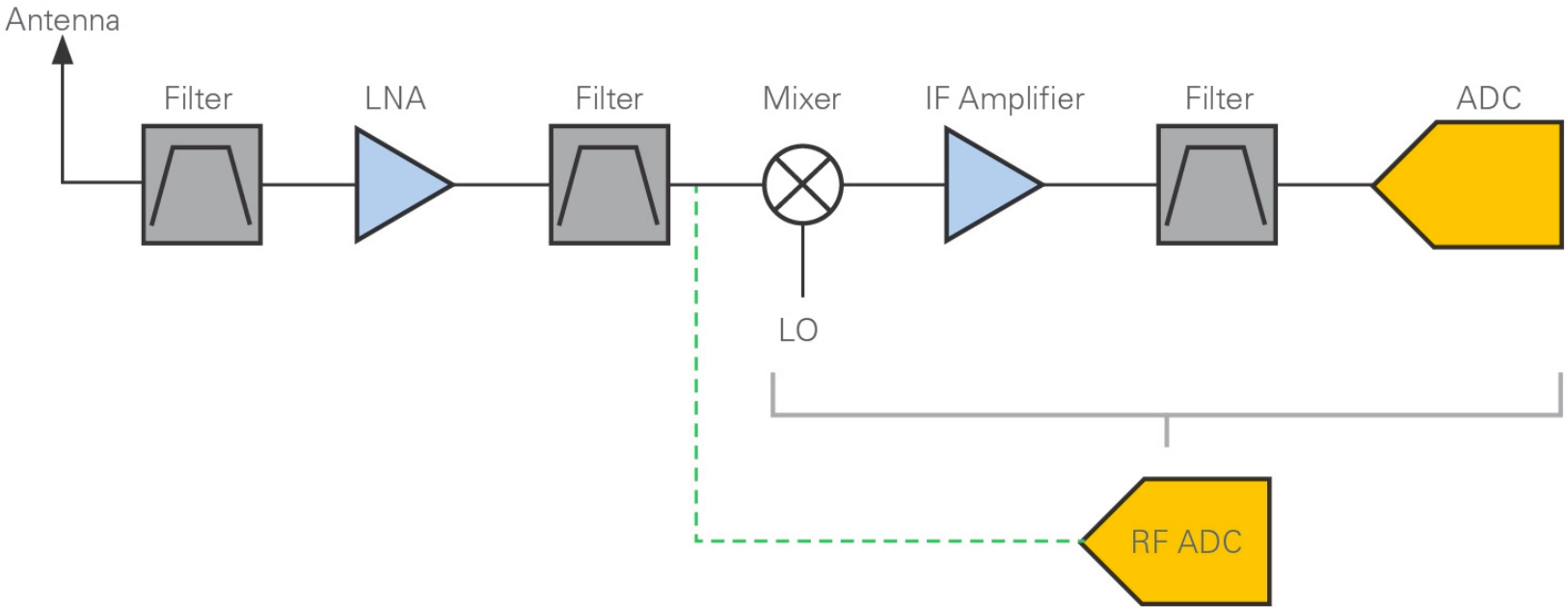
- ADC architecture for sampling at RF with low power and area.

Introduction



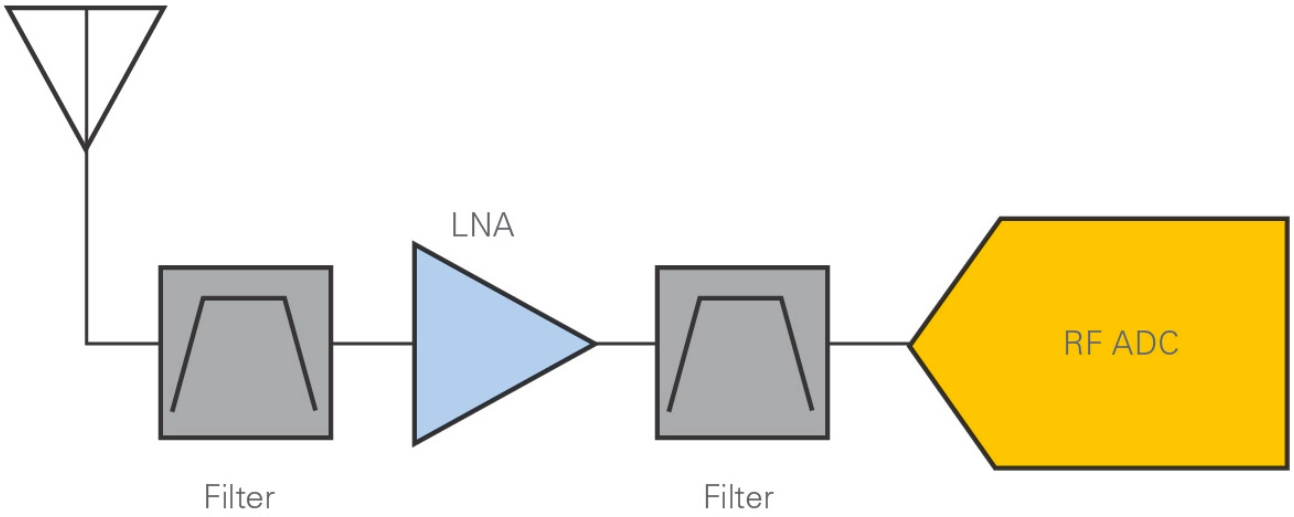
- ADC architecture for sampling at RF with low power and area.
- High sampling rate with relatively slow circuits, *Time-Interleaved ADC*.

Introduction



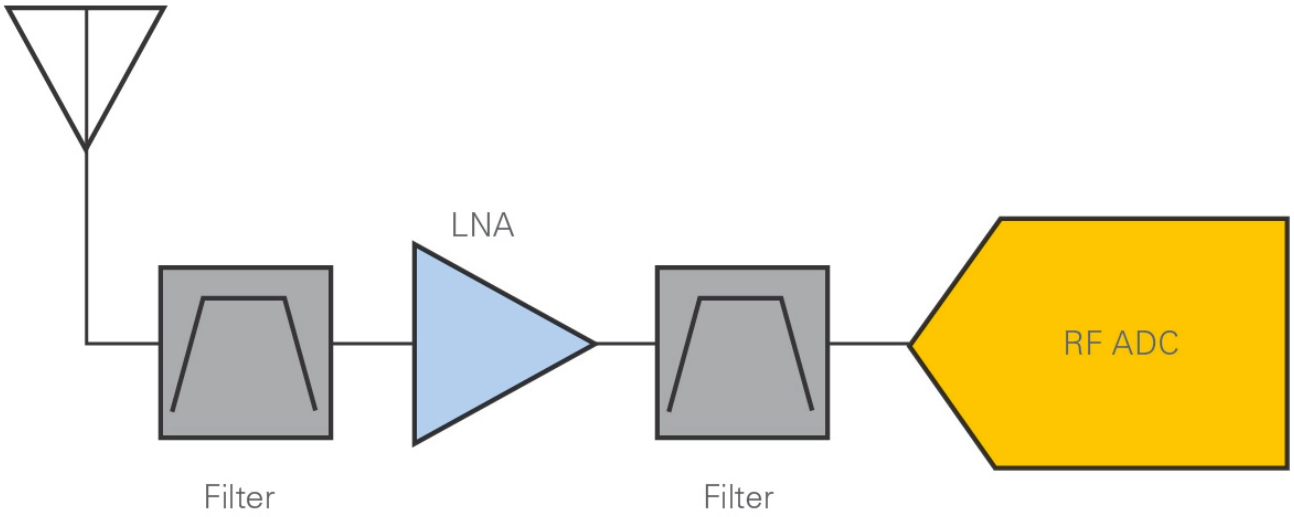
- ADC architecture for sampling at RF with low power and area.
- High sampling rate with relatively slow circuits, *Time-Interleaved ADC*.
- Minimize quantisation and noise error.

Motivation for RF sampling



- Simpler hardware design due to elimination of analog frequency conversion.

Motivation for RF sampling



- Simpler hardware design due to elimination of analog frequency conversion.
- Exploit the computing power of DSPs.

Analog-to-Digital Converters

Time-Interleaved ADC

Challenges

Thank You