EE5192

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Mini-project 2

1. Design an LNA to meet the following specifications:

   - Gain $>$ 20 dB
   - Input return loss $>$ 15 dB
   - NF $<$ 2 dB
   - IIP_3 $>$ -30 dBm
   - Centre frequency: 2.5 GHz
   - Load capacitance: 100 fF

   System-level constraints:

   - Supply voltage $<$ 1.2 V
   - Inductors available: Value $<$ 10 nH, Q=10 @ 2.5 GHz.

   Objective is to minimize power consumption while satisfying the above specifications.

   Submit a report with the following:

   - Brief justification for the choice of LNA topology.
   - Design details.
   - Input return loss plot from 2 GHz to 3 GHz.
   - Gain plot from 2 GHz to 3 GHz.
   - NF plot from 2 GHz to 3 GHz.
   - IIP_3 plot at centre frequency.
   - Netlist.

   CAD info:

   - Use ideal capacitors and resistors. All inductors must have loss modelled by adding a series resistance corresponding to required Q value.
   - Use the MOS models and library for LTspice uploaded along with the instruction.
   - Use transient analysis for estimating IIP3.