ADCs for Direct RF Sampling

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IIT Hyderabad

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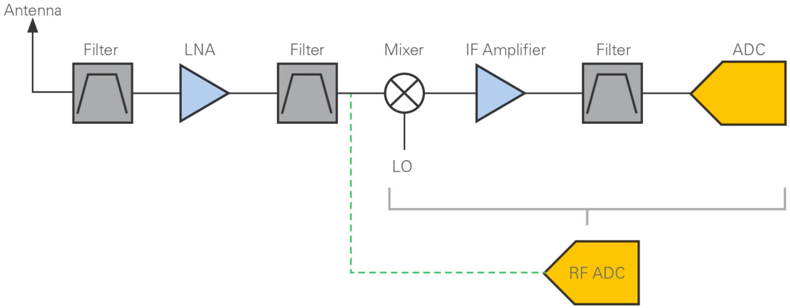
Introduction



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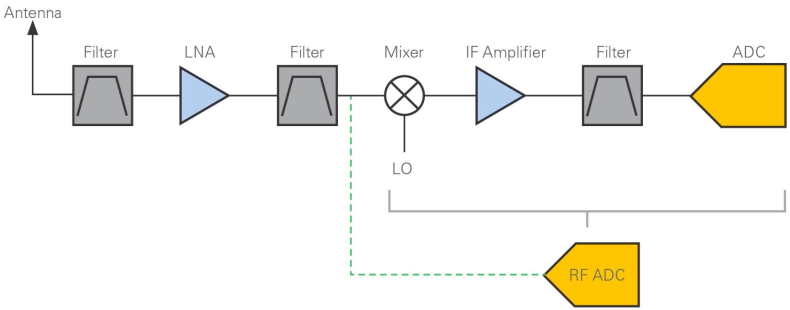

- ADC architecture for sampling at RF with low power and area.

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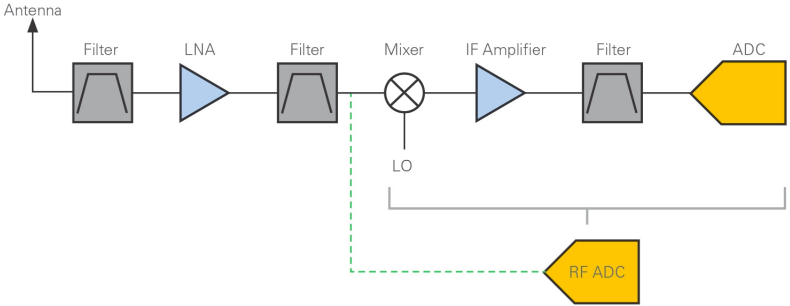

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- High sampling rate with relatively slow circuits, *Time-Interleaved ADC*.

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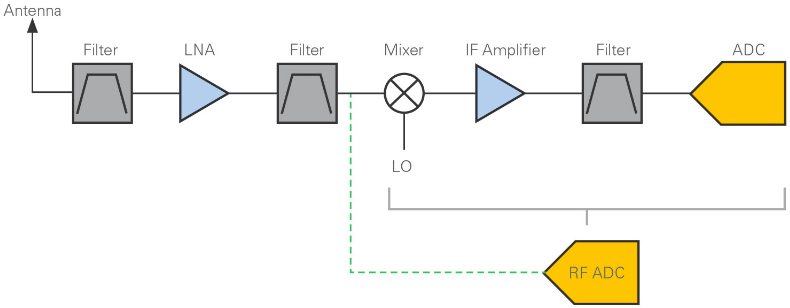
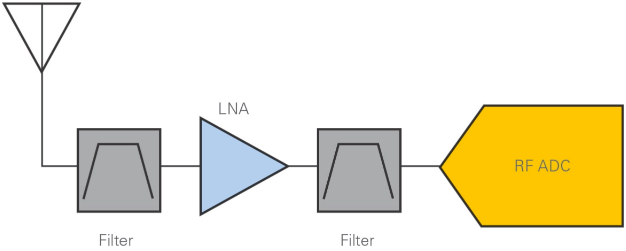


- ADC architecture for sampling at RF with low power and area.
- High sampling rate with relatively slow circuits, *Time-Interleaved ADC*.
- Minimize quantisation and noise error.

Motivation for RF sampling



- Simpler hardware design due to elimination of analog frequency conversion.

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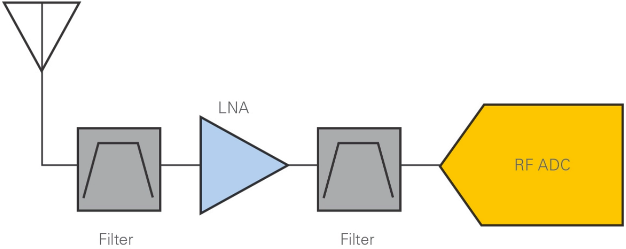

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- Exploit the computing power of DSPs.

Analog-to-Digital Converters

- Sample the input signal at reconstructable rate and then Quantize.

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$$SQNR = 6.02ENOB + 1.76dB$$

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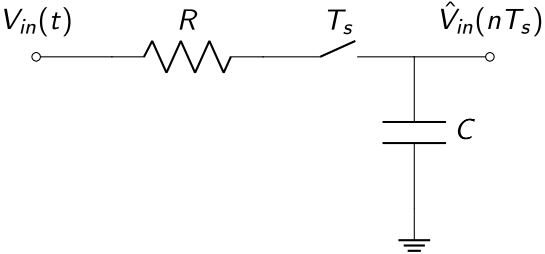
  Noise spectral density at ROI is less!!

Limitations of S/H Circuit



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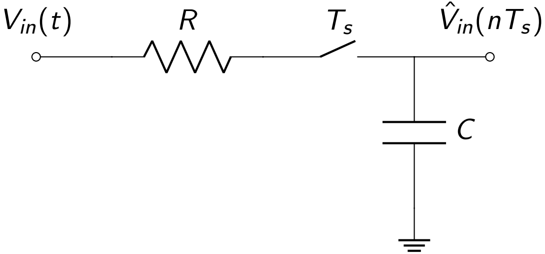

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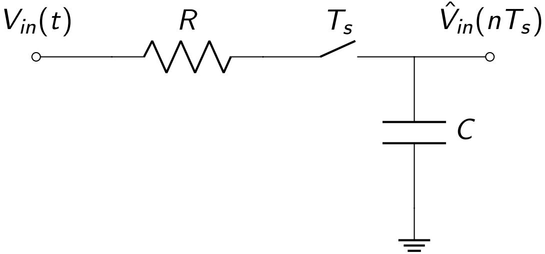

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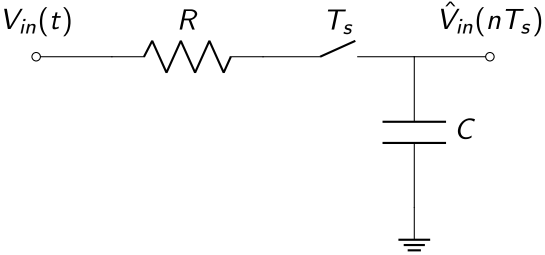

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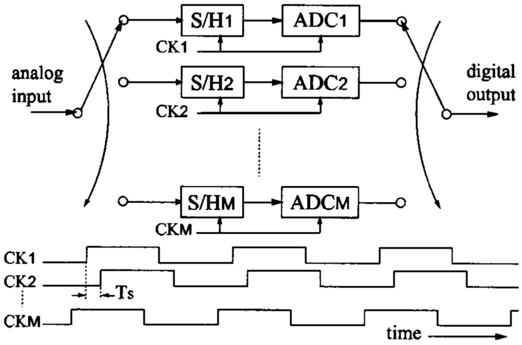
- Difficult to construct S/H circuit with very high tracking BW.
- Due to Low pass nature RF signal will attenuate.

Time-Interleaved ADC



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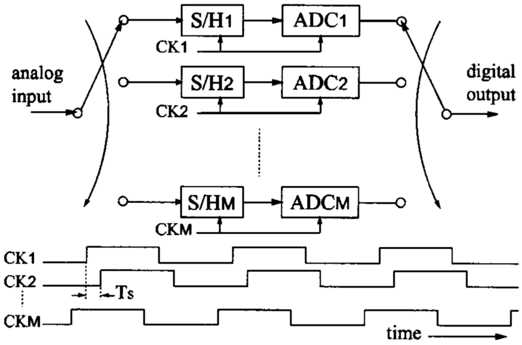

- Required clock, $f_{clk} = f_s/M$

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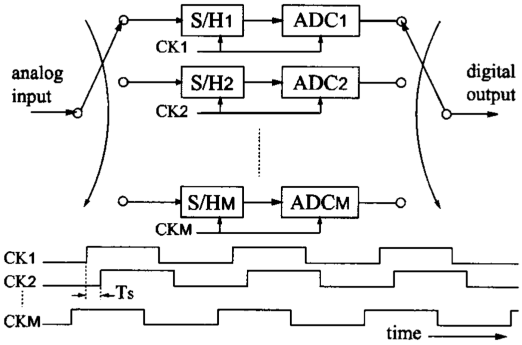
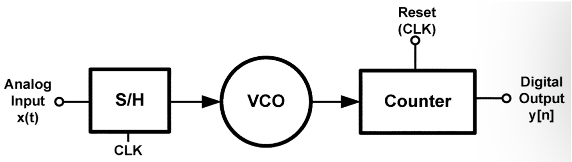


- Required clock, $f_{clk} = f_s/M$
- Phase difference, $\phi_i = \frac{2\pi(i-1)}{M}$

Analysis of ADC based on VCO



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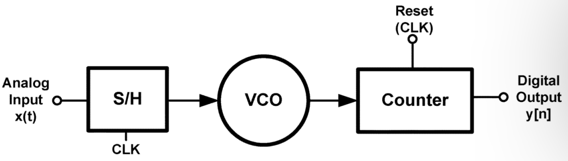

- VCO translates the input voltage to phase.

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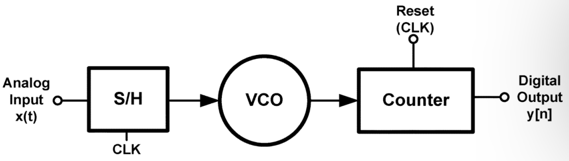

- VCO translates the input voltage to phase.
- Counter, counts the number of rasing/falling edges.

$$\phi[n] = \int_{nT_s}^{(n+1)T_s} K_v x[n] dt + p_i[n] = G_v x[n] + e[n-1]$$

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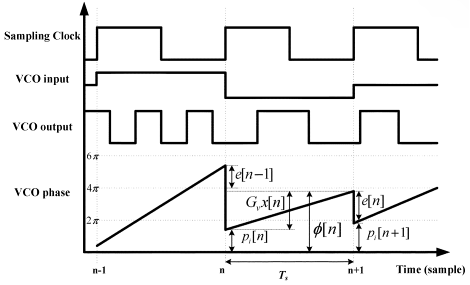

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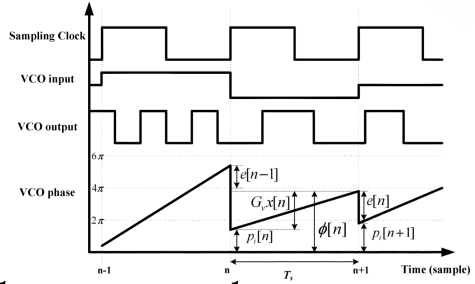

$$y[n] = \frac{1}{2\pi}(\phi[n] - e[n]) = \frac{1}{2\pi}(G_v x[n] + e[n-1] - e[n])$$

$$Y(z) = \frac{1}{2\pi}(G_v X(z) + (z^{-1} - 1)E(z))$$

$$NTF(z) = \frac{1}{2\pi}(z^{-1} - 1) \implies |NTF(e^{j\omega})| = |2sin(\omega/2)|$$

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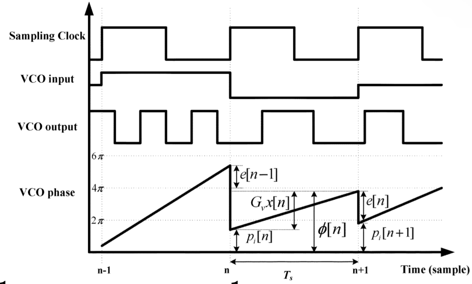

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- First order high-pass filter.

Extension for N-th order ADC

$$NTF(z) = \frac{1}{2\pi}(z^{-N} - 1)$$

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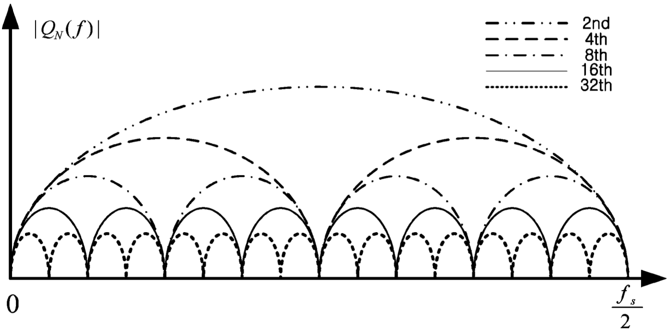
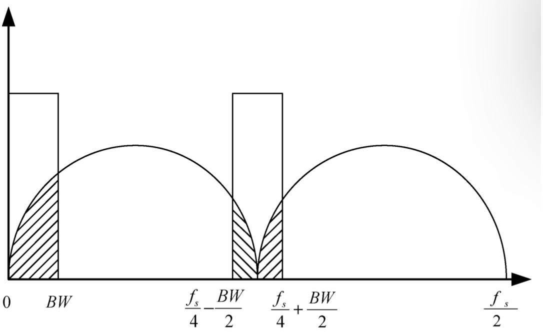


Which Zero to center at?



- At $\omega = 0 or \pi$,

$$SQNR = 6.02ENOB - 3.41 + 30log(OSR)dB$$

- At intermediate zeroes,

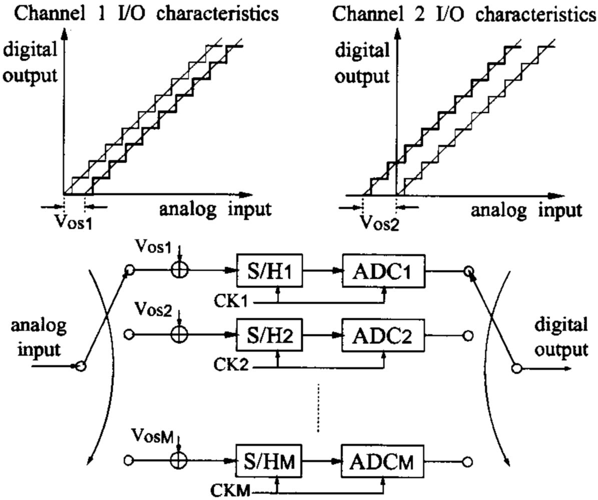
$$SQNR = 6.02ENOB - 3.41 + 6.02 + 30log(OSR)dB$$

Increase of 6.02dB is equivalent to increase in 1-bit precision of ADC!!

Non-idealities

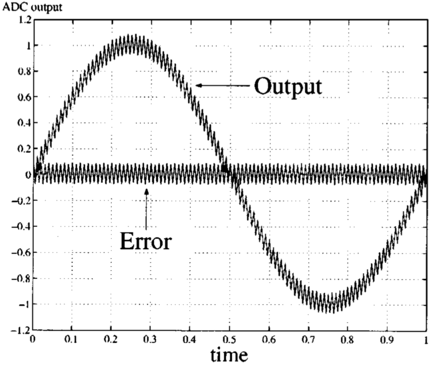
- DC offset
- Gain mismatch
- Clock Jitter/Skew
- Bandwidth mismatch
- Non-linearity in VCO

DC offset

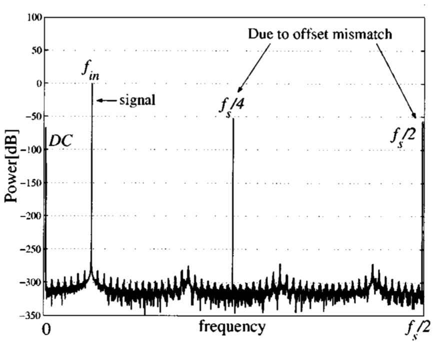


Channel 1 I/O characteristics
digital output
analog input
Vos1
Channel 2 I/O characteristics
digital output
analog input
Vos2
Vos1
S/H1
ADC1
CK1
Vos2
S/H2
ADC2
CK2
analog input
digital output
VosM
S/HM
ADCM
CKM

DC offset

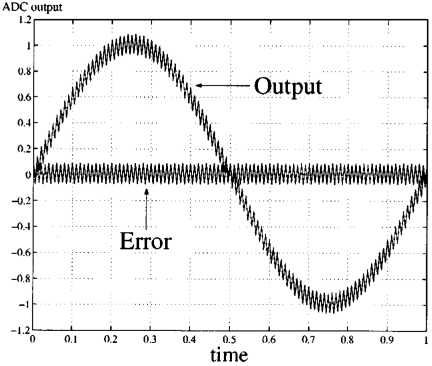


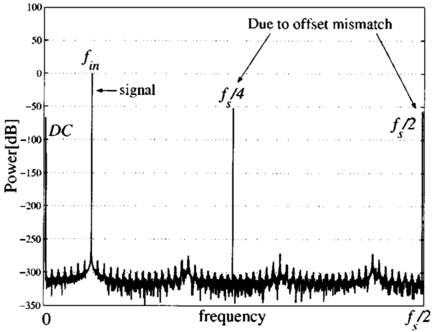
ADC output
Output
Error
time



Due to offset mismatch
f_{in}
signal
$f_s/4$
DC
$f_s/2$
Power[dB]
frequency

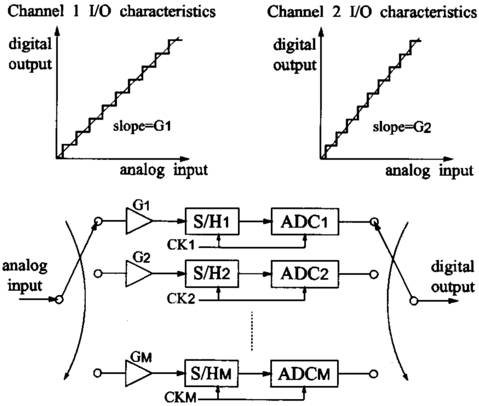
DC offset





- We can see that dc offset periodicity $\implies$ peaks at $\frac{k}{M} f_s$

Gain mismatch



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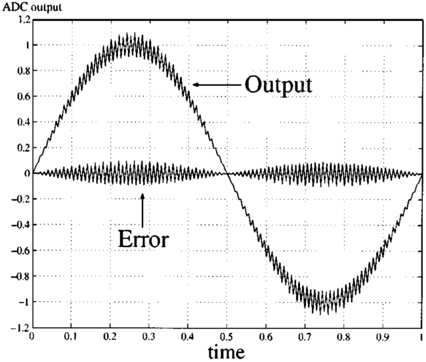
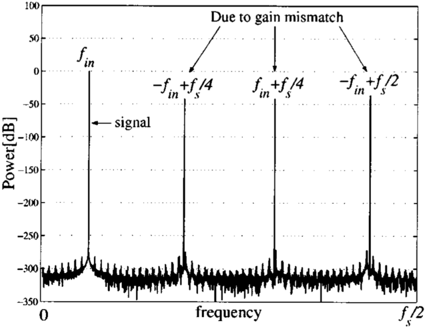
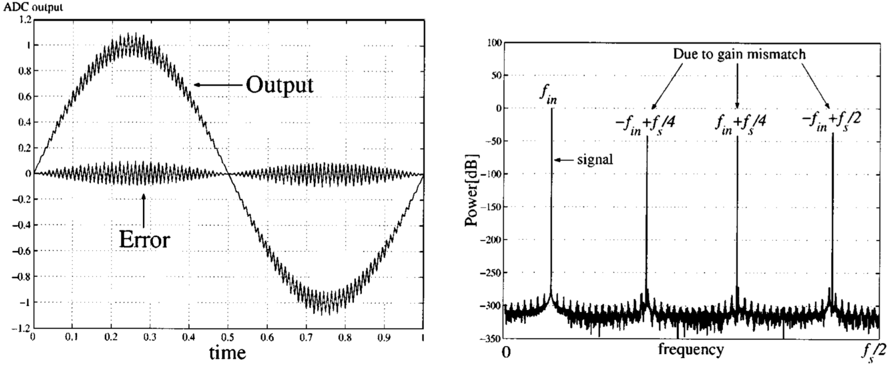


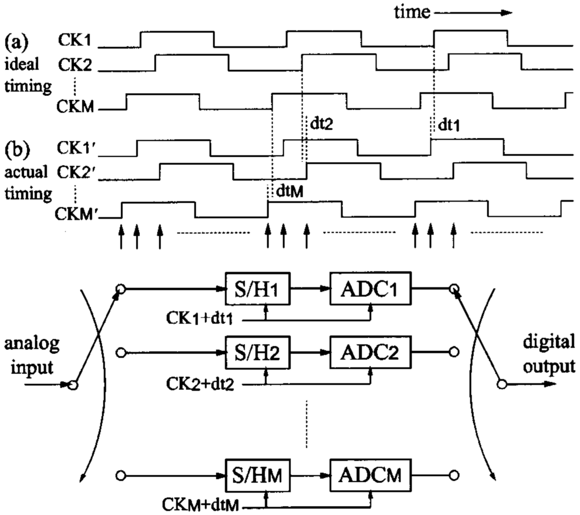


Gain mismatch



- Gain mismatch can be looked as A.M $\implies$ peaks at $\pm f_{in} + \frac{k}{M} f_s$
- Error at higher amplitude is more.

Clock jitter



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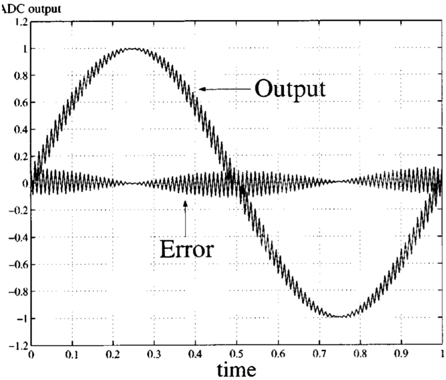

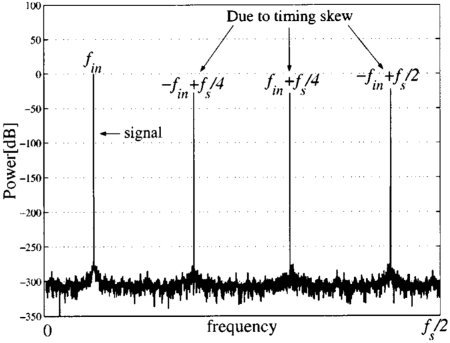

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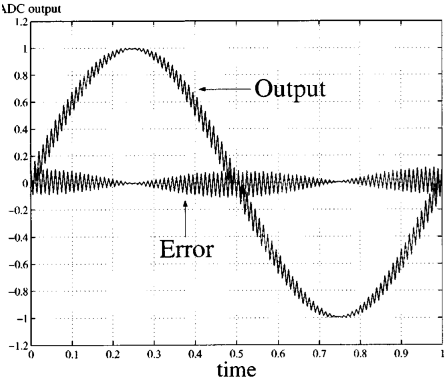
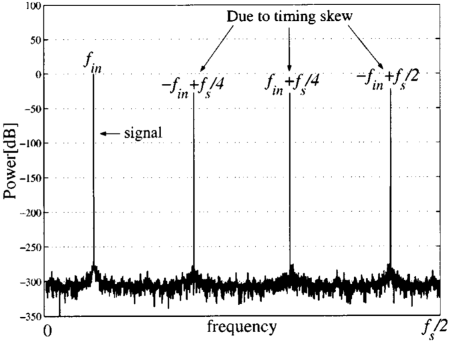
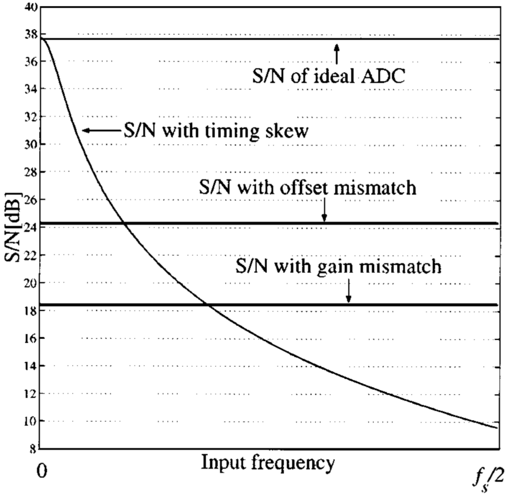




- Clock skew behaves like P.M $\implies$ peaks at $\pm f_{in} + \frac{k}{M} f_s$.
- Error is high at places where slew rate is more.

SNR comparisions



Thank You