# PT430 COL.BAR GEN.

Supply information:

Unit can be supplied from AC or DC. (Negative ground)

DC supply: 11.5 - 20V input range (82mA for video board).
+ to pins 25 + 26.
- to pins 29 + 30 (Ground).

(Note minimum DC can be lowered to 10.5V by shorting diode D1).

AC supply: 18V - 30V centre tapped (9-0-9 to 15-0-15).

Centre tap to pins 29 + 30. (Ground).
One leg to pins 25 + 26.
Other leg to pins 27 + 28.

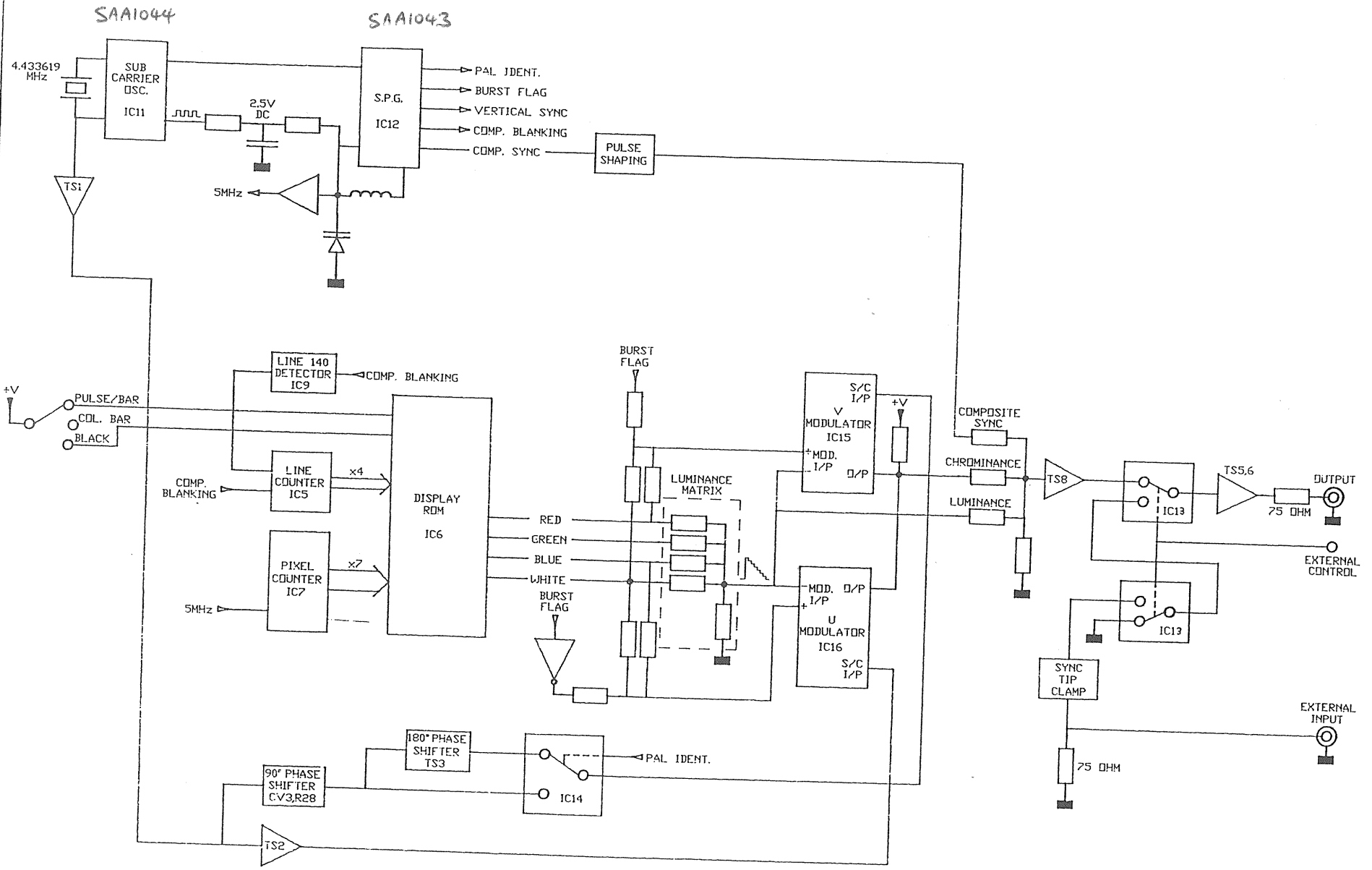
Note: Supply diodes D1 + D2 can be used to "OR" two external DC supplies.
Connect one supply to pins 25 + 26.
Other supply to pins 27 + 28.
- to pins 29 + 30 (Ground).

PRACTEL

ISSUE: 1 | DRN: 16/1/86 | DWG 1 OF 1

# COLOUR BAR GENERATOR

## BLOCK DIAGRAM PT-430



## PT430 CIRCUIT OPERATION

IC11 is the subcarrier oscillator and is crystal controlled at 4.433619MHz and is adjusted in frequency by CV1. Another oscillator in IC12, which is the colour sync pulse generator operates at 5MHz, as set by R19,L1 and adjusted by CV2.
IC11 and 12 are connected together via R16-18, C12-14 and a varicap D17, so that the 5MHz oscillator in IC12 is phase locked to the 4.43MHz subcarrier. This circuit phase locks the horizontal sync output from IC12 to the oscillator frequency with a 25Hz offset. The pulse waveform from pin 9 of IC11 is filtered by R16, R17, C12 and C13 to give a D.C. component at test point 2 (TP2). This D.C. level adjusts the capacitance value of D17 to keep the circuit in lock. During alignment CV2 is adjusted such that the D.C. level at TP2 is approx. half the supply voltage (2.5V). This voltage then changes in normal operation to keep this oscillator phase locked, to the subcarrier oscillator.

As the signals generated by the Colour bar generator, are digitally derived the dot clock sets the number of pixels across the screen. In this case 128 pixels are generated from the 5MHZ signal.

The 5MHz signal on pin 11 of IC12 is buffered by an invertor IC10e, and used as dot clock for the digital R.G.B. generator circuit, IC's 5-9.

After each vertical sync pulse, IC9a and IC9b, which form the Vertical Line counter, are reset by pin 19 of IC12. IC9 is then incremented every line by composite blanking (Pin 25 IC12 via invertor IC10b). For the first 140 lines of the screen after the field sync, IC5 will be held reset. IC7 is clocked by the dot clock(5MHz) and thus 128 dots will be addressed from the Screen ROM (IC6). These 128 dots or pixels produce the horizontal R.G.B. colours.
The same line is repeated until the 140th line.

IC5 is the Identification Text Line Counter; and as IC5 is held reset for the first 140 lines. The same line of pixels will then appear on the top part of the screen, until IC5 is enabled.
On line 140 the output of IC9,(LE), will be 8CH. IC9 will then dead end at the count 140, as determined by D10-D12, by putting pins 1 and 9 of IC9 high.
This will lift pin 5 of IC10c high and release the reset on IC5.
IC5 is now incremented every line by composite blanking.

For the next 14 lines a different 128 pixels will be the output from the Screen ROM (IC6). These lines will contain any Identification Text information.

On the sixteenth line pins 1 and 9 of IC5 will go high as determined by D7,8,9 and 13; dead ending IC5, until the next vertical interval.
Then the sixteenth line is repeated until the end of the field.

The output of the Screen ROM is clocked into IC8, at the pixel rate (2.5MHz), via IC10b. IC8 is enabled by composite blanking, via IC10d.
This ensures that the R.G.B. outputs are always stable.

This pixel clock is derived from the Dot clock divided by 2, and is provided by IC7, pin 3.

Composite sync resets IC7, the pixel counter during Horizontal Blanking.

The two most significant address lines of IC6 are connected to an external switch such that three different "BANKS" in the ROM can be selected. This gives the possibility of three different output signals. These three output signals are usually colour black, colour bars with or without Identification Text and a split screen of colour bars and pulse and bar, with or without Identification Text.

The subcarrier is taken from pin 7 of IC11 and buffered by a FET (TS1). The subcarrier is then fed to an emitter follower buffer, TS2. The output on the emitter of TS2 is fed to the U balanced modulator(IC16). The signal on the collector of TS2 is fed through an adjustable phase shifting circuit formed by CV3, C19 and R28.
The signal on the base of TS3 should be 90° out of phase with, and leading, the signal at the collector of TS2. Adjusting CV3 will adjust this phase shift and thus adjust the quadrature.Fine turning of quadrature is achieved by adjusting CV4 and RV1. The phase shifted subcarrier is then fed to an input of the analogue switch IC14a, from the emitter of TS3. The inverted phase shifted subcarrier on the collector of TS3 is then fed through an emitter follower (TS4) to the second input of the analogue switch. The two inputs to the analogue switch (IC14) lag and lead the subcarrier going to IC16 by (90°). The analogue switch is driven by the PAL Ident output of the sync circuit, pin 2 of IC12. This forms the PAL switch. The output of IC14a drives the "V" balanced modulator (IC15).

Thus the phase of the subcarrier to IC15 changes by 180° every line or ±90° with respect to the "U" subcarrier. The D.C. level at the subcarrier inputs to the balanced modulators is set by R102 and R101 and the differential inputs to the balanced modulators pins 8 and 10, are kept at the same D.C. level by connecting the two inputs via a 100Ω resistor (R97 and R93).

R54, 55, 56, 60, 61, 66, 67, 70 and 71 form the luminance matrix.

A white signal is generated from the R.G.B. circuit to give a 100% white bar. This luminance signal Y, a staircase,is then fed to "-" differential inputs of both the U and V modulators.
The blue signal is then fed to the "+" differential input of the "V" modulator via R62 and R63. Thus the differential inputs of the "V" balanced modulator form the "Y-B" matrix. Similarly the red signal is fed to the "+" differential input of the "U" balanced modulator to form the "Y-R" matrix.
The white signal must also be added to the blue and red signals via R59,R58, R64 and R65 to cancel out the effect of the 100% white bar.

The D.C. levels on the "+" inputs is fixed by R73, R72,R74 and R75. The DC level on the "-" inputs to the modulators is set by fixed resistors R79, R87, R86, R79,R76, R84,R85,R77 and adjustable resistors RV5 and RV6.

RV5 and RV6 are used to fine tune the D.C. levels to null out the subcarrier from the black and white output levels.

The colour burst is derived by adding the burst flag to the red signal fed to the V modulator and adding the inverted burst (Via IC10a) to the blue signal fed to the U modulator. The gain of the "U" modulator is set by R103 and RV7. RV7 is used to adjust the U-V balance.
TP4 is the "-" output of the V modulator and TP5 is the "-" output of the U modulator. The "+" outputs of the U+V modulators pin 6, are connected to R50, thus adding the U + V outputs to give full chroma (CR).
The chroma is then passed to the mixer (TS7) via a band pass filter formed by L2 and CV5.

The mixer is formed by a common base amplifier (TS7). The chroma is fed to the emitter via RV4 which is used to adjust the overall chroma level for the output.
The luminance Y is taken from the luminance matrix, via R48 and buffered and level shifted by TS8. The luminance is then fed to the emitter of TS7 via RV2. RV2 is then used to adjust the overall luminance level at the output.
The composite sync output of IC12 is inverted by IC10f and filtered by C29. The composite sync signal is then attenuated by R51 and R52, AC. coupled by C31, filtered again by R53 and C30 before being fed to the emitter of TS7 via RV3. RV3 is then used to adjust the overall sync Level at the Output.
This filtering provides the correct pulse shape for the sync signal.

The composite video signal on the collector of TS7 is then fed to Pin 1 of IC13.
Provided no external signal is selected, the composite internal signal is fed through to the output driver formed by TS6 and TS5.

When in the internal mode, pin 4 of IC13 will be low and this enables IC12, the SPG, to function via pin 18 of IC12. When pins 9, 10 and 11 of IC13 are brought low, pin 4 of IC13 will go high, switching off the sync generator and disabling the R.G.B. circuit.
This eliminates crosstalk from the colour bar generator into an external signal.

When external video is selected, the output of the composite video mixer, at pin 1 IC13a, should show less than 5mV pp. of subcarrier.

The external signal is terminated by R39, AC. coupled by C25 and clamped by D18, R41, R60 and C26 before being fed to the analogue switch IC13 pin 12. The external signal is fed via two analogue switches IC13a and 13b to the output driver formed by TS5 and TS6. Two analogue switches are used to reduce the amount of crosstalk from the external signal into the colour bar generator, when the external signal is present, but not selected.

The selection of internal or external signals may be accomplished either by a front panel switch or by automatic circuitry, located on the overlay PCB, PT431. (See separate page.)

The automatic selection of internal/external video and audio is determined by the presence and suitability of the syncs in the external signal. If the external Horizontal Sync is either low in amplitude or the incorrect frequency then the internal signal is automatically routed to the output.
This board is described in detail elsewhere.

PT430 ALIGNMENT PROCEDURE

## ADJUSTMENTS

1. Switch on unit and allow to warm up for 2-3 minutes.

2. View terminated output on a waveform monitor and vector scope.

SYNC LEVEL

3. Adjust RV3 until the sync is 0.3V in amplitude or 40 IRE units.

LUMINANCE LEVEL.

4. Adjust RV2 until the white level is 0.7V above the blanking level.

SUBCARRIER FREQUENCY.

5. Connect an accurate frequency meter to Tp1 and adjust CV1 until the frequency is 4.433619MHz.

HORIZONTAL LOCK.

6. View test point 2 (TP2) on a C.R.O. with volts/division set at 1V/Div and the input D.C. coupled. Using a trimming tool adjust CV2 until the D.C. voltage at TP2 is 2.5V.

SUBCARRIER NULL.

7. Adjust RV6 for minimum subcarrier on black and white levels. Adjust RV7 for minimum subcarrier on black and white levels. Repeat these adjustments a number of times.

QUADRATURE.

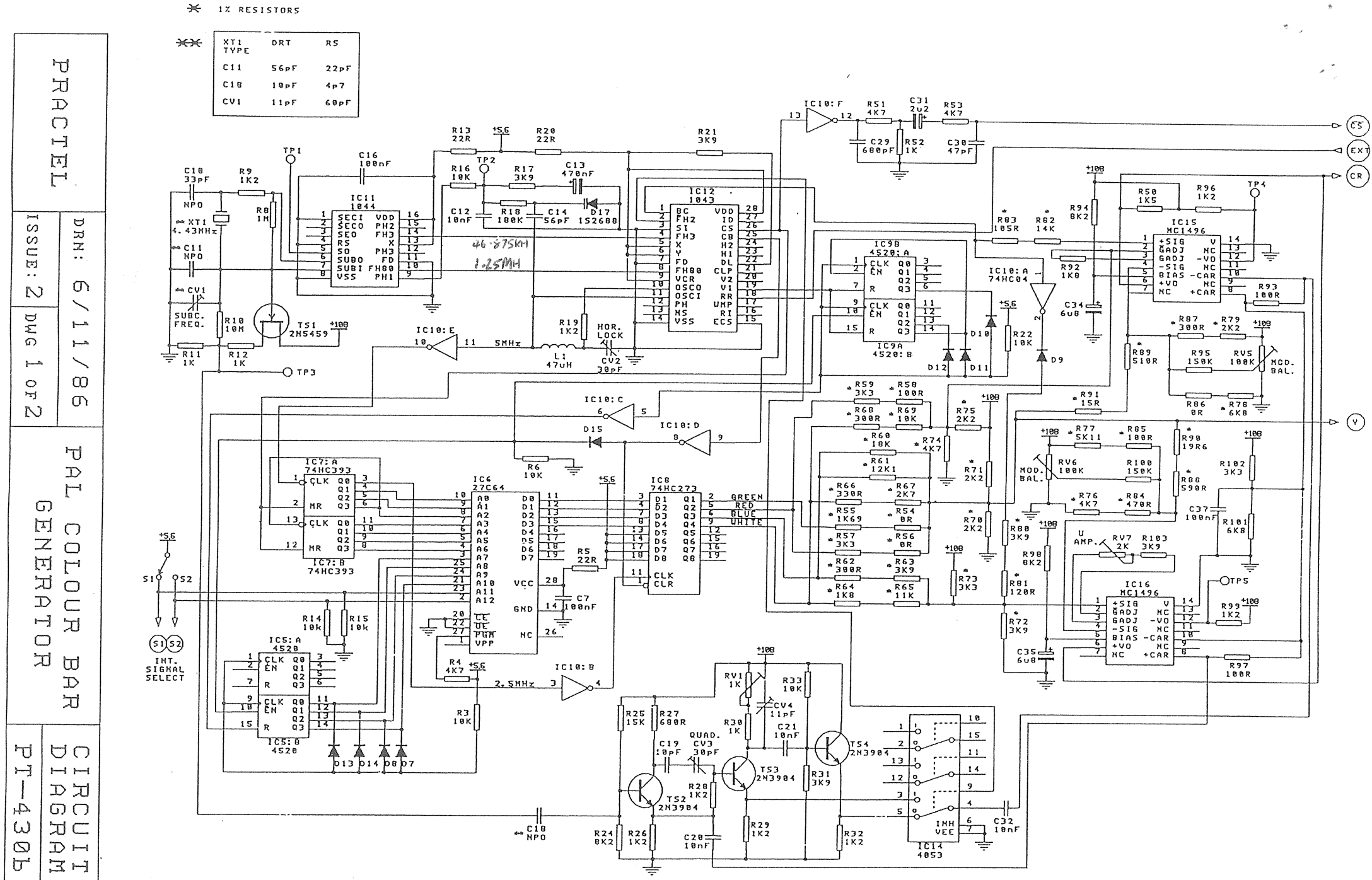
8. Adjust CV3, CV4 and RV1 for optimum vector display. RV7 sets the U-V balance, where as CV3 adjusts the quadrature. CV4 and RV1 are used for fine tuning. All controls are interactive so repeatedly go through the process.

CHROMA FILTER.

9. Adjust CV5 with a trimming tool for maximum chroma level and then tune slightly off centre to reduce spikes in middle chroma transition.

CHROMA LEVEL.

10. Adjust RV4 until the chroma is the correct level.


* 1% RESISTORS
XT1 TYPE | DRT | RS
C11 | 56pF | 22pF
C18 | 10pF | 4p7
CV1 | 11pF | 60pF
PRACTEL
DRN: 6/11/86
ISSUE: 2
DWG 1 OF 2
PAL COLOUR BAR GENERATOR
CIRCUIT DIAGRAM
PT-430b
IC11 1044
IC12 1043
IC9B 4520:A
IC9A 4520:B
IC10:A 74HC04
IC10:B
IC10:C
IC10:D
IC10:E
IC10:F
IC7:A 74HC393
IC7:B 74HC393
IC6 27C64
IC8 74HC273
IC5:A 4520
IC5:B 4520
IC15 MC1496
IC16 MC1496
IC14 4053
TS1 2N5459
TS2 2N3904
TS3 2N3904
TS4 2N3904
D17 1S2688
D10 D11 D12 D9 D15 D13 D14 D8 D7
XT1 4.43MHz
C11 NPO
CV1 SUBC. FREQ.
C10 33pF NPO
C16 100nF
C13 470nF
C12 10nF
C14 56pF
C18 10pF NPO
C29 680pF
C30 47pF
C31 2u2
C34 6u8
C35 6u8
C37 100nF
C7 100nF
C32 10nF
CV2 30pF
CV3 30pF
CV4 11pF
C21 10nF
C19 10pF
C20 10nF
L1 47uH
HOR. LOCK
MOD. BAL.
U AMP.
INT. SIGNAL SELECT
S1 S2
TP1 TP2 TP3 TP4 TP5
+5.6 +10.0
46.875KH
1.25MH
5MHz
2.5MHz
GREEN RED BLUE WHITE
CS EXT CR Y

PRACTEL

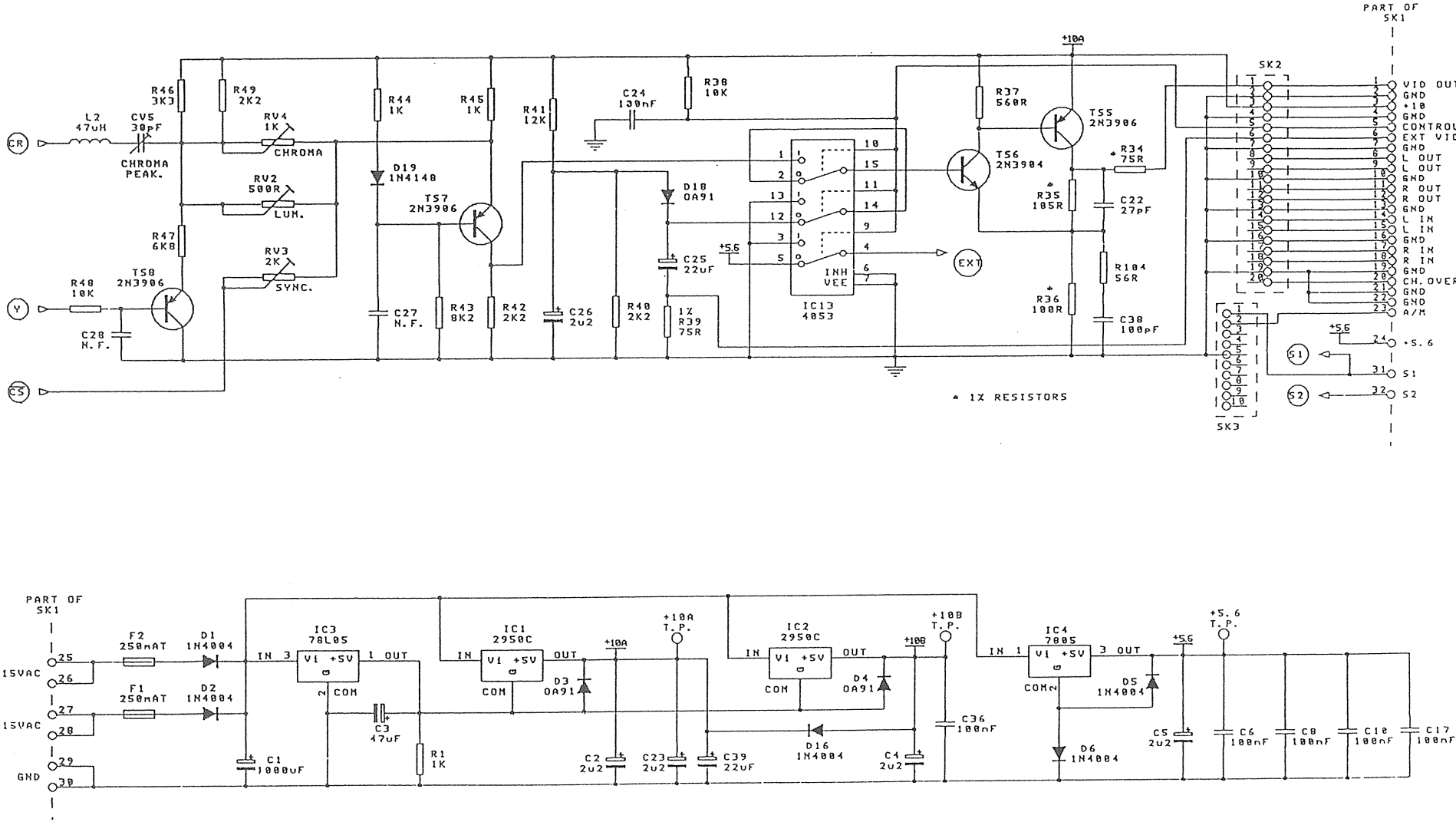
DRN: 6/11/86

ISSUE: 2 DWG 2 OF 2

# PAL COLOUR BAR GENERATOR

## CIRCUIT DIAGRAM

PT—430b



## PT431 CIRCUIT OPERATION

### AUDIO SECTION

IC4(a) is a Wien bridge oscillator which operates at 1KHz. RV1 is used to change the gain of IC10a to adjust the output level to 8dbm. The output of the oscillator via IC10a is connected to the analog switch IC5a and then to an inverting amplifier IC7a which drives the left "+" output. The left "+" output is inverted by the unity gain amplifier IC7b to drive the left "-" output, thus providing a balanced left output.

IC10b is configured as an astable multivibrator and its output, pin 7, goes high for 3 seconds and low for 0.25 of a second. This signal is used to switch the output of the oscillator through to the right channel output via IC5(c). R33 and C18 filter the chopped signal to remove spikes and the signal then goes through another analog IC5b switch to IC8(a). IC8(a) drives the right "+" output and this output is then inverted by IC8(b) and used to drive the right "-" output thus providing the balanced right output. All the output amplifiers have a capacitor across their feedback resistors to filter any noise picked up from the video board. IC6a and IC6b take the external left and right balanced input signals and converts them to an unbalanced signal.

Analog switches IC5a and IC5b are controlled by the changeover signal C/O generated by the video detection circuit. When no external video signal is present the changeover C/O signal will be high and this will allow the oscillator output through to the left output and the interrupted oscillator output through to the right output. If an external video signal is present the changeover signal C/O will be low and this will allow the external audio signals to pass through to the output amplifiers. When pin 3 of IC4a is connected to the collector of TS4 via link LK1, and colour black is selected, the oscillator IC4a will stop. The 78L05, IC9 is used to create an artificial ground to allow the amplifier to have an artificial plus and minus rail from a +10v only supply.

### VIDEO DETECTOR CIRCUIT

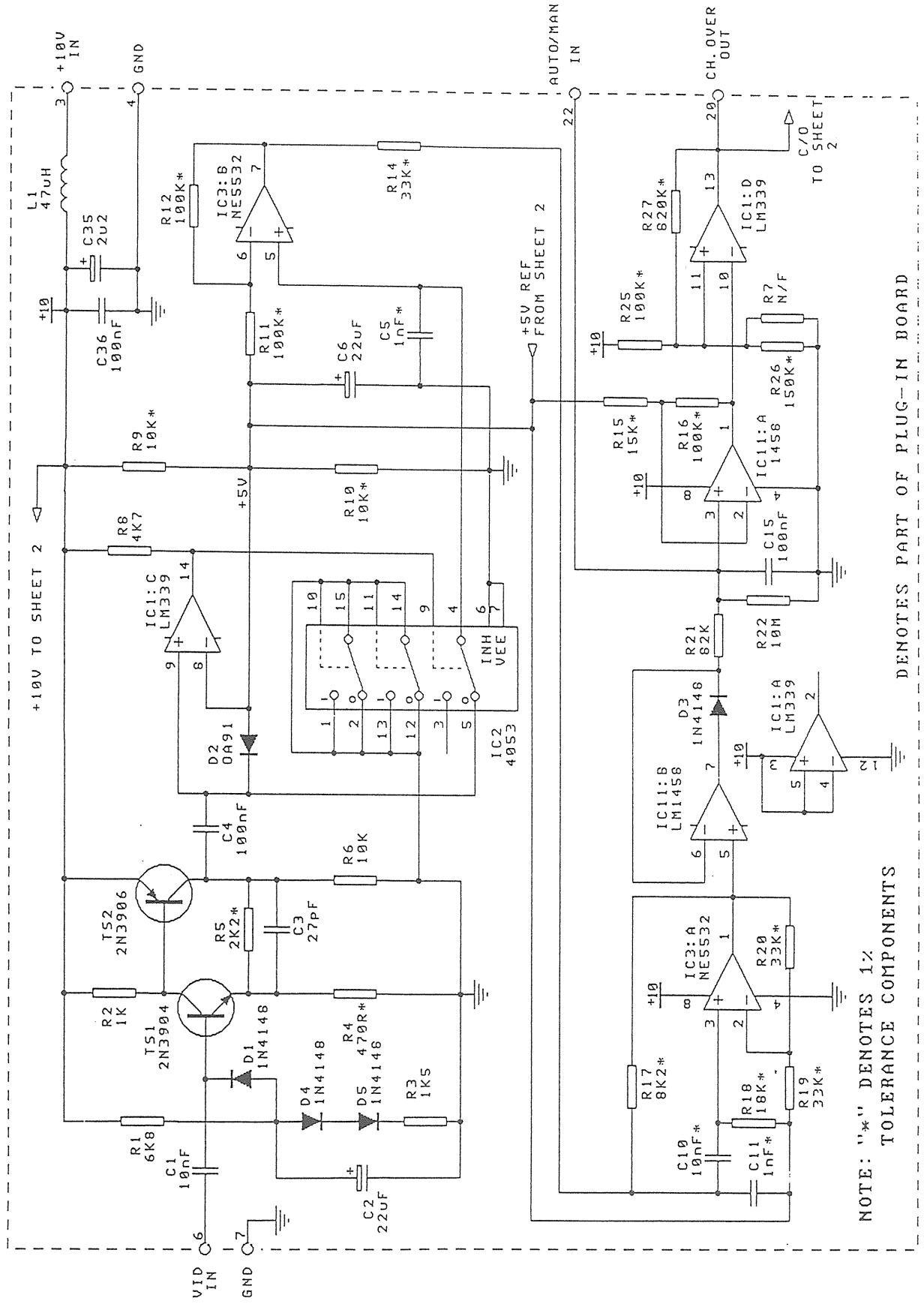
The external video signal is coupled via C1, sync tip clamped via R1,R3 C2 and D1 and buffered by TS1. Any chroma is then filtered out by R5 and C3 with D5 providing a clamping action for signals exceeding 2Vpp, to prevent overloading. The signal is then passed through a buffer (TS2) and sync tip Clamped to slightly below 0v. IC1(a) then compares the clamped signal to the ground reference and pin 14 of IC1(a) outputs the separated composite sync.

This compsync is then used to control the analog switch (IC2) to separate the sync pulses from the external video. The separated syncs on pin 4 of IC2 are amplified by a common emitter amplifier (TS3). These amplified sync pulses are the filtered by a 15KHz band-pass filter formed by IC3 to ensure that large levels of random noise will not be recognised as video. The filtered sync pulses are then clamped to ground by C13 and D4 and rectified by D3 and C14. C15 is then charged via R21 and discharged via R22. IC1(b) then compares the D.C. voltage on C15 to a reference set by R25, R26 and R27. When the external signal is large enough the voltage on pin 10 of IC1(b) will rise above the

voltage on pin 11 of IC1(b) and pin 13 of IC1(b) will go low. This changeover signal C/O will change over the video and audio circuits to allow the external signals to pass. R27 provides hysteresis.

With the values of R25 and R26 shown, the changeover from external to internal video will occur when the incoming video signals sync levels go below 150mVpp. The return from internal to external signal occurs when the external sync level returns to greater than 200mVpp. To stop multiple switching, pin 10 of IC1(b) is brought to the edge connector so that it may be switched to ground to force the changeover signal high and have the audio and video boards output test signals irrespective of external video level or forced low to pass the external signals irrespective of video level.

The time constant of the C15, R21, R22 network allows approximately 100mSec delay from the removal of, or return of external video before the automatic changeover to or from internal video.

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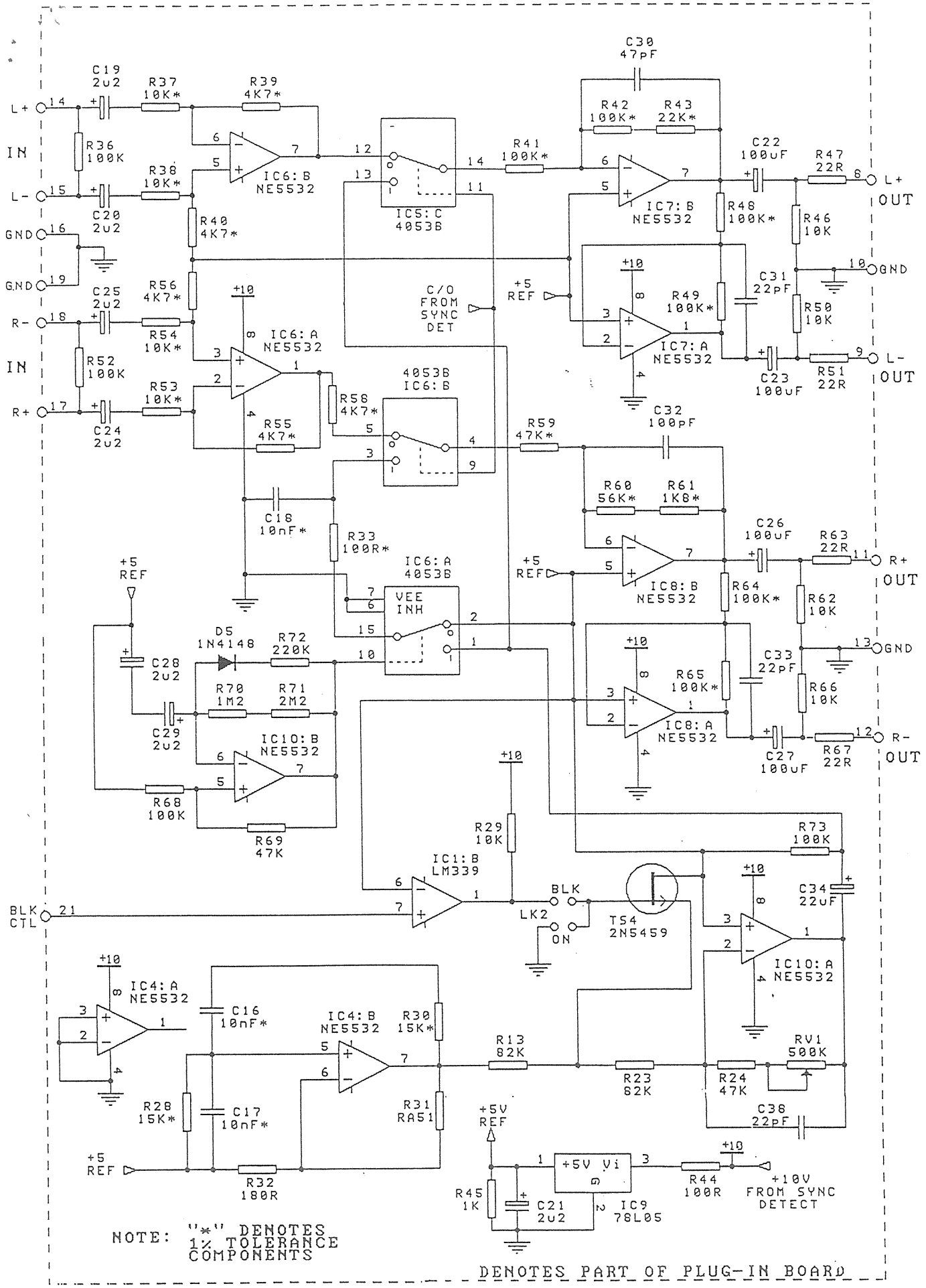
|---|---|---|---|
| PRACTEL | DRN: 11/5/88 | STEREO TONE GENERATOR SYNC DETECTOR | CIRCUIT DIAGRAM |
| | REV: 3 SH 1 OF 2 | | PT-431b |

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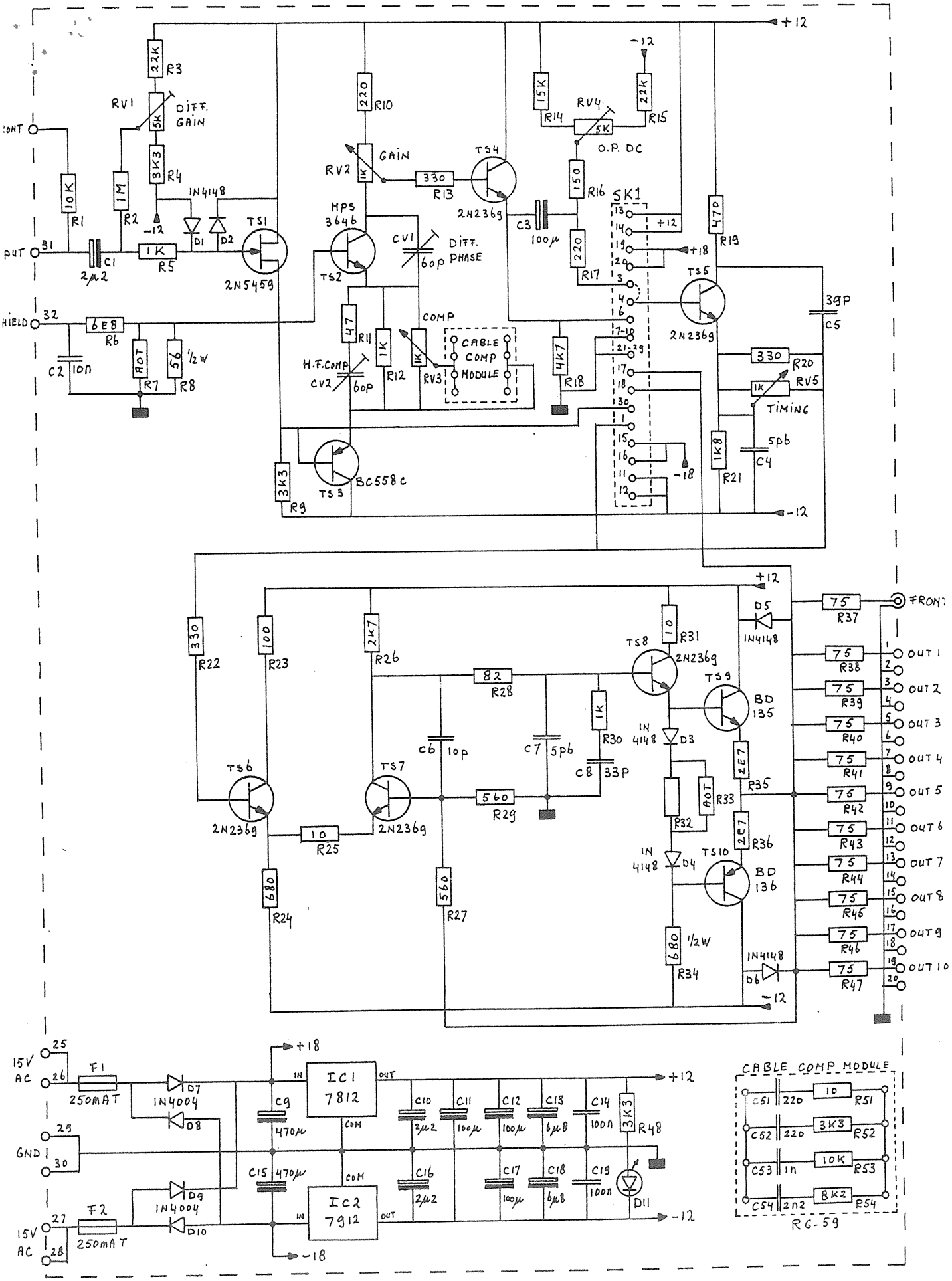
|---|---|---|---|---|
| PRACTEL | DRN: 11/5/88 | | STEREO TONE GENERATOR SYNC DETECTOR | CIRCUIT DIAGRAM |
| | REV: 3 | SH 2 OF 2 | | PT-431b |


+12
-12
+18
-18
22K R3
RV1 DIFF. GAIN 5K
3K3 R4
10K R1
1M R2
1K R5
2µ2 C1
IN4148
D1
D2
TS1 2N5459
220 R10
RV2 GAIN 1K
330 R13
TS4 2N2369
MPS 3646 TS2
CV1 DIFF. PHASE 60p
C3 100µ
15K R14
RV4 5K O.P. DC
22K R15
150 R16
220 R17
SK1
470 R19
TS5 2N2369
39p C5
330 R20
RV5 1K TIMING
1K8 R21
5p6 C4
4K7 R18
47 R11
1K R12
COMP
RV3 1K
CABLE COMP MODULE
H.F.COMP CV2 60p
3K3 R9
TS3 BC558c
6E8 R6
C2 10n
R7
56 1/2W R8
330 R22
100 R23
2K7 R26
82 R28
1K R30
C6 10p
C7 5p6
C8 33P
560 R29
10 R25
680 R24
560 R27
TS6 2N2369
TS7 2N2369
10 R31
TS8 2N2369
TS9 BD 135
IN 4148 D3
2E7 R35
R33
R32
IN 4148 D4
2E7 R36
TS10 BD 136
680 1/2W R34
D5 IN4148
D6 IN4148
75 R37
FRONT
OUT 1
OUT 2
OUT 3
OUT 4
OUT 5
OUT 6
OUT 7
OUT 8
OUT 9
OUT 10
75 R38
75 R39
75 R40
75 R41
75 R42
75 R43
75 R44
75 R45
75 R46
75 R47
15V AC
GND
15V AC
F1 250mAT
F2 250mAT
D7 IN4004
D8 IN4004
D9 IN4004
D10 IN4004
IC1 7812
IC2 7912
C9 470µ
C10 2µ2
C11 100µ
C12 100µ
C13 6µ8
C14 100n
3K3 R48
C15 470µ
C16 2µ2
C17 100µ
C18 6µ8
C19 100n
D11
CABLE COMP MODULE
C51 220 10 R51
C52 220 3K3 R52
C53 1n 10K R53
C54 2n2 8K2 R54
RG-59

# PT430 COL.BAR GEN.

DJUSTMENTS:

V1 Sub Carrier Frequency
V2 Horizontal lock
V3 Quadrature
V4 Quadrature
V5 Filter

V1 Quadrature
√2 Video amplitude
√3 Sync amplitude
√4 Chroma amplitude
√5 Modulator balance
√6 Modulator balance
√7 U amplitude (U-V balance)