ECE 445

MOS transistor characterization using Cadence virtuoso

Lab #1 Report

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1.1 Introduction

This lab focuses on the characterization of NMOS transistors, analyzing their behavior in different operating regions. The objective is to understand MOS transistor physics, use industry-standard tools for CMOS circuit design, and interpret experimental results through simulation. The report documents the key observations, analysis, and conclusions drawn from the experiments.

1.2 Part I: Transistor Characterization

1.2.1 1. ID(VDS) Plot for NMOS Transistor

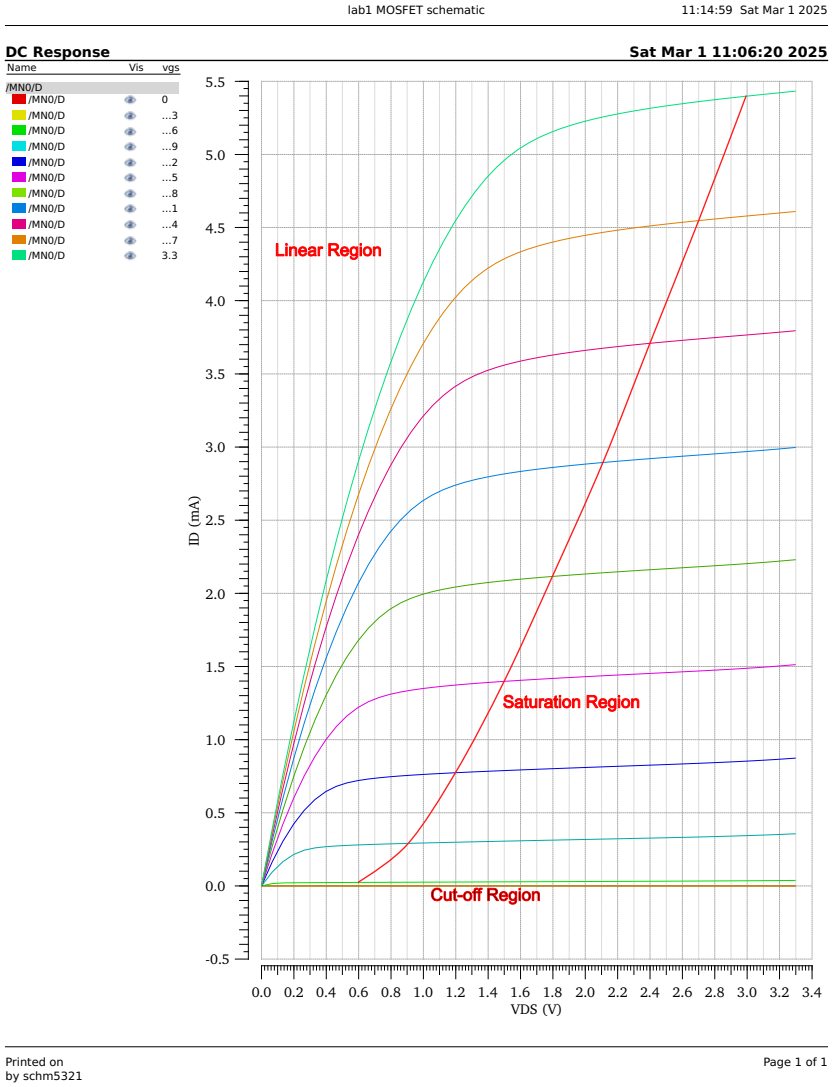

Figure 1.1: ID(VDS) plot for NMOS transistor with different VGS.

Analysis

- Different regions of operation: Cut-off, Linear, and Saturation.

- The non-zero slope in the saturation region is due to channel-length modulation, which leads to a small increase in current with increasing VDS.
- The plot demonstrates how increasing VGS shifts the transistor from cut-off into conduction, with higher VGS resulting in higher ID.

1.2.2 Questions for Part I:

1. **Describe the behavior of the NMOS transistor in the different operating regions observed in the ID(VDS) plot.**
   - In the cut-off region, no current flows. In the linear region, the current increases linearly with VDS. In the saturation region, the current stabilizes with increasing VDS, with a slight increase due to channel-length modulation.
2. **How does the saturation region current change with increasing VDS, and what is the reason for this change?**
   - The current increases slightly due to channel-length modulation, where the effective channel length decreases as VDS increases.
3. **How does increasing VGS affect the current ID in the transistor in this plot?**
   - Increasing VGS reduces the threshold voltage, allowing more current to flow through the transistor.

1.2.3 2. ID(VGS) with Small VDS

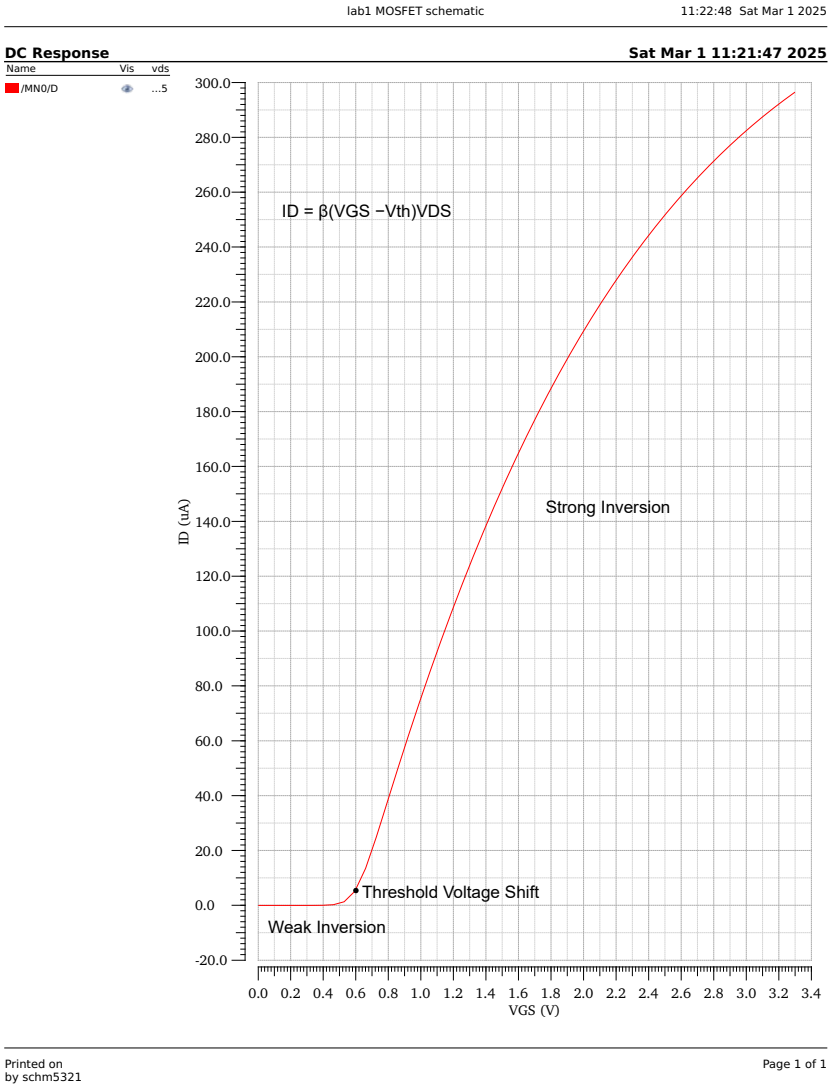

Figure 1.2: ID(VGS) plot for NMOS transistor with small VDS.

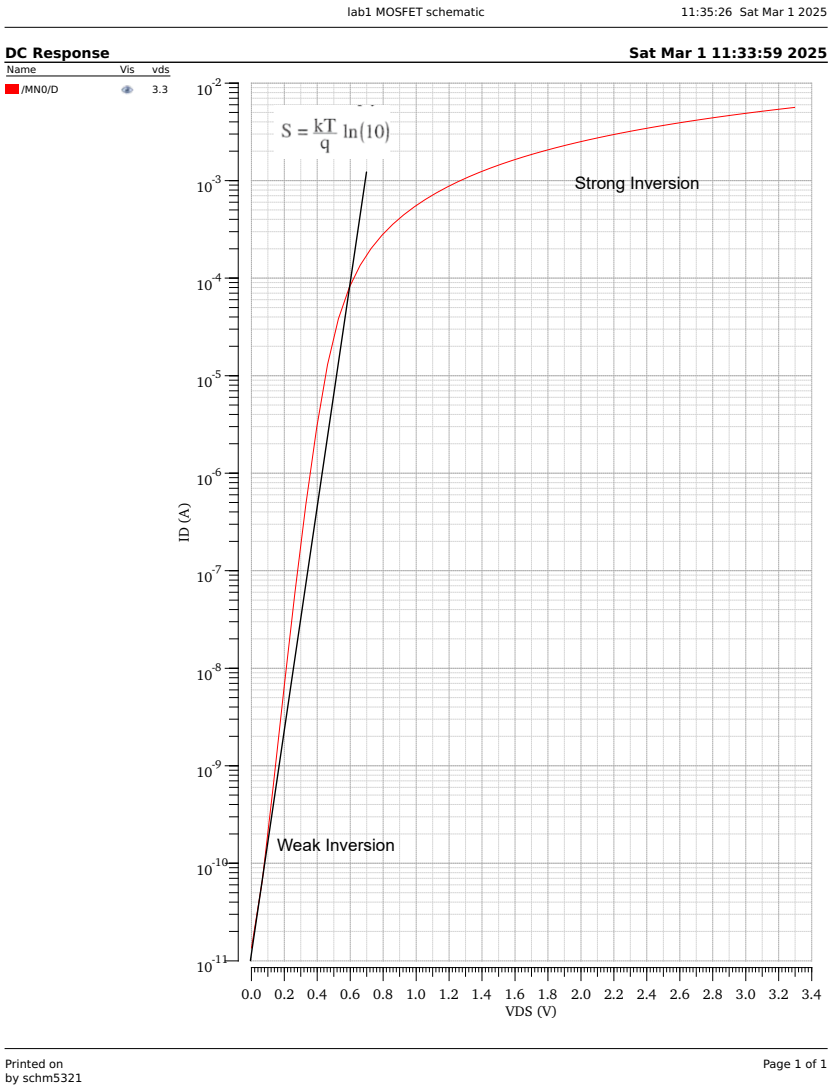

Figure 1.3: ID(VGS) plot for NMOS transistor with non-zero VBS.

Analysis

- When VGS is near VDD and VDS is small, the transistor operates in the linear (triode) region.
- The Shockley long-channel transistor model simplifies to:

$$I_D \approx \frac{\mu_n C_{ox} W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{1.1}$$

for small VDS.

- Threshold voltage (V_T) $can be extracted from the ID(VGS) curve by finding the extrapolated point where ID becomes zero. A length modulation, reducing errors in threshold voltage extraction.$

- Applying a non-zero VBS shifts the threshold voltage due to the body effect, following:

$$V_T = V_{T0} + \gamma(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}) \tag{1.2}$$

where γ is the body effect coefficient.

- When VGS is high, ID saturates due to velocity saturation and mobility degradation.

1.2.4 Questions for Part II:

1. **What does the Shockley model describe for an NMOS transistor operating in the linear region?**

   - The Shockley model describes the relationship between ID, VGS, VDS, and V_T, $where current increases linearly with VD$

2. **How can the threshold voltage be extracted from the ID(VGS) curve, and what impact does small VDS have on this process?**

   - Threshold voltage is found where ID starts to increase. Small VDS minimizes channel-length modulation, improving accuracy.

3. **How does the threshold voltage change when a non-zero VBS is applied, and what effect does this have on transistor behavior?**

   - A non-zero VBS increases the threshold voltage due to the body effect, requiring a higher VGS to turn the transistor on.

1.2.5 3. log10[ID(VGS)] with VDS = VDD

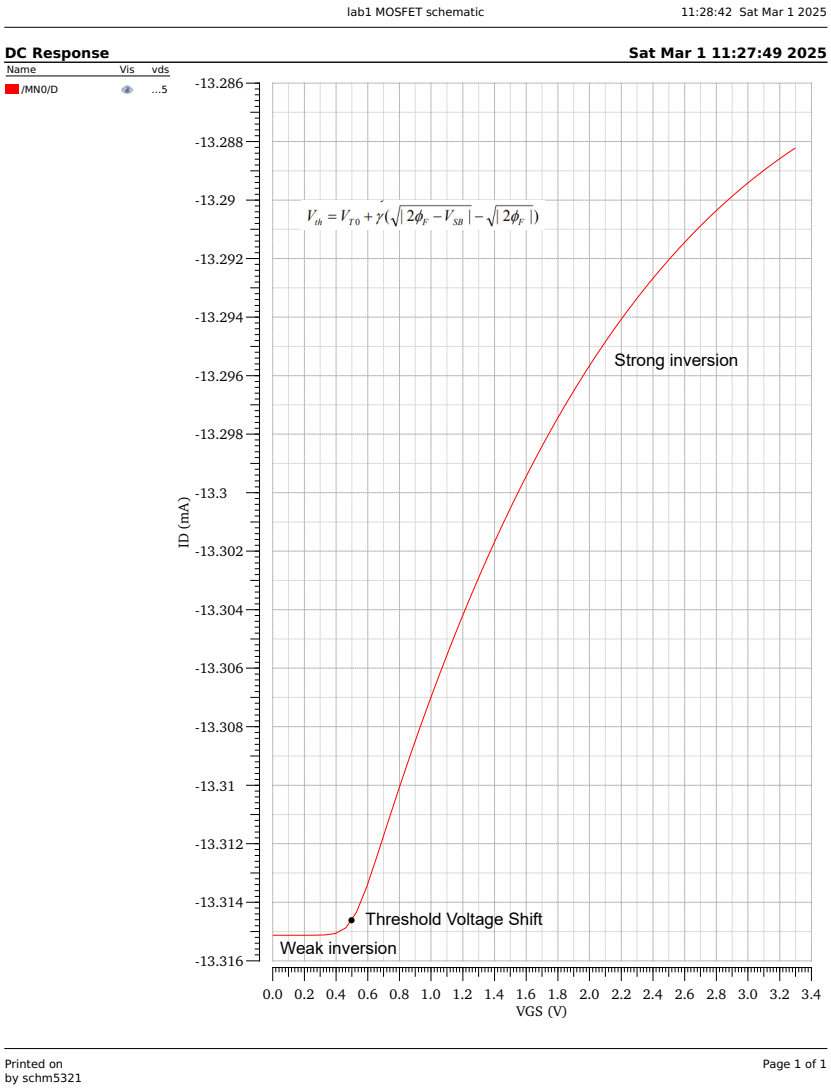

Figure 1.4: log10[ID(VGS)] plot for NMOS transistor with VDS = VDD.

Analysis

- The plot helps distinguish weak and strong inversion regions.
- For low VGS, the transistor operates in weak inversion (subthreshold region), where:

$$I_D \approx I_{D0} e^{(V_{GS} - V_T)/nV_T} \tag{1.3}$$

with n being the subthreshold slope factor.

- The subthreshold slope (SS) can be determined from the plot as:

$$SS = \frac{dV_{GS}}{d(log_{10}I_D)} \approx \frac{2.3kT}{q}n \tag{1.4}$$

and is affected by process variations.

1.2.6 Questions for Part III:

1. **What does the log10[ID(VGS)] plot show about the weak and strong inversion regions of the NMOS transistor?**
   - The plot distinguishes weak inversion (exponential increase) and strong inversion (linear increase) regions.
2. **How does the subthreshold slope (SS) relate to the transistor's behavior in weak inversion, and how is it affected by process variations?**
   - SS measures how quickly current increases with VGS in weak inversion and is affected by process variations like channel length and doping.
3. **How can the subthreshold behavior be characterized using the log10[ID(VGS)] plot?**
   - Subthreshold behavior is characterized by the slope of the log10[ID(VGS)] plot, which gives the subthreshold slope (SS).

1.3 Conclusion

This lab provided valuable hands-on experience in analyzing the behavior of NMOS transistors through simulation. The experiments helped reinforce key theoretical concepts, including how to extract threshold voltage, understand subthreshold behavior, and recognize the effects of process variations. Some important takeaways include:

- Gaining a deeper understanding of how NMOS transistors operate in different regions.
- Observing non-ideal behaviors like channel-length modulation and the body effect.
- Learning how to extract threshold voltage from ID(VGS) plots and understanding how it changes with VBS.
- Using log-scale ID plots to better characterize subthreshold behavior.

These insights are crucial for improving CMOS circuit design and refining device modeling techniques.