SOLOMON SYSTECH

SSD2832G24 Guide

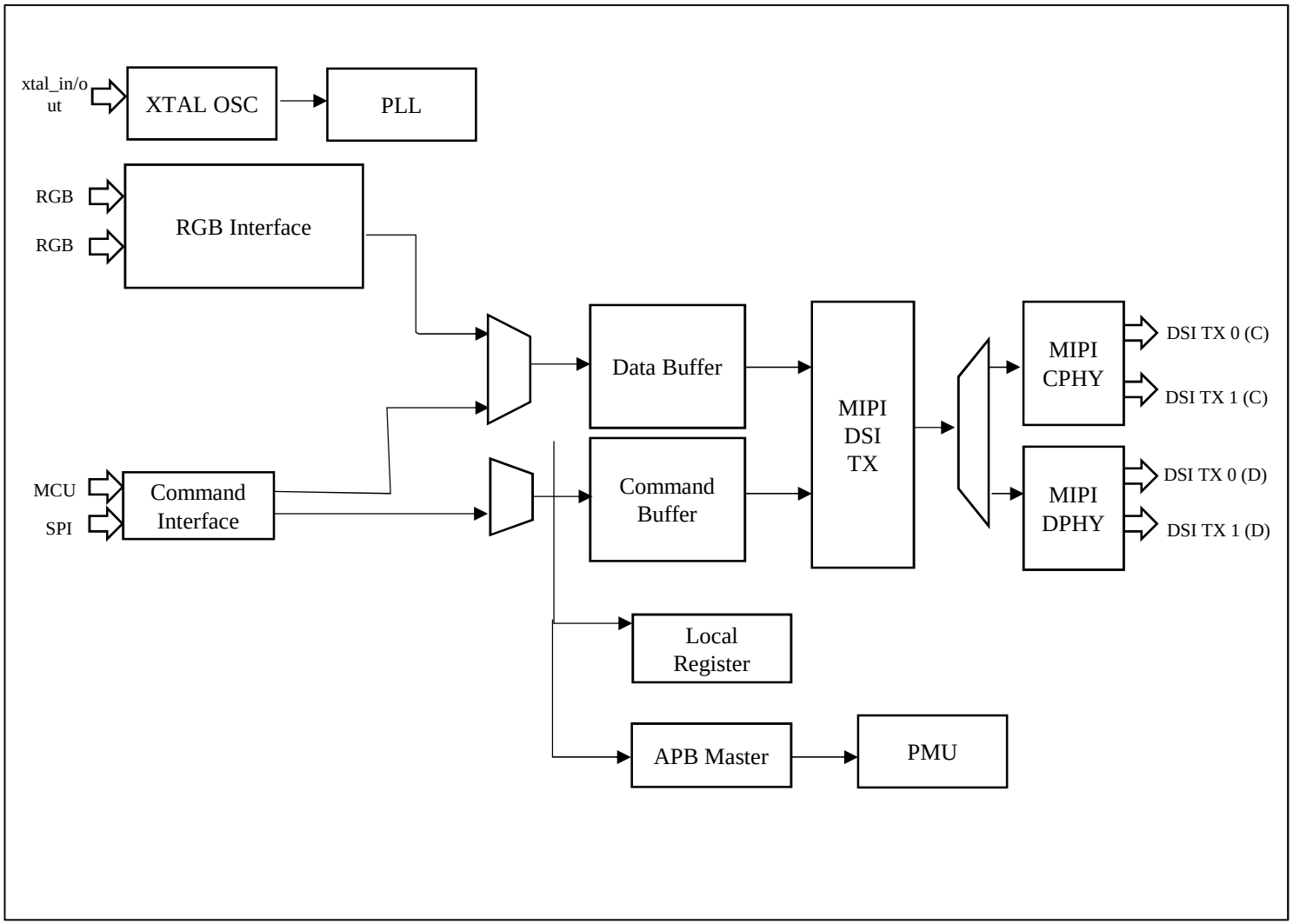
Solomon Systech Limited

晶門科技有限公司

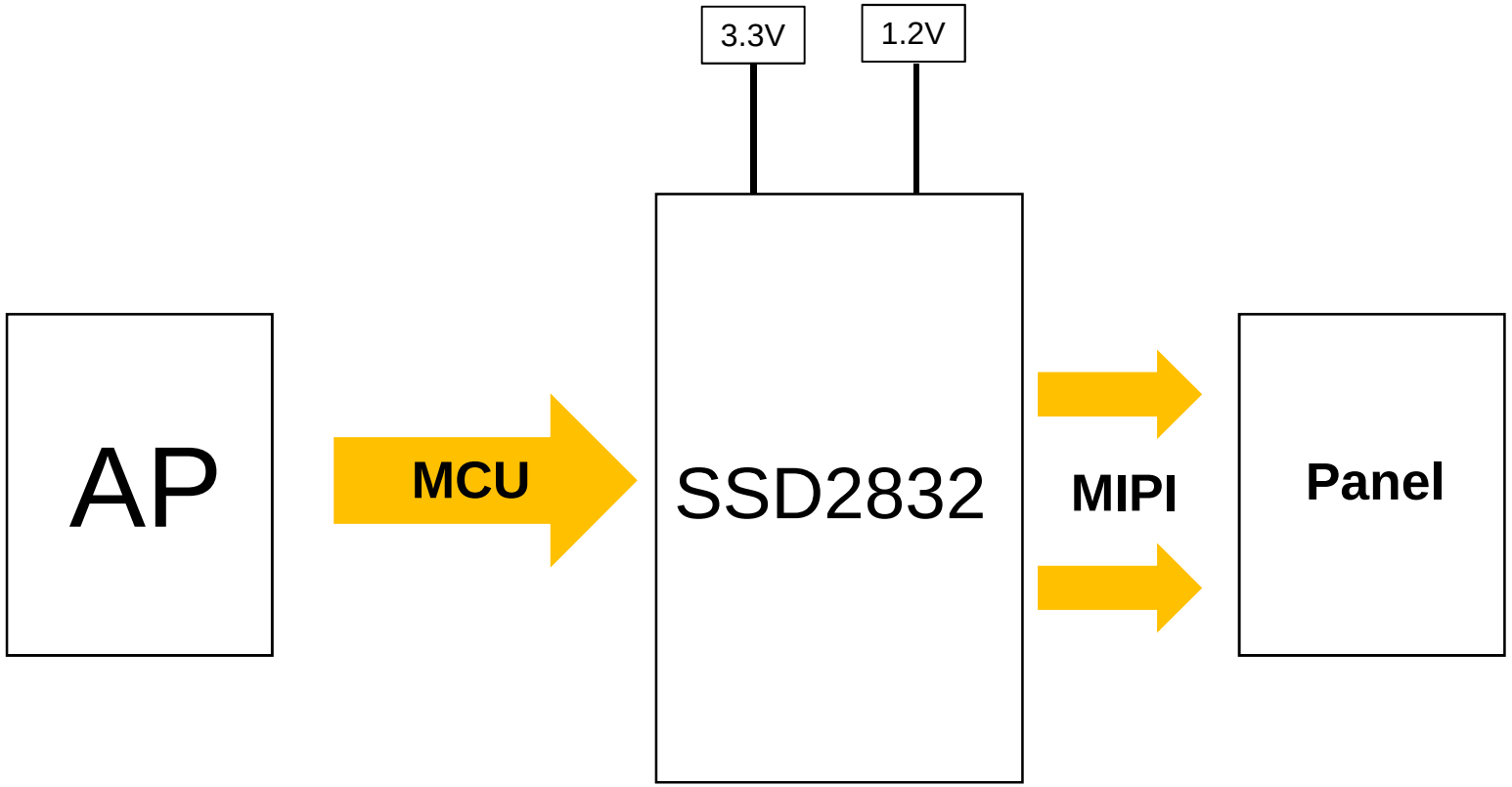
Revision History

Rev.	Date	Author	Description
V0.0	2017. 12.13	Paul Lau	First draft

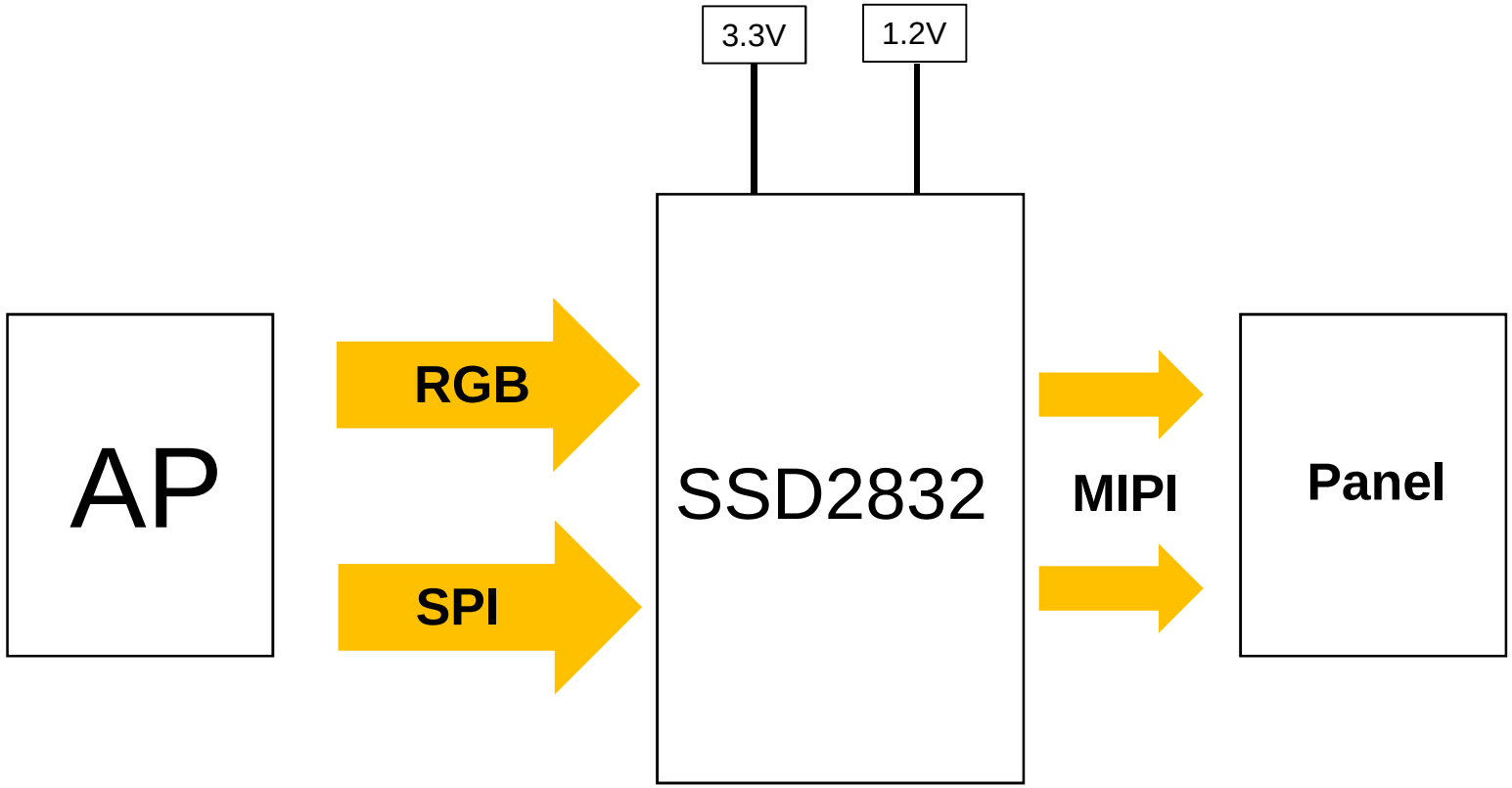
Application block diagram



Block Diagram - MCU Interface



Block Diagram – SPI+RGB Interface



Checklist

1) Hardware
   A. Power supply
   B. OSC
   C. SPI / MCU interface
   D. RGB interface
   E. Jumper settings
2) Software
   A. PLL settings
   B. LP clock settings
   C. Sync width, porch and active display settings
   D. Pixel input assignment (RGB and MCU interface)
   E. DPHY / CPHY register settings
   F. DSC settings
   G. V2C settings
3) MIPI output waveforms
   A. CPHY LP/HS command mode
   B. CPHY video mode
   C. DPHY LP/HS command mode
   D. DPHY video mode

Checklist

4) Reference information
   A. Schematic
   B. Layout guide
   C. Initial code, 2 x 1440 x 2560
5) Debug steps
   A. OSC check
   B. SPI read back
   C. MIPI LP read back
   D. MIPI HS read back
   E. MIPI video BIST mode

Checklist

6) Q&A

A. No display

1. No MIPI output
2. Incorrect MIPI waveform
3. Correct MIPI waveform

B. Abnormal display

1. Fade out display
2. Display shift
3. Tearing display
4. Flickering display
5. Dotted display

C. V2C mode

1. Random RAM display only
2. Shifted display
3. Cannot update display image

D. DSC mode

1. Random RAM display only
2. Incorrect decompression image

1. Hardware

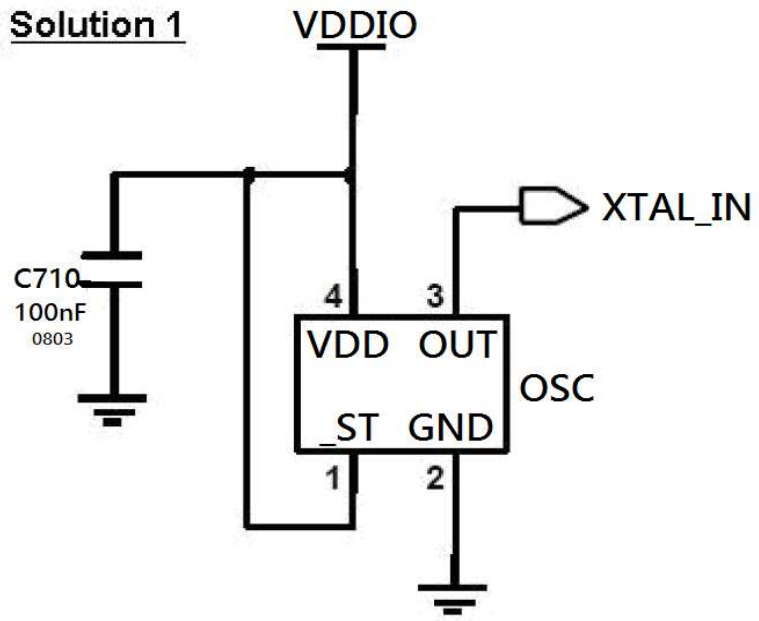
A. Power supply
B. Oscillator
C. SPI Interface
D. RGB Interface
E. MCU Interface

1A Power Supply

- AVDD & VDD_CORE
  - Connect to 1.2V
- VDD3IO
  - Connect to 1.8V or 3.3V
- VCIP
  - Connect to 3.3V

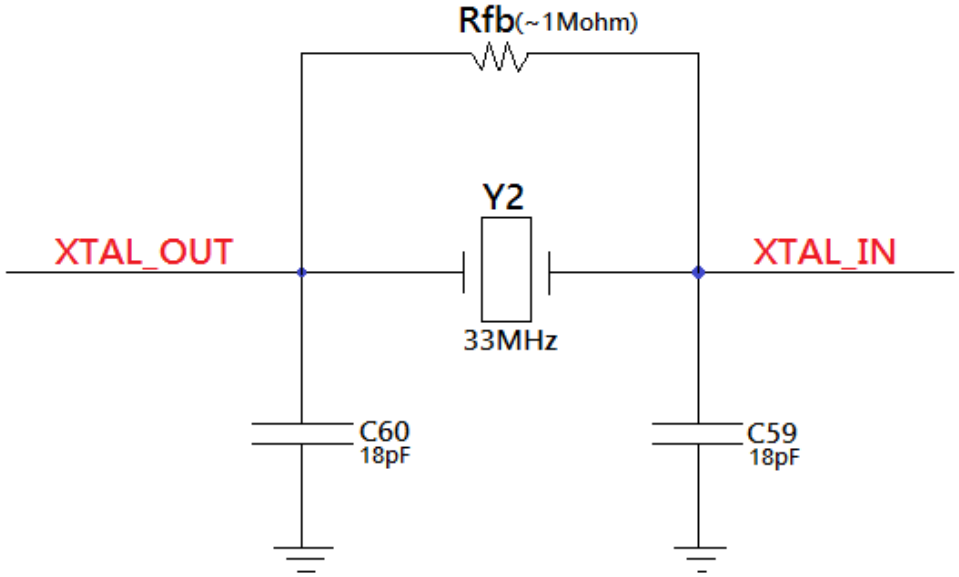
1B Oscillator

- Solution 1
  - 5MHz < XTAL_IN ≤ 40MHz
  - Keep XTAL_OUT **OPEN**



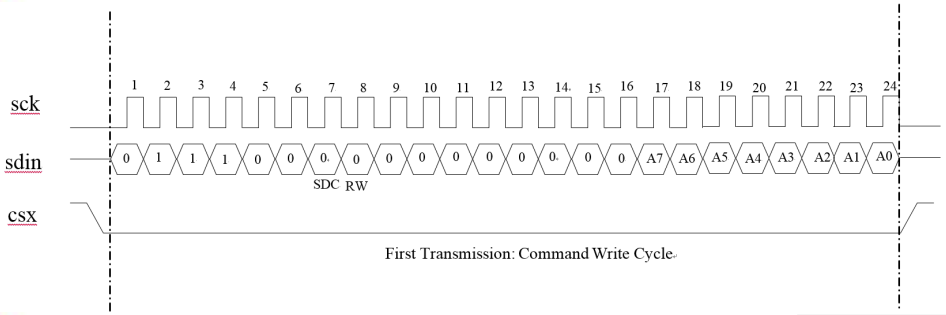
1B Oscillator

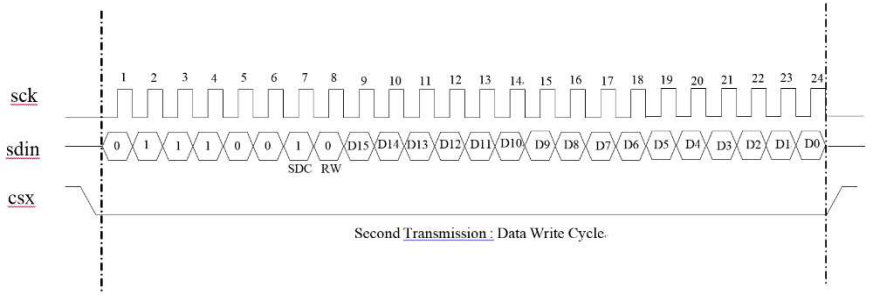
- Solution 2
  - 5MHz < XTAL_IN ≤ 40MHz



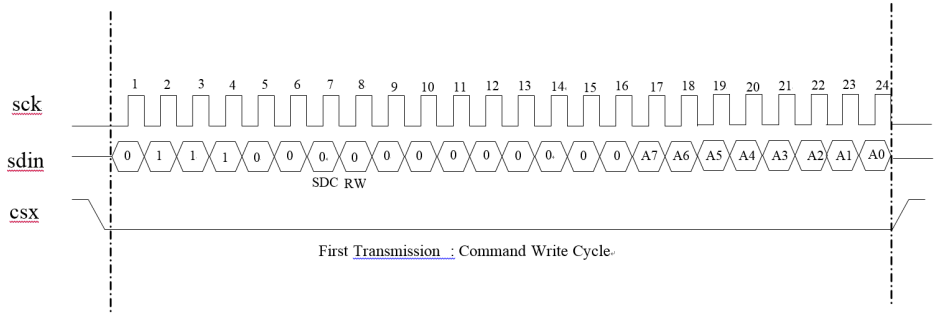
1C SPI Interface

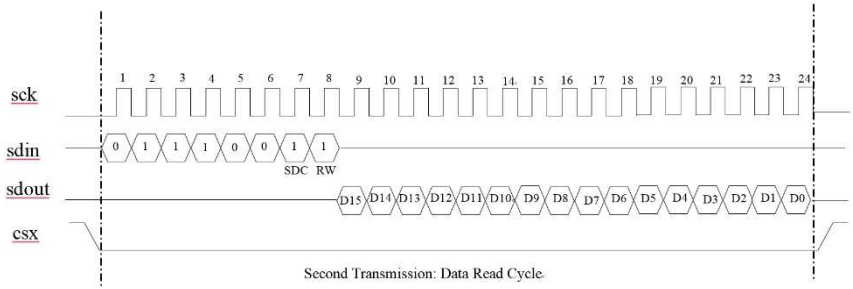
- 3 wire 24bit SPI interface





Write Operation

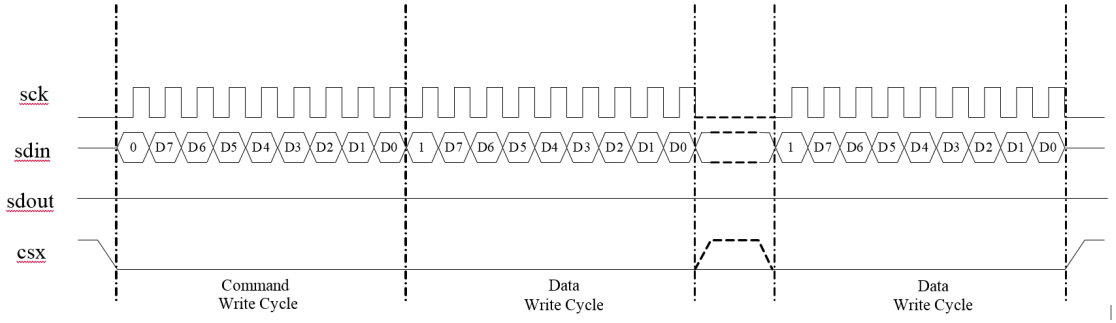




Read Operation

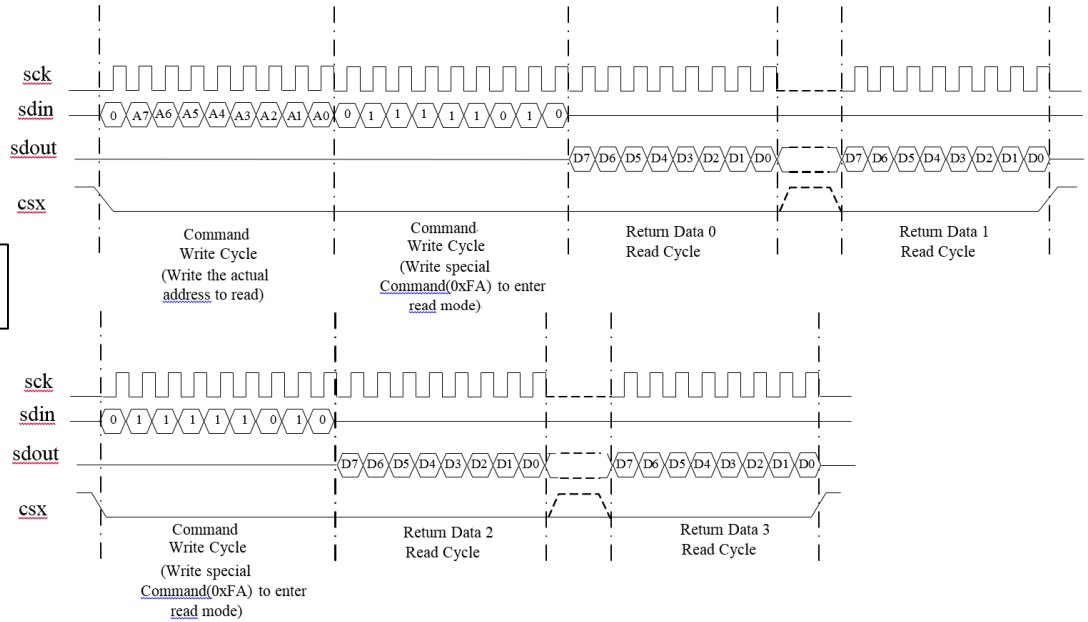
1C SPI Interface

- 3 wire 8 bit



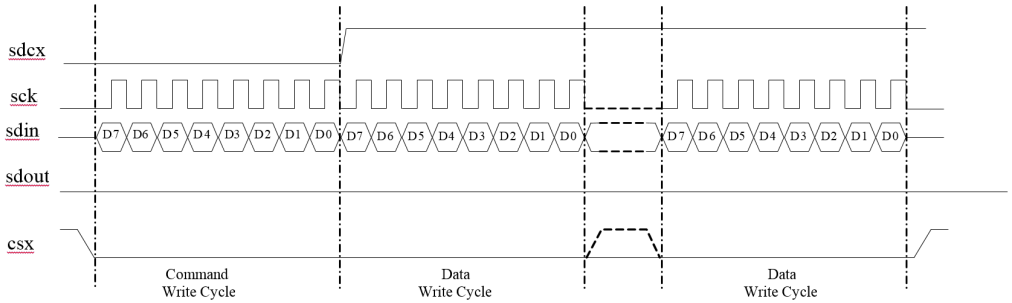
Write Operation

Read Operation



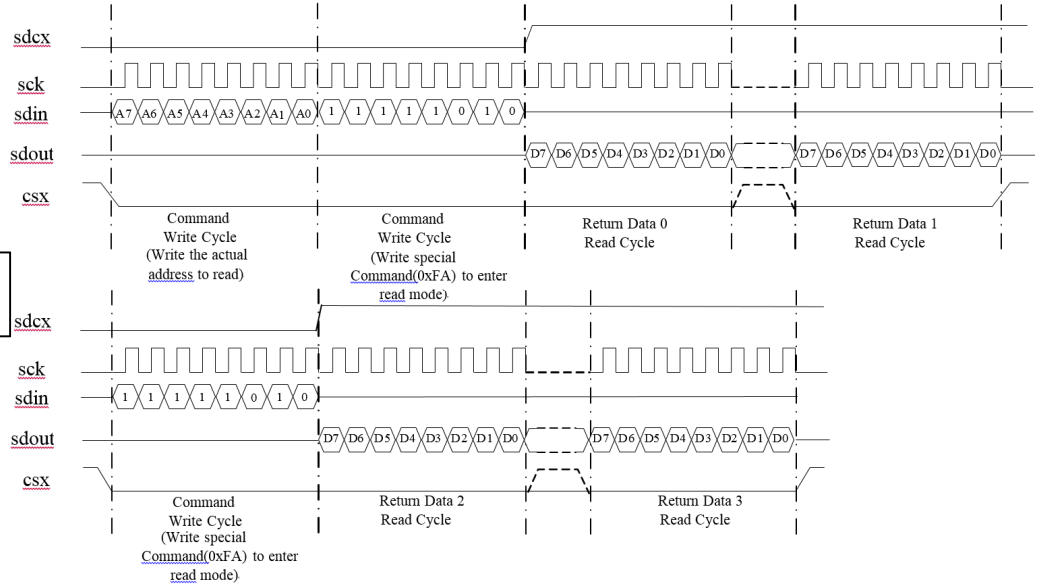
1C SPI Interface

- 4 wire 8 bit



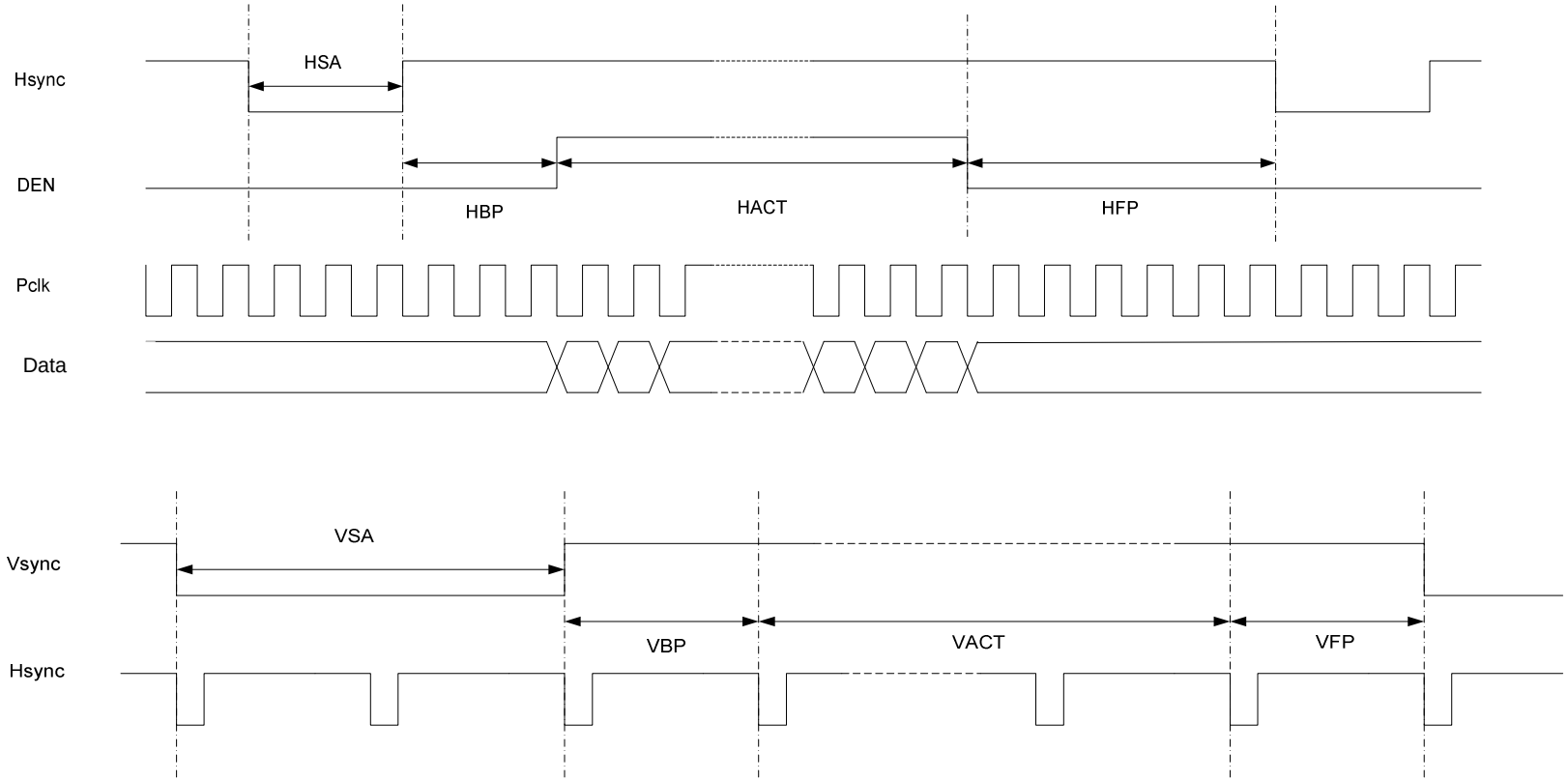
Write Operation

Read Operation



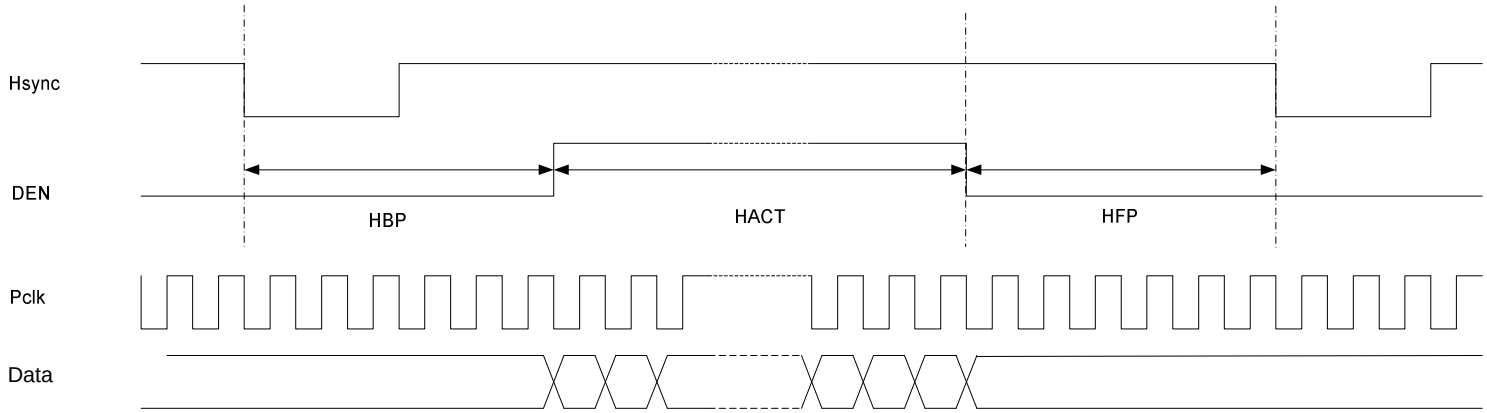
1D RGB Interface

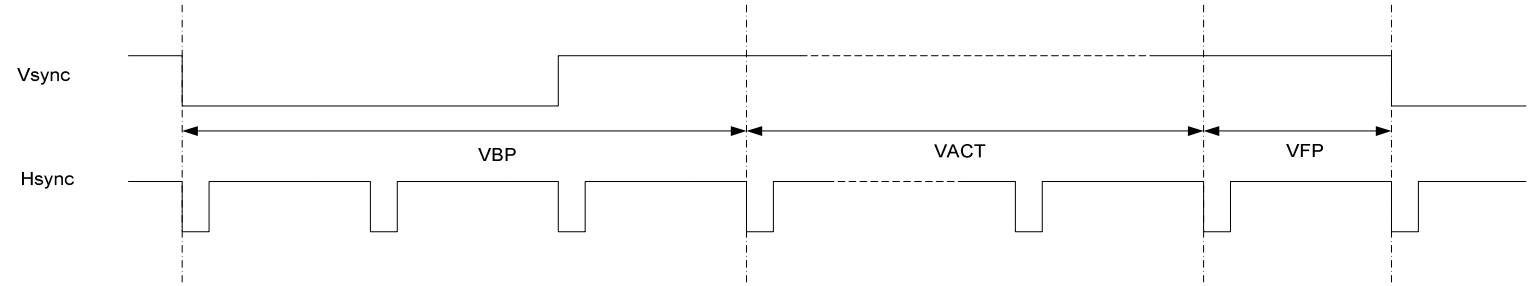
- Sync Pulses
- SYNC width will not be counted for back porch value



1D RGB Interface

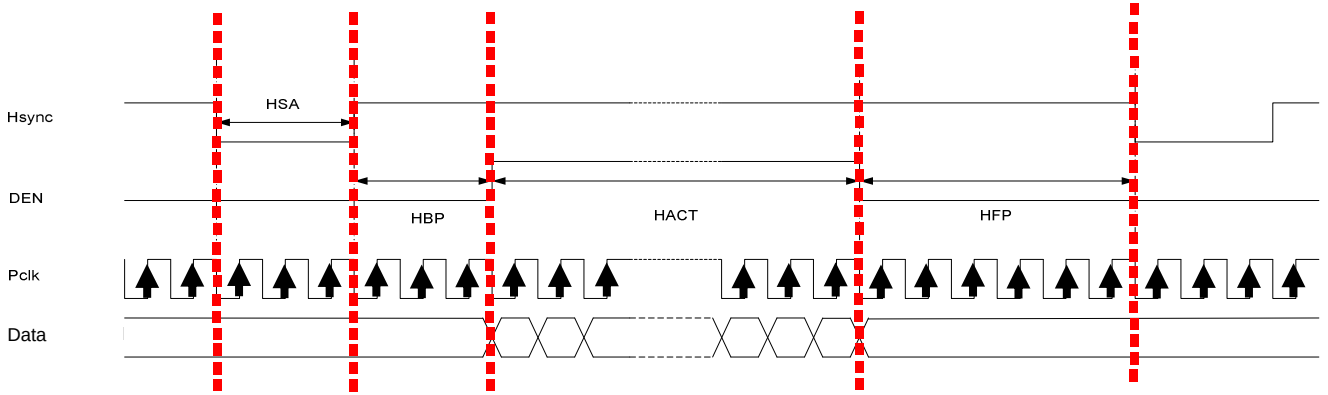
- Sync event
- SYNV width will be counted for back porch value





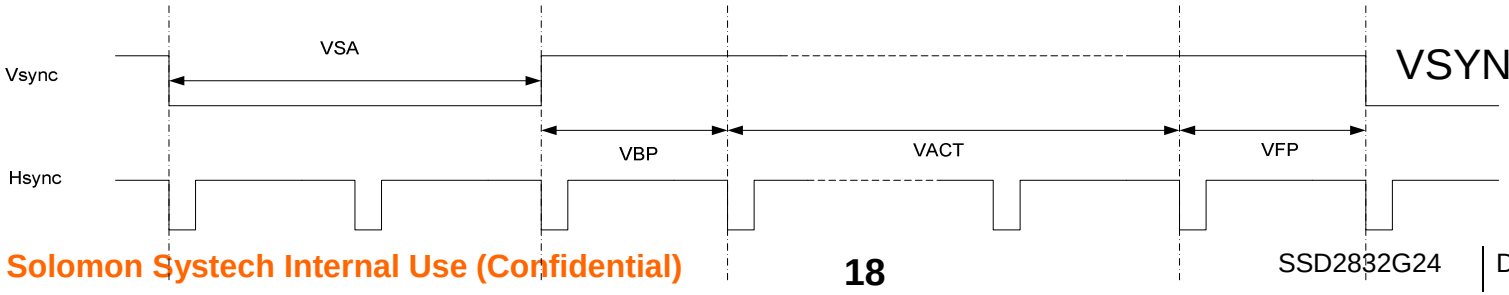
1D RGB Interface

- HSYNC is active **LOW**
- Den is active **HIGH**
- VSYNC is active **LOW**
- Make sure PCLK is rising edge trigger
- Rising/Falling edge of HSYNC/VSYNC/DEN/DATA must be matched with PCLK falling edge



HSYNC is active low

DEN is active high



VSYNC is active low

1E MCU Interface

- Type A, fixed E mode

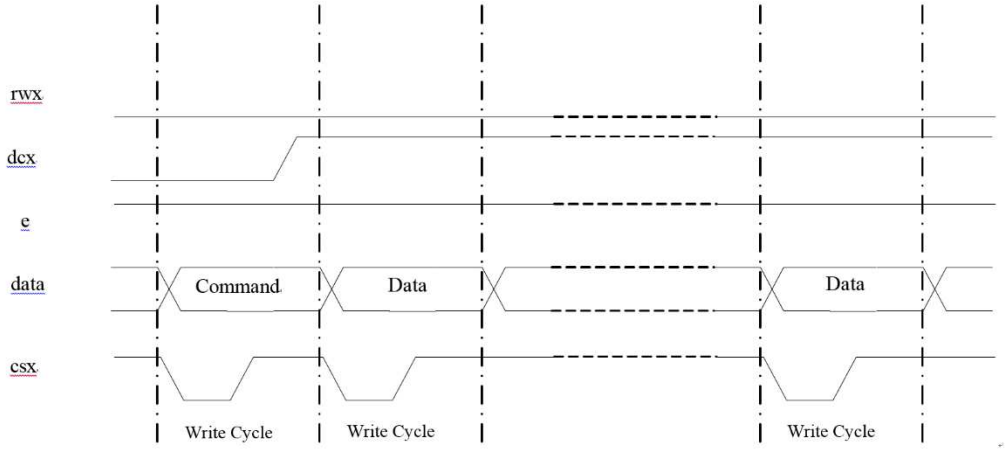
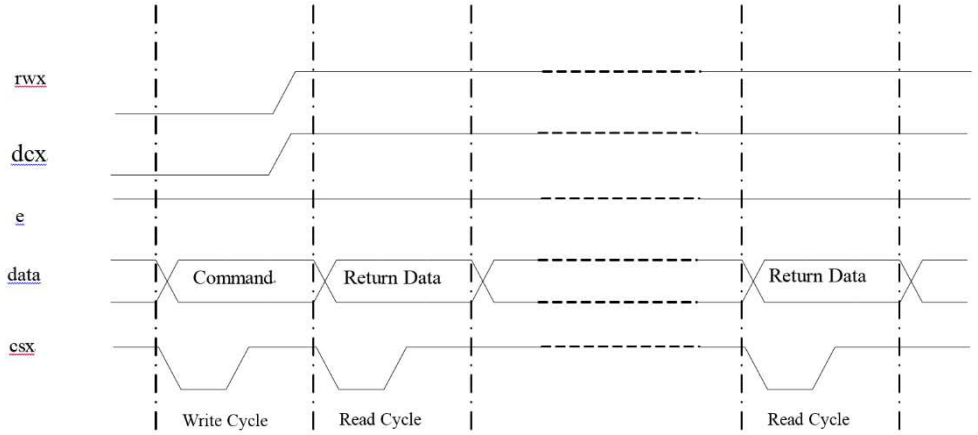


Illustration of Write Operation

Illustration of Read Operation



1E MCU Interface

- Type A, Clocked E mode

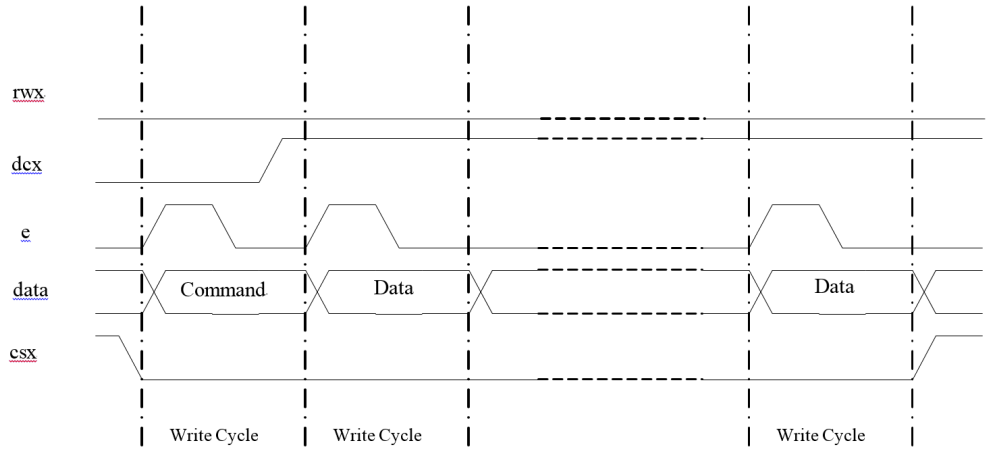
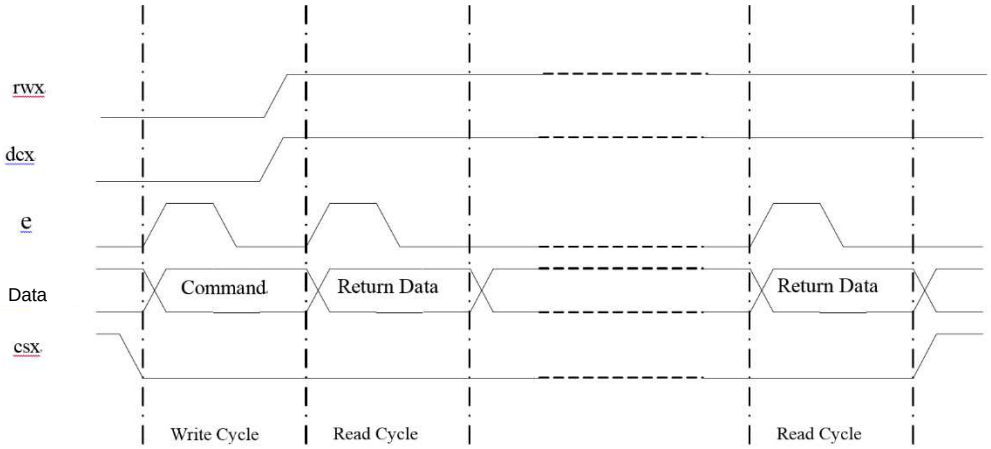


Illustration of Write Operation

Illustration of Read Operation



1E MCU Interface

- Type B

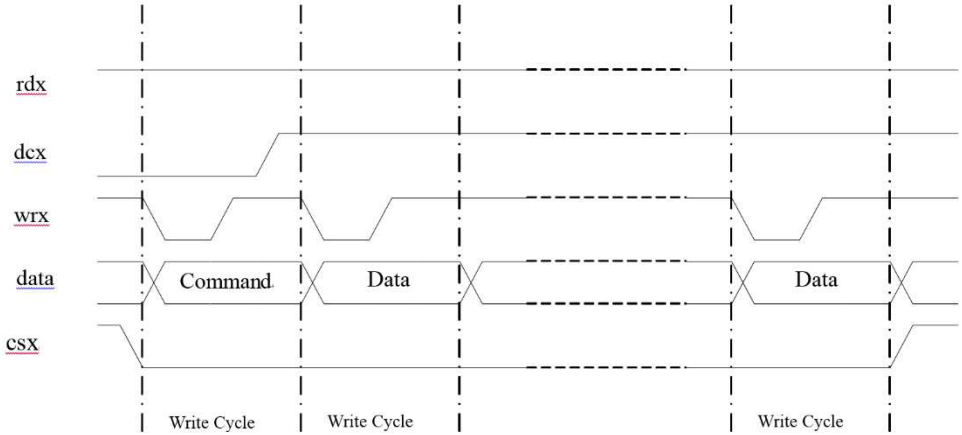
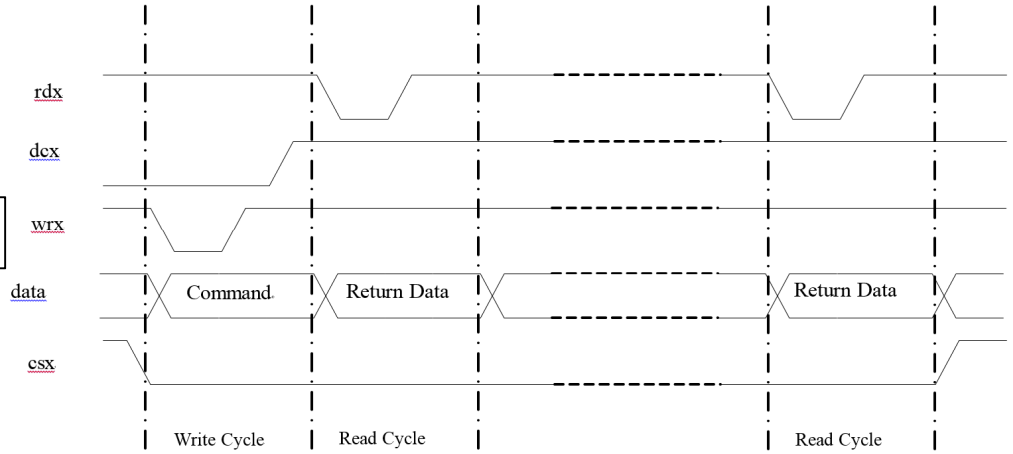


Illustration of Write Operation

Illustration of Read Operation



1E Jumper setting

- TEST_MODE0:
  - 0: CPHY
  - 1: DPHY
- IF_SEL_0:
  - 0: SPI + RGB interface
  - 1: MCU interface
- PN_D:
  - 0: sleep mode
  - 1: normal operation

2. Software

A. PLL settings
B. LP clock settings
C. Input Sync width, porch and active display settings
D. Output Sync width, porch and active display settings
E. Pixel input assignment (RGB and MCU interface)
F. DPHY / CPHY register settings
G. DSC settings
H. V2C settings

2A PLL setting - **D**PHY

- Related commands:
- 0xB9 Control PLL on/off
- 0xBA PLL freq. setting
- PLL freq. can only be changed when PLL is off

- Minimum PLL clock frequency is related to PCLK
- Min. PLL = pclk x 30 x 2/ no. of lanes (for 30-bit color)
- E.g. PCLK=130MHz, 30bit color, 8 lanes
- Min.PLL freq. = 975M**bps**

2A PLL setting - **C**PHY

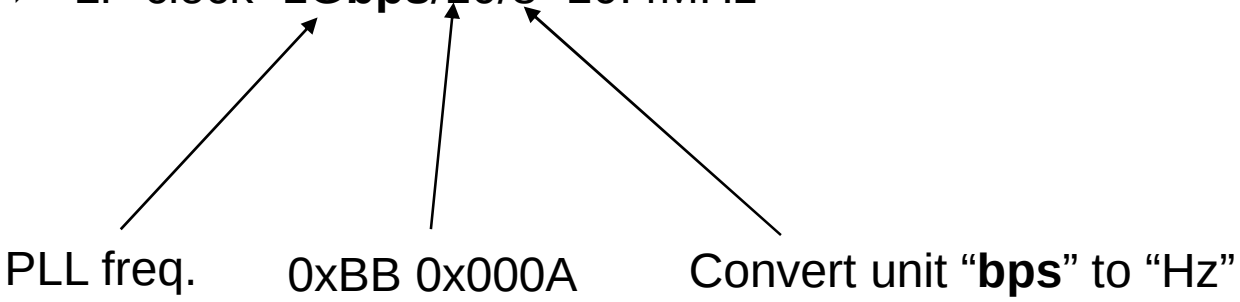
- Related commands:
- 0xB9 Control PLL on/off
- 0xBA PLL freq. setting
- PLL freq. can only be changed when PLL is off

- Minimum PLL clock frequency is related to PCLK
- Min. PLL = pclk x 30 x 2 / no. of lanes / 2.28
- E.g. PCLK=130MHz, 30bit color, 6 lanes
- Min.PLL freq. = 571Msps

- *PS : 1sps = 2.28bps

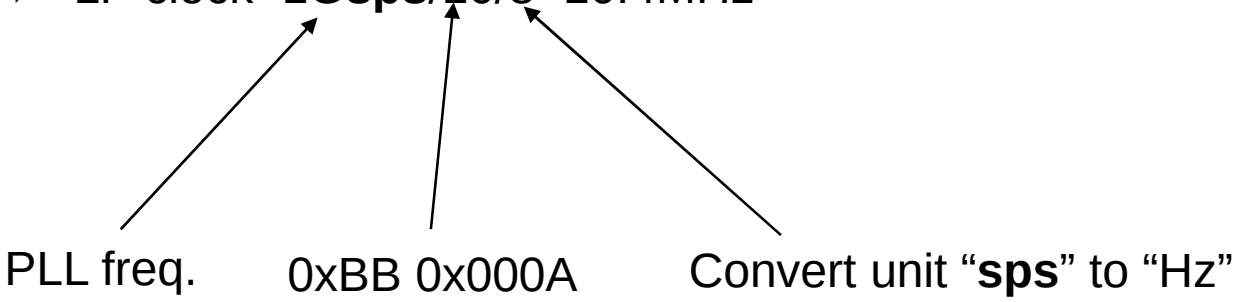
2B LP clock setting - **D**PHY

- Related commands:
  - 0xB9 Control PLL on/off
  - 0xBA PLL freq. setting
  - 0xBB LP clock setting
- E.g. TX_CLK=20MHz, 0xBA 0xc132, 0xBB 0x000A
  - LP clock=1G**bps**/10/8=10.4MHz



2B LP clock setting - **C**PHY

- Related commands:
  - 0xB9 Control PLL on/off
  - 0xBA PLL freq. setting
  - 0xBB LP clock setting
- E.g. TX_CLK=20MHz, 0xBA 0xc132, 0xBB 0x000A
  - LP clock=1G**sps**/10/8=10.4MHz



2C Input Sync width, porch and active display settings

- SSD2832 has 1 port of 60-bit RGB input
- Sync width, porch and active display settings of **horizontal** should be half of the panel setting
- Sync width, porch and active display settings of **vertical** remain unchanged
- E.g.

	Panel setting	Input setting
Horizontal Sync width	10	5
Horizontal back porch	36	18
Horizontal front porch	100	50
Horizontal Active display	1440	720
Vertical Sync width	2	2
Vertical back porch	10	10
Vertical front porch	10	10
Vertical Active display	2560	2560

2D Output sync width, porch and active display setting

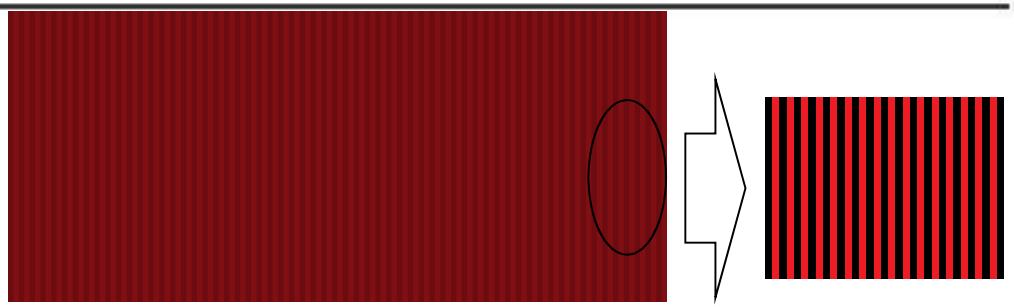
- SSD2832 has 2 DSI output
- Sync width, porch and active display setting depends on the no. of DSI output selected

	Related Register	Panel setting	Output setting of **1 DSI**	Output setting of **2 DSI**
Horizontal Sync width	0xB1	10	10	5
Horizontal back porch	0xB2	36	36+10	18+5
Horizontal front porch	0xB3	100	100	50
Horizontal Active display	0xB4	1440	1440	720
Vertical Sync width	0xB1	2	2	2
Vertical back porch	0xB2	10	10+2	10+2
Vertical front porch	0xB3	10	10	10
Vertical Active display	0xB5	2560	2560	2560

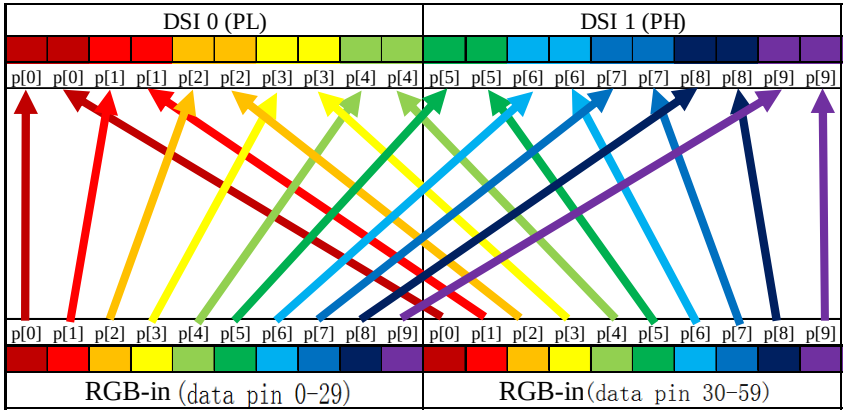
*Horizontal / Vertical back porch of output is the sum of horizontal / vertical sync width and back porch of input

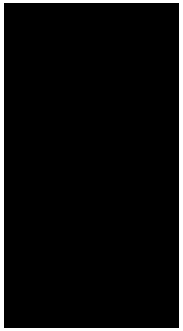
2E Pixel input assignment – RGB Interface

- Left/Right mode



Output: 1440x2560



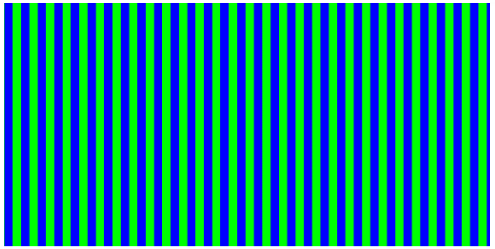


Original Image(RGB in)
Input: 720x2560

Original Image(RGB in)
Input: 720x2560

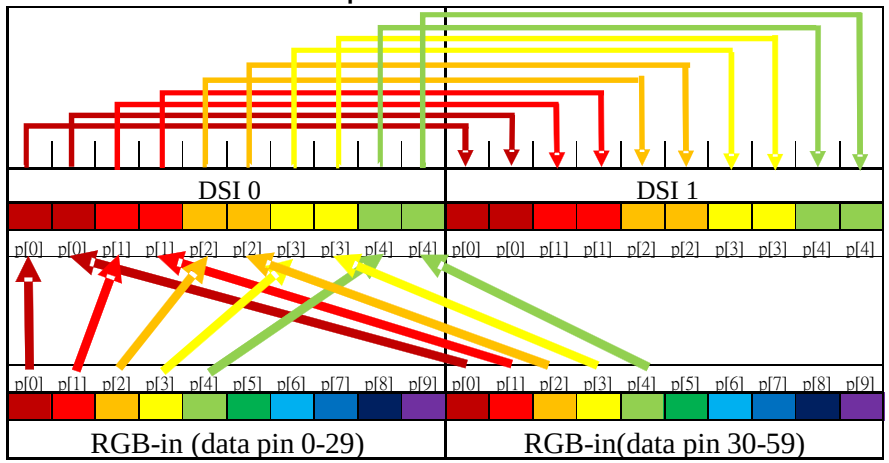
2E Pixel input assignment – RGB Interface

- Broadcast mode

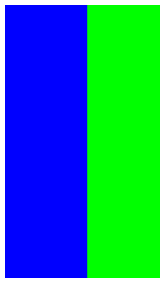


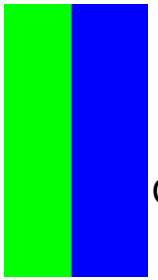
Output 1440x2560

Copy DSI 0 to DSI 1



Original Image(RGB in)
Input: 720x2560



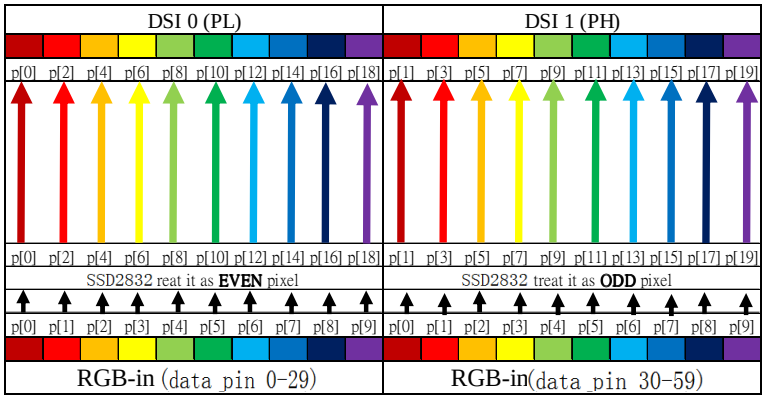


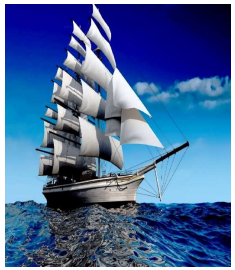
Original Image(RGB in)
Input: 720x2560

2E Pixel input assignment – RGB Interface

- Odd/Even mode

Output: 1440x2560





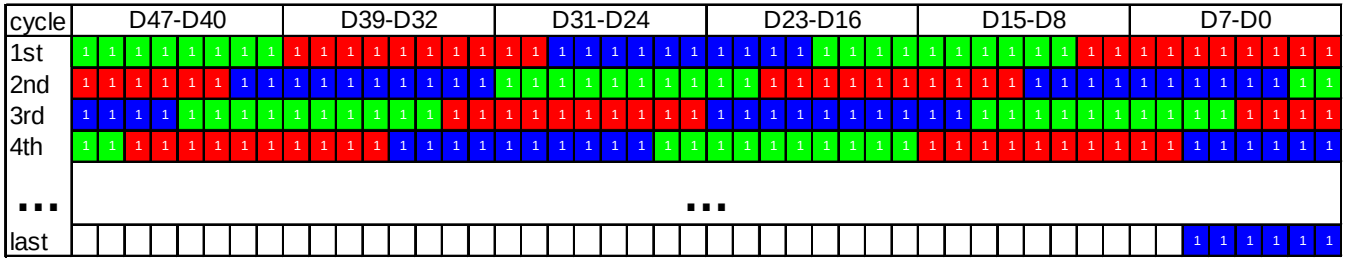
Original Image(RGB in)
Input: 720x2560

Original Image(RGB in)
Input: 720x2560

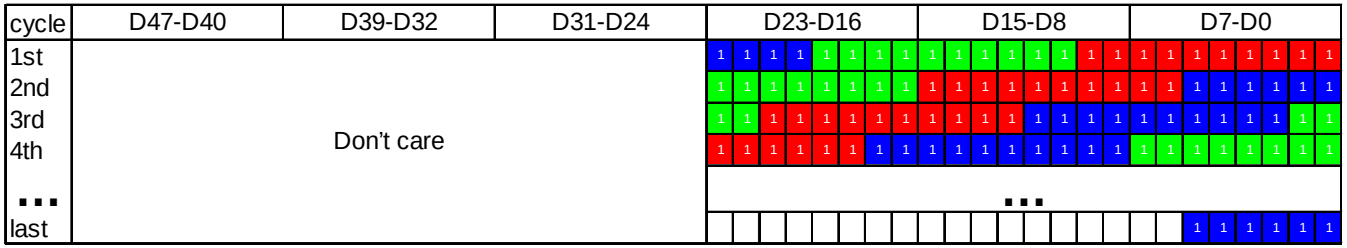
2E Pixel input assignment – MCU Interface

- 30bit RGB: 10(R)-10(G)-10(B)

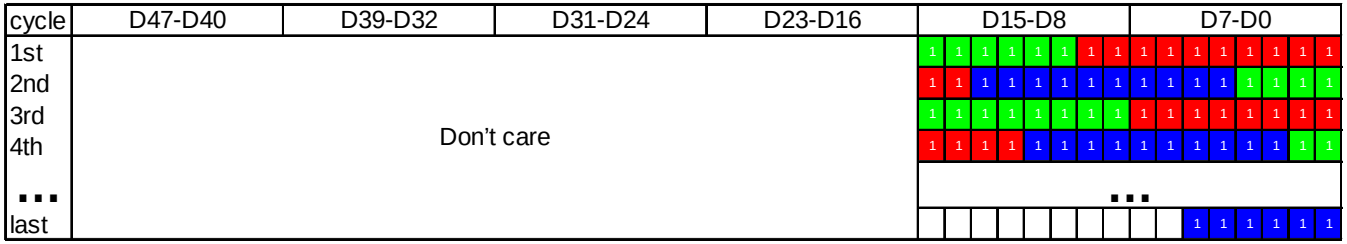
48bit interface



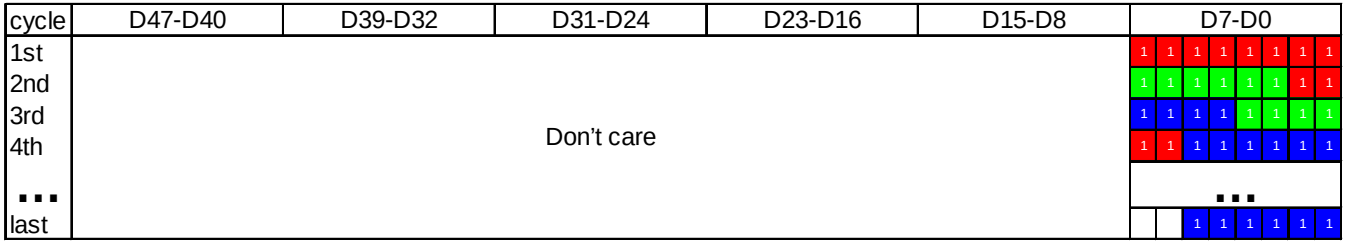
24bit interface



16bit interface

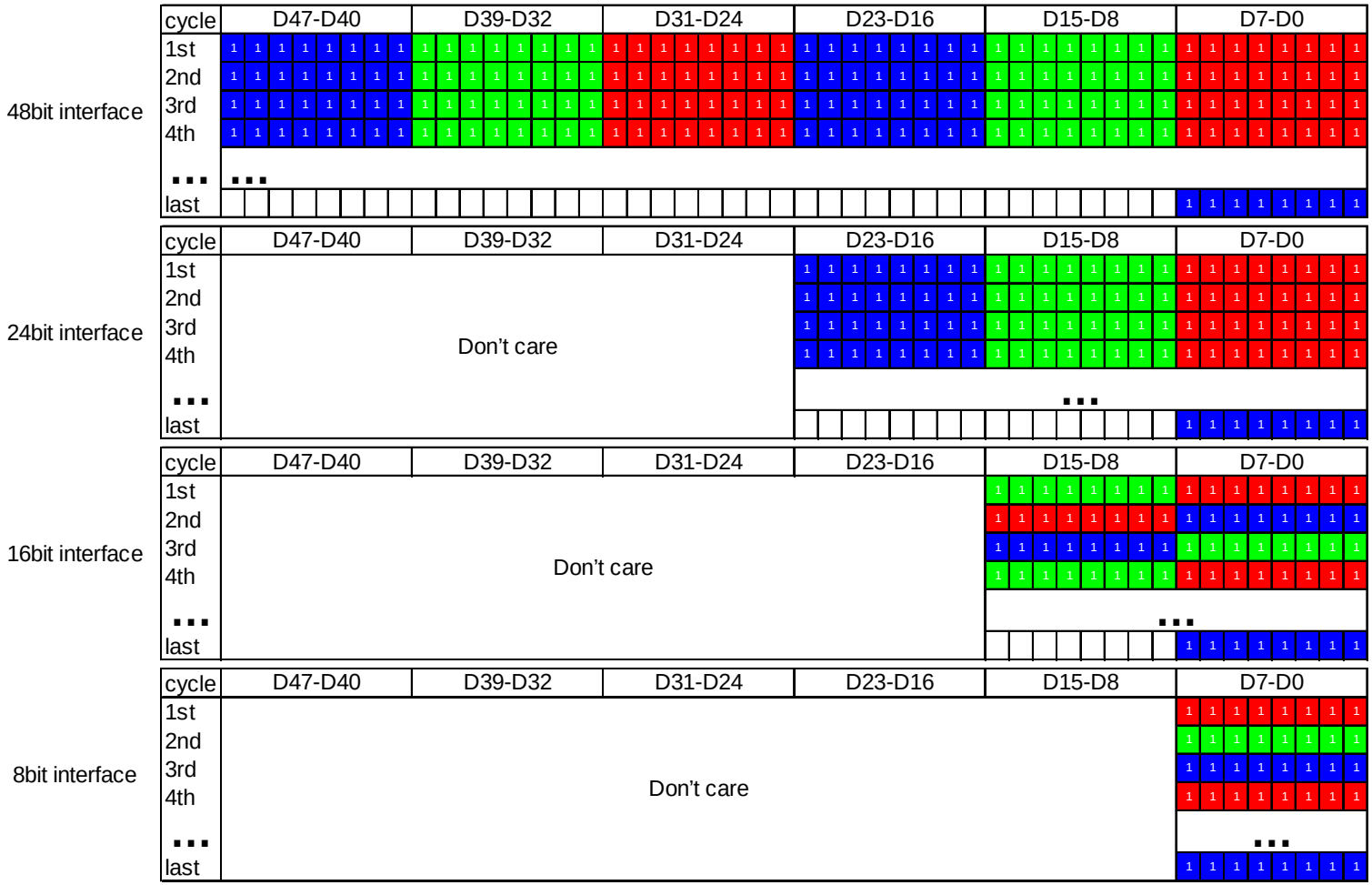


8bit interface



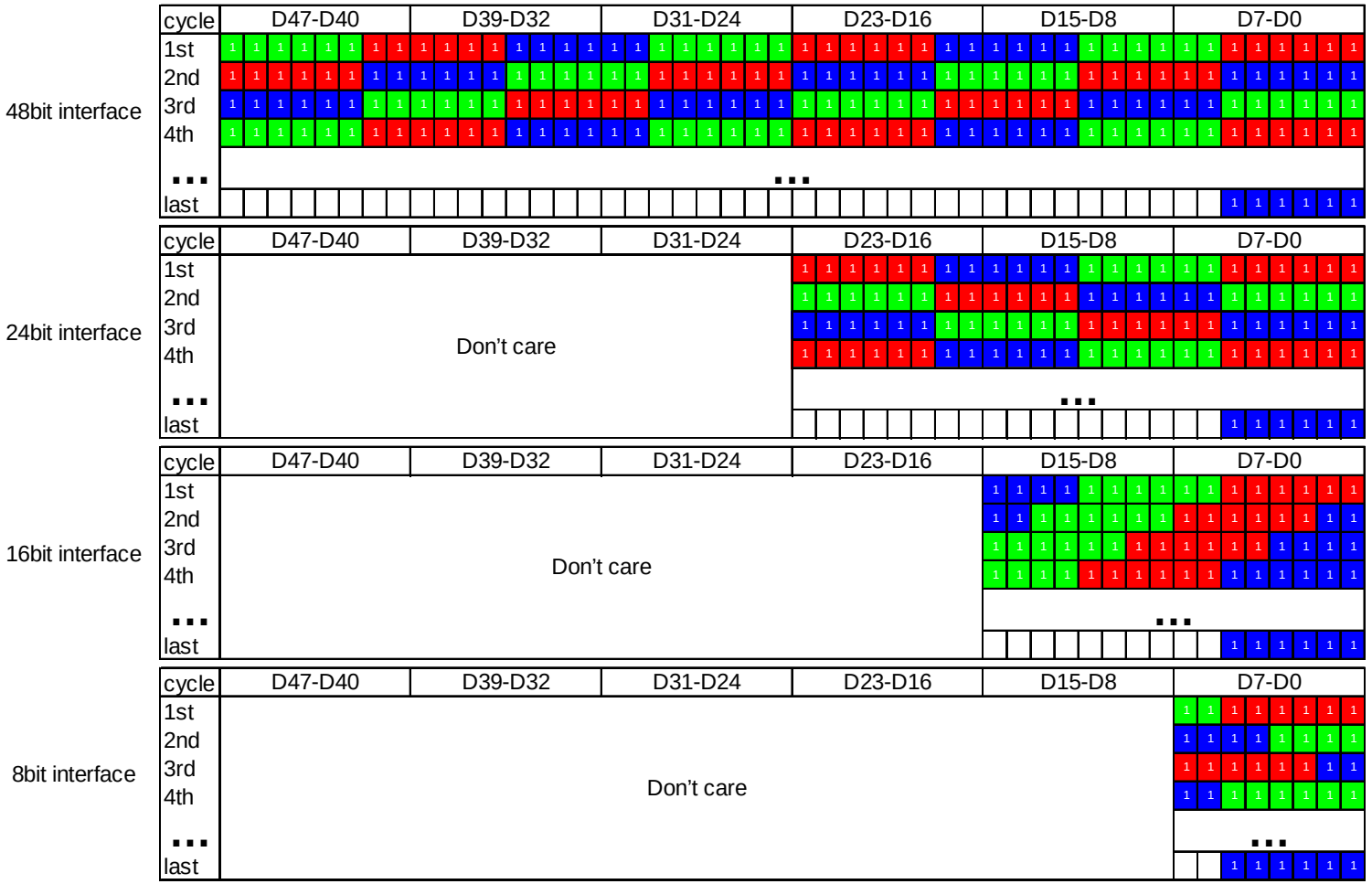
2E Pixel input assignment – MCU Interface

- 24bit RGB: 8(R)-8(G)-8(B)



2E Pixel input assignment – MCU Interface

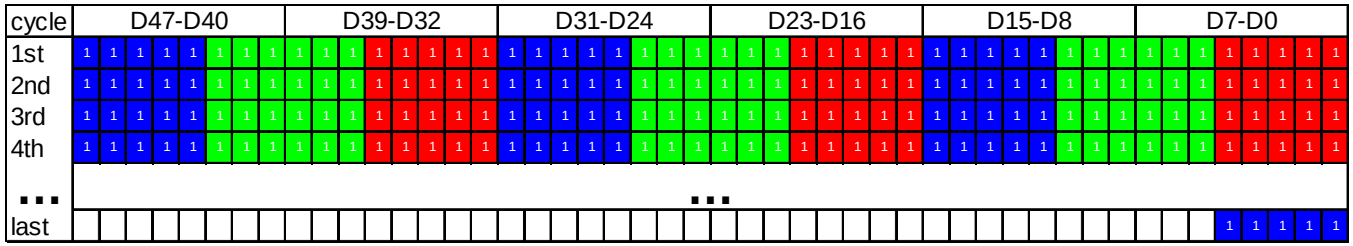
- 18bit RGB: 6(R)-6(G)-6(B)



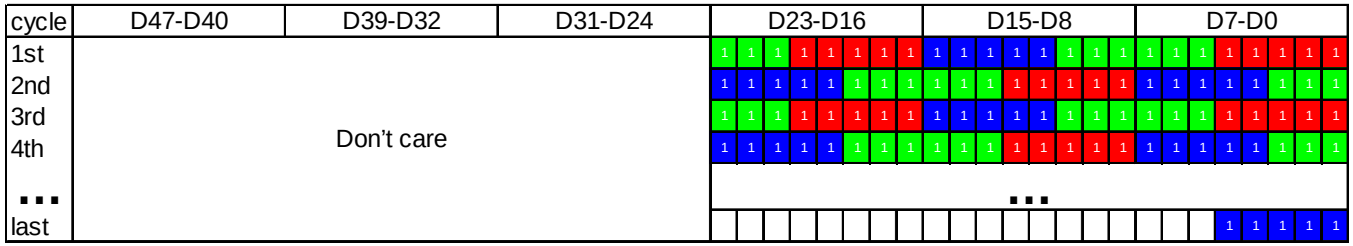
2E Pixel input assignment – MCU Interface

- 16bit RGB: 5(R)-6(G)-5(B)

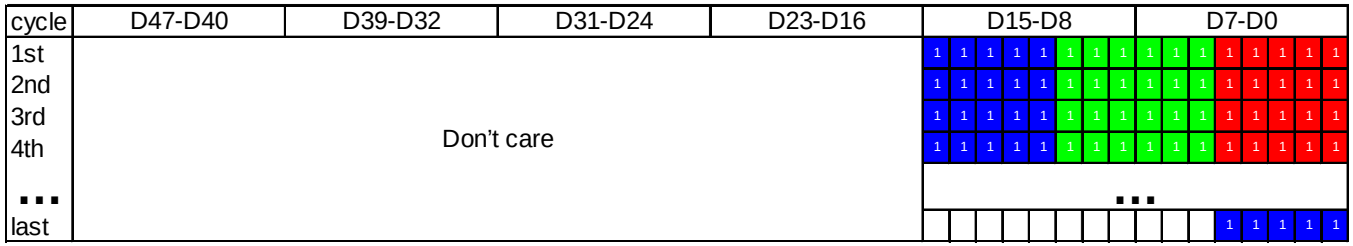
48bit interface



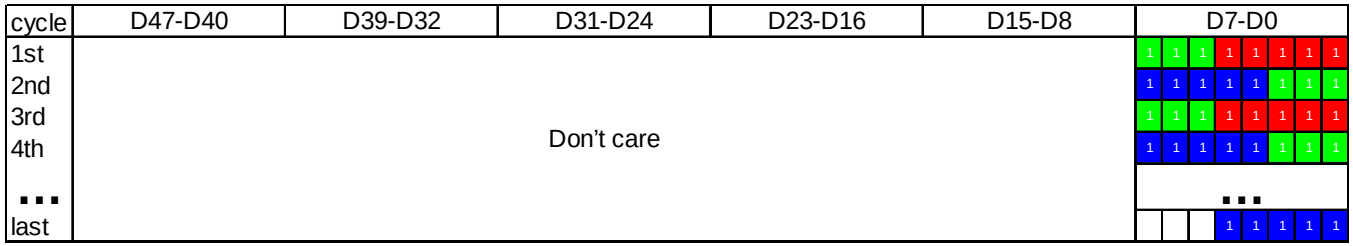
24bit interface



16bit interface



8bit interface



2F DPHY / CPHY register setting

- SSD2832 supports both DPHY and CPHY MIPI

- Related register:
- 0xBB

Bit-28	PHY
0	CPHY
1	DPHY

2G DSC setting

- SSD2832 supports DSC compression mode packet transmission
- Related register: 0xB7

Compression mode entry setting:

0xB7	DSC setting	Default setting
Bit-12	1	0
Bit-6	1	0

Keep other settings as normal Video mode except video timing

2H V2C setting

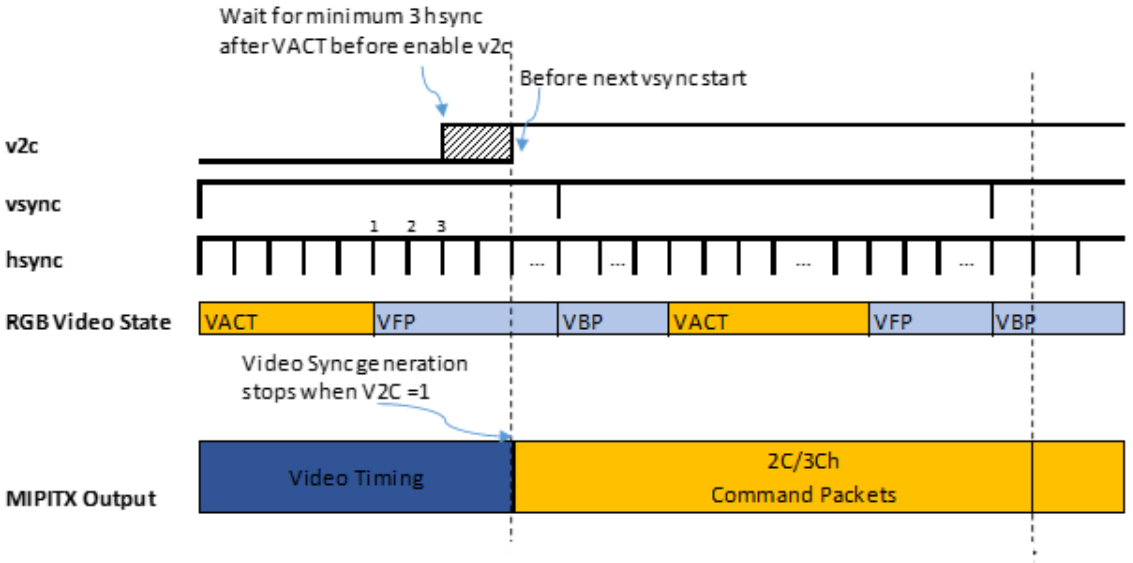
- SSD2832 supports Video to Command(V2C) mode
- This function allows MIPI Tx output convert video packets to command mode packets
- Software control in SCM.0x0010.bit16
  - 0: Disable
  - 1: Enable

Note

- Once V2C is turned on, the MIPI would be in HS link when there is active video input
- It would remain in HS link until the mode is turned off
- User is recommended to switch off V2C periodically (e.g. after 2-3 frames of conversion) as there is a built-in HS timeout

2H V2C setting

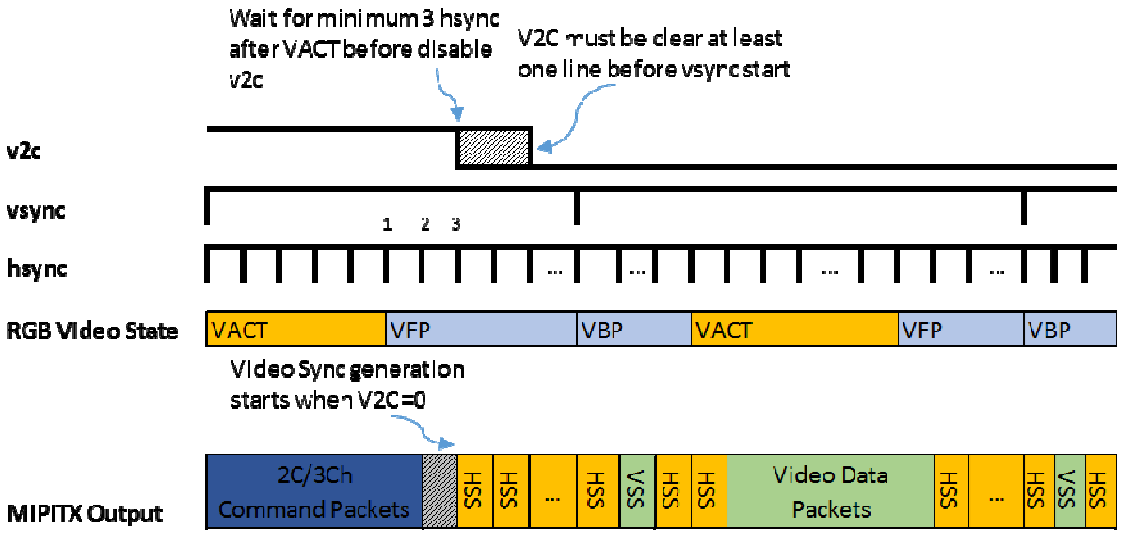
- Switching of Video mode to V2C mode
- Set SCM.0x0010.bit16 – v2c during VFP of incoming video timing
- To ensure all video data has been transmitted on the TX link, host shall wait for min of 3 hsync after VACT before setting v2c



2H V2C setting

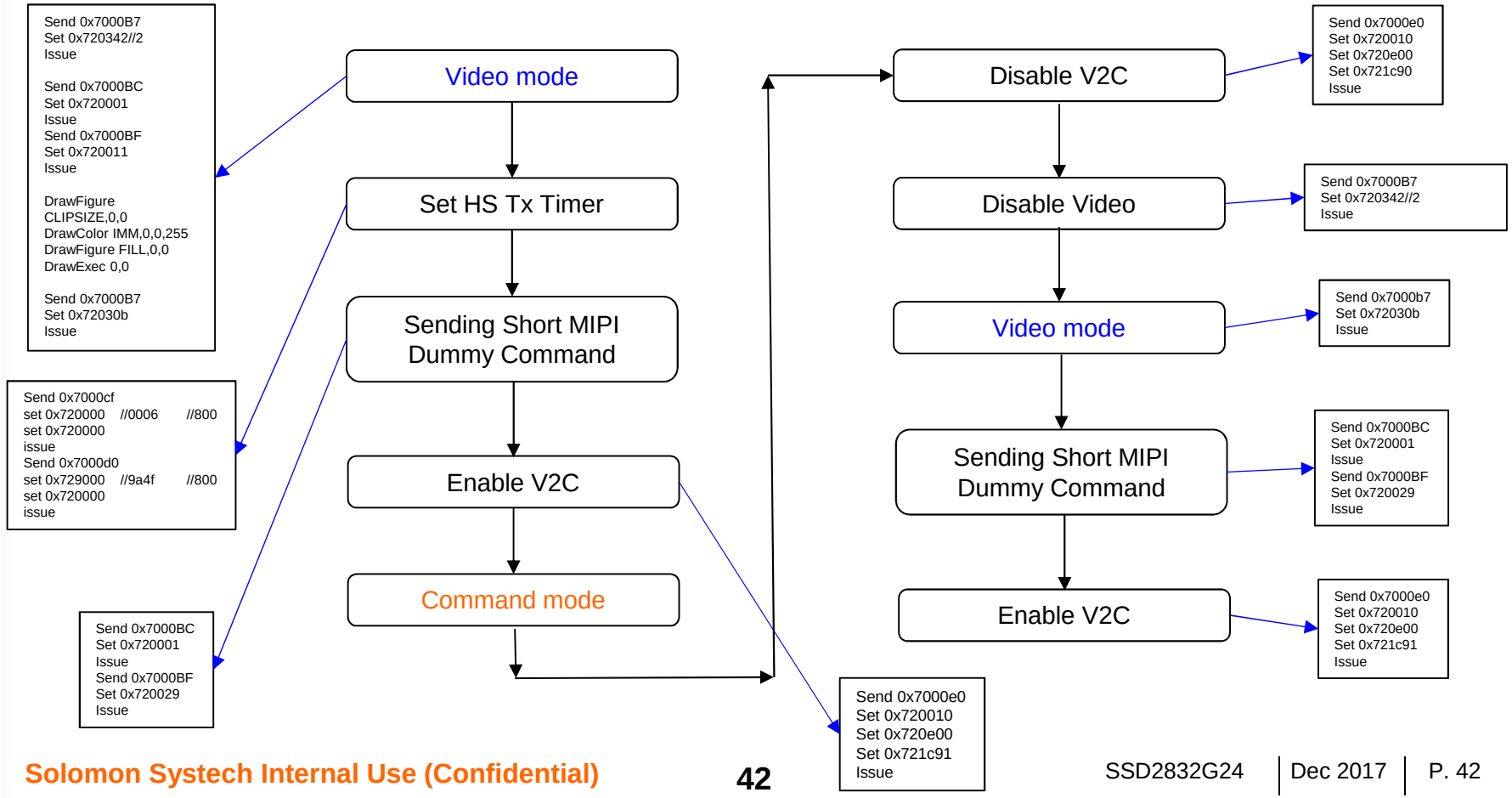
- Switching of V2C mode to Video mode
  1. Ensure 0xB7.bit3 – VEN is cleared
  2. Clear SCM.0x0010.bit16 – v2c during VFP of incoming video timing

     To ensure all video data has been transmitted on the TX link, host shall wait for min of 3 hsync after VACT before clearing v2c



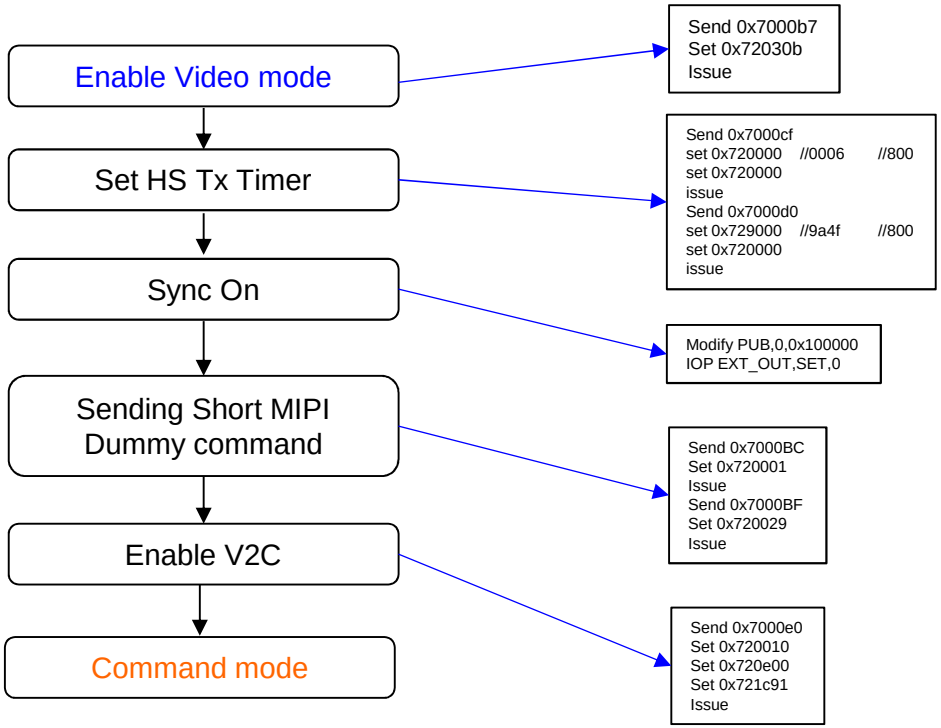
2H V2C setting - Initialization

Register adr	Data [31:24]	Data [23:16]	Data [15:8]	Data [7:0]	Description
0x00CF	0x00	0x00	0x00	0x06	// set HS TX timer
0x00D0	0x00	0x00	0x9A	0x4F	// set HS TX timer
0x0010	0x1C	0x91	0x0E	0x00	// enable v2c
0x0010	0x1C	0x90	0x0E	0x00	// disable v2c



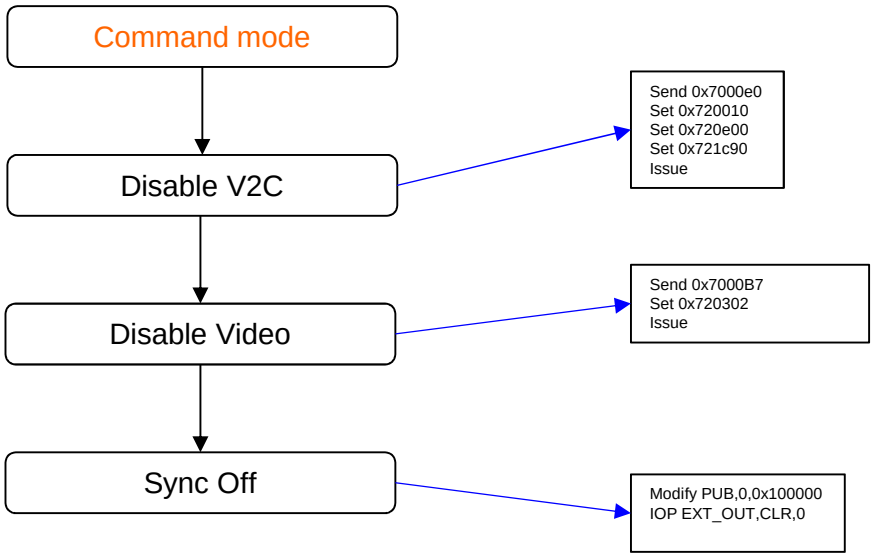
2H V2C setting – V2C ON

Register adr	Data [31:24]	Data [23:16]	Data [15:8]	Data [7:0]	Description
0x00CF	0x00	0x00	0x00	0x06	// set HS TX timer
0x00D0	0x00	0x00	0x9A	0x4F	// set HS TX timer
0x0010	0x1C	0x91	0x0E	0x00	// enable v2c



2H V2C setting – V2C OFF

Register adr	Data [31:24]	Data [23:16]	Data [15:8]	Data [7:0]	Description
0xB7	0x00	0x00	0x03	0x00	// video mode is disable, i.e. VEN=0
0x0010	0x1C	0x90	0x0E	0x00	// disable v2c



3. MIPI output waveforms

A. CPHY LP/HS command mode
B. CPHY video mode
C. DPHY LP/HS command mode
D. DPHY video mode

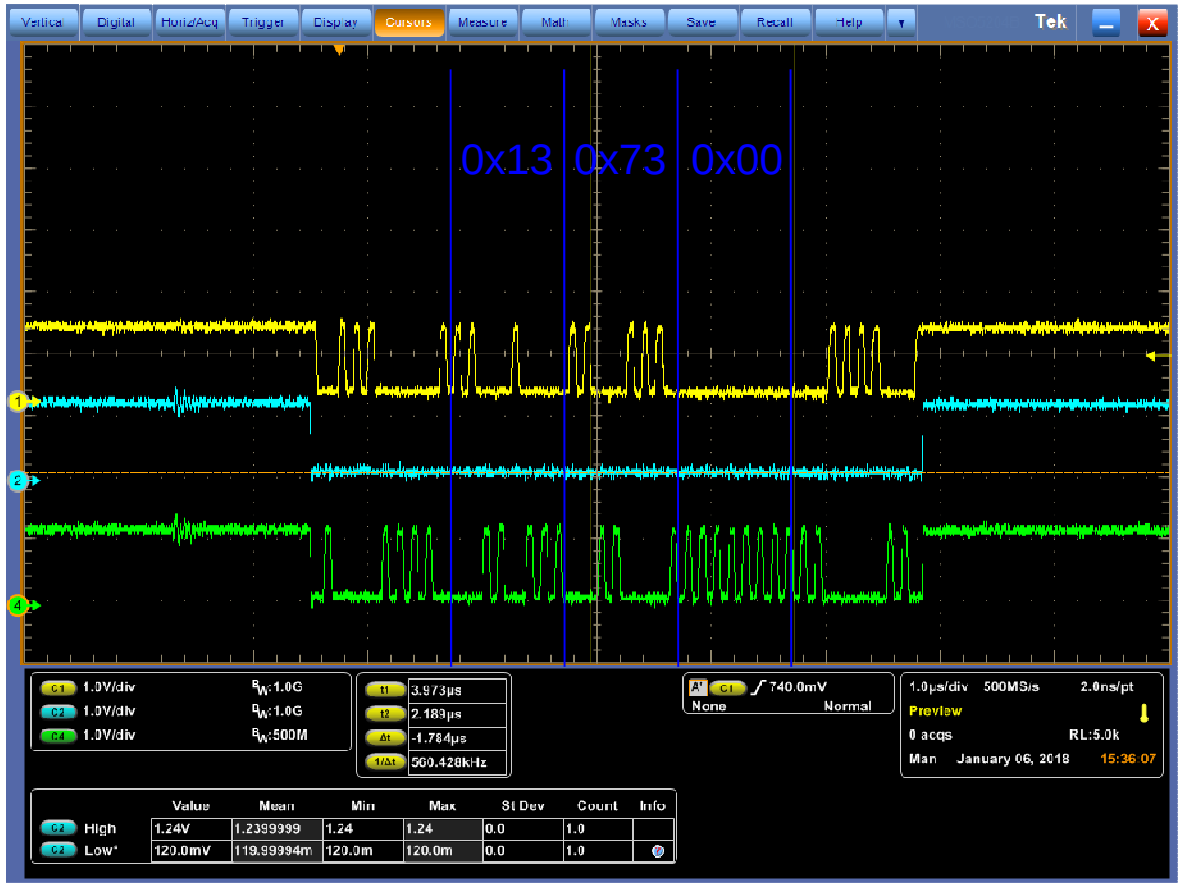
3A CPHY CMD mode MIPI output waveform

- LP command mode
  - 0x7000b7, 0x720302
  - 0x7000bc, 0x720001
  - 0x7000bf, 0x720073

TXA_A0

TXA_B0

TXA_C0

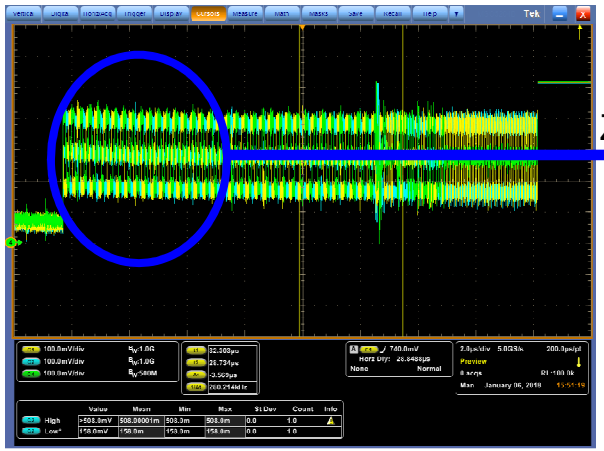


3A CPHY CMD mode MIPI output waveform

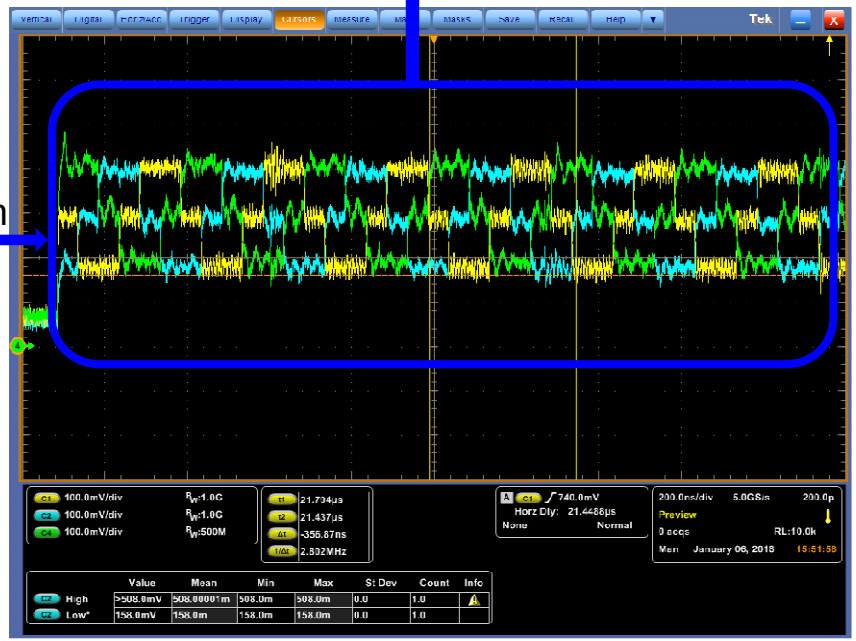
- HS command mode
  - 0x7000b9, 0x720000
  - 0x7000c4, 0x720001
  - 0x7000b7, 0x720303
  - 0x7000bc, 0x720001
  - 0x7000bf, 0x723873

The written value can't be identified directly, need decoding according to the CPHY Wire states.(please refer to CPHY MIPI spec)

TXA_A0(Yellow)
TXA_B0(Blue)
TXA_C0(Green))



Zoom in

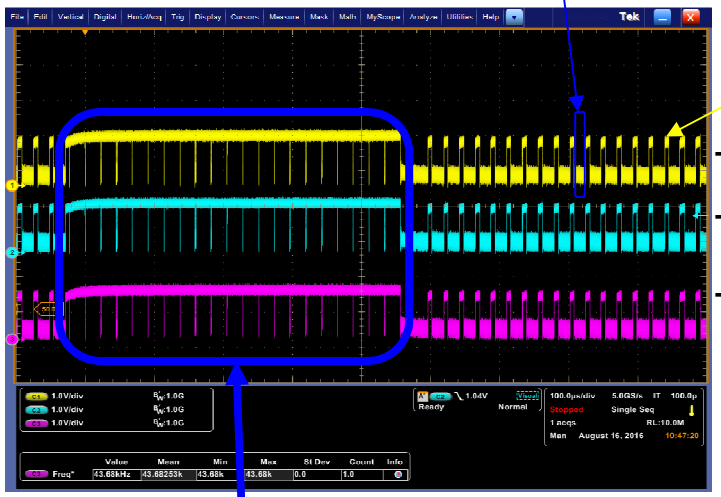


3B CPHY Video mode MIPI output waveform

- Video Mode

HS period
(Display time)

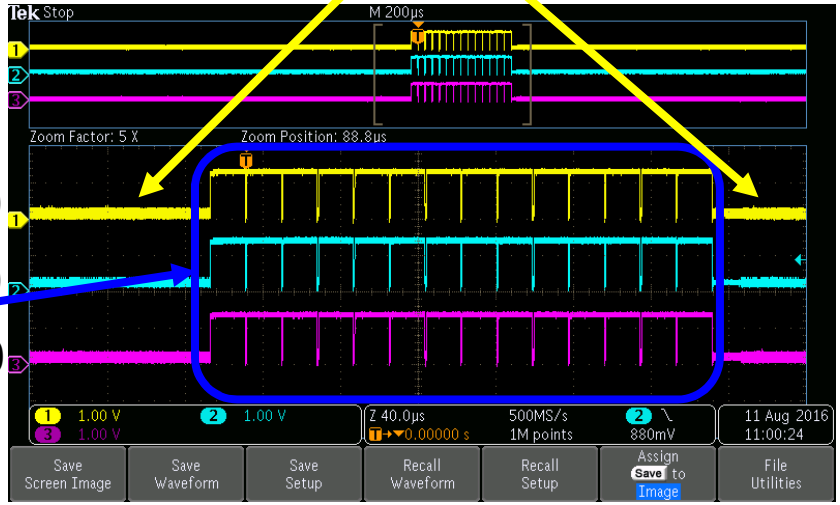
LP period
MIPI lanes go to LP at the end of each line



TXA_A0
TXA_B0
TXA_C0

Burst Mode

HS period



TXA_A0
TXA_B0
TXA_C0

Blanking period

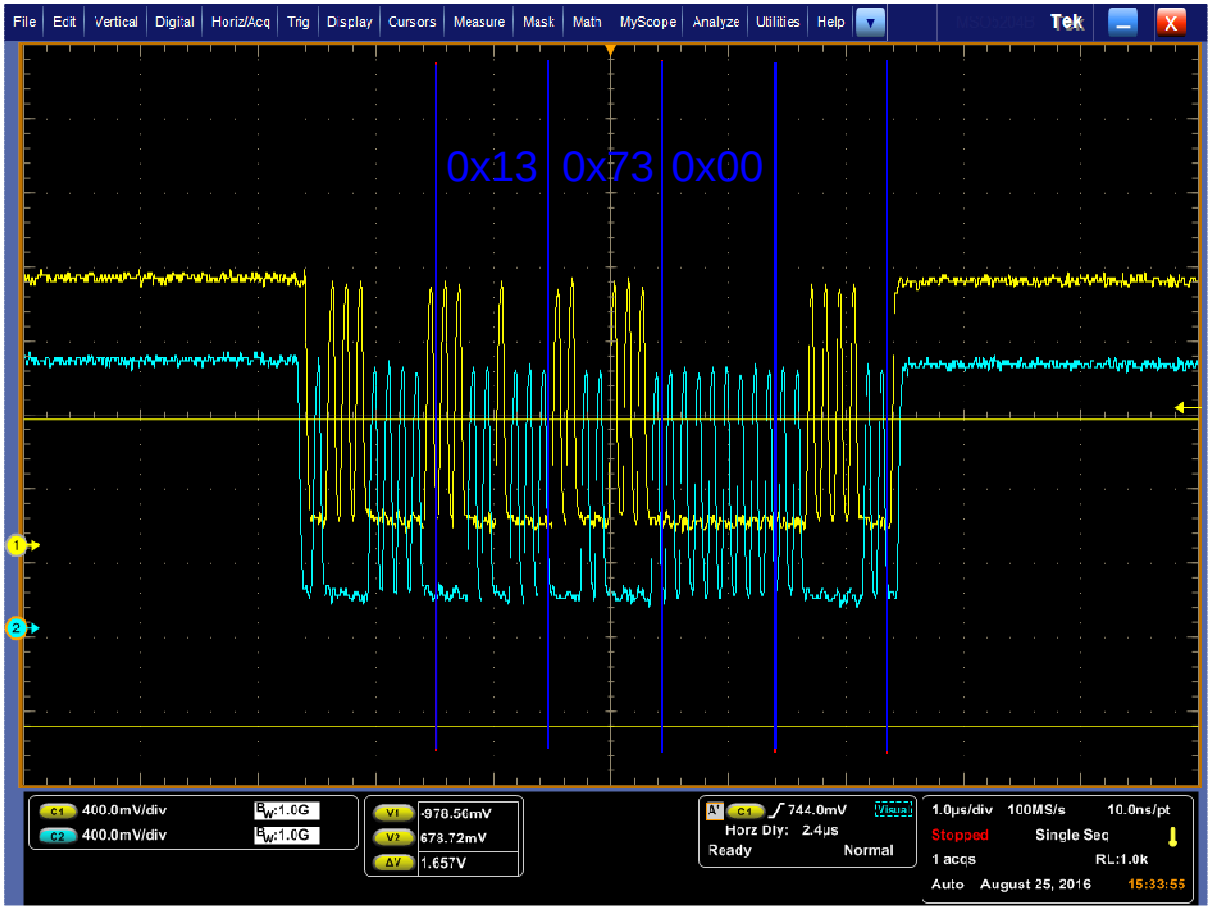
Non Burst Mode

3C DPHY CMD mode output MIPI waveform

- LP command(generic short write, 1 parameter)
- 0x7000b7, 0x720302
- 0x7000bc, 0x720001
- 0x7000bf, 0x723873

TXA_DP0

TXA_DN0



3C DPHY CMD mode output MIPI waveform

- HS Command(generic short write, 1 parameter)
- 0x7000b9, 0x720000
- 0x7000c4, 0x720001
- 0x7000b7, 0x720303
- 0x7000bc, 0x720001
- 0x7000bf, 0x720073

TXA_CP

TXA_DP0

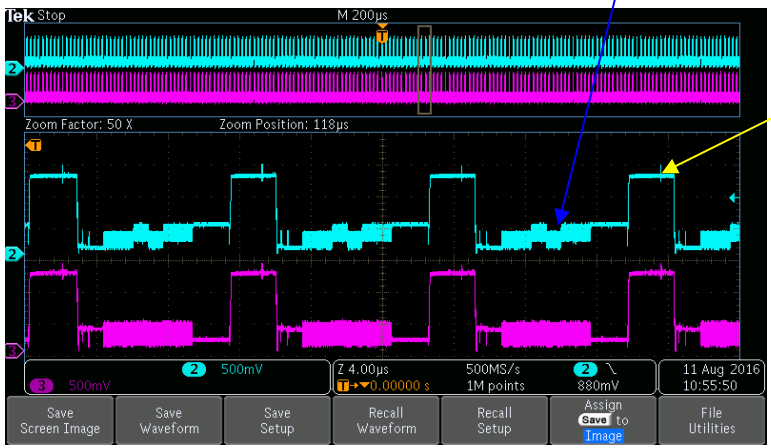
TXA_DN0

3D DPHY Video mode output MIPI waveform

- Video Mode

HS period
(Display time)

LP period
MIPI lanes go to LP at the end of each line



TXA_DP0

TXA_DN0

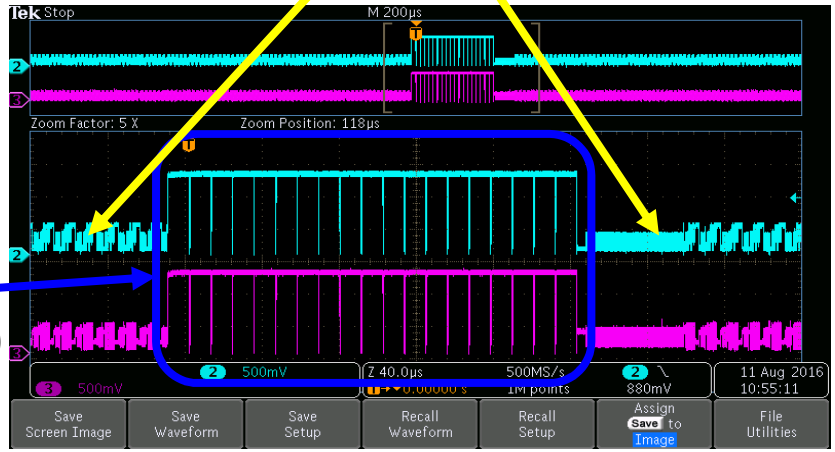
Burst Mode

HS period

Blanking period

TXA_DP0

TXA_DN0



Non Burst Mode

4. Reference Information

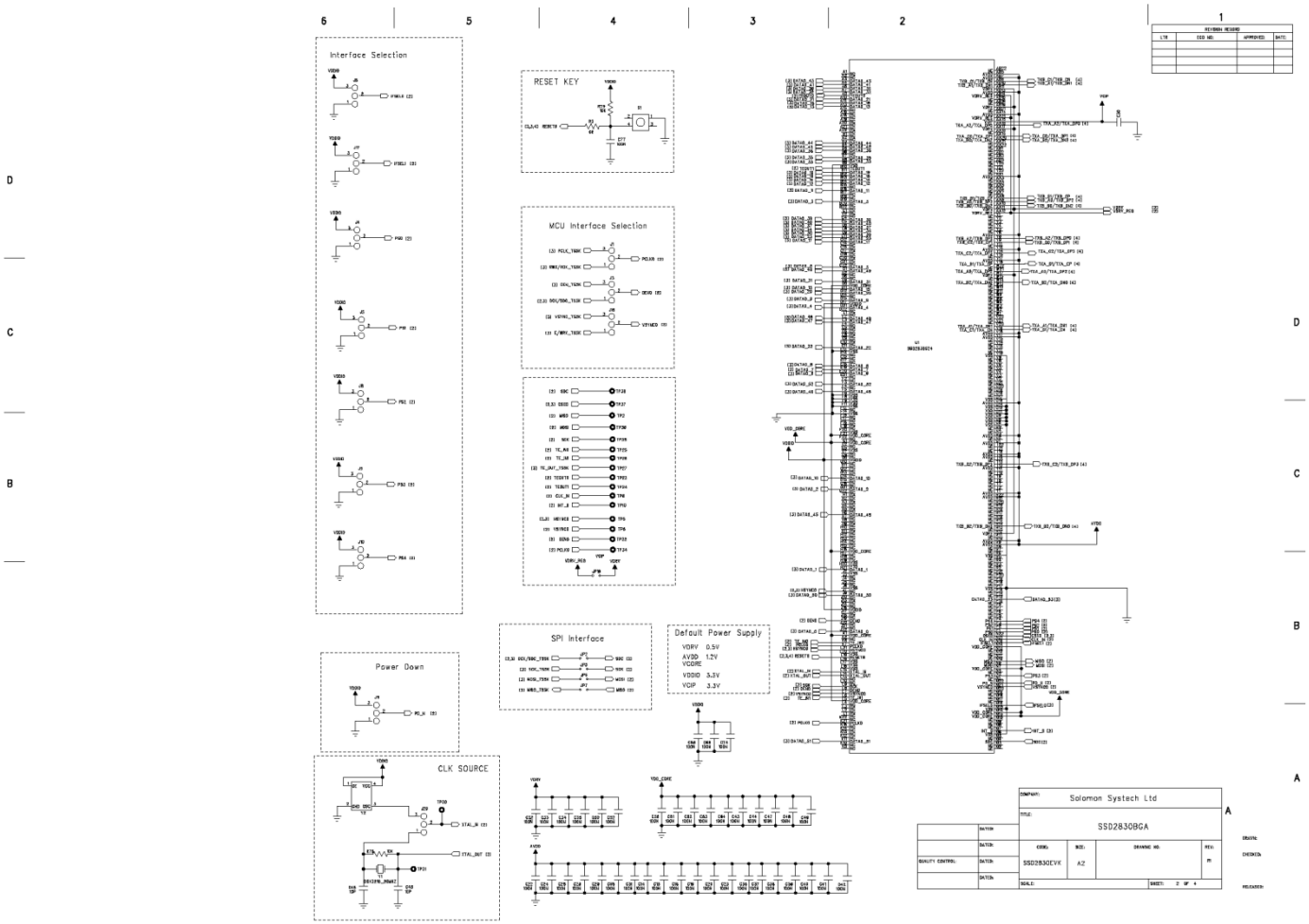
A. Schematic

B. Layout guideline

C. Reference Initial Code

4A Schematic

- SSD2832 reference schematic



4B Layout Guideline - CPHY

- **MIPI lanes**
  - MIPI lane traces should be routed with controlled 50 Ohm Single-ended impedance (+/-15%).
  - Length matching is required.
  - Length of MIPI lane should be as short as possible, no more than 20cm.
  - Bends on traces should be ≥135º. Tighter bends should be avoided.

- **Layer of PCB board**
  - 4 layers is suggested

- **Via of BGA**
  - Via of BGA should be 8mil

4B Layout Guideline - DPHY

- **MIPI lanes**
  - P/N pairs of MIPI should be routed with controlled 100ohm differential impedance(+/-20%)
  - Length matching is required.
  - Length of MIPI lane should be as short as possible, no more than 20cm.
  - The traces length difference should be less than 5mil

- **Layer of PCB board**
  - 4 layers is suggested

- **Via of BGA**
  - Via of BGA should be 8mil

4C Reference Initial Code

- 4 Initial codes in the excel worksheet
  - 24-bit MCU mode
  - 48-bit MCU mode
  - 30-bit DPHY Video mode
  - 30-bit CPHY Video mode

Modify FPB,0,1.8		osc freq: 26MHz
VDDVoltage VDD1,0		panel size: 2560x1600
Modify PUB,0,0x100F90		pll: 1Gbps
IOP EXT_OUT,CLR,0		Pclk: 130Mhz
Modify PUB,0,0x0080		output: DPHY 2DSI 8 lanes
IOP EXT_OUT,SET,0		
Modify PUB,0,0x0100		
IOP EXT_OUT,SET,0		
Modify PUB,0,0x0200		
IOP EXT_OUT,SET,0		
Modify PUB,0,0x0800		
IOP EXT_OUT,SET,0		
Modify PUB,0,0x100000	//sync on	
IOP EXT_OUT,SET,0		
//Modify PUB,0,0x100000	//sync off, check bist mode	
//IOP EXT_OUT,CLR,0		
Modify PUB,0,0x0010		
IOP EXT_OUT,SET,0		
Modify PUB,0,0x0400		
IOP EXT_OUT,SET,0		
Issue		
wait 200ms		
Modify FPB,0,1.8		
VDDVoltage VDD0,0		
Modify FPB,0,1.8		
VDDVoltage VDD1,0		
wait 200ms		
ClipImg 1280, 1600	//2560, 1600	
SetClock 0,50,130/80.0 //set pixel clock		
Modify FPGA,23,0x40	//vsyn -ve	
Modify FPGA,15,3 //set HSync		
Modify FPGA,16,27 //set HBP		
Modify FPGA,17,1280	//set HActive	
Modify FPGA,18,60 //set HFP		
Modify FPGA,19,4 //set VHync		
Modify FPGA,20,4 //set VBP		
Modify FPGA,21,1600 //set VActive		
Modify FPGA,22,12 //set VFP		
//display image		
DrawFigure CLIPSIZE,0,0		
DrawColor IMM,0,0,0		
DrawFigure LOCATE,0,0		
DrawFigure LINE,159,0		
DrawColor IMM,255,0,0		
DrawFigure LOCATE,160,0		
DrawFigure LINE,319,0		
DrawColor IMM,0,255,0		
DrawFigure LOCATE,320,0		
DrawFigure LINE,479,0		
DrawColor IMM,255,255,0		

5. Debug Steps

A. OSC check
B. SPI read back
C. MIPI LP read back
D. MIPI HS read back
E. MIPI video BIST mode

5A. OSC Check

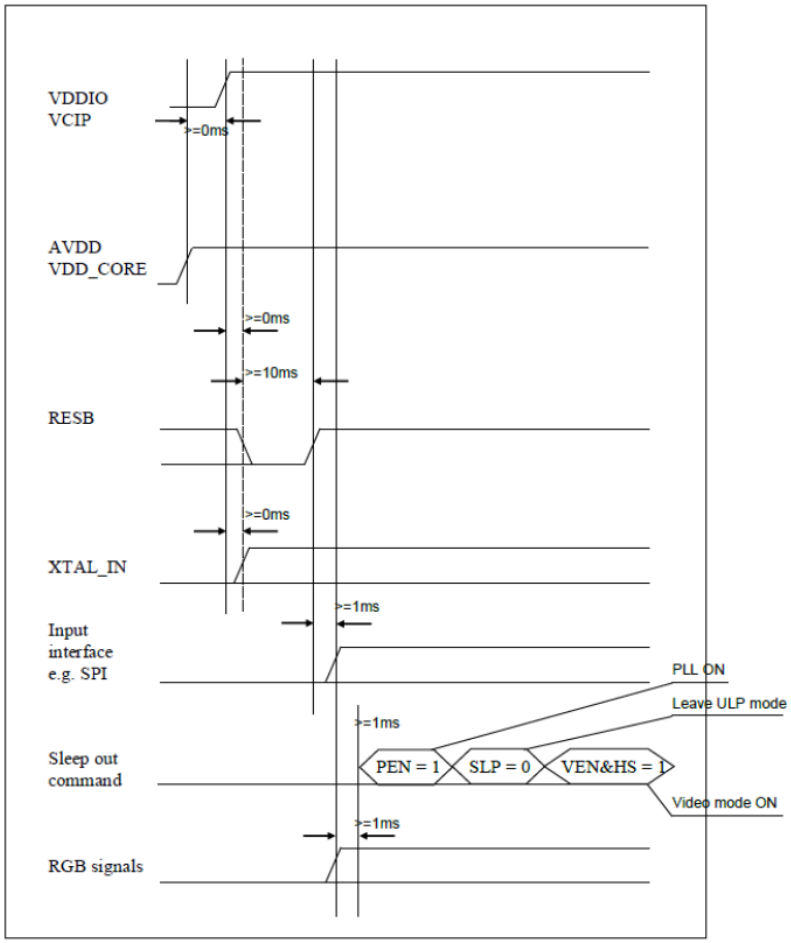
- Both Oscillator and Crystal can be clock solutions
- 5MHz < OSC frequency ≤ 40MHz

- **TE_OUT_0 can output same frequency of the external clock.**

- If oscillator is adopted as clock source, make sure to keep XTAL_OUT pin open

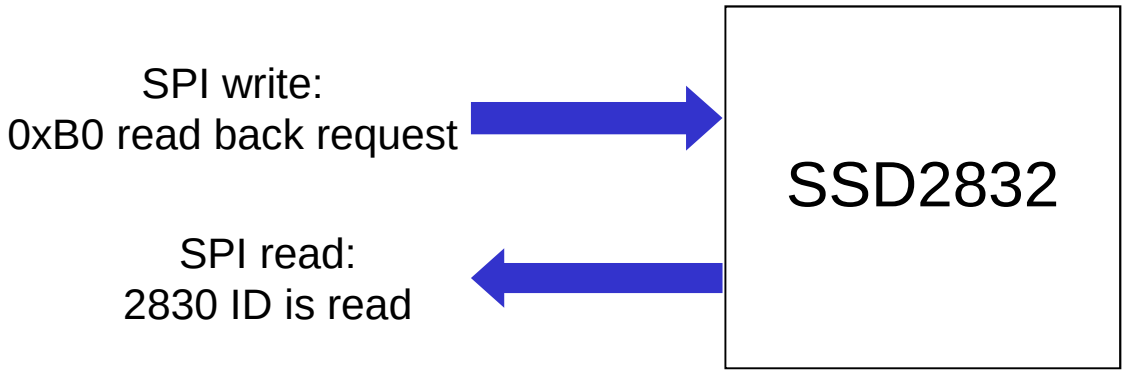
5B. Reset Timing

- Reset “low” pulse width must ≥ 10us
- Initialization of SSD2832 should be after reset high

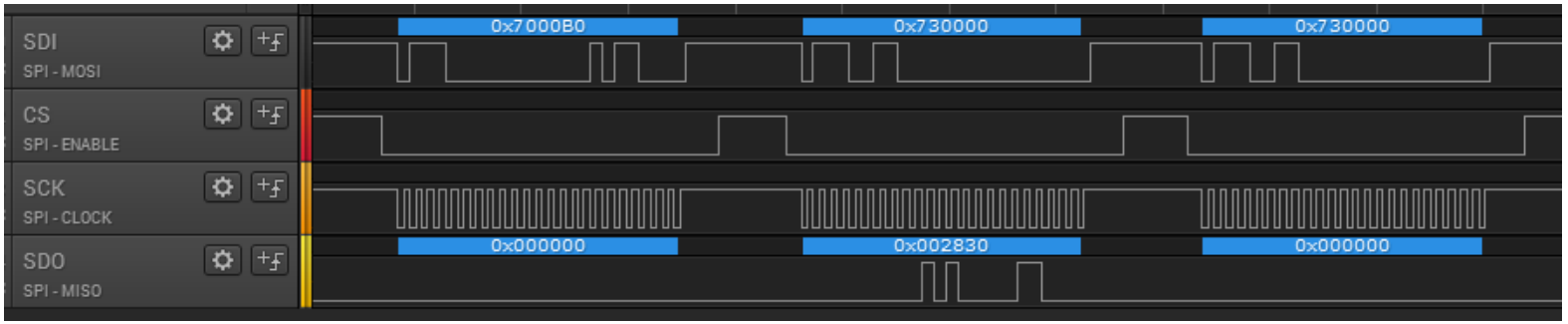


5C. SPI read back

- Read SSD2832 ID(0xB0)



- E.g. 3 wire 24-bit SPI read
- 0x002830 will be returned



5D. MIPI LP read back

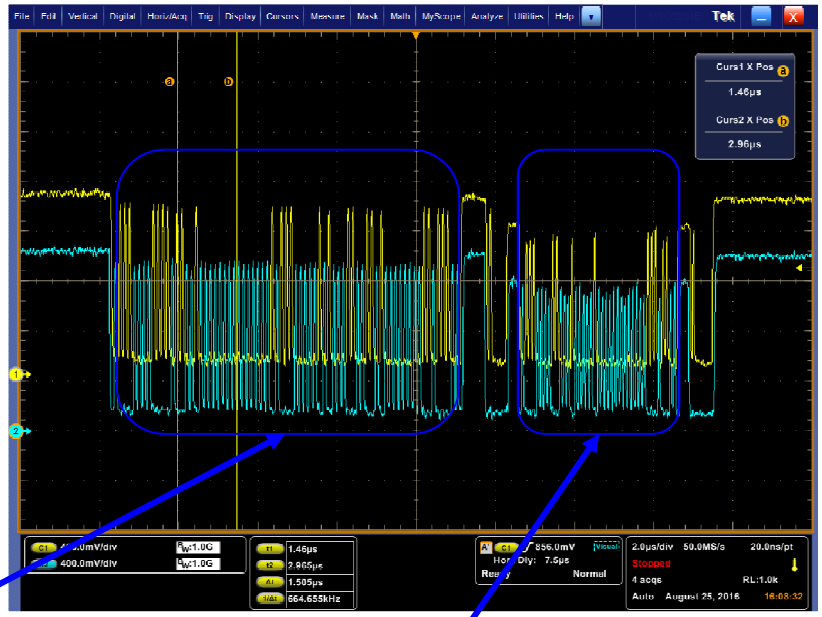
MIPI LP write:
Rx register (BTA)

Tx SSD2832	⇄	Rx Display Driver

MIPI read:
Rx register data

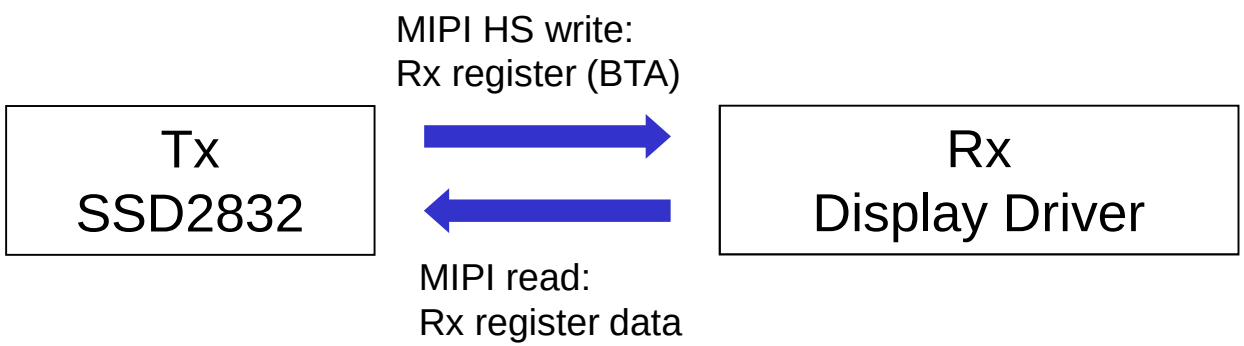
- E.g. LP Generic read back

0x7000b7, 0x720382
0x7000c1, 0x720001
0x7000c0, 0x720001
0x7000bc, 0x720001
0x7000bf, 0x7000b3



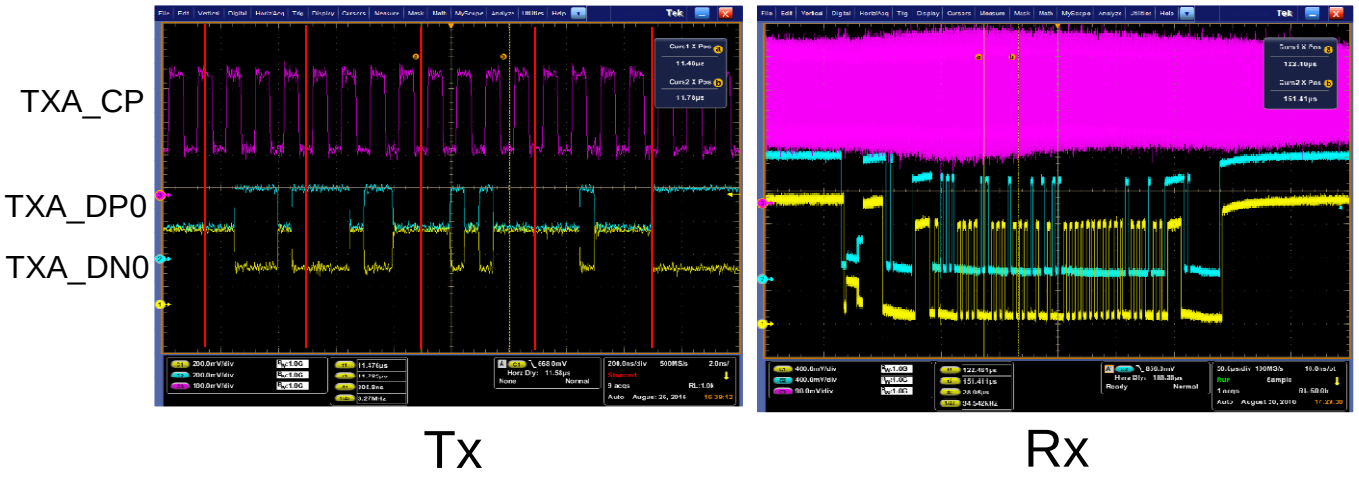
*LP frequency of Tx should match with RX

5E. MIPI HS read back



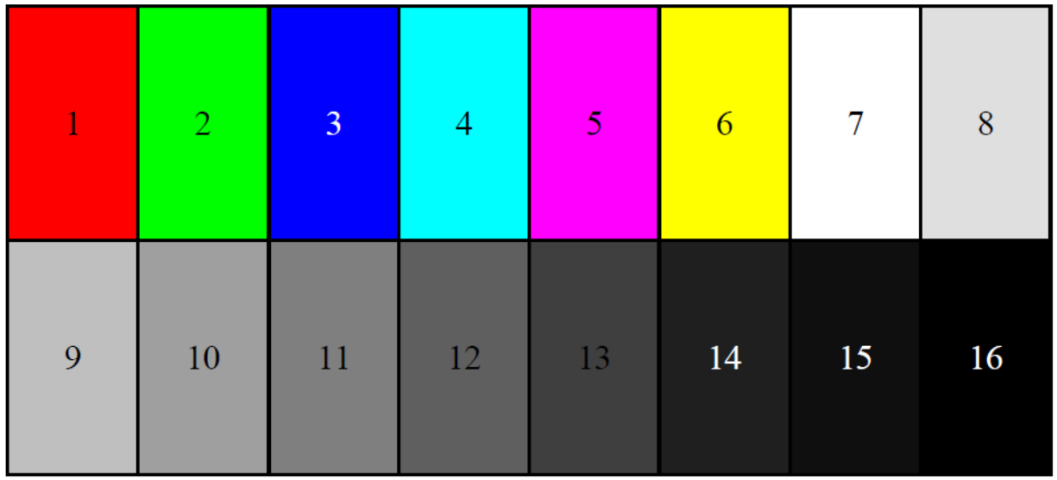
- HS Generic read back

0x7000b9, 0x720000
0x7000c4, 0x720001
0x7000b7, 0x720383
0x7000c1, 0x720001
0x7000c0, 0x720001
0x7000bc, 0x720001



5F. MIPI Video Bist Mode

- Related APB register:
  - 0x5000
  - 0x5004
  - 0x5008
  - 0x500C
  - 0x5010
  - 0x5014
  - 0x5018



Display Pattern of bist mode 0

SSD2832_CPHY_Bist Demo Code.txt

SSD2832_DPHY_Bist Demo Code.txt

6. Q&A

A. No display
   1. No MIPI output
   2. Incorrect MIPI waveform
   3. Correct MIPI waveform
   4. MIPI read error

B. Abnormal display
   1. Fade out display
   2. Display shift
   3. Tearing display
   4. Flickering display
   5. Dotted display

C. V2C mode
   1. Random RAM display only
   2. Shifted display
   3. Cannot update display image

D. DSC mode
   1. Random RAM display only
   2. Incorrect decompression image

6A. No Display

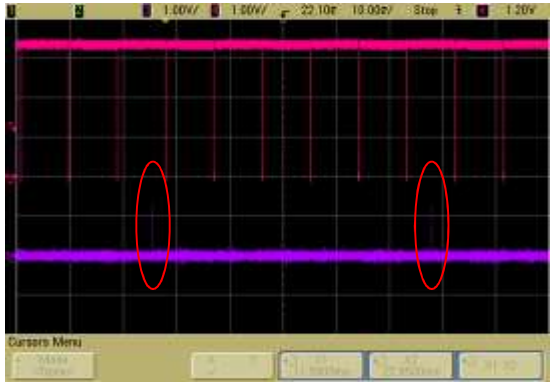
- 1. No MIPI Output
  - check power supply (refer to section 1A)
  - check oscillator (refer to section 1B and 5A)
  - check SPI interface (refer to section 1C)
  - try SPI read (refer to section 5C)
  - check resect timing (refer to section 5B)

6A. No Display

- 2. Incorrect MIPI waveform
  - Check whether PLL is greater than min. PLL requirement (refer to section 2A)
  - Make sure PLL ≤ 1.5G**bps** for **D**PHY and 1.5G**sps** for **C**PHY

6A. No Display

- 3. No display even have correct MIPI waveform
  - Check whether MIPI video can sync with VSYNC



  - Check porch setting, display size(refer to section 2C and 2D)
  - Check Pclk / Hsync / Vsync polarity(refer to section 1D)
  - Several MIPI Rx ICs do not have internal oscillator, so they need MIPI clock for normal operation including generic/DCS command. 0xB7 bit-1 “CKE” must be “1” to enable HS clock output all the time.
  - Try Bist Mode(refer to section 5E)

6A. No Display

- 4. MIPI read error
  - SoT Error
    - Check prepare / zero timing
  - Sot Sync Error
    - Check prepare / zero timing
  - EoT Sync Error
    - Check EOT timing
  - Peripheral Timeout Error
    - Check LP frequency, need to match with panel
  - ECC Error, single-bit(detected and corrected)
    - Lane quality issue, check MIPI lane connection or slow down PLL
  - ECC Error, multi-bit(detected, not corrected)
    - Lane quality issue, check MIPI lane connection or slow down PLL
  - DSI Protocol Violation
    - Check MIPI lane connection e.g. Open circuit? Lane swapped?

6B. Abnormal display

- 1. Fade out display
  - Check video input connection, discontinue of Hsync / Vsync / DEN / PCLK will cause fading out display.
  - Check MIPI link quality, packet dropped will cause this issue
    - Can try to decrease both PCLK and PLL for debug

Process of fading out

6B. Display shift

- 2. Display shift
  - Check VSYNC / HSYNC setting(refer to section 2C)
  - Check polarity and porch setting(refer to section 1D and 2D)

6B. Abnormal Display

- 3. Tearing display
  - Pixel clock is too fast or PLL is too slow will cause such tearing effect.

Tearing effect

6B. Abnormal Display

- 4. Flickering display
  - Check PLL frequency which maybe too fast(refer to section 2A)

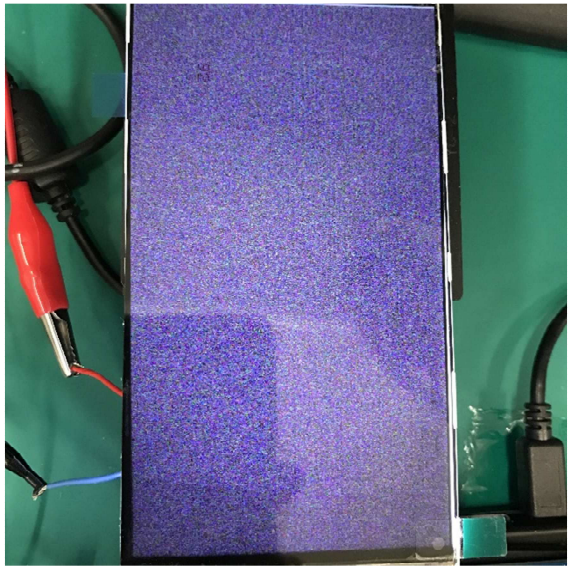
6B. Abnormal Display

- 5. Dotted display
  - Noise from PCLK / HSYNC / VSYNC. Please reduce the noise or adjust delay time for PCLK.

red / blue / green dots

6C. V2C mode

- 1. Random RAM display only
  - Check whether the panel is in CMD mode
  - Check whether MIPI lane is in HS mode
  - Check V2C initialization sequence(follow section 2H, page__)
  - Check whether PLL is too slow(refer to section 2A)
  - Check HS read back from panel



6C. V2C mode

- 2. Shift display
  - Check RAM size related settings
    - Related command : 0xBCh, 0xBDh, 0xBEh
  - Check RAM Size of the panel
    - Related command: 0x2Ah, 0x2Bh of panel register

6C. V2C mode

- 3. Cannot update display image
  - User is recommended to switch off V2C periodically (e.g. after 2-3 frames of conversion) as there is a built-in HS timeout (refer to section 2H, page__)
    - Send V2C ON command in order to update display image(refer to section 2H, page__)

6D. DSC mode

- 1. Random RAM display only
  - Check whether command mode output is enabled
    - Make sure the correct settings of 0xBCh, 0xBDh and 0xBE
  - Check whether the HS communication has no error
    - Make sure the correct HS read from panel

6D DSC mode

- 2. Incorrect decompression image
  - Check whether compression mode packet is enabled(refer to section 2G)
    - Enable bit-12 and bit-6 of 0xB7
  - Check whether RGB input signal is correct
    - Make sure the connection of all data pins
  - Check whether panel initial code is correct
    - Make sure panel compression mode is enabled

Thank You