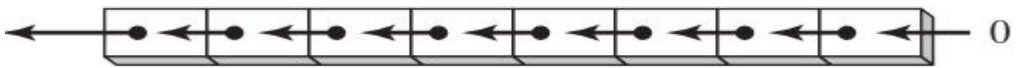
Shifting

Bit ***Shifting*** means to move bits left or right inside an operand.

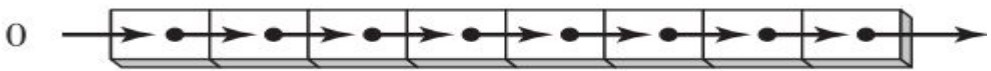
There are two ways to shift the bits in an operand

1. ***Logical shift***: fills the newly created bit position with zero



SHL (shift left)

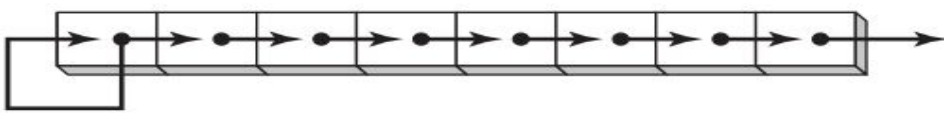
SHR (shift right)



2. ***Arithmetic shift***: fills the newly created bit position is with a copy of the sign bit

(shift *arithmetic* right preserves the sign bit)

shift *arithmetic* right



note: 'shift arithmetic left' works the same way as 'logical shift left', we can simply say Shift Left

Shifting

Arithmetic right shift: shift all bits to the right
preserves the sign bit
fills the MSB with a copy of the original sign bit

Right Shift = Division by powers of 2

$$a \gg n = \left\lfloor \frac{a}{2^n} \right\rfloor$$

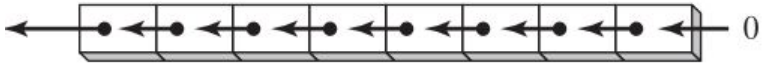
```
user@host $ cat shift_s.py
num = 128
for i in range(10):
    print( num )
    num =  num >> 1


user@host $ python shift_s.py
128
64
32
16
8
4
2
1
0
0
user@host $
```

source: https://realpython.com/python-bitwise-operators/

Shifting

Shift Left:



Shifting any operand left by *n* bits multiplies the operand by 2^n.

Example: shifting the integer 5 left by 1 bit yields the product of $5 * 2^1 = 10$:

Left Shift = multiplication by powers of 2

```
user@host $ cat shift.py
num = 5
print( num )
print( num << 1 )
print( num << 2 )
print( num << 3 )


user@host $ python shift.py
5
10
20
40
user@host $
```

Truth Tables

Order of Precedence

Precedence	Name	Operator	C++
1	Parentheses	()	()
2	NOT	′	!
3	AND	×	&&
4	XOR	⊕	N/A
5	OR	+	||

p	p′
0	1
1	0

NOT

Can only ever be 2 inputs. [0,1]

Number of inputs = x
Number of outputs = y

$$y = 2^n$$

p	q	p × q
0	0	0
0	1	0
1	0	0
1	1	1

AND

Number of inputs = 2
Number of outputs = 4

$4 = 2^2$

p	q	r	p × q × r
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

AND

Number of inputs = 3
Number of outputs = 8

$8 = 2^3$

p	q	p + q
0	0	0
0	1	1
1	0	1
1	1	1

OR

Number of inputs = 2
Number of outputs = 4

$4 = 2^2$

p	q	r	p + q + r
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

OR

Number of inputs = 3
Number of outputs = 8

$8 = 2^3$

p	q	p ⊕ q
0	0	0
0	1	1
1	0	1
1	1	0

XOR

Number of inputs = 2
Number of outputs = 4

$4 = 2^2$

p	q	r	p ⊕ q ⊕ r
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

XOR

Number of inputs = 3
Number of outputs = 8

$8 = 2^3$

p	q	r	p × q + r
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Try for yourself #1

Number of inputs = ?
Number of outputs = ?

$? = 2^{?}$

p	q	r	p × (q + r)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Try for yourself #2

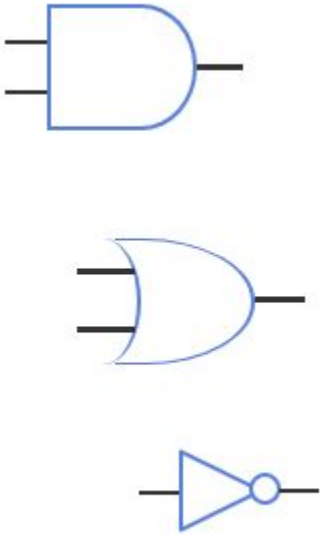
Number of inputs = ?
Number of outputs = ?

$? = 2^{?}$

Building blocks: transistors & logic gates

Building blocks

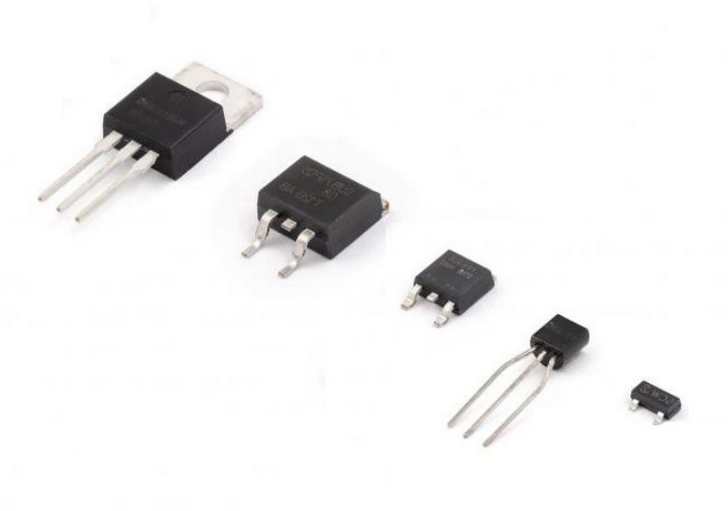
Integrated Circuit
(IC)



logic gates

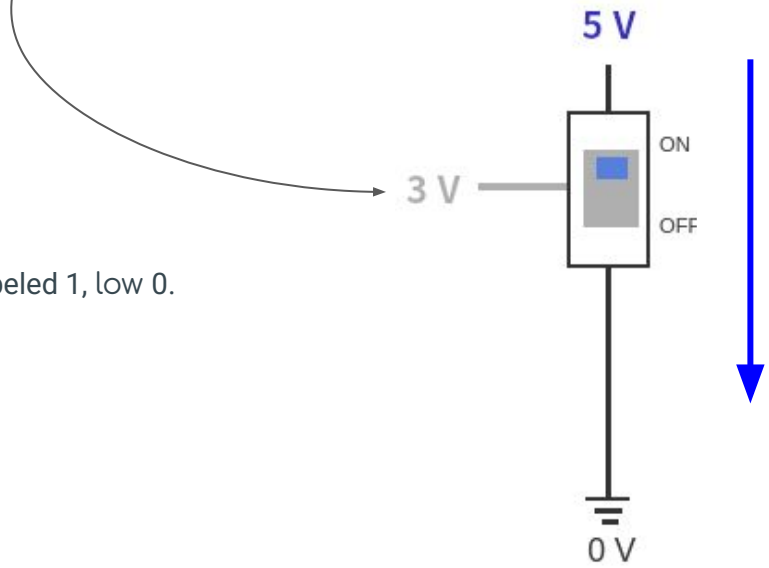
transistors

transistors

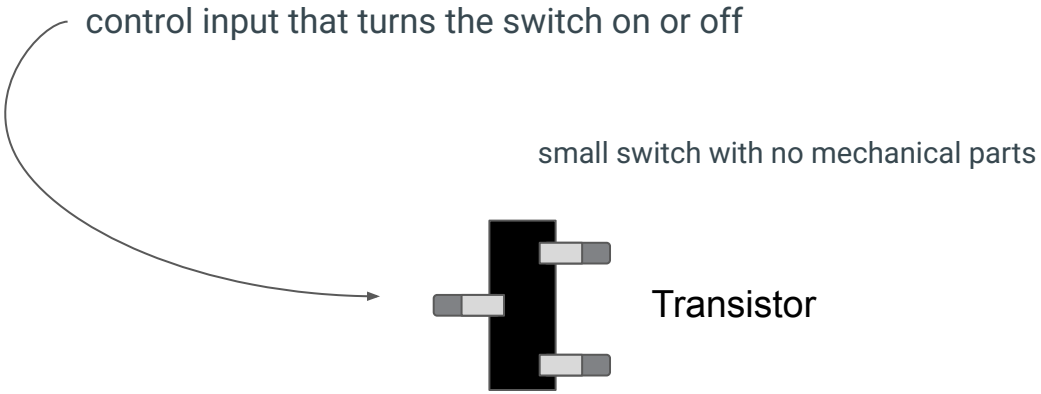


pushbutton - type of switch

instead of a finger to push the button
control input that turns the switch on or off



A ***digital circuit*** has voltages that are treated as either *high* or low, high is labeled 1, low 0.



CMOS (**C**omplementary **M**etal-**O**xide-**S**emiconductor) technology uses pMOS and nMOS transistors to implement: microprocessors, microcontrollers, BIOS chips, and other digital circuits. CMOS technology is also used for image sensors.

Definition

nMOS conducts when control input is **1**

pMOS conducts when control input is 0.

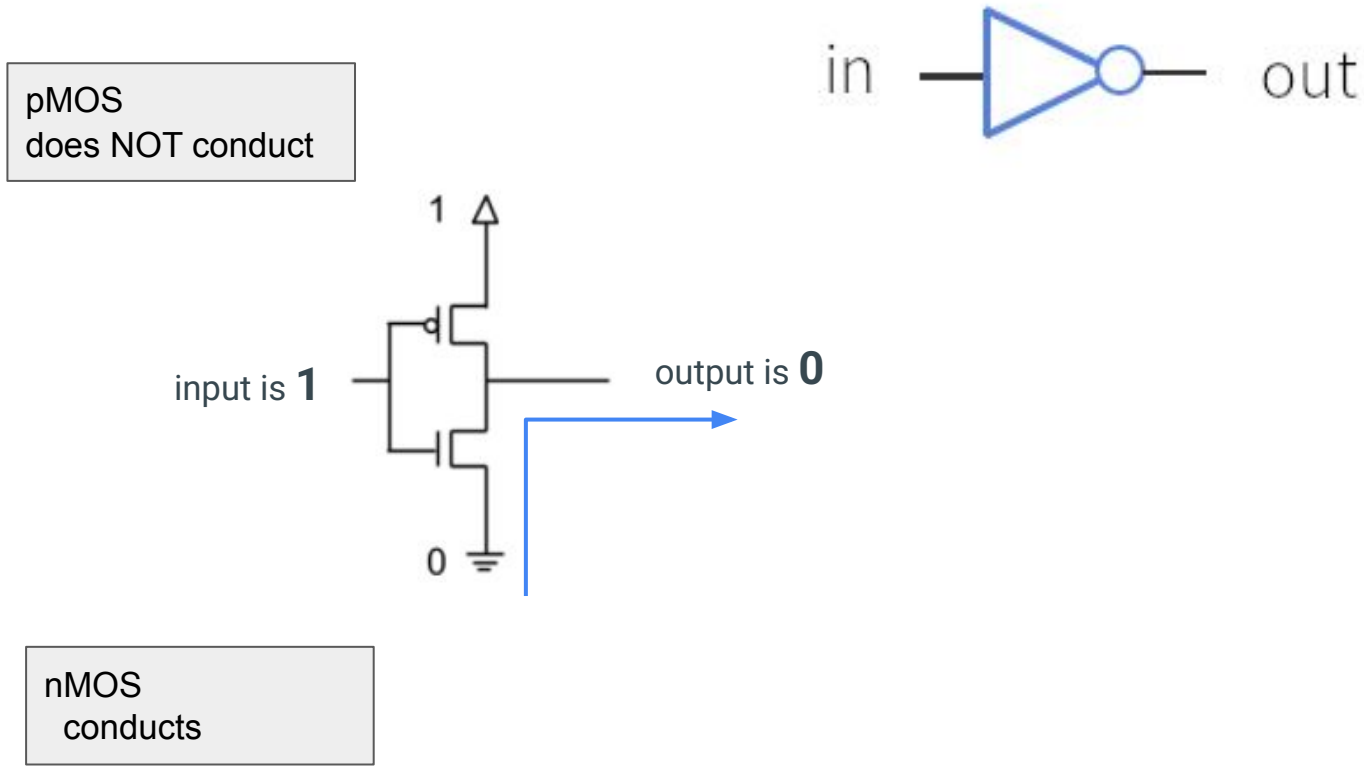
nMOS and pMOS transistors

CMOS

Gates:

NOT, NAND, AND, NOR, OR, XOR, XNOR

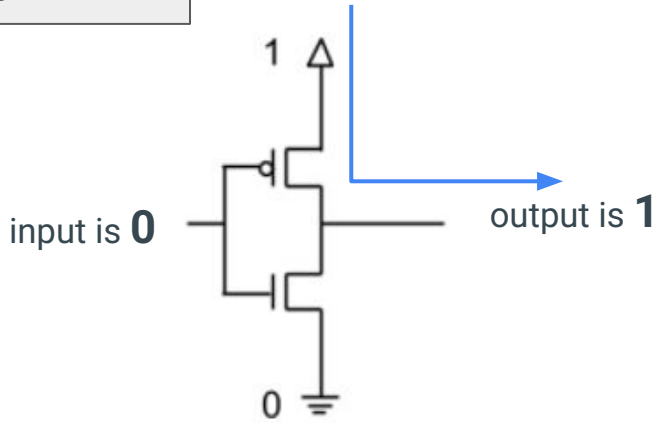
NOT Gate (inverter)



Inverter

NOT gate

pMOS
conducts

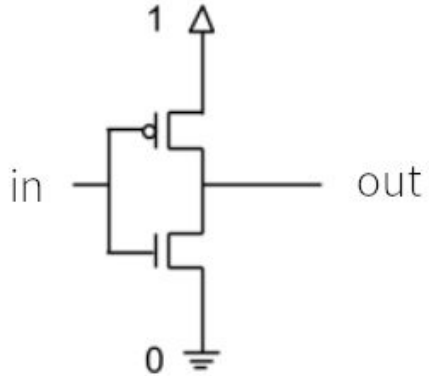


nMOS
does NOT conduct

Inverter

NOT gate

in	out
0	1
1	0



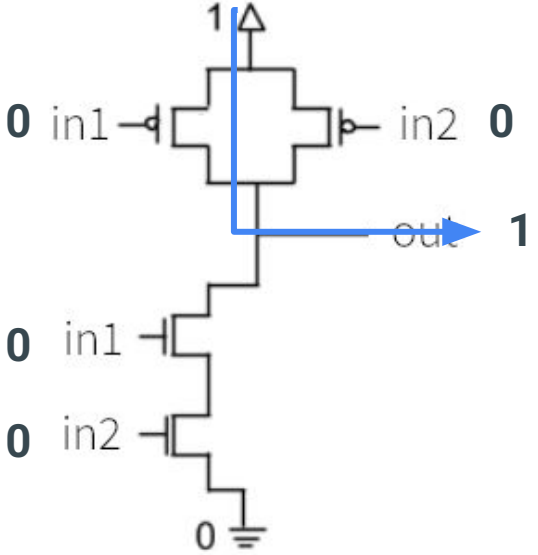
Inverter

NOT gate

NAND Gate

in1	in2	out
0	0	1
0	1	1
1	0	1
1	1	0

pMOS
conducts



nMOS
does NOT conduct

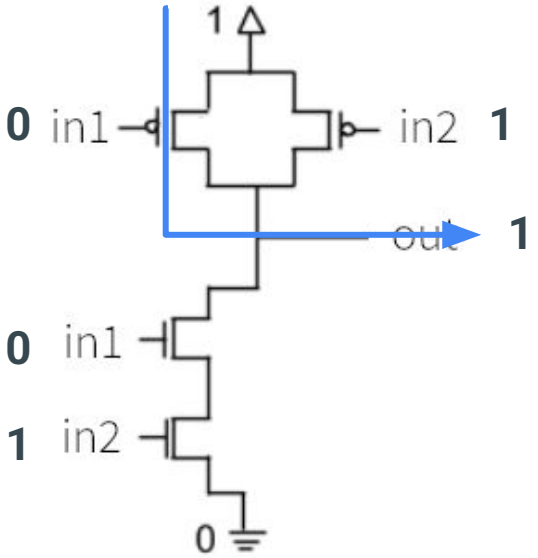
NAND Gate

in1	in2	out
0	0	1
0	1	1
1	0	1
1	1	0

⇦

pMOS conducts in1

pMOS does NOT conduct in2



nMOS conduct in2

nMOS does NOT conduct in1

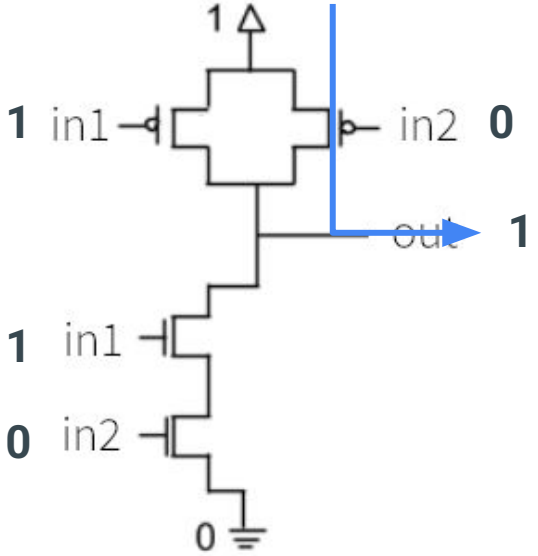
NAND Gate

in1	in2	out
0	0	1
0	1	1
1	0	1
1	1	0

⇦

pMOS does NOT conduct in1

pMOS conduct in2



nMOS does NOT conduct in2

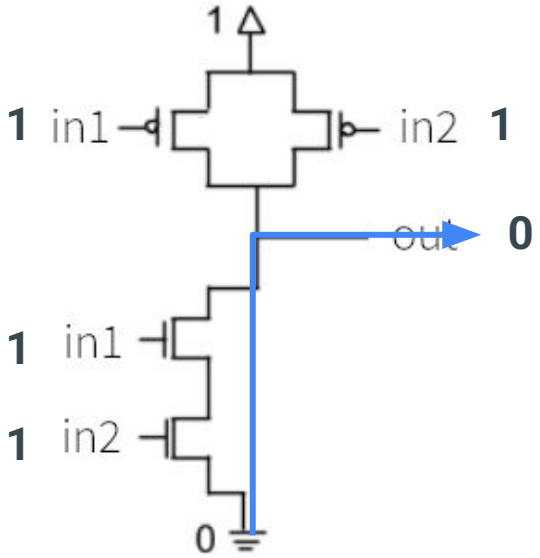
nMOS conducts in1

NAND Gate

in1	in2	out
0	0	1
0	1	1
1	0	1
1	1	0

⇦

pMOS
does NOT conduct



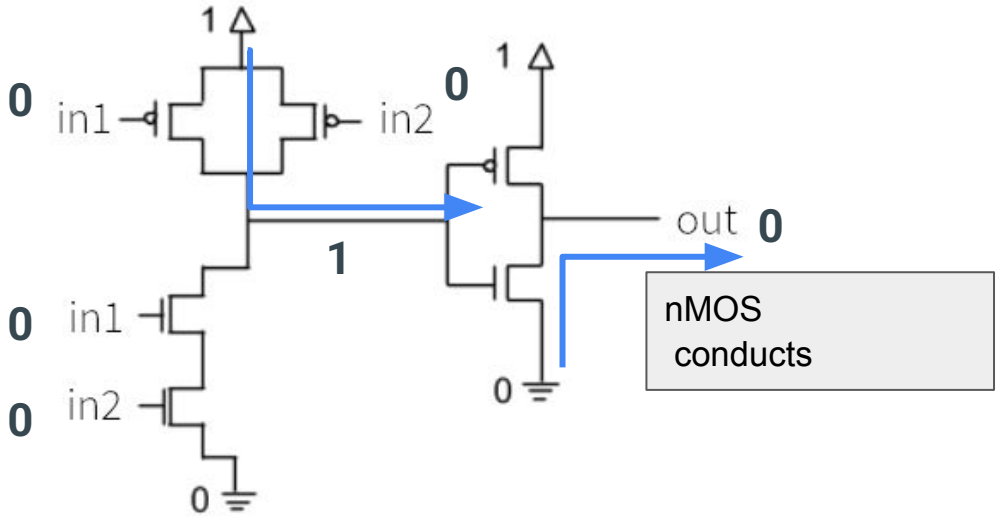
nMOS
conducts

NAND Gate

AND Gate

in1	in2	out
0	0	0
0	1	0
1	0	0
1	1	1

pMOS conducts



nMOS conducts

nMOS does NOT conduct

AND Gate

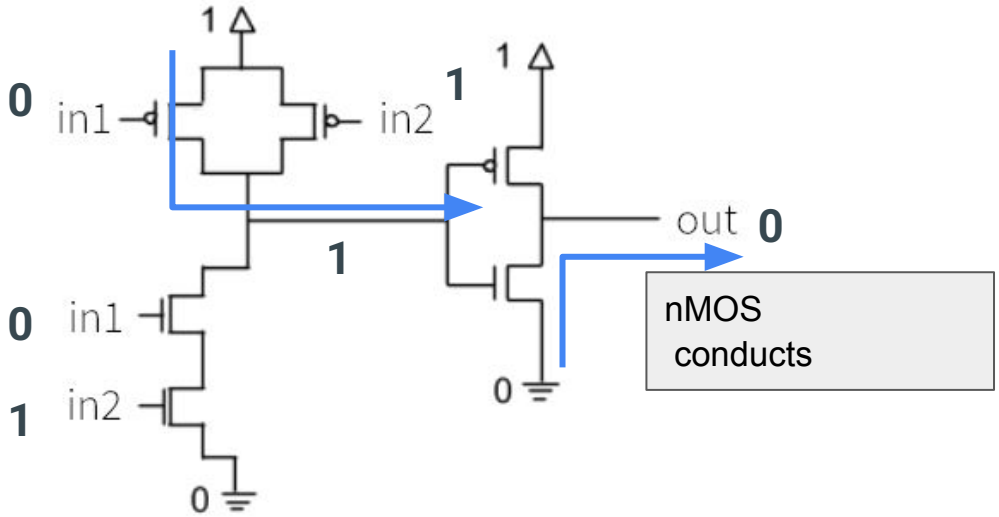
AND gate is built by inverting the output of a NAND gate

(due to physics: pMOS is a poor conductor of 0's, and nMOS a poor conductor of 1's)

in1	in2	out
0	0	0
0	1	0
1	0	0
1	1	1

⇦

pMOS
conducts for in1



nMOS
conducts

nMOS does NOT
conduct for in1

AND Gate

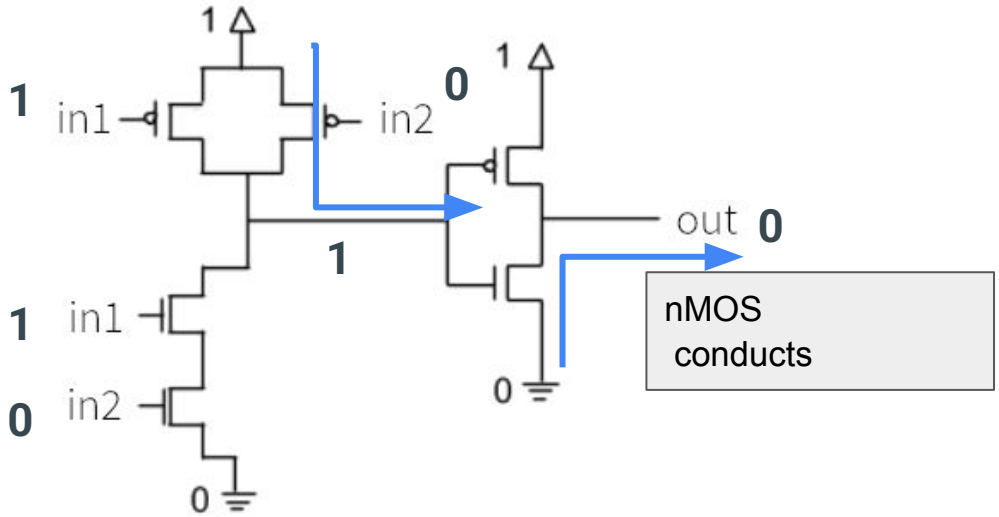
AND gate is built by inverting the output of a NAND gate

(due to physics: pMOS is a poor conductor of 0's, and nMOS a poor conductor of 1's)

in1	in2	out
0	0	0
0	1	0
1	0	0
1	1	1

⇦

pMOS
conducts for in2



nMOS
conducts

nMOS does NOT
conduct for in2

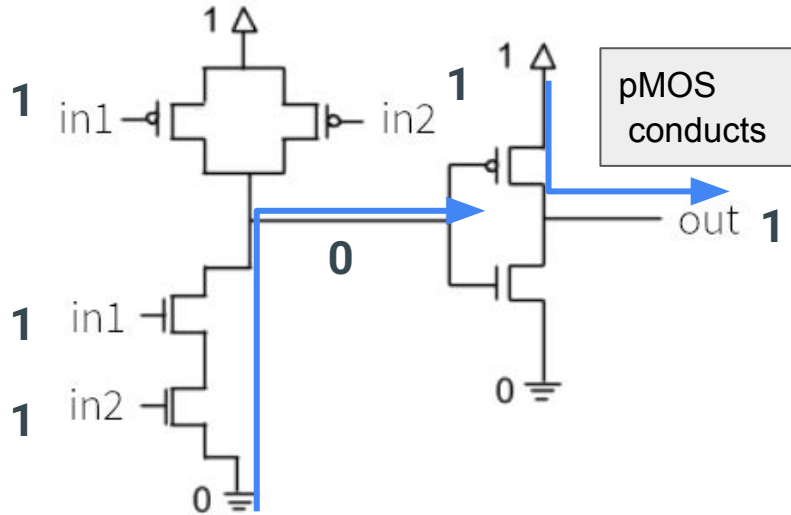
AND Gate

AND gate is built by inverting the output of a NAND gate

(due to physics: pMOS is a poor conductor of 0's, and nMOS a poor conductor of 1's)

in1	in2	out
0	0	0
0	1	0
1	0	0
1	1	1 ⇦

pMOS
does NOT conduct



pMOS
conducts

nMOS
conducts

AND Gate

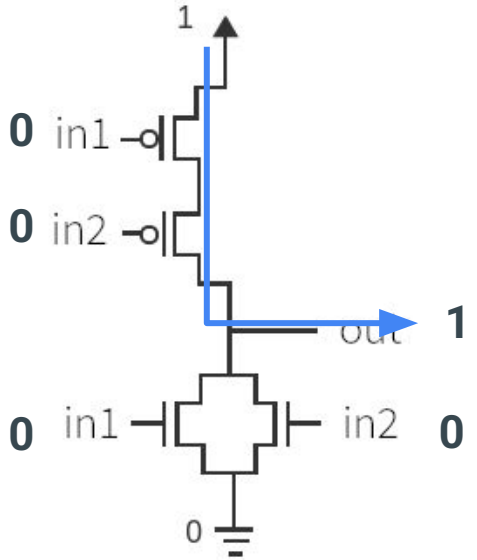
AND gate is built by inverting the output of a NAND gate

(due to physics: pMOS is a poor conductor of 0's, and nMOS a poor conductor of 1's)

NOR Gate

in1	in2	out
0	0	1
0	1	0
1	0	0
1	1	0

pMOS conducts



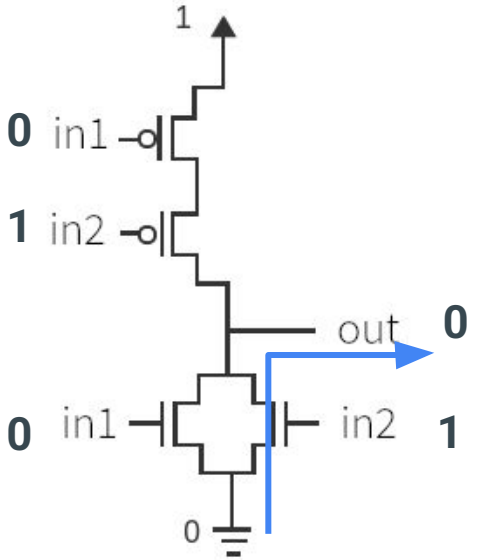
nMOS does NOT conduct

NOR Gate

in1	in2	out
0	0	1
0	1	0
1	0	0
1	1	0

⇦

pMOS does NOT conduct for in2



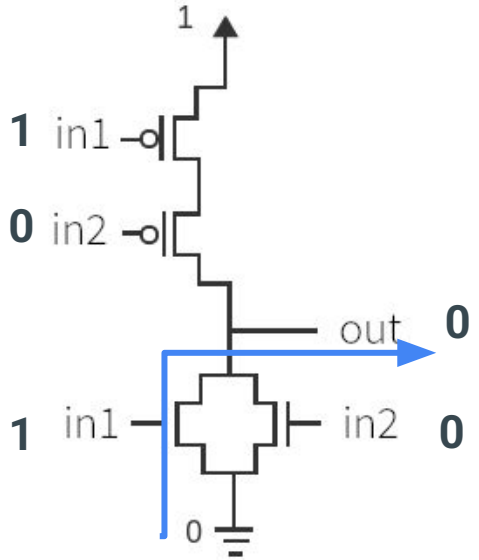
nMOS conducts for in2

NOR Gate

in1	in2	out
0	0	1
0	1	0
1	0	0
1	1	0

⇦

pMOS does NOT conduct for in1

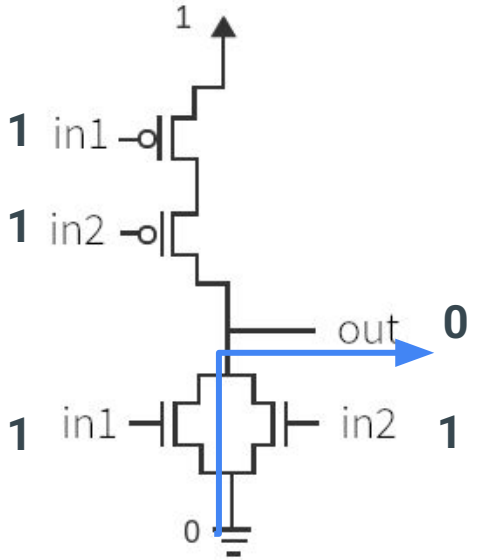


nMOS conducts for in1

NOR Gate

in1	in2	out
0	0	1
0	1	0
1	0	0
1	1	0 ⇦

pMOS
does NOT conduct

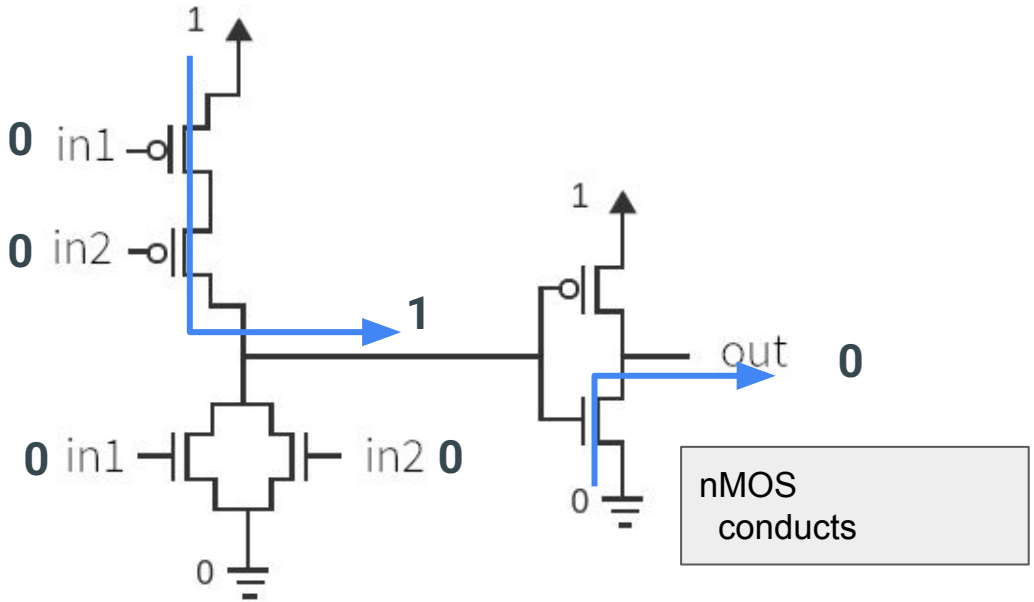


nMOS
conducts

NOR Gate

OR Gate

in1	in2	out
0	0	0
0	1	1
1	0	1
1	1	1



OR Gate

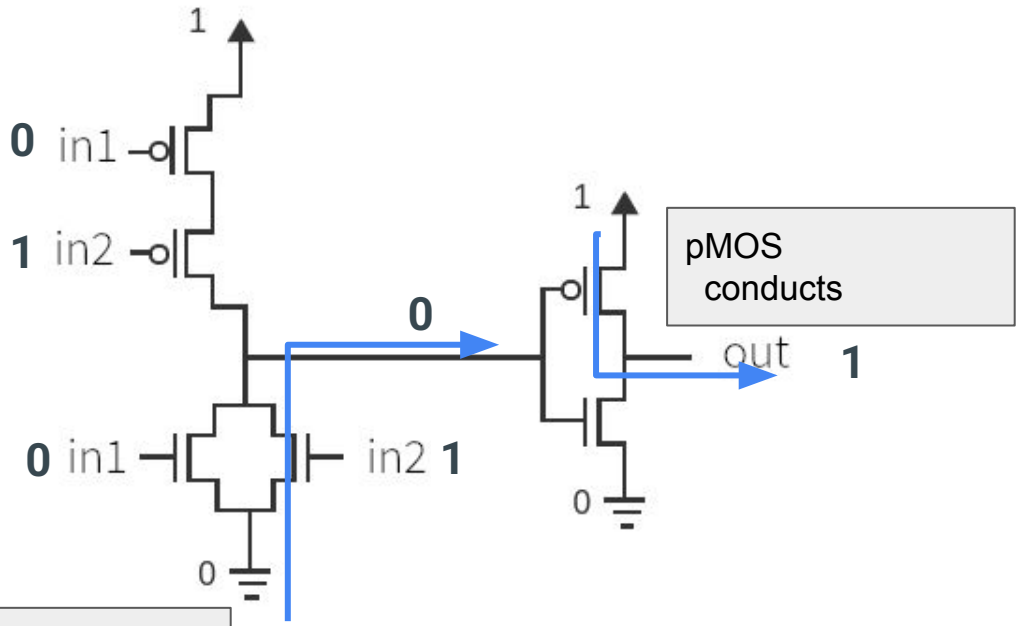
OR gate is built by inverting the output of a NOR gate

(due to physics: pMOS is a poor conductor of 0's, and nMOS a poor conductor of 1's)

in1	in2	out
0	0	0
0	1	1
1	0	1
1	1	1

⇦

pMOS does NOT conduct for in2



nMOS conducts for in2

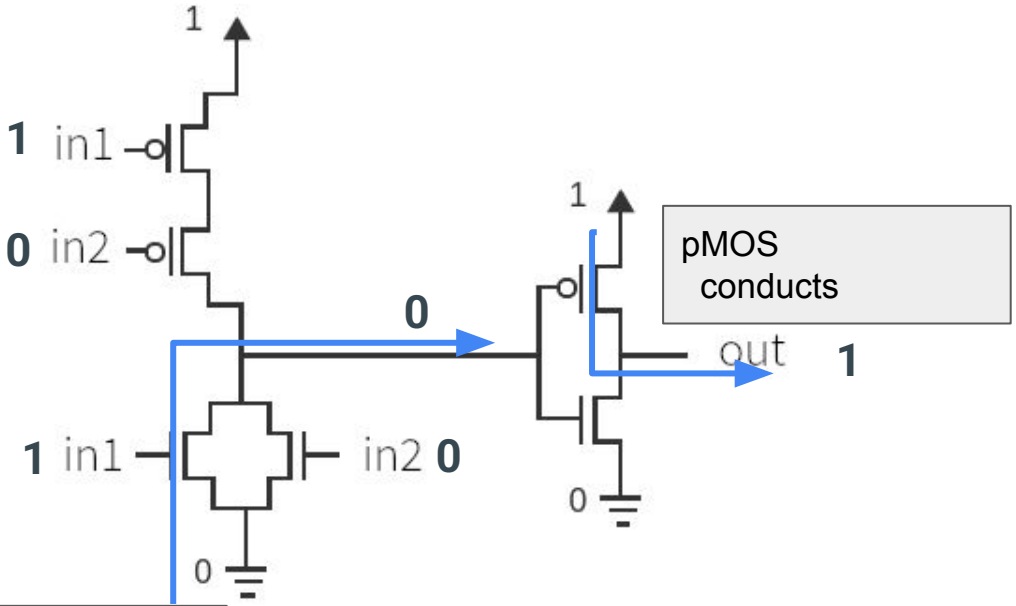
OR Gate

OR gate is built by inverting the output of a NOR gate

(due to physics: pMOS is a poor conductor of 0's, and nMOS a poor conductor of 1's)

in1	in2	out
0	0	0
0	1	1
1	0	1
1	1	1

pMOS does NOT conduct for in1



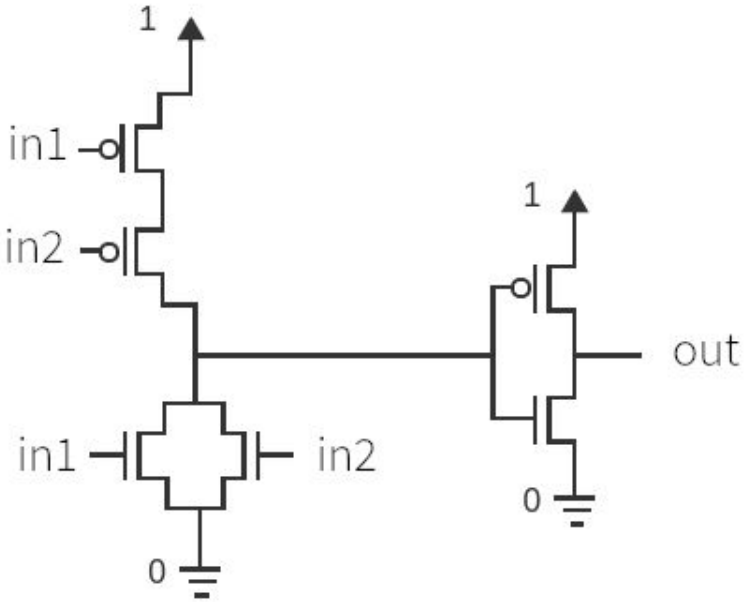
nMOS conducts for in1

OR Gate

OR gate is built by inverting the output of a NOR gate

(due to physics: pMOS is a poor conductor of 0's, and nMOS a poor conductor of 1's)

in1	in2	out
0	0	0
0	1	1
1	0	1
1	1	1



OR Gate

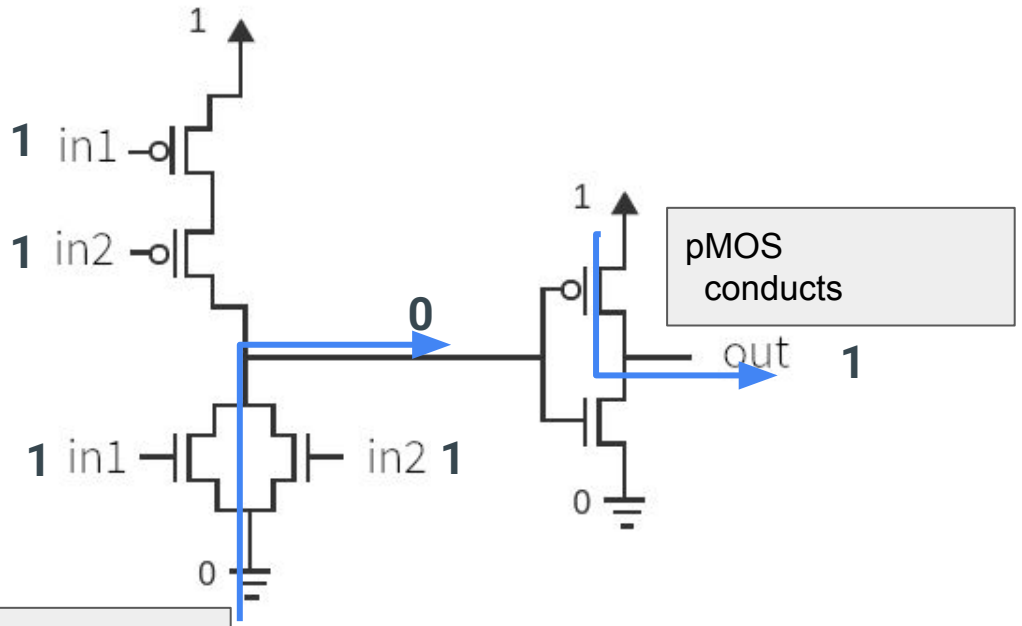
OR gate is built by inverting the output of a NOR gate

(due to physics: pMOS is a poor conductor of 0's, and nMOS a poor conductor of 1's)

in1	in2	out
0	0	0
0	1	1
1	0	1
1	1	1

⇦

pMOS does NOT conduct



nMOS conducts

OR Gate

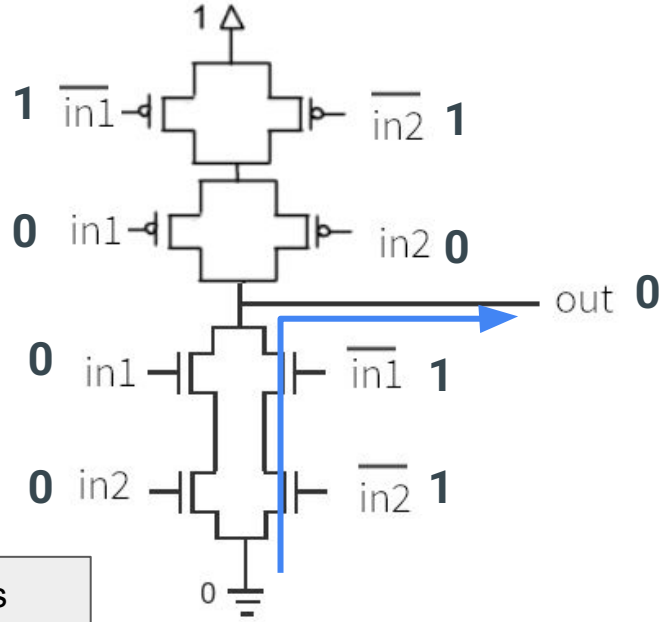
OR gate is built by inverting the output of a NOR gate

(due to physics: pMOS is a poor conductor of 0's, and nMOS a poor conductor of 1's)

XOR Gate (Exclusive-OR)

in1	in2	out
0	0	0 ⇦
0	1	1
1	0	1
1	1	0

pMOS does NOT conduct $\overline{in1}$, $\overline{in2}$



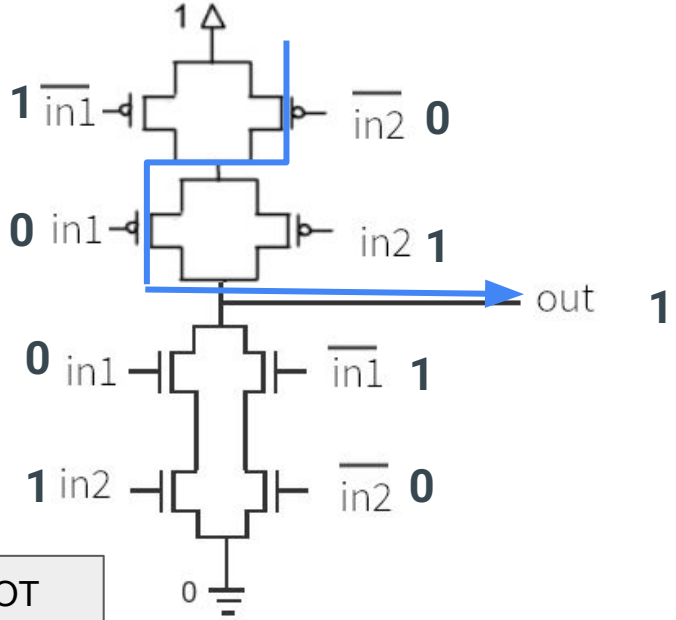
nMOS conducts for $\overline{in2}$, $\overline{in1}$

XOR Gate

in1	in2	out
0	0	0
0	1	1 ⇦
1	0	1
1	1	0

pMOS does NOT conduct $\overline{in1}$, in2

pMOS conducts in1, $\overline{in2}$



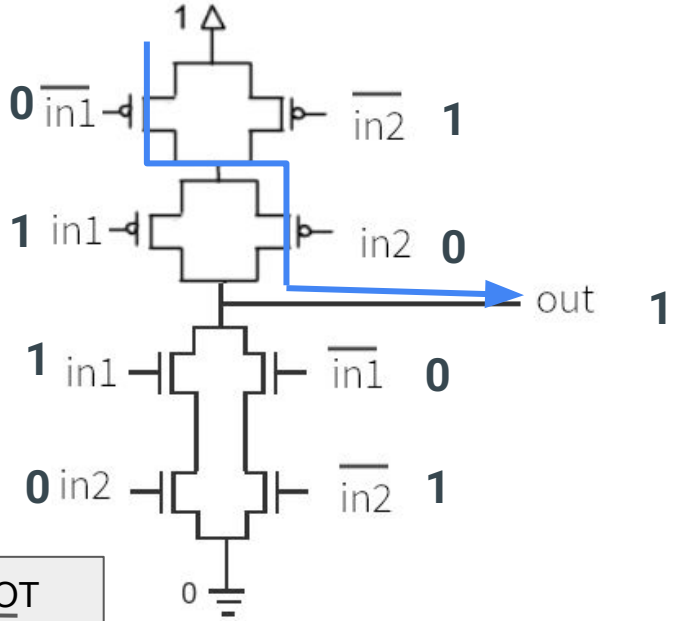
nMOS does NOT conduct $\overline{in2}$, in1

XOR Gate

in1	in2	out
0	0	0
0	1	1
1	0	1 ⇦
1	1	0

pMOS does NOT conduct in1, $\overline{in2}$

pMOS conducts $\overline{in1}$, in2

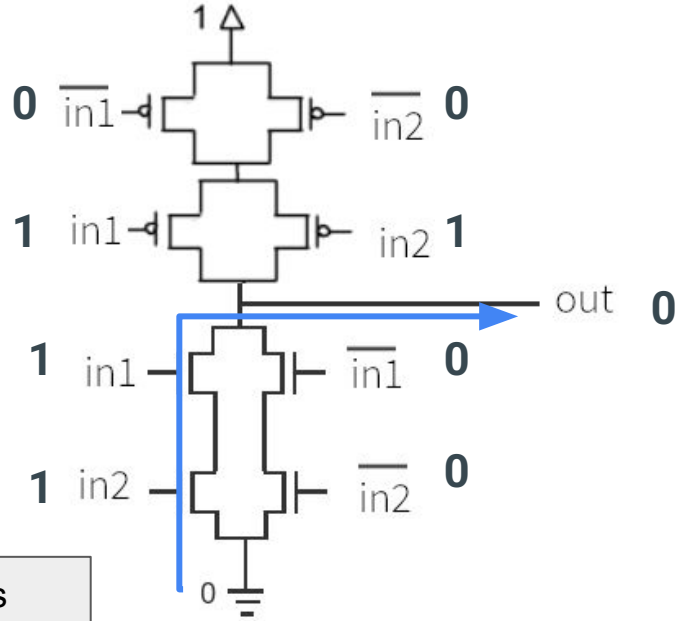


nMOS does NOT conduct in2, $\overline{in1}$

XOR Gate

in1	in2	out
0	0	0
0	1	1
1	0	1
1	1	0 ⇦

pMOS does NOT conduct in1, in2



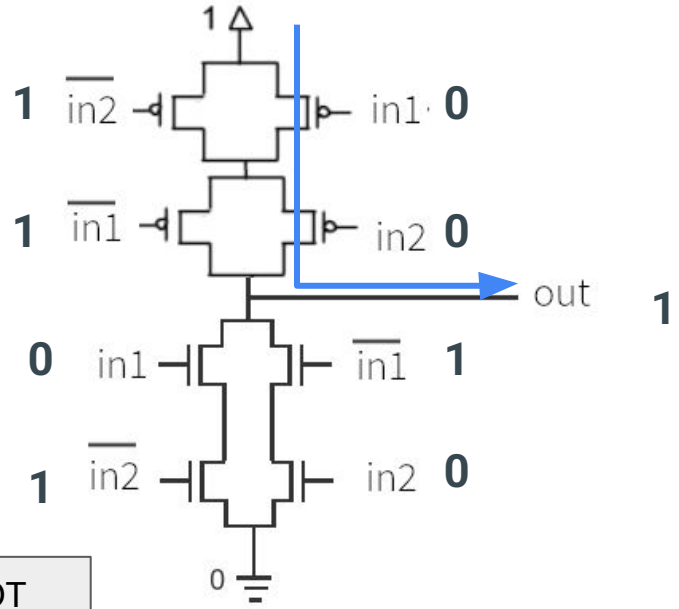
nMOS conducts in2, in1

XOR Gate

XNOR Gate (Exclusive-NOR)

in1	in2	out
0	0	1
0	1	0
1	0	0
1	1	1

pMOS
conducts in1, in2

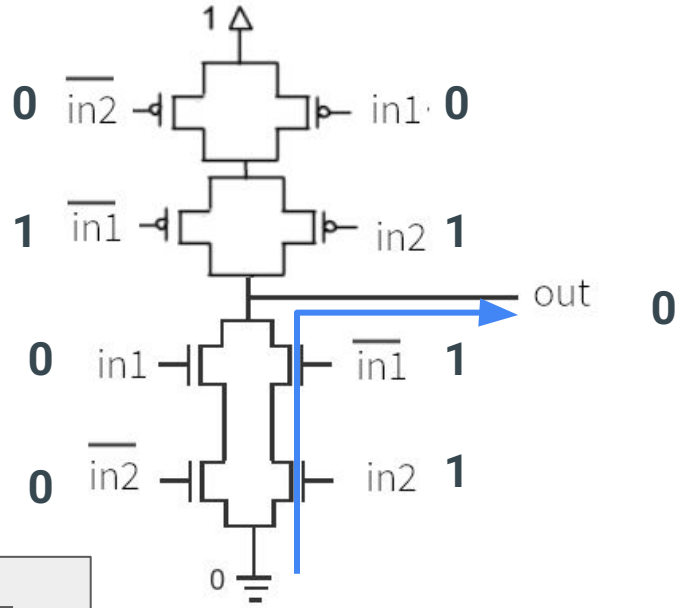


nMOS does NOT
conduct in2, in1

XNOR Gate

in1	in2	out
0	0	1
0	1	0
1	0	0
1	1	1

pMOS does NOT conduct $\overline{in1}$, in2



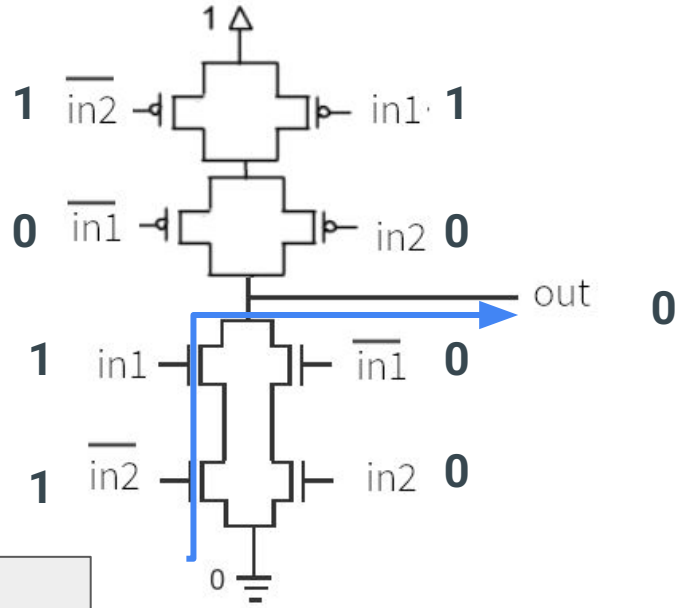
nMOS conducts in2, $\overline{in1}$

XNOR Gate

in1	in2	out
0	0	1
0	1	0
1	0	0
1	1	1

⇦

pMOS does NOT conduct in1, $\overline{in2}$

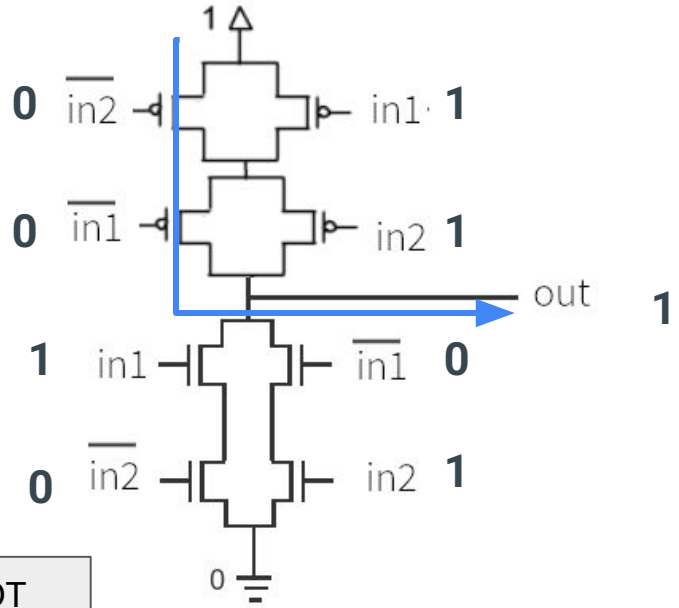


nMOS conducts $\overline{in2}$, in1

XNOR Gate

in1	in2	out
0	0	1
0	1	0
1	0	0
1	1	1 ⇦

pMOS
conducts $\overline{in1}$, $\overline{in2}$



nMOS does NOT
conduct $\overline{in2}$, $\overline{in1}$

XNOR Gate